

The Embedded I/O Company



TA308

Cable Kit for Modules with XRS JTAG Connector

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User Manual

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TA308-10R

Cable Kit for Modules with XRS JTAG Connector

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an 'Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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1 **Product Description**

The TA308-10R is a JTAG adapter that allows connecting the Xilinx platform cable USB programmer to TEWS FPGA modules with XRS connector based JTAG and debug interface.

The TA308 provides LEDs for the debug interface GPIO pins and includes a 150 mm XRS cable.

2 Pin Assignment – I/O Connector

2.1 Overview

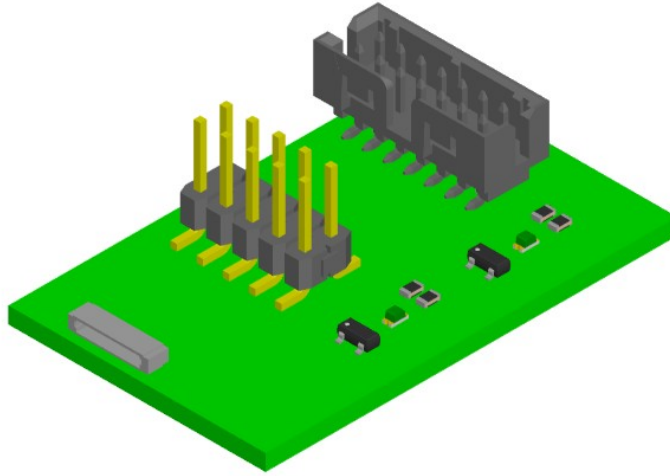


Figure 2-1 : TA308 Overview

Please note the connector pin 1 markings on the PCB (not visible in the picture).

2.2 XRS Connector

Pin-Count	10
Connector Type	JST XRS 10pol 0,6 mm Pitch IDC Connector
Source & Order Info	SM10B-XSRS-ETB

Mating socket is JST 10XSR-36S. A 10XSRXSR36L150 150 mm cable assembly is included in TA308.

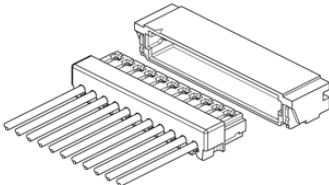
	Pin	Description
	1	GND
	2	TCK
	3	TMS
	4	TDI
	5	TDO
	6	GND
	7	GPIO0
	8	GPIO1
	9	PRESENT#
	10	V _{REF}

Table 2-1 : XRS Connector Pin Assignment

GPIO0 and GPIO1 are connected to high-active LEDs powered from V_{REF}.

PRESENT# is tied to GND on the TA308 and is used to activate the JTAG interface on the target board.

2.3 BScan JTAG Connector

Pin-Count	10
Connector Type	10 pol, 2,54 mm header
Source & Order Info	Samtec TSM-105-01-L-DV

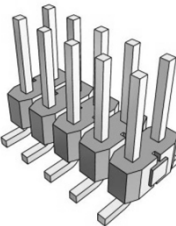
Description	Pin		Pin	Description
PWR_CTRL# (opt.)	10		9	TRST# (optional)
GND	8		7	TDO
GND	6		5	TDI
GND	4		3	TMS
GND	2		1	TCK

Table 2-2 : BScan JTAG Connector Pin Assignment

2.4 Xilinx JTAG Connector

Pin-Count	14
Connector Type	14 pol, 2 mm shrouded header
Source & Order Info	MOLEX 87832-142

Compatible with the Xilinx Platform Cable USB II.

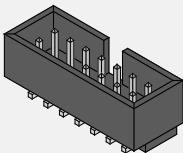
Description	Pin		Pin	Description
HALT (n. c.)	14		13	PGND
not connected	12		11	GND
TDI	10		9	GND
TDO	8		7	GND
TCK	6		5	GND
TMS	4		3	GND
V _{REF}	2		1	not connected

Table 2-3 : Xilinx JTAG Connector Pin Assignment