The Embedded I/O Company

TEWS TECHNOLOGIES

TA900

Program and Debug Box

Version 1.0

User Manual

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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

TA900-10R

Program and Debug Box, USB and JTAG Connectors, extended temperature range

(RoHS compliant)

TEWS TECHNOLOGIES GmbH has made any effort to ensure that this manual is accurate and complete. However TEWS TECHNOLOGIES GmbH reserves the right to change the product described in this document at any time without notice.

TEWS TECHNOLOGIES GmbH is not liable for any damage arising out of the application or use of the device described herein.

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial issue	June 2011
1.0.1	General revision	July 2012

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1 Product Description

The TA900 is an Interface Box which can be used to program and debug hardware modules providing a corresponding connector.

The Interface Box connects to compatible modules via a 20-pin Flexible Printed Circuit (FPC) Connector which can provide access to the module's JTAG Chain and the additional interfaces A and B. The TA900 can be accessed by USB 2.0 and by a 14-pin JTAG Header, and is equipped with a Pushbutton Switch which is offering the possibility to send an impulse to one of the connected module's I/O pins. A green LED indicates the assertion of this impulse by interrupting illumination.

In case of the user programmable FPGA boards TAMC631 and TAMC640/641, Interface A provides access to the UART of the onboard Module Management Controller (MMC), and Interface B connects to two user pins of the module's onboard FPGA. If a UART core is implemented in the module's FPGA, serial communication via Interface B is possible. By setting DIP Switches, the provided yellow LEDs located in the TA900 front panel can either indicate the logic level of the Interface's lines or can be configured to visualize serial communication on the Rx and Tx lines, if they are connected to the UART interfaces of the USB Controller. Level Shifters can handle I/O voltages between 1.2V and 3.3V at the FPC Connector which offers a wide range of possible configurations for Interface A, B and the JTAG Chain of the connected hardware module.

The JTAG Chain of the connected hardware module which is useful to program and debug onboard devices can be accessed in two different ways: If it is accessed via the 14-pin Header, which must be the case when communicating with Xilinx Devices, a "Xilinx Platform Cable USB II" (which is required) can be connected without any adaption. If the JTAG Chain is accessed via the USB interface, Channel A of the USB Controller is not used to communicate with Interface A, but to generate JTAG signals for debugging or programming reasons. In this configuration, Lattice Devices for example can directly be programmed without the necessity of an additional Programming Cable, as the TA900 is directly supported by Lattice's Software Tool "ispVM".

The TA900 is self-powered by the FPC Connector which means that it is not necessary to connect the Interface Box to USB to provide a supply voltage. The Interface Box meets the requirements to operate in extended temperature range from -30° to +75°C and comes with a **USB A to USB B Cable** and an **FPC Flexcable**.

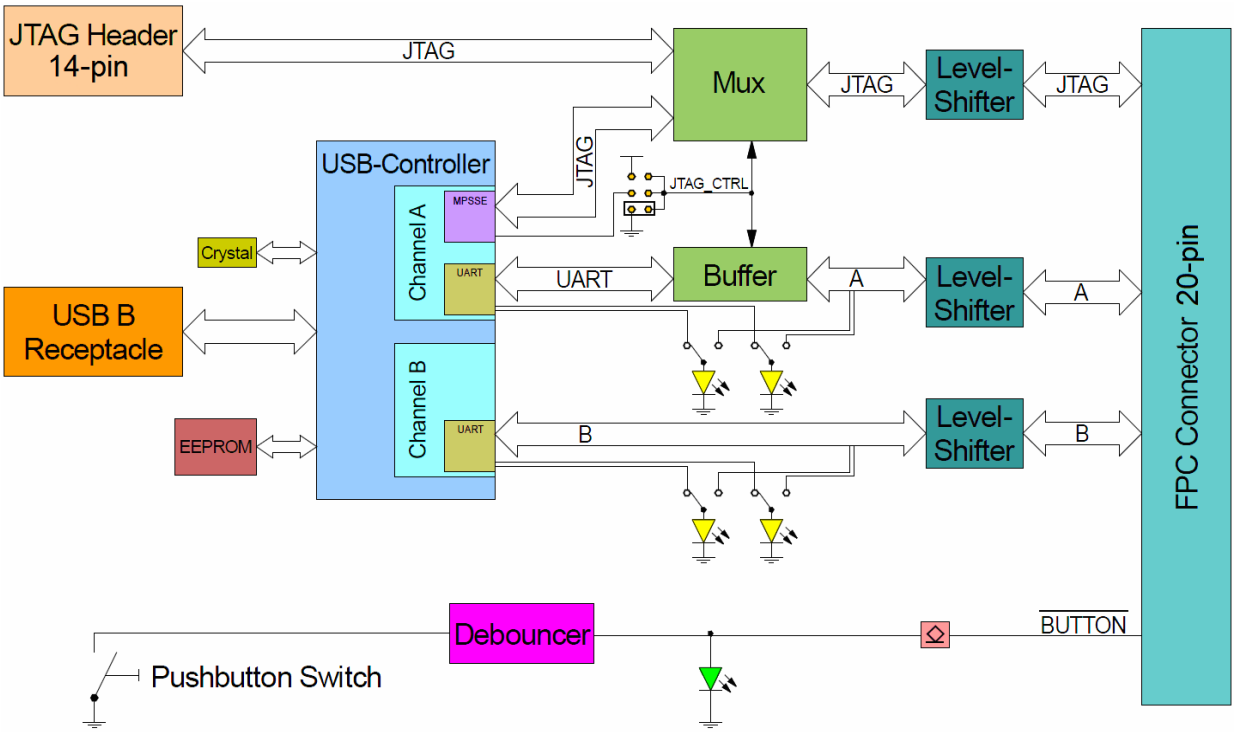


Figure 1-1 : Block Diagram

2 Technical Specification

FPC Connector Interface	
Mechanical Interface	20-pin Flexible Printed Circuit (FPC) Connector (Tyco 2-84953-0 or compatible)
Electrical Interface	JTAG Interface Interface A Interface B User I/O pin $\overline{BUTTON}$
I/O Voltages	1.2V to 3.3V

On Board Devices	
USB to UART/JTAG Controller	FT2232H (FTDI Chip)

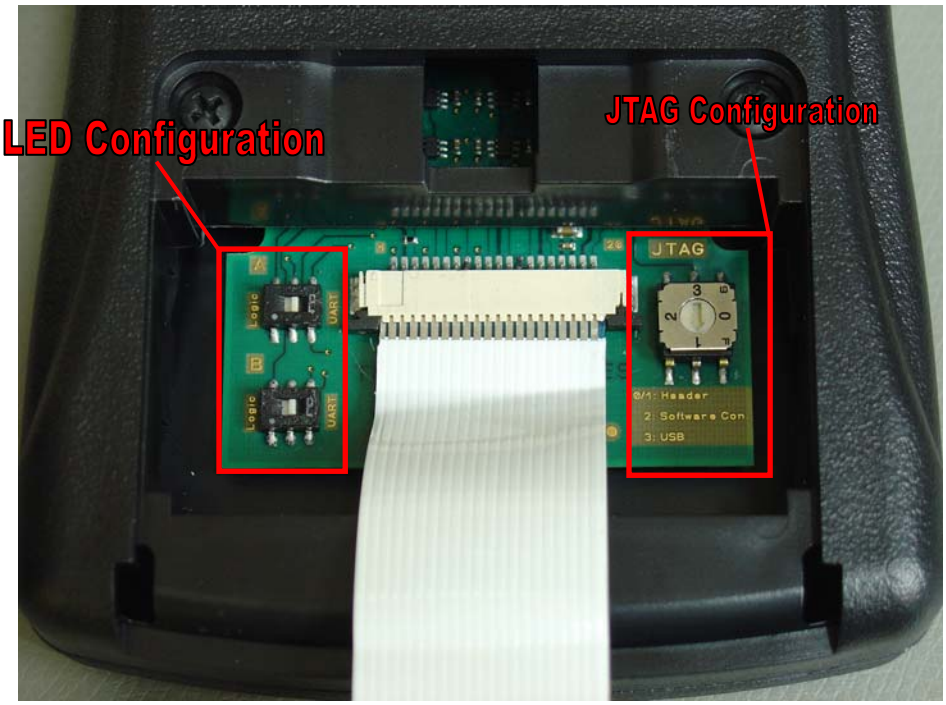
USB Interface	
Mechanical Interface	USB B Receptacle (Kycon KUSBX-BS1N-W or compatible)
Electrical Interface	USB 2.0 High Speed (480Mb/s) and Full Speed (12Mb/s) (Self-Powered)
Vendor ID	0x0403
Product ID	0x6010
Interface A	UART / MPSSE Mode JTAG Supported by "Lattice ispVM"
Interface B	UART
JTAG Header Interface	
Mechanical Interface	14-pin Shrouded Header (Molex 87833-1420 or compatible)
Electrical Interface	V_{REF}, GND, TCK, TMS, TDI, TDO Matches the "Xilinx Platform Cable USB II" pinout

Physical Data		
Power Requirements	120mA maximum @ +3.3V DC	
Temperature Range	Operating Storage	-30°C to +75°C -30°C to +75°C
MTBF	639000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	132 g	
Size	139.7mm x 82.6mm x 26.2mm	

Table 2-1 : Technical Specification

3 Configuration

To modify the LED Configuration and the JTAG Configuration remove the PCB Compartment Door and set the DIP Switches and the Rotary Selector Switch accordingly.



3.1 JTAG Configuration

The JTAG Chain of the connected hardware module which is useful to program and debug onboard devices can be accessed in two different ways:

If it is accessed via the 14-pin Header, which must be the case when communicating with Xilinx Devices, a "Xilinx Platform Cable USB II" (which is required) can be connected without any adaption.

If the JTAG Chain is accessed via the USB interface, Channel A of the USB Controller is not used to communicate with Interface A, but to generate JTAG signals for debugging or programming reasons. In this configuration, Lattice Devices for example can directly be programmed without the necessity of an additional Programming Cable, as the TA900 is directly supported by Lattice's Software Tool "ispVM".

Whether the JTAG Chain of the module connected to the FPC Connector is accessed by the JTAG Header or by USB is determined by the configuration of the Rotary Selector Switch:

Position	Function
0	The JTAG Chain can be accessed via JTAG Header
1	The JTAG Chain can be accessed via JTAG Header **[default]**
2	Software Controlled: o Outputting HIGH level at GPIOH7 Pin when Interface A is configured to MPSSE-Mode enables JTAG over USB. o Outputting LOW level enables JTAG over JTAG Header
3	The JTAG Chain can be accessed via USB-Controller if Interface A is configured to MPSSE-Mode

3.2 LED Configuration

The yellow LEDs for Interface A and Interface B in the TA900 Front Panel can be configured to operate in two different ways by setting DIP Switches:

o Set to **Logic**, the LEDs indicate the logic level of the corresponding interface pins.

o Set to **UART**, they indicate UART traffic on the Rx Line and Tx Line of the corresponding interface. **[default]**

4 Drivers

FTDI provides Virtual COM Port (**VCP**) drivers which cause the USB device to appear as two additional COM ports available on the PC. These COM ports can be accessed like standard COM ports by the operating system. The following operating systems are supported:

- Windows 2000, Windows XP, Windows Server 2003, Windows Vista, Windows Server 2008, Windows 7, Windows Server 2008 R2 (32-bit and 64-bit)
- Linux (32-bit and 64-bit)
- Mac OS X (32-bit, 64-bit and PPC)
- Windows CE 4.2-5.2 (32-bit, ARM, MIPSII, MIPSIV, SH4)
- Windows CE 6.0 (32-bit, ARM, MIPSII, MIPSIV, SH4)

Additionally, FTDI provides **D2XX** drivers which allow direct access to the USB device through a DLL. This offers the user to design application software which can access the USB device through a series of DLL function calls. The project FTCJTAG DLL can be downloaded at the FTDI homepage to handle all Multi-Protocol Synchronous Serial Engine (MPSSE) commands necessary to create a USB to JTAG interface. The following operating systems are supported:

- Windows 2000, Windows XP, Windows Server 2003, Windows Vista, Windows Server 2008, Windows 7, Windows Server 2008 R2 (32-bit and 64-bit)
- Linux (32-bit and 64-bit)
- Mac OS X (32-bit, 64-bit and PPC)
- Windows CE 4.2-5.2 (32-bit, ARM, MIPSII, MIPSIV, SH4)
- Windows CE 6.0 (32-bit, ARM, MIPSII, MIPSIV, SH4)

5 Pin Assignment – I/O Connector

5.1 Front I/O

The following figure shows the Front I/O Interface of the TA900.

Figure 5-1 : TA900 Front I/O

5.1.1 USB B-type Receptacle

Pin-Count	4
Connector Type	USB B-type Receptacle
Source & Order Info	Kycon KUSBX-BS1N-W or compatible

Table 5-1 : USB B-type Receptacle details

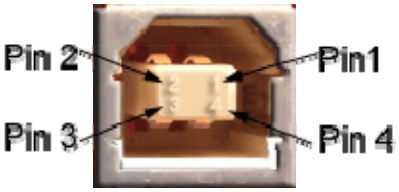


Figure 5-2 : USB B-type Receptacle view

The TA900 comes with a USB A to USB B Cable (Reichelt AK 672/2-3,0 or compatible)

5.1.1.1 Pin Assignment

Pin	Signal	Description	Driven by
1	VBUS	+5V	PC
2	D-	Data -	PC, TA900
3	D+	Data +	PC, TA900
4	GND	Ground	

Table 5-2 : Pin Assignment USB B-type Receptacle

5.1.2 JTAG Header

Pin-Count	14
Connector Type	2mm grid right-angled Box Header
Source & Order Info	Molex 87833-1420 or compatible

Table 5-3 : JTAG Header details

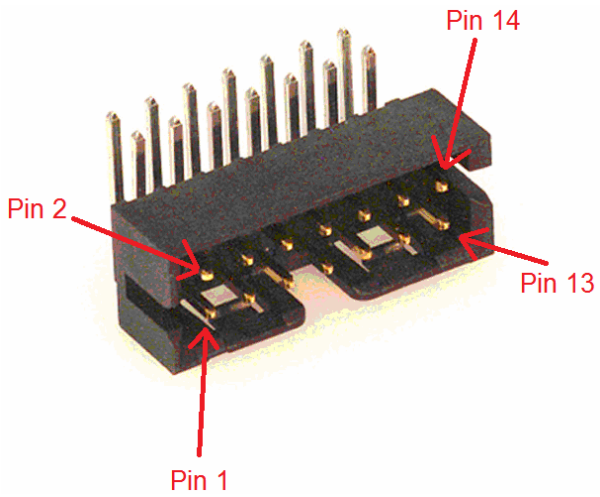


Figure 5-3 : JTAG Header view

5.1.2.1 Pin Assignment

The pinout of the TA900 JTAG Header matches the pinout of the "Xilinx Platform Cable USB II". This means that the Xilinx 14-pin ribbon cable can be connected to the TA900 without any adaption.

Pin	Signal	Description	Driven by
1	NC	Not connected	
2	V_{REF}	+3.3V Reference Voltage	TA900
3	GND	Ground	
4	TMS	Test Mode Select Input	JTAG Programmer
5	GND	Ground	
6	TCK	Test Clock	JTAG Programmer
7	GND	Ground	
8	TDO	Test Data Output	TA900
9	GND	Ground	
10	TDI	Test Data Input	JTAG Programmer
11	GND	Ground	
12	NC	Not connected	
13	NC	Not connected	
14	NC	Not connected	

Table 5-4 : Pin Assignment JTAG Header

5.2 FPC Connector

Pin-Count	20
Connector Type	1mm pitch Flexible Printed Circuit Connector
Source & Order Info	Tyco 2-84953-0 or compatible

Table 5-5 : FPC Connector details

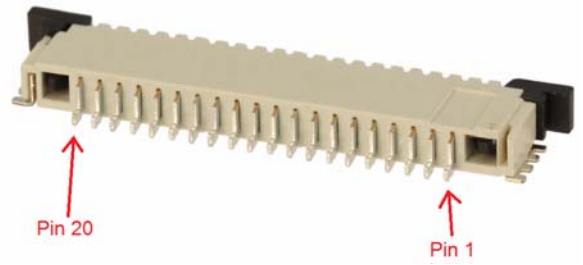


Figure 5-4 : FPC Connector view

The TA900 comes with an FPC Flexcable
(Adapt SYSTEM 280-1.00-B-20-200-5-5-10-10 or compatible)

5.2.1 Pin Assignment

Pin	Signal	Description	Driven by
1	$\overline{BOX\_PRESENT}$	Tied low by TA900	TA900
2	$V_{I/O}$ JTAG	JTAG Chain I/O Voltage	Module
3	TDO	Test Data Output	Module
4	GND	Ground	
5	TDI	Test Data Input	TA900
6	TMS	Test Mode Select Input	TA900
7	GND	Ground	
8	TCK	Test Clock Input	TA900
9	GND	Ground	
10	Tx Interface B	Interface B Transmitted Data	TA900
11	$V_{I/O}$ Interface B	Interface B I/O Voltage	Module
12	Rx Interface B	Interface B Received Data	Module
13	GND	Ground	
14	Tx Interface A	Interface A Transmitted Data	TA900
15	$V_{I/O}$ Interface A	Interface A I/O Voltage	Module
16	Rx Interface A	Interface A Received Data	Module
17	GND	Ground	
18	+3,3V	Supply Voltage	Module
19	$V_{I/O}$ $\overline{Button}$	$\overline{Button}$ I/O Voltage	Module
20	$\overline{Button}$	Pulse to module's FPGA I/O pin	TA900

Table 5-6 : Pin Assignment FPC Connector