The Embedded I/O Company

TAMC220

3 Slot IndustryPack® Carrier for MTCA.4 Rear-I/O

Version 1.0

User Manual

Issue 1.0.0

November 2011

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TAMC220-10R

3 Slot IndustryPack® Carrier for MTCA.4 Rear I/O, Mid-Size front panel ***)**

TAMC220-11R

3 Slot IndustryPack® Carrier for MTCA.4 Rear I/O, Full-Size front panel

***)** Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module can be used in the desired system. Otherwise, damage to the TAMC220 or the slot it is used in may occur!

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	November 2011

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1 Product Description

The TAMC220 is a standard double mid-size/full-size AMC.1 (PCI-Express) and MTCA.4 compliant carrier for up to three single-size, or one double-size and one single-size IndustryPack (IP) modules. It can be used to build modular, flexible and cost effective I/O solutions for all kinds of applications like process control, medical systems, telecommunication and traffic control. The TAMC220 is a versatile solution to upgrade well known legacy I/O solutions to a high performance form factor.

Two AirMaxVS connectors provide access to all IP I/O lines via a Micro Rear Transition Module (µRTM). The TAMC002-TM is such a µRTM that is fully compatible to the TAMC220 and offers full access to all IP I/O signals over two types of connectors.

The IP power lines are protected by self-healing fuses and are RF filtered. The operating temperature range is -40°C to +85°C.

According to AMC.0, the TAMC220 provides an IPMI compliant Module Management Controller (MMC) with temperature monitoring and hot-swap support.

The TAMC220 is available as a mid-size module or as a full-size module. Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module can be used in the system. Otherwise, damage to the TAMC220 or the slot it is used in may occur!

TCLKA and TCLKB are connected to the µRTM via M-LVDS transceivers. Both signals can be used as bi-directional single-ended signals.

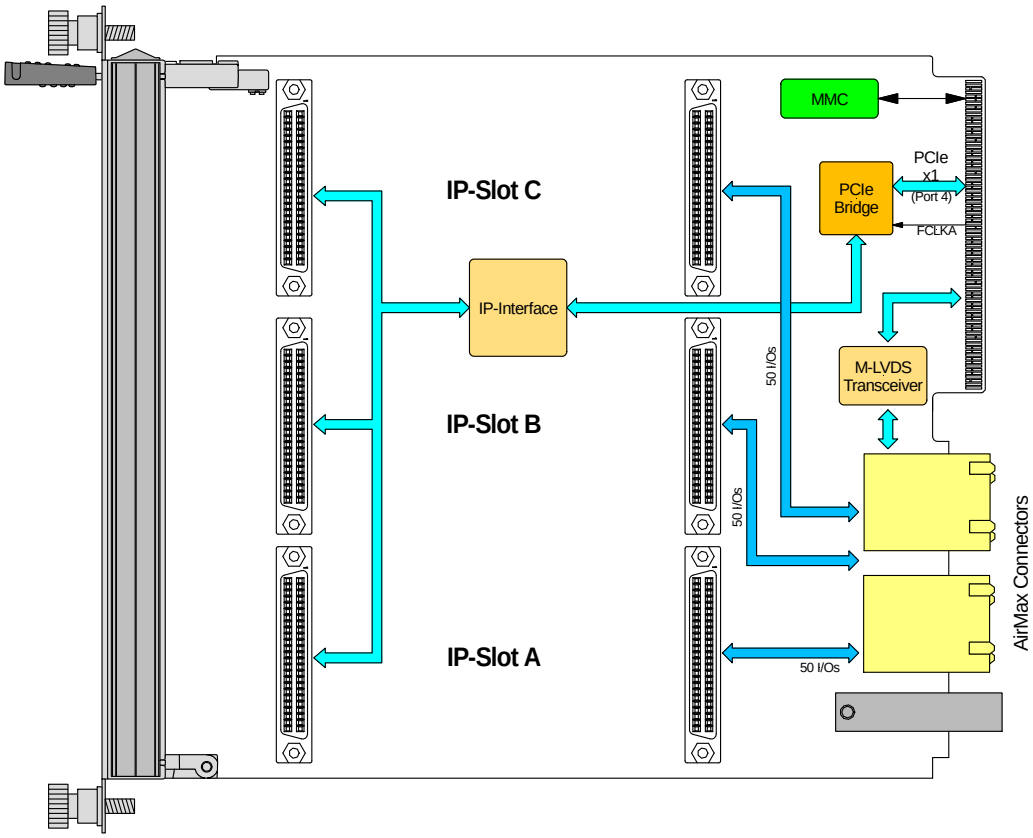


Figure 1-1 : Block Diagram

2 Technical Specification

AMC Interface	
Mechanical Interface	Advanced Mezzanine Card (AMC) Interface conforming to MTCA.4 Module Type: Double Mid-Size Module (-10R) Module Type: Double Full-Size Module (-11R)
Electrical Interface	PCI Express x1 Link conforming to PICMG® AMC.1 R1.0 (PCI Express® on AdvancedMC™) AMC.1 Fabric Type 1
IPMI Support	
IPMI Version	1.5
Front Panel LEDs (MMC controlled)	Blue Hot-Swap LED Red Failure Indication LED (LED1) Green Board OK / Activity LED (LED2)
Main Onboard Devices	
PCI Express to PCI Bridge	PEX8112 (PLX Technology)
PCI Target Device	PCI9030 (PLX Technology)
IP Interface Device	XC2S50 (Xilinx)
IP Interface	
IP Interface	According to IndustryPack specification ANSI / VITA 4-1995 8- / 16-Bit Access 8 / 32 MHz selectable per IP slot 8 MByte memory space per IP slot TTL Level
IP Slots	Three single-size IP slots (A, B, C). IP Slots A+B may be used for a double-size IP Module
Mapping of IP Interrupts	Routing of all IP interrupts to PCIe INTA/MSI. Local interrupt status register
DMA	Not supported
32-Bit Access	Not supported in the current implementation
Power Supply	Resettable fuses and RF-filtering on all IP power lines
IP LEDs	One LED per IP slot. Indicate IP module activity (LEDs flash on when the respective IP module generates the acknowledge signal)
I/O Interface	
I/O Connector	Rear-I/O: FCI AirmaxVS™ 90-pos, Right-Angle Receptacle (10056335-101LF), accessible via a compatible µRTM
Physical Data	
Power Requirements	Management Power: 45mA typical @ +3.3V DC
	Payload Power: 400mA typical @ +12V DC (Without any IP Modules plugged into the slots. IP Modules require additional power)
	max. Current Draw as per Module Current Requirements record: 4.0A

Temperature Range	Operating	-40°C to +85°C
	Storage	-40°C to +85°C
MTBF	268000h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	217g	

Table 2-1 : Technical Specification

3 Handling and Operating Instructions

3.1 ESD Protection

The AMC module is sensitive to static electricity. Packing, unpacking and all other module handling has to be done in an ESD/EOS protected Area.

3.2 Thermal Considerations

Forced air cooling is recommended during operation. Without forced air cooling, damage to the device can occur.

3.3 Mid-size Option Usage Restrictions

Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module with its component height violation can be used in the system. Otherwise, damage to the TAMC220 or the slot it is used in may occur!

Refer to the chapter “Component Height Violation on TAMC220-10R” for details.

3.4 Voltage Limits on IndustryPacks

The AMC.0 specification limits the voltages on AMC modules. These limits also apply to mounted IndustryPacks.

Refer to the chapter “Voltage Limits on IndustryPack Modules” for details.

4 IPMI Support

The AMC module provides a Module Management Controller (MMC) that performs health monitoring, hot-swap functionality and stores the Field Replaceable Unit (FRU) information. The MMC communicates via an Intelligent Platform Management Interface (IPMI).

4.1 Temperature and Voltage Sensors

The MMC monitors onboard sensors and signals sensor events to the superordinated IPMI controller / shelf manager. Available sensors are listed in the table below.

Sensor Number	Signal Type	Thresholds	Signal Monitored
0	Event	-	Hot-swap switch
1	Temperature	lnr lcr lnc unc ucr unr	LM75 #1
2	Temperature	lnr lcr lnc unc ucr unr	LM75 #2
3	Voltage	lnr lcr lnc unc ucr unr	+12V (PWR)
4	Voltage	lnr lcr lnc unc ucr unr	+1.5V
5	Voltage	lnr lcr lnc unc ucr unr	+12V (IP)
6	Voltage	lnr lcr lnc unc ucr unr	-12V (IP)

Table 4-1 : Temperature and Voltage Sensors

unr: upper non-recoverable, ucr: upper critical, unc: upper non-critical
lnr: lower non-recoverable, lcr: lower critical, lnc: lower non-critical

4.2 FRU Information

The MMC stores the module FRU information in a non-volatile EEPROM. Some of the records are writeable. If records are modified, the user is responsible for setting the proper checksums. The actual FRU information data is shown below.

Area	Size (in Bytes)	Writeable
Common Header	8	no
Internal Use Area	0	no
Chassis Info Area	0	no
Board Info Area	variable	no
Product Info Area	variable	no
Multi Record Area		
Module Current Requirements	variable	yes
AMC Point-to-Point Connectivity	variable	yes
Clock Configuration	variable	yes
Zone 3 Interface Compatibility Record	variable	yes

Table 4-2 : FRU Information

4.2.1 Board Info Area

Product Information	Value
Version	1
Language Code	0x00 - English
Manufacturer date/time	determined at manufacturing
Board manufacturer	TEWS TECHNOLOGIES GmbH
Board product name	TAMC220
Board serial number	determined at manufacturing (see board label)
Board part number	TAMC220-xxR -xx = -10 / -11

Table 4-3 : Board Info Area

4.2.2 Product Info Area

Product Information	Value
Version	1
Language Code	0x00 - English
Product manufacturer	TEWS TECHNOLOGIES GmbH
Product name	TAMC220
Board part/model number	TAMC220-xxR -xx = -10 / -11
Product version	V1.0 Rev. A (see board label)
Product serial number	determined at manufacturing (see board label)
Asset tag	= Product serial Number

Table 4-4 : Product Info Area

4.2.3 Multi Record Area

4.2.3.1 Module Current Requirements

The “Current Draw” value holds the Payload Power (PWR) requirement of the module given as current requirement in units of 0.1A at 12V.

The AMC module announces the value of “Current Draw” as current demand to the shelf manager. If the allocated power budget for the actual AMC slot is lower than this value, the shelf manager may not enable Payload power for this slot.

If required, the “Current Draw” value in the Module Current Requirements record may be modified to a value that falls within the given power budget. Make sure that the modified value still satisfies the power requirements for both the AMC module and the mounted IP modules.

Product Information	Value
Current Draw	0x28 (4.0 A)

Table 4-5 : Module Current Requirements

4.2.3.2 Zone 3 Interface Compatibility Record

In the Multi-Record Area, the AMC module must provide at least one Zone 3 Interface Compatibility Record defined as follows.

Offset	Length	Description
0	1	Record Type ID Value C0h (OEM)
1	1	[7:7] End of list. Set to one for the last record. [6:4] Reserved. Write as 0h. [3:0] Record format version (2h for this definition)
2	1	Record Length
3	1	Record Checksum Holds the zero checksum of the record
4	1	Header Checksum Holds the zero checksum of the header
5	3	Manufacturer ID 0x00315A, LSB first
8	1	PICMG Record ID Value 30h
9	1	Record Format Version Value 1h
10	1	Type of Interface Identifier 3h = OEM interface identifier
11	3	Interface Identifier Body Manufacturer ID (IANA) of the OEM that owns the definition of the interface. LS Byte first. 0x0071E3 (TEWS Technologies Private Enterprise Number)
14	4	Interface Identifier Body OEM-defined interface designator, 32 bits, LS Byte first 0x8DC0000 (0x8 = TAMC, 0xDC = 220)

Table 4-6: µRTM FRU Zone 3 Interface Compatibility Record

If any Zone 3 Interface Compatibility record in the µRTM's FRU information matches the Zone 3 Interface Compatibility record shown, the TAMC220 considers the µRTM to be compatible. Otherwise the TAMC220 considers the µRTM to be incompatible.

The Zone 3 Interface Compatibility records are considered as matching if the records are the same length and are identical from offset 9 to the end of the record. Otherwise the record is considered as not matching.

4.2.3.3 AMC Point-to-Point Connectivity

The AMC module provides the following AMC Point-to-Point Connectivity Record Data.

Channel	Port	Link Type	Link Type Extension	Link Grouping ID	Asymmetric Match
0	4	AMC.1 PCI Express	Gen 1 PCI Express, non-SSC	Single Channel Link	PCI Express Primary Port
		AMC.1 PCI Express	Gen 1 PCI Express, SSC	Single Channel Link	PCI Express Primary Port

Table 4-7 : AMC Point-to-Point Connectivity

4.2.3.4 Clock Configuration

AMC FCLKA (CLK3) is used as the PCI Express Reference Clock.

Clock ID	Clock Features	Clock Family	Clock Accuracy	Clock Frequency
FCLKA	Clock Receiver	PCI Express	PCI Express Gen 1	100 MHz nominal

Table 4-8 : Clock Configuration

4.2.4 Modifying FRU Records

Some of the records are writeable to allow adaption to certain systems. If records are modified, the user is responsible for setting the proper checksums.

5 Addressable Resources

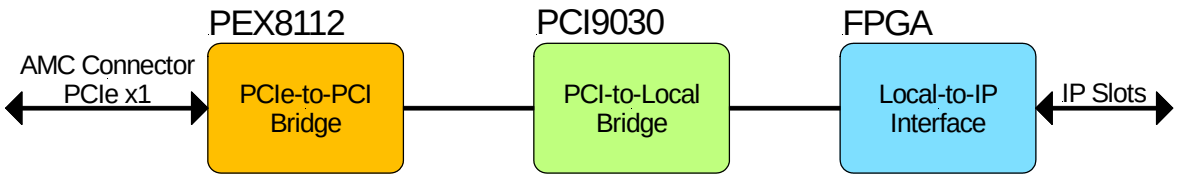
This chapter describes system resources, such as memory mapping and register sets.

5.1 Overview

A PEX8112 PCIe-to-PCI bridge is used as the bridging device between the AMC PCI Express interface and the PCI bus on the TAMC220.

The PCI9030 PCI Target chip is located on the TAMC220 onboard PCI bus.

The IndustryPack interface is implemented in an onboard FPGA device, located on the local bus of the PCI9030 PCI Target chip.



5.2 PEX8112 PCIe-to-PCI Bridge

The PEX8112 is a PCIe-to-PCI bridge. On the TAMC220, the PEX8112 is used in forward mode only.

5.2.1 PEX8112 Register Map

Register Group	PCI Space	Offset Address Range
PCI-Compatible Configuration (Type 1) Registers	PCI Express Configuration	0x00 - 0x3C
	Memory Mapped (BAR0)	
PCI-Compatible Extended Capability Registers for PCI Express Interface	PCI Express Configuration	0x40 - 0xFF
	Memory Mapped (BAR0)	
PCI Express Extended Capability Registers	PCI Express Configuration	0x100 - 0xFFF
	Memory Mapped (BAR0)	
Main Control Registers	Memory Mapped (BAR0)	0x1000 - 0x1FFF

Table 5-1 : PEX8112 Register Map

5.2.2 PCI-Compatible Configuration (Type 1) Registers

PCI CFG Register Address	31 24	23 16	15 8	7 0	Initial Configuration Settings
0x00	PCI Device ID		PCI Vendor ID		8112 10B5
0x04	PCI Status		PCI Command		0010 0000
0x08	PCI Class Code			PCI Device Revision ID	060400 AA
0x0C	PCI Built-In Self-Test (Not Supported)	PCI Header Type	Internal PCI Bus Latency Timer	PCI Cache Line Size	00 01 00 00
0x10	PCI Base Address 0				0000000C
0x14	PCI Base Address 1				00000000
0x18	Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	00 00 00 00
0x1C	Secondary Status		I/O Limit	I/O Base	0200 00 00
0x20	Memory Limit		Memory Base		0000 0000
0x24	Prefetchable Memory Limit		Prefetchable Memory Base		0000 0000
0x28	Prefetchable Memory Base Upper 32 Bits				00000000
0x2C	Prefetchable Memory Limit Upper 32 Bits				00000000
0x30	I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		0000 0000
0x34	Reserved			PCI Capabilities Pointer	000000 40
0x38	PCI Base Address for Expansion ROM (Not Supported)				
0x3C	Bridge Control		Internal PCI Interrupt Wire	Internal PCI Interrupt Line	0000 01 00

Table 5-2 : PEX8112 PCI-Compatible Configuration (Type 1) Registers

5.2.3 PCI-Compatible Extended Capability Registers

PCI CFG Register Address	31 24	23 16	15 8	7 0	Initial Configuration Settings
0x40	Power Management Capabilities		Power Management Next Capability Pointer	Power Management Capability ID	CA02 5001
0x44	Power Management Data	Power Management Bridge Support	Power Management Control/Status		00 00 0000
0x48	Device-Specific Control				0000 0000
0x4C	Reserved				-
0x50	Message Signaled Interrupts Control		Message Signaled Interrupts Next Capability Pointer	Message Signaled Interrupts Capability ID	0080 60 05
0x54	Message Signaled Interrupts Address				0000 0000
0x58	Message Signaled Interrupts Upper Address				0000 0000
0x5C	Reserved		Message Signaled Interrupts Data		0000 0000
0x60	PCI Express Capabilities		PCI Express Next Capability Pointer	PCI Express Capability ID	0071 00 10
0x64	Device Capabilities				0000 0000
0x68	PCI Express Device Status		PCI Express Device Control		0000 2000
0x6C	Link Capabilities				0000 4C11
0x70	Link Status		Link Control		1011 0000
0x74	Slot Capabilities				0000 0C80
0x78	Slot Status		Slot Control		0400 0000
0x7C	Reserved		Root Control		0000 0000
0x80	Root Status				0000 0000
0x84	Main Control Register Index				0000 0000
0x88	Main Control Register Data				0000 0000
0x8C - 0xFF	Reserved				-

Table 5-3 : PEX8112 PCI-Compatible Extended Capability Registers

5.2.4 Configuration EEPROM

After reset, the PEX8112 loads initial configuration register data from an onboard configuration EEPROM. Only register settings differing from default values are stored in the EEPROM.

For detailed information please refer to the PEX8112 manual.

Modifications to default values are:

- Address Stepping is disabled (PCI Command Register)
- 66 MHz Capable Bit is cleared (I/O Limit & Secondary Status Register)
- Slot Clock Configuration is enabled (Link Status/Control Register)
- PCI Express Enable Bit is set (Device Initialization Register)

5.3 PCI9030 PCI Target Device

The PCI9030 is the only PCI Target Device on the onboard PCI Bus (device number 0). The PCI9030 maps the IndustryPack Interface and the IndustryPack interface control/status registers to the TAMC220 PCI bus (PCI memory space).

5.3.1 PCI9030 PCI Configuration Registers

Register Offset	31 24	23 16	15 8	7 0	Initial Configuration Settings
0x00	Device ID (PCI9030)		Vendor ID (PLX Technology)		9030 10B5
0x04	Status		Command		0280 0003
0x08	Class Code			Revision ID	0680 0000
0x0C	Not Supported	Header	Not Supported	Cache Line	0000 0000
0x10	PCI Base Address 0 (PCIBAR0) (PCI9030 Local Configuration Register Memory Mapped)				FFFF FF80 (128 Byte)
0x14	PCI Base Address 1 (PCIBAR1) (PCI9030 Local Configuration Register I/O Mapped) (disabled)				0000 0000
0x18	PCI Base Address 2 (PCIBAR2) (Local Space 0) **(IP Interface Control/Status Register)**				FFFF FF00(1) (256 Byte)
0x1C	PCI Base Address 3 (PCIBAR3) (Local Space 1) **(IP Interface I/O, ID, INT Space)**				FFFF FC00(1) (1 Kbyte)
0x20	PCI Base Address 4 (PCIBAR4) (Local Space 2) **(IP Interface Memory Space)**				FE00 0000(1) (32 Mbyte)
0x24	PCI Base Address 5 (PCIBAR5) (Local Space 3) **(IP Interface 8bit only Memory Space)**				FF00 0000(1) (16 Mbyte)
0x28	Not used				0000 0000
0x2C	Subsystem ID (TAMC220)		Subsystem Vendor ID (TEWS TECHNOLOGIES)		80DC 1498
0x30	PCI Expansion ROM Base Address				0000 0000
0x34	Reserved			Cap. Pointer	0000 0040
0x38	Reserved				0000 0000
0x3C	Not Supported	Not Supported	Interrupt Pin	Interrupt Line	0000 0100
0x40	PM Capabilities		PM NxtCap	PM CapID	4801 4801
0x44	PM Data	PM CSR EXT	PM CSR		0000 0000
0x48	Reserved	HS CSR	HS NxtCap	HS CapID	0000 4C06
0x4C	VPD Address		VPD NxtCap	VPD CapID	0000 0003
0x50	VPD Data				0000 0000

(1) Read back value after writing all 1's.

Table 5-4 : PCI9030 PCI Configuration Registers

5.3.2 Local Configuration Register

The PCI base address for the PCI9030 Local Configuration Registers (PCI Memory mapped) can be obtained from the PCIBAR0 register at offset 0x10 in the PCI9030 PCI configuration register space.

Register Offset	Local Configuration Register	Name	Setting
0x00	Local Space 0 Range	LAS0RR	0x0FFF_FF00
0x04	Local Space 1 Range	LAS1RR	0x0FFF_FC00
0x08	Local Space 2 Range	LAS2RR	0x0E00_0000
0x0C	Local Space 3 Range	LAS3RR	0x0F00_0000
0x10	Expansion ROM Range	EROMRR	0x0000_0000
0x14	Local Space 0 Remap	LAS0BA	0x0800_0001
0x18	Local Space 1 Remap	LAS1BA	0x0400_0001
0x1C	Local Space 2 Remap	LAS2BA	0x0000_0001
0x20	Local Space 3 Remap	LAS3BA	0x0200_0001
0x24	Expansion ROM Remap	EROMBA	0x0000_0000
0x28	Local Space 0 Descriptor	LAS0BRD	0xD441_60A0
0x2C	Local Space 1 Descriptor	LAS1BRD	0x1441_20A2
0x30	Local Space 2 Descriptor	LAS2BRD	0x1441_20A2
0x34	Local Space 3 Descriptor	LAS3BRD	0x1401_20A2
0x38	Expansion ROM Descriptor	EROMBRD	0x0000_0000
0x3C	Local Chip Select 0	CS0BASE	0x0800_0081
0x40	Local Chip Select 1	CS1BASE	0x0400_0201
0x44	Local Chip Select 2	CS2BASE	0x0100_0001
0x48	Local Chip Select 3	CS3BASE	0x0280_0001
0x4C	Serial EEPROM / Interrupt Control & Status	PROT_ AREA/ INTCSR	0x0030_0049
0x50	Miscellaneous	CNTRL	0x007A_5000
0x54	General Purpose I/O	GPIOC	0x0224_9252

Table 5-5 : PCI9030 Local Configuration Registers

Shown values are register values after serial EEPROM configuration.

5.3.3 Configuration EEPROM

After reset, the PCI9030 loads initial configuration register data from an onboard configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

EEPROM Address	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9030	0x10B5	0x0280	0x0000	0x0680	0x0000	0x80DC	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0x0FFF	0xFF00	0x0FFF	0xFC00
0x30	0x0E00	0x0000	0x0F00	0x0000	0x0000	0x0000	0x0800	0x0001
0x40	0x0400	0x0001	0x0000	0x0001	0x0200	0x0001	0x0000	0x0000
0x50	0xD441	0x60A0	0x1441	0x20A2	0x1441	0x20A2	0x1401	0x20A2
0x60	0x0000	0x0000	0x0800	0x0081	0x0400	0x0201	0x0100	0x0001
0x70	0x0280	0x0001	0x0030	0x0049	0x007A	0x5000	0x0224	0x9252
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 5-6 : PCI9030 Configuration EEPROM Content

5.4 FPGA

An FPGA resides on the PCI9030 local bus.

The FPGA implements the IndustryPack Interface Control/Status Registers and maps the IndustryPack slots to the PCI9030 local bus.

The FPGA configures from a serial Flash after power-up. An onboard SMD LED indicates successful FPGA configuration.

6 Functional Description

6.1 IP Interface

The IP Interface and the IP Interface Control/Status registers are mapped to the onboard PCI bus via the local spaces of the onboard PCI9030 PCI Target Chip.

6.1.1 PCI9030 PCI Base Address Configuration

The PCI base address for each local space is obtained from the PCI9030 PCI configuration register space.

PCI9030 PCI BAR	PCI9030 Local Space	Size (Byte)	Port Width (Bit)	Endian Mode	PCI Space	IP Interface Space
2	0	256	16	Little	MEM	IP Interface Control/Status Register
3	1	1 K	16	Little	MEM	IP A-C ID, INT, IO Space (8/16 bit)
4	2	32 M	16	Little	MEM	IP A-C MEM Space (8/16 bit)
5	3	16 M	8	Little	MEM	IP A-C MEM Space (8 bit only port)

Table 6-1 : PCI9030 PCI Base Address Configuration

Note: The PCI9030 will convert 32-Bit transfer-size accesses to the actual port width. E.g. an aligned 32-Bit write to a 16-Bit port is automatically splitted into two 16-Bit writes.

6.1.2 IP Interface Register Map

The PCI9030 BAR 2 space is used for the IP Interface Control/Status registers.

The following Control/Status registers are implemented:

PCI Base Address: PCI9030 PCI Base Address 2 (Offset 0x18 in the PCI9030 PCI configuration register space).

Offset (Base = PCI Base Address 2)	Size (Byte)	Register
0x00	2	REVISION ID
0x02	2	IP A CONTROL
0x04	2	IP B CONTROL
0x06	2	IP C CONTROL
0x08	2	Reserved
0x0A	2	IP RESET
0x0C	2	IP STATUS
0x0E	2	Reserved
0x10 - 0xFF	240	Reserved

Table 6-2 : IP Interface Register Map

6.1.2.1 Revision ID Register (Offset 0x00)

The Revision ID Register shows the revision of the onboard IP FPGA logic.

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect
14		
13		
12		
11		
10		
9		
8		
7	REV_ID	Read: FPGA Logic Revision ID Write : No Effect
6		
5		
4		
3		
2		
1		
0 (LSB)		

Table 6-3 : IP Interface Revision ID Register

6.1.2.2 IP Control Registers (Offsets 0x02, 0x04, 0x06)

The IP Control Registers are used to control IP interrupts, recover time and clock rate on the IP interface.

There is one IP Control Register for each IP Slot (A-C).

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect. Should be written with 0's
14		
13		
12		
11		
10		
9		
8	SEL_MODE	0 : Single IP Select Cycle 1 : Extended IP Select Cycle IP Select is held active until the first IP Acknowledge Cycle is detected. May be required by some IP modules.
7	INT1_EN	0 : IP Interrupt 1 Disabled 1 : IP Interrupt 1 Enabled
6	INT0_EN	0 : IP Interrupt 0 Disabled 1 : IP Interrupt 0 Enabled
5	INT1_SENSE	0 : IP Interrupt 1 Level Sensitive 1 : IP Interrupt 1 Edge Sensitive
4	INT0_SENSE	0 : IP Interrupt 0 Level Sensitive 1 : IP Interrupt 0 Edge Sensitive
3	ERR_INT_EN	0 : IP Error Interrupt Disabled 1 : IP Error Interrupt Enabled
2	TIME_INT_EN	0 : IP Timeout Interrupt Disabled 1 : IP Timeout Interrupt Enabled
1	RECOVER	0 : IP Recover Time Disabled 1 : IP Recover Time Enabled
0 (LSB)	CLKRATE	0 : IP Clock Rate 8 MHz 1 : IP Clock Rate 32 MHz

Table 6-4 : IP Interface Control Registers

After reset, all bits in the IP Control Registers are cleared.

If IP recover time is enabled for an IP slot, an IP cycle for this slot will not begin until the IP recover time is expired. The IP recover time is app. 1µs.

6.1.2.3 IP Reset Register (Offset 0x0A)

The IP Reset Register is used to assert the IP RESET# signal and to detect when the IP reset phase is done.

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect. Should be written with 0's
14		
13		
12		
11		
10		
9		
8		
7		
6		
5		
4		
3		
2		
1		
0 (LSB)	IP_RESET	Read : 0 : IP RESET# Signal is De-asserted 1 : IP RESET# Signal is Asserted Write : 0 : No Effect 1 : Assert IP RESET# Signal (Automatic Negation)

Table 6-5 : IP Interface Reset Register

The IP RESET# signal is also asserted during payload reset.

6.1.2.4 IP Status Register (Offset 0x0C)

The IP Status Register is used to read IP timeout, error and interrupt status for the IP slots.

Bit	Name	Description	
15 (MSB)	-	Reserved. Undefined for reads.	
14	TIME_C	Read : 0 : No Timeout on IP_C 1 : IP_C Timeout has occurred	Write : 0 : No Effect 1 : Clear IP_C Timeout Status
13	TIME_B	Read : 0 : No Timeout on IP_B 1 : IP_B Timeout has occurred	Write : 0 : No Effect 1 : Clear IP_B Timeout Status
12	TIME_A	Read : 0 : No Timeout on IP_A 1 : IP_A Timeout has occurred	Write : 0 : No Effect 1 : Clear IP_A Timeout Status
11	-	Reserved. Undefined for reads.	
10	ERR_C	Read : 0 : No Error on IP_C 1 : IP_C ERROR# Signal Asserted	Write : No Effect
9	ERR_B	Read : 0 : No Error on IP_B 1 : IP_B ERROR# Signal Asserted	Write : No Effect
8	ERR_A	Read : 0 : No Error on IP_A 1 : IP_A ERROR# Signal Asserted	Write : No Effect
7	-	Reserved. Undefined for reads.	
6	-	Reserved. Undefined for reads.	
5	INT1_C	Read : 0 : No Interrupt 1 Request on IP_C 1 : Active IP_C Interrupt 1 Request	Write : 0 : No Effect 1 : Clear Edge Sensitive IP_C Interrupt 1 Status
4	INT0_C	Read : 0 : No Interrupt 0 Request on IP_C 1 : Active IP_C Interrupt 0 Request	Write : 0 : No Effect 1 : Clear Edge Sensitive IP_C Interrupt 0 Status
3	INT1_B	Read : 0 : No Interrupt 1 Request on IP_B 1 : Active IP_B Interrupt 1 Request	Write : 0 : No Effect 1 : Clear Edge Sensitive IP_B Interrupt 1 Status
2	INT0_B	Read : 0 : No Interrupt 0 Request on IP_B 1 : Active IP_B Interrupt 0 Request	Write : 0 : No Effect 1 : Clear Edge Sensitive IP_B Interrupt 0 Status
1	INT1_A	Read : 0 : No Interrupt 1 Request on IP_A 1 : Active IP_A Interrupt 1 Request	Write : 0 : No Effect 1 : Clear Edge Sensitive IP_A Interrupt 1 Status
0 (LSB)	INT0_A	Read : 0 : No Interrupt 0 Request on IP_A 1 : Active IP_A Interrupt 0 Request	Write : 0 : No Effect 1 : Clear Edge Sensitive IP_A Interrupt 0 Status

Table 6-6 : IP Interface Status Register

The IP timeout time is app. 8µs.

An IP timeout occurs if the IP module fails to generate the IP ACK# signal within the IP timeout time. An IP timeout is not reported to the PCI9030 or the PCI Master but in the Status Register. For timeout reads all 'F''s are returned as read data.

6.1.3 IP Interface I/O, ID, INT Space Address Map

The PCI9030 BAR 3 space is used for the IP A-C I/O, ID and INT space.

PCI Base Address: PCI9030 PCI Base Address 3 (Offset 0x1C in the PCI9030 PCI configuration register space).

Offset (Base = PCI Base Address 3)		Size (Byte)	IP Slot	IP Space
Start	End			
0x0000_0000	0x0000_007F	128	A	I/O
0x0000_0080	0x0000_00BF	64	A	ID
0x0000_00C0	0x0000_00FF	64	A	INT
0x0000_0100	0x0000_017F	128	B	I/O
0x0000_0180	0x0000_01BF	64	B	ID
0x0000_01C0	0x0000_01FF	64	B	INT
0x0000_0200	0x0000_027F	128	C	I/O
0x0000_0280	0x0000_02BF	64	C	ID
0x0000_02C0	0x0000_02FF	64	C	INT
0x0000_0300	0x0000_03FF	256	Reserved	

Table 6-7 : IP I/O, ID, INT Space Address Map

The TAMC220 will perform write cycles to the IP ID space.

Any access to the IP INT space will assert the IP INTSEL# signal on the selected IP slot. The TAMC220 will perform write cycles to the IP INT space.

The user should perform IP INT space read cycles on the desired IP slot to generate an IP INTSEL# cycle and read the interrupt vector from the IP module. For this read cycle the address must reflect if the IP INTSEL# cycle is for IP INT0# (additional offset 0x0) or for IP INT1# (additional offset 0x2).

6.1.4 IP Interface Memory Space Address Map

The PCI9030 BAR 4 space is used for the IP A-C Memory space (8/16-Bit).

PCI Base Address: PCI9030 PCI Base Address 4 (Offset 0x20 in the PCI9030 PCI configuration register space).

Offset (Base = PCI Base Address 4)		Size (Byte)	IP Slot	IP Space
Start	End			
0x0000_0000	0x007F_FFFF	8 M	A	MEM (16 bit)
0x0080_0000	0x00FF_FFFF	8 M	B	MEM (16 bit)
0x0100_0000	0x017F_FFFF	8 M	C	MEM (16 bit)
0x0180_0000	0x01FF_FFFF	8 M	Reserved	

Table 6-8 : IP Memory Space Address Map

6.1.5 IP Interface 8-Bit only Memory Space Address Map

The PCI9030 BAR 5 space is used for the IP A-C Memory space for 8-Bit only configurations.

PCI Base Address: PCI9030 PCI Base Address 5 (Offset 0x24 in the PCI9030 PCI configuration register space).

Offset (Base = PCI Base Address 5)		Size (Byte)	IP Slot	Description
Start	End			
0x0000_0000	0x003F_FFFF	4 M	A	MEM Space (8 bit)
0x0040_0000	0x007F_FFFF	4 M	B	MEM Space (8 bit)
0x0080_0000	0x00BF_FFFF	4 M	C	MEM Space (8 bit)
0x00C0_0000	0x00FF_FFFF	4 M	Reserved	

Table 6-9 : IP 8-Bit only Memory Space Address Map

The 8-Bit IP Memory space should be used for memory space linear byte addressing of IP modules that use IP data lines D[7:0] only.

6.2 Interrupts

6.2.1 Interrupt Sources

The TAMC220 provides the following main interrupt sources:

- IP_A_INT#[1:0]
- IP_B_INT#[1:0]
- IP_C_INT#[1:0]

All the IP interrupts are low active and may be set to level or edge sensitive by the IP Control registers.

Note that there are additional interrupt sources, since both the PCI9030 and the PEX8112 provide the capability of software controlled or internally generated interrupts. None of these interrupts are used for the main TAMC220 functionality.

6.2.2 Interrupt Mapping

The IP Interface address map provides an interrupt status register as well as register bits for interrupt enable control.

If any of the interrupt bits is set in the IP status register and the corresponding interrupt enable bit is set in the IP control register, the PCI9030 LINT1# line on the PCI9030 local bus is asserted.

Upon LINT1# assertion, the PCI9030 asserts the INTA# line on the PCI bus (if enabled in the PCI9030 Interrupt Control/Status register).

The INTA# line of the TAMC220 local PCI bus connects to the INTA# pin of the PEX8112.

On the PEX8112, in Forward Bridge mode, INTA# is an input from the PCI bus. The PEX8112 maps INTA# activity into Assert_INTx or Deassert_INTx messages on the PCI Express interface.

6.2.3 Interrupt Handling

Upon receiving a PCI Express Assert_INTA message, software should check the PCI9030 Interrupt Control/Status register. Interrupts from the IP interface will have the LINTi1 status bit set. The PCI9030 local bus interrupts are set to be level sensitive, so there is no need for clearing here.

Upon detecting IP interrupts, software should check the IP Status register to determine which IP interrupts are active.

For edge sensitive IP interrupts, the interrupt is cleared by writing a ‘1’ to the corresponding bit in the IP Status register. For level sensitive IP interrupts, interrupt clearing is scope of the IP module used.

6.3 M-LVDS Signals TCLKA and TCLKB

Two radial clocks are defined in AMC.0 that are used to distribute low jitter, high quality clocks by radial links from all AMC slots to the MCH. They are differential and bidirectional.

These two clocks, TCLKA and TCLKB, are implemented on the TAMC220 with an M-LVDS transceiver that translates both clocks into single-ended signals, each with a corresponding direction signal. TCLKA, TCLKB and the direction signals may be used on the µRTM for various purposes, which are not in the scope of this user manual.

The direction signals have to be driven by the µRTM. The µRTM has to make sure that these signals have a valid level if the TCLKx signals are used.

TCLKx_DIR Signal Level	TCLKx Direction from µRTM point of view
0	Input to µRTM
1	Output of µRTM

Table 6-10 : TCLKx and direction signals

For the pin assignment of these signals on J30, please see the chapter “I/O Connectors”.

6.4 Zone 3 Quiesce Actions

The TAMC220 does not support any quiesce actions (except for bypassing the JTAG chain), because all 150 I/O lines are directly controlled by the specific IP modules that are mounted on the TAMC220.

Any required Zone 3 quiesce actions have to be implemented on the µRTM.

7 Installation

This chapter contains general notes regarding installing the AMC module into a system.

7.1 Installation of IP Modules

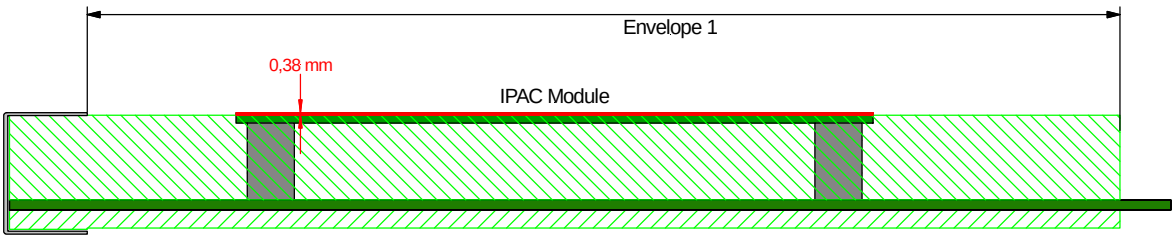
Before installing IP Modules, be sure that the power supply for the TAMC220 is turned off!

The component is sensitive to Electrostatic Discharge (ESD). Use an anti-static mat connected to a wristband when handling or installing the components.

Installing IP Modules on the TAMC220 is done by simply snapping them into the IP slot. The connectors are keyed, so the modules can only be installed correctly. After an IP has been installed, it can be fastened to the carrier board by screws. This is usually only necessary in high vibration or shock environments. Screws and spacers are required to fix a single IP on the TAMC220. They can be ordered from TEWS TECHNOLOGIES separately (Part number: TIPxxx-HK).

7.1.1 Component Height Violation on TAMC220-10R

The TAMC220 Mid-Size options (-10/-10R) will violate the MicroTCA.4 component height limits for Mid-Size Modules. With a standard IndustryPack Module of 1.6mm PCB thickness, the height limit is violated by 0.38mm. The figure below shows the violation of the AMC component envelope in red.



TAMC220-10R

Figure 7-1 : Component Height Violation

The TAMC220-10R is intended for the use in µTCA systems where the adjacent AMC module provides enough spacing (no components on the adjacent AMC modules back side) for the protruding IP Module. This allows improving the density of the µTCA system.

If any of the mounted IP Modules has devices assembled on its back side or if it cannot be guaranteed that the available spacing is sufficient, it is strongly recommended to use the full-height TAMC220-11R. It is within the responsibility of the user to carefully check if the Mid-Size module can be used in the system. Otherwise, damage to the TAMC220 or the slot it is used in may occur!

7.1.2 Voltage Limits on IP Modules

The AMC.0 specification limits the voltages on AMC modules to the following thresholds:

	DC voltage	AC voltage
Positive	+27V	+27V peak
Negative	-15V	-15V peak

Table 7-1 : Voltage Limits on IP Modules

For IP modules using voltages (including I/O voltages) that exceed these thresholds, an additional insulation to adjacent modules or carrier boards becomes necessary.

7.1.3 IP Power Supply Rating

IP Power Supply	Max. Current Rating (See fuse section for a detailed temperature table)
+5V	Max. 2A per IP slot (TA <= 23°C, less for higher temperatures)
+12V	Max. 500mA total, max. 200mA for an IP slot @ 23°C (e.g. the IP modules in slots A & B may use 200mA each on +12V while the IP module in slot C is using 100mA on +12V)
-12V	Max. 300mA total, max. 200mA for an IP slot @ 23°C (e.g. the IP module in slot A may use 200mA on -12V, while the IP module in slot B uses 100mA on -12V and the IP module in slot C does not use the -12V)

Table 7-2 : IP Power Supply Rating

7.1.4 IP Power Supply Filters

The TAMC220 provides RF filtering and decoupling capacitors on all IP power lines.

There are 3 power supply filters (Murata Type NFM61R00T361) for each IP slot, one for the +12V supply pin, one for the -12V supply pin and one for the two +5V supply pins.

7.1.5 IP Power Supply Fuses

There is a resettable fuse for the +5V supply at each IP slot.

Type: Bourns MF-MSMF200 (R1 max 0.080 Ohm)

IP 5V Fuse Operating Current Rating I_hold (Ampere) @ TA								
-40°C	**-20°C**	**0°C**	**23°C**	**40°C**	**50°C**	**60°C**	**70°C**	**85°C**
3.08	2.71	2.35	2.00	1.80	1.60	1.50	1.40	1.25

Table 7-3 : IP +5V Fuse Operating Current Rating

There is a resettable fuse for the +12V supply and a PolyFuse for the -12V supply at each IP slot.

Type: Bourns MF-NSMF020 (R1 max 2.60 Ohm)

IP +12V/-12V Fuse Operating Current Rating I_hold (Ampere) @ TA								
-40°C	**-20°C**	**0°C**	**23°C**	**40°C**	**50°C**	**60°C**	**70°C**	**85°C**
0.30	0.27	0.24	0.20	0.18	0.16	0.14	0.12	0.11

Table 7-4 : IP +12V/-12V Fuse Operating Current Rating

7.1.6 IP Logic Interface

The IP logic interface signals driven by the TAMC220 IP carrier have LVTTL signal levels (3.3V high level), except IP_RESET#, which is a 5V level signal.

IP modules may drive LVTTL, TTL or 5V CMOS signal levels.

7.1.7 IP I/O Interface

All pins of the IP slot I/O connectors are routed to the AirmaxVS™ connectors for Rear-I/O access; with a maximum current rating of 0.5A per pin (maximum rating of the AirmaxVS™ connector).

7.2 AMC Module Installation

During insertion and extraction, the operational state of the AMC is visible via the blue LED in the AMCs front panel. The following table lists all valid combinations of Hot-swap handle position and blue LED status, including a short description of what's going on.

Blue LED / Handle	On	Off	Long Blink	Short Blink
Open (Pulled out)	Extraction: Module can be extracted Insertion: Module is waiting for closed Handle	Module is waiting for hot swap negotiation	-	Hot swap negotiation in progress (Extraction)
Closed (Pushed all way in)	Module is waiting for hot swap negotiation	Module is active (operating)	Hot swap negotiation in progress (Insertion)	-

Figure 7-2 : Hot-Swap states

7.2.1 Insertion

Typical insertion sequence:

1. Insert the AMC module into its slot, with the board edges aligned to the card guides
2. Fasten the screws of the front plate, so the module cannot be pushed out by the µRTM if it is inserted afterwards
3. Make sure that the module handle is pushed into the inserted position
    a. Blue LED turns "ON." (Module is ready to attempt activation by the system)
    b. Blue LED starts "Long Blink" (Hot Swap Negotiation / Module activation in progress)
    c. Blue LED turns "OFF", and green LED turns "ON" (Module is ready and powered)

When the Blue LED does not go off but returns to the "ON" state, the module FRU information is invalid or the system cannot provide the power requested by the AMC module.

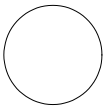
7.2.2 Extraction

Typical Extraction sequence:

1. Pull the module handle out ½ way
    a. Blue LED starts "Short Blink" (Hot Swap Negotiation in progress)
    b. Blue LED turns "ON" (Module is ready to be extracted)
2. Loosen the screws of the front plate
3. Pull the module handle out completely and extract the AMC module from the slot.

7.3 Zone 3 Keying

The TAMC220 provides the following female keying module:

N	A Rotation	View	Voltage Levels
0	NA	 View from the µRTM to the rear of the AMC white = clearance	Dependent on IP Modules

The keying module on the TAMC220 is just for alignment purposes, not for actual keying. This is due to the fact, that the voltage levels depend on the mounted IP modules and not the TAMC220 itself.

8 Indicators

8.1 LED Indicators

8.1.1 Front Panel LEDs

For a quick visual inspection, the AMC module provides the following front panel LEDs:

Figure 8-1 : Front Panel LED View

8.1.1.1 AMC Module related LEDs

LED	Color	State	Description
HS	Blue	Off	No Power or Module is ready for normal operation
		Short Blink	Hot-Swap negotiation (extraction)
		Long Blink	Hot-Swap negotiation (insertion)
		On	Module is ready to attempt activation by the system or Module is ready to be extracted
FAIL	Red	Off	No fault
		On	Failure or out of service status
ACT	Green	Off	Board is not powered up
		On	Board is powered and OK
		Blink	PCI bus activity

Table 8-1 : Front Panel LEDs (MMC controlled)

8.1.1.2 IP Module related LEDs

LED	Color	State	Description
ACK A	Green	On	Indicates IP Slot A 5V Power Supply valid during Payload Reset
		On (flash)	IP Slot A IP Access Acknowledge
		Off	IP Slot A No IP Access
ACK B	Green	On	Indicates IP Slot B 5V Power Supply valid during Payload Reset
		On (flash)	IP Slot B IP Access Acknowledge
		Off	IP Slot B No IP Access
ACK C	Green	On	Indicates IP Slot C 5V Power Supply valid during Payload Reset
		On (flash)	IP Slot C IP Access Acknowledge
		Off	IP Slot C No IP Access

Table 8-2 : Front Panel LEDs (IP Interface controlled)

8.1.2 Onboard LEDs

The AMC module provides a couple of board-status LEDs as shown below.

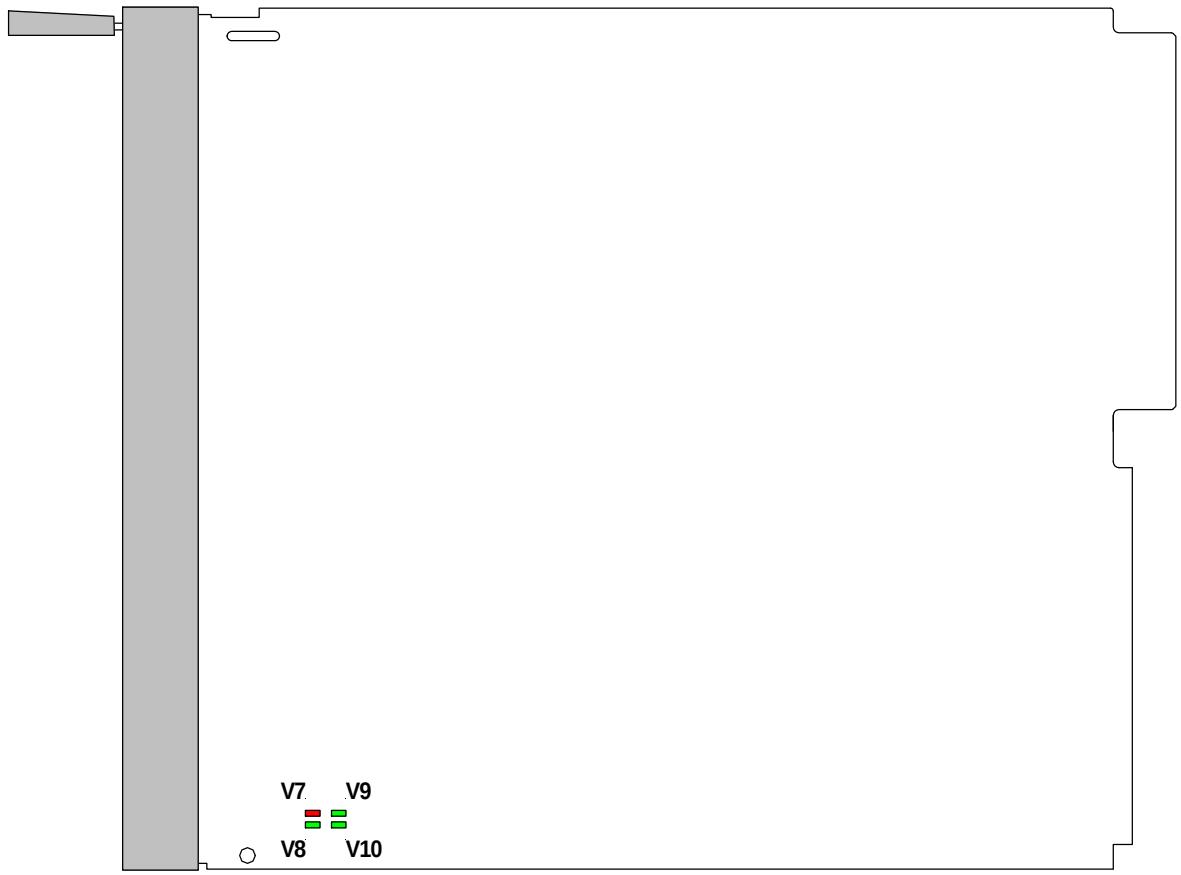


Figure 8-2 : Onboard LED View

LED		Color	State	Description
V7	Link Down	Red	Off	PCIe link is up
			On	PCIe link is down
V8	FPGA Done	Green	Off	FPGA is not configured
			On	FPGA is configured
V9	+5V Power Good	Green	Off	+5V Power Supply is not OK
			On	+5V Power Supply is OK
V10	+3.3V Power Good	Green	Off	+3.3V Power Supply is not OK
			On	+3.3V Power Supply is OK

Table 8-3 : Onboard LEDs

9 I/O Connectors

9.1 Overview

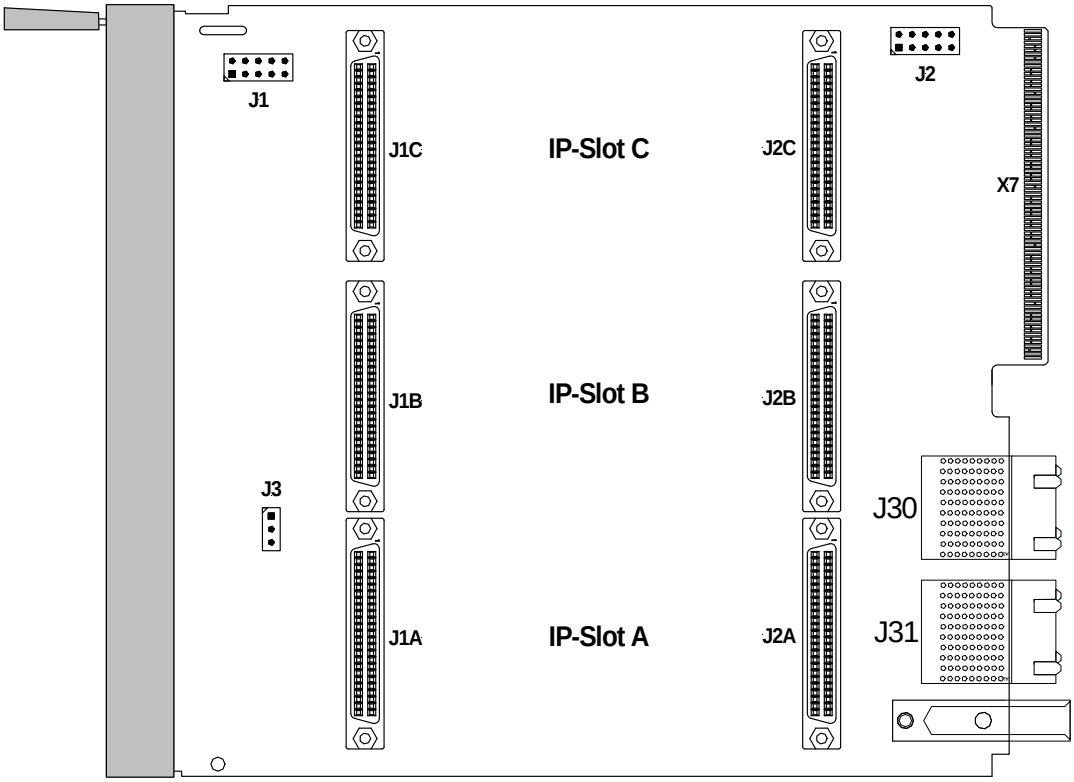


Figure 11-1 : Board Connectors and Headers

ID	Description
X7	AMC Connector
J1	Factory Only (Do not use)
J2	Factory Only (Do not use)
J3	IP Strobe Header
J30	MTCA.4 Rear-I/O and Management Signals Connector
J31	MTCA.4 Rear-I/O Connector
J1A	IP Slot A Logic Interface Connector
J2A	IP Slot A I/O Interface Connector
J1B	IP Slot B Logic Interface Connector
J2B	IP Slot B I/O Interface Connector
J1C	IP Slot C Logic Interface Connector
J2C	IP Slot C I/O Interface Connector

Table 11-1 : Board Connectors and Headers

9.2 Board Connectors

9.2.1 AMC Connector

This is an excerpt from the AMC-connector pin assignment. Only the user available signals are listed.

Pin	Signal	Description
44	Tx4+	AMC port 4 PCI Express Lane
45	Tx4-	
47	Rx4+	
48	Rx4-	
80	FCLKA+	Fabric Clock (100MHz)
81	FCLKA-	
78	TCLKB-	Differential Clock
77	TCLKB+	
75	TCLKA-	Differential Clock
74	TCLKA+	

Table 9-1 : Pin Assignment AMC Connector X7

9.2.2 IP A J1 Connector

Pin-Count	50
Connector Type	AMPLIMITE 0.50 Series
Source & Order Info	5173280-3 (Tyco)

Pin Assignment		
Pin	**Description**	**Note**
1	GND	
2	IP_A_CLK	
3	IP_RESET#	Common to all IP slots
4	IP_AC_D00	
5	IP_AC_D01	
6	IP_AC_D02	
7	IP_AC_D03	
8	IP_AC_D04	
9	IP_AC_D05	
10	IP_AC_D06	
11	IP_AC_D07	
12	IP_AC_D08	
13	IP_AC_D09	
14	IP_AC_D10	
15	IP_AC_D11	
16	IP_AC_D12	
17	IP_AC_D13	
18	IP_AC_D14	
19	IP_AC_D15	
20	IP_A_BS0#	
21	IP_A_BS1#	
22	IP_A_-12V	Fused for 200mA @ 23°C
23	IP_A_+12V	Fused for 200mA @ 23°C
24	IP_A_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
25	GND	
26	GND	
27	IP_A_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
28	IP_WRITE#	Common to all IP slots
29	IP_A_IDSEL#	
30	(IP_A_DMAREQ0#)	Not supported, Pull-up to 5V
31	IP_A_MEMSEL#	
32	(IP_A_DMAREQ1#)	Not supported, Pull-up to 5V
33	IP_A_INTSEL#	
34	(IP_A_DMAACK#)	Not supported, Pull-up to 5V
35	IP_A_IOSEL#	

36	IP_A_RESERVED0	Pull-up to 5V
37	IP_A1	Common to all IP slots
38	(IP_A_DMAEND#)	Not supported, Pull-up to 5V
39	IP_A2	Common to all IP slots
40	IP_A_ERROR#	Pull-up to 5V
41	IP_A3	Common to all IP slots
42	IP_A_INTREQ0#	Pull-up to 5V
43	IP_A4	Common to all IP slots
44	IP_A_INTREQ1#	Pull-up to 5V
45	IP_A5	Common to all IP slots
46	IP_A_STROBE#	Onboard header
47	IP_A6	Common to all IP slots
48	IP_A_ACK#	Pull-up to 5V
49	IP_A_RESERVED1	Pull-up to 5V
50	GND	

Table 9-2 : IP Slot A J1 Connector

9.2.3 IP B J1 Connector

Pin-Count	50
Connector Type	AMPLIMITE 0.50 Series
Source & Order Info	5173280-3 (Tyco)

Pin Assignment		
Pin	**Description**	**Note**
1	GND	
2	IP_B_CLK	
3	IP_RESET#	Common to all IP slots
4	IP_B_D00	
5	IP_ B_D01	
6	IP_B_D02	
7	IP_B_D03	
8	IP_B_D04	
9	IP_B_D05	
10	IP_B_D06	
11	IP_B_D07	
12	IP_B_D08	
13	IP_B_D09	
14	IP_B_D10	
15	IP_B_D11	
16	IP_B_D12	
17	IP_B_D13	
18	IP_B_D14	
19	IP_B_D15	
20	IP_B_BS0#	
21	IP_B_BS1#	
22	IP_B_-12V	Fused for 200mA @ 23°C
23	IP_B_+12V	Fused for 200mA @ 23°C
24	IP_B_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
25	GND	
26	GND	
27	IP_B_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
28	IP_WRITE#	Common to all IP slots
29	IP_B_IDSEL#	
30	(IP_B_DMAREQ0#)	Not supported, Pull-up to 5V
31	IP_B_MEMSEL#	
32	(IP_B_DMAREQ1#)	Not supported, Pull-up to 5V
33	IP_B_INTSEL#	
34	(IP_B_DMAACK#)	Not supported,

		Pull-up to 5V
35	IP_B_IOSEL#	
36	IP_B_RESERVED0	Pull-up to 5V
37	IP_A1	Common to all IP slots
38	(IP_B_DMAEND#)	Not supported, Pull-up to 5V
39	IP_A2	Common to all IP slots
40	IP_B_ERROR#	Pull-up to 5V
41	IP_A3	Common to all IP slots
42	IP_B_INTREQ0#	Pull-up to 5V
43	IP_A4	Common to all IP slots
44	IP_B_INTREQ1#	Pull-up to 5V
45	IP_A5	Common to all IP slots
46	IP_B_STROBE#	Onboard header
47	IP_A6	Common to all IP slots
48	IP_B_ACK#	Pull-up to 5V
49	IP_B_RESERVED1	Pull-up to 5V
50	GND	

Table 9-3 : IP Slot B J1 Connector

9.2.4 IP C J1 Connector

Pin-Count	50
Connector Type	AMPLIMITE 0.50 Series
Source & Order Info	5173280-3 (Tyco)

Pin Assignment		
Pin	**Description**	**Note**
1	GND	
2	IP_C_CLK	
3	IP_RESET#	Common to all IP slots
4	IP_AC_D00	
5	IP_AC_D01	
6	IP_AC_D02	
7	IP_AC_D03	
8	IP_AC_D04	
9	IP_AC_D05	
10	IP_AC_D06	
11	IP_AC_D07	
12	IP_AC_D08	
13	IP_AC_D09	
14	IP_AC_D10	
15	IP_AC_D11	
16	IP_AC_D12	
17	IP_AC_D13	
18	IP_AC_D14	
19	IP_AC_D15	
20	IP_C_BS0#	
21	IP_C_BS1#	
22	IP_C_-12V	Fused for 200mA @ 23°C
23	IP_C_+12V	Fused for 200mA @ 23°C
24	IP_C_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
25	GND	
26	GND	
27	IP_C_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
28	IP_WRITE#	Common to all IP slots
29	IP_C_IDSEL#	
30	(IP_C_DMAREQ0#)	Not supported, Pull-up to 5V
31	IP_C_MEMSEL#	
32	(IP_C_DMAREQ1#)	Not supported, Pull-up to 5V
33	IP_C_INTSEL#	
34	(IP_C_DMAACK#)	Not supported,

		Pull-up to 5V
35	IP_C_IOSEL#	
36	IP_C_RESERVED0	Pull-up to 5V
37	IP_A1	Common to all IP slots
38	(IP_C_DMAEND#)	Not supported, Pull-up to 5V
39	IP_A2	Common to all IP slots
40	IP_C_ERROR#	Pull-up to 5V
41	IP_A3	Common to all IP slots
42	IP_C_INTREQ0#	Pull-up to 5V
43	IP_A4	Common to all IP slots
44	IP_C_INTREQ1#	Pull-up to 5V
45	IP_A5	Common to all IP slots
46	IP_C_STROBE#	Onboard header
47	IP_A6	Common to all IP slots
48	IP_C_ACK#	Pull-up to 5V
49	IP_C_RESERVED1	Pull-up to 5V
50	GND	

Table 9-4 : IP Slot C J1 Connector

9.2.5 IP x J2 Connector (x = A, B, C)

Pin-Count	50
Connector Type	AMPLIMITE 0.50 Series
Source & Order Info	5173280-3 (Tyco)

Pin Assignment				
Pin	**Description**		**Pin**	**Description**
1	IO_x_01		26	IO_x_26
2	IO_x_02		27	IO_x_27
3	IO_x_03		28	IO_x_28
4	IO_x_04		29	IO_x_29
5	IO_x_05		30	IO_x_30
6	IO_x_06		31	IO_x_31
7	IO_x_07		32	IO_x_32
8	IO_x_08		33	IO_x_33
9	IO_x_09		34	IO_x_34
10	IO_x_10		35	IO_x_35
11	IO_x_11		36	IO_x_36
12	IO_x_12		37	IO_x_37
13	IO_x_13		38	IO_x_38
14	IO_x_14		39	IO_x_39
15	IO_x_15		40	IO_x_40
16	IO_x_16		41	IO_x_41
17	IO_x_17		42	IO_x_42
18	IO_x_18		43	IO_x_43
19	IO_x_19		44	IO_x_44
20	IO_x_20		45	IO_x_45
21	IO_x_21		46	IO_x_46
22	IO_x_22		47	IO_x_47
23	IO_x_23		48	IO_x_48
24	IO_x_24		49	IO_x_49
25	IO_x_25		50	IO_x_50

Table 9-5 : IP J2 I/O Connectors (onboard)

9.2.6 IP Strobe Signal Header

The Strobe Header may be used to connect the Strobe signals of mounted IP modules.

Pin-Count	3
Connector Type	Std. 1-row 3 Pin Header
Source & Order Info	-

Pin Assignment		
Pin	**Description**	**Note**
1	IP_A_STROBE#	Square pad
2	IP_B_STROBE#	
3	IP_C_STROBE#	

Table 9-6 : J3 IP Strobe Signal Header

9.2.7 J30 Rear-I/O

Pin-Count	90
Connector Type	FCI AirmaxVS®, Female
Source & Order Info	FCI 10056335-101LF

Pin Assignment									
	I	**H**	**G**	**F**	**E**	**D**	**C**	**B**	**A**
1	IO_C_26	IO_C_01	PWR	GND	PWR	IO_C_27	IO_C_28	IO_C_02	IO_C_03
2	IO_C_29	IO_C_30	GND	PWR	PWR	IO_C_04	IO_C_05	IO_C_31	IO_C_32
3	IO_C_06	IO_C_07	PWR	GND	PWR	IO_C_33	IO_C_34	IO_C_08	IO_C_09
4	IO_C_35	IO_C_36	GND	PWR	PWR	IO_C_10	IO_C_11	IO_C_37	IO_C_38
5	IO_C_12	IO_C_13	MP	GND	SCL	IO_C_39	IO_C_40	IO_C_14	IO_C_15
6	IO_C_41	IO_C_42	GND	SDA	PS#	IO_C_16	IO_C_17	IO_C_43	IO_C_44
7	IO_C_18	IO_C_19	TCLKA	GND	TDO*)	IO_C_45	IO_C_46	IO_C_20	IO_C_21
8	IO_C_47	IO_C_48	GND	TCLKA_DIR	TDI*)	IO_C_22	IO_C_23	IO_C_49	IO_C_50
9	IO_C_24	IO_C_25	TCLKB	GND	TCK*)	IO_B_26	IO_B_01	IO_B_27	IO_B_28
10	IO_B_02	IO_B_03	GND	TCLKB_DIR	TMS*)	IO_B_29	IO_B_30	IO_B_04	IO_B_05

***)** = See chapter "µRTM Hardware Requirements" for details about the inclusion of the µRTM into the TAMC220 JTAG chain.

9.2.8 J31 Rear-I/O

Pin-Count	90
Connector Type	FCI AirmaxVS®, Female
Source & Order Info	FCI 10056335-101LF

	I	**H**	**G**	**F**	**E**	**D**	**C**	**B**	**A**
1	IO_B_31	IO_B_32	IO_B_06	IO_B_07	IO_B_33	IO_B_34	IO_B_08	IO_B_09	IO_B_35
2	IO_B_36	IO_B_10	IO_B_11	IO_B_37	IO_B_38	IO_B_12	IO_B_13	IO_B_39	IO_B_40
3	IO_B_14	IO_B_15	IO_B_41	IO_B_42	IO_B_16	IO_B_17	IO_B_43	IO_B_44	IO_B_18
4	IO_B_19	IO_B_45	IO_B_46	IO_B_20	IO_B_21	IO_B_47	IO_B_48	IO_B_22	IO_B_23
5	IO_B_49	IO_B_50	IO_B_24	IO_B_25	IO_A_26	IO_A_01	IO_A_27	IO_A_28	IO_A_02
6	IO_A_03	IO_A_29	IO_A_30	IO_A_04	IO_A_05	IO_A_31	IO_A_32	IO_A_06	IO_A_07
7	IO_A_33	IO_A_34	IO_A_08	IO_A_09	IO_A_35	IO_A_36	IO_A_10	IO_A_11	IO_A_37
8	IO_A_38	IO_A_12	IO_A_13	IO_A_39	IO_A_40	IO_A_14	IO_A_15	IO_A_41	IO_A_42
9	IO_A_16	IO_A_17	IO_A_43	IO_A_44	IO_A_18	IO_A_19	IO_A_45	IO_A_46	IO_A_20
10	IO_A_21	IO_A_47	IO_A_48	IO_A_22	IO_A_23	IO_A_49	IO_A_50	IO_A_24	IO_A_25

10 µRTM Requirements

10.1 µRTM Mechanical Requirements

10.1.1 Connector Type

Pin-Count	90
Connector Type	FCI AirmaxVS®, Male
Source & Order Info	FCI 10034249-101LF (without Short-Pin) FCI 10034249-111LF (with Short-Pin)

10.1.2 Connector Placement & PCB Outline

Only dimensions that differ from MTCA.4 are shown in the diagram. For all other dimensions, MTCA.4 shall be used.

Dimensions are color-marked for the placement of the connectors, the keying pin and for modifications of the board outline.

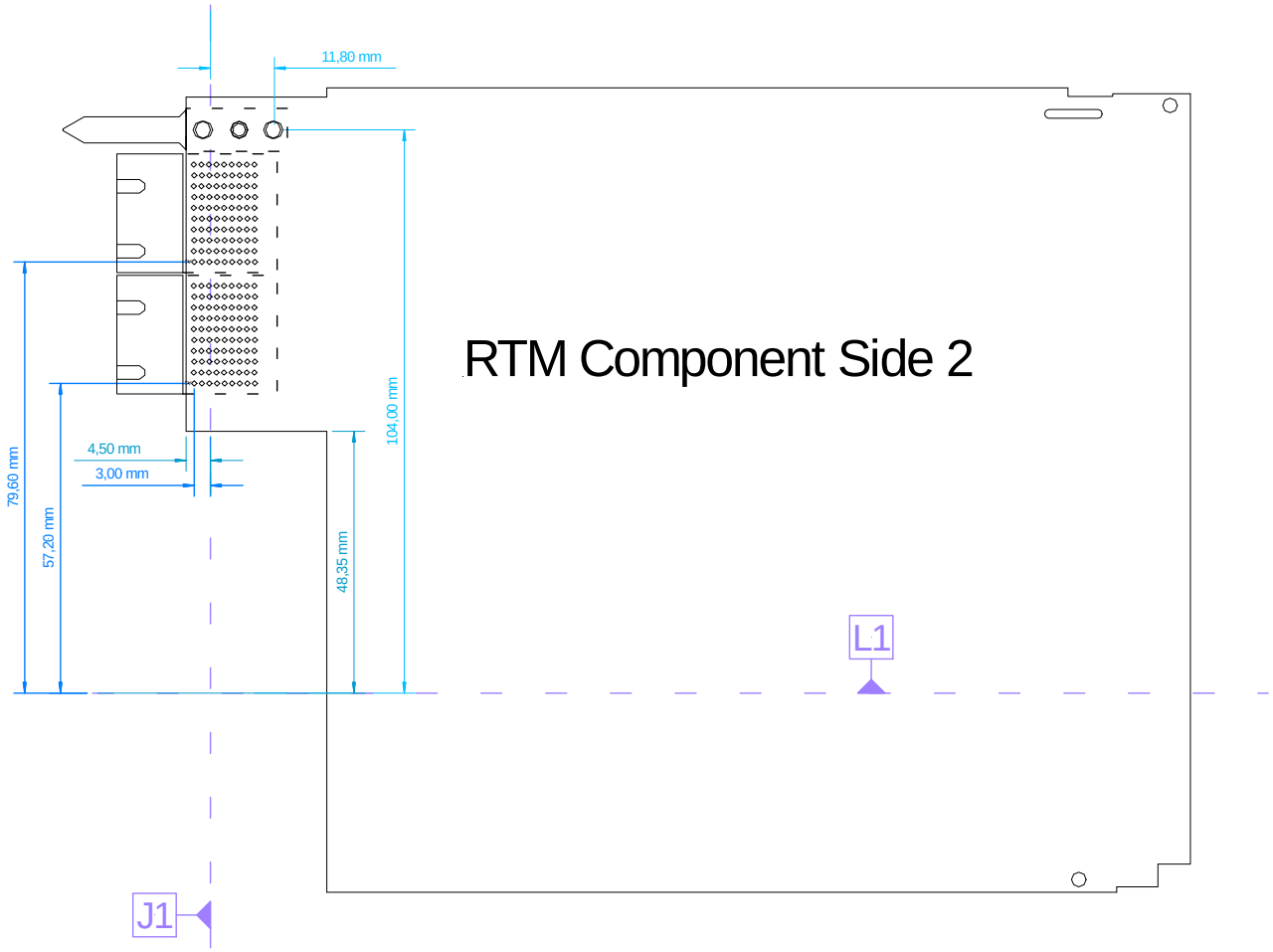


Figure 10-1: µRTM Board Outline

10.1.3 Pin Assignment

µRTMs shall implement pin assignment matching the pin assignment of the TAMC220. Please see chapter "I/O Connectors" for details.

10.1.4 Keying

µRTMs shall implement keying as defined in MTCA.4 R1.0.

10.2 µRTM Hardware Requirements

10.2.1 Present Detection

The µRTM must connect the µRTM_PS# signal to the ground signal.

The TAMC220 provides a pull-up resistor (to the AMC-MP power supply rail) on the µRTM_PS# signal.

Note: The TAMC220 monitors the µRTM_PS# signal for µRTM module present detection. The TAMC220 will gate the AMC Management Power to the µRTM upon µRTM present detection.

10.2.2 Power Good Detection

The µRTM must provide a kind of overall Payload Power Good signal via an Open-Drain Driver (pull-up to Management Power). See I2C I/O Extender section for additional information.

10.2.3 JTAG Signals

The TAMC220 provides 3.3V level JTAG signals at the Zone 3 Interface.

The µRTM module must not break the JTAG chain. If the µRTM module does not use JTAG, µRTM_TDI must be connected to µRTM_TDO on the µRTM module.

The JTAG signals at the Zone 3 Interface are not powered by the management power supply.

The JTAG signals (except TDO) will be driven by the TAMC220 when all of the following is true:

- The µRTM is present
- The AMC has enabled payload power to the µRTM (µRTM is compatible)

The µRTM must provide means for safe JTAG signal levels during the time the µRTM JTAG devices are not powered properly.

10.2.4 I2C Management Bus

The TAMC220 supports the following I2C devices / addresses on the µRTM I2C management bus:

Device	Supported Devices	I2C Address	
EEPROM	AT24C32 or compatible	50h	1010000b
Temperature Sensor	LM75 or compatible	48h	1001000b
8-bit I2C I/O Port	PCA9534 or compatible	20h	0100000b

Table 10-1: Supported µRTM I2C Devices

Other I2C devices or addresses are not supported and are also not allowed.

The TAMC220 reserves the following I2C addresses for the AMC board: 70h (1110000), 71h (1110001).

All devices on the µRTM modules I2C management bus must be powered by the µRTM_MP power supply.

MTCA.4 limits the total current for the µRTM_MP power supply to 30mA. This must be taken into account for the µRTM hardware design (LED's etc.).

The µRTM must provide pull-up resistors to µRTM_MP on the I2C 2-wire signals.

10.2.4.1 EEPROM

The µRTM must provide a serial EEPROM on the I2C management bus (AT24C32 or compatible).

The EEPROM I2C address must be 50h (1010000b).

The EEPROM must contain FRU information for the µRTM module.

The EEPROM must be powered by the µRTM_MP power supply.

10.2.4.2 Temperature Sensor

The µRTM must provide a temperature sensor on the I2C management bus, as defined below.

The Temperature Sensor must be powered by the µRTM_MP power supply.

A LM75 or compatible device with I2C address 48h (1001000b) must be used.

10.2.4.3 I2C I/O Extender

The µRTM must provide an 8-bit I2C I/O Extender device on the I2C management bus used for controlling certain management signals on the µRTM.

The I2C I/O device must be powered by the µRTM_MP power supply.

A PCA9534 or compatible device with I2C address 20h (0100000b) must be used.

The TAMC220 supports the following pin/signal assignment for the µRTM I2C I/O Extender device:

I/O Port	I/O Direction	Description
7	I	Payload Power Supply Status 0 = Payload Power Supply status is not Good 1 = Payload Power Supply status is Good
6	O	Payload (Zone 3) Enable Control 0 = Payload Enable signal not active 1 = Payload Enable signal active
5	O	Payload Reset Control 0 = Payload Reset signal not active 1 = Payload Reset signal active
4	O	EEPROM Write Protect Control 0 = EEPROM write protection not active 1 = EEPROM write protection active
3	O	LED2 (Green) Control 0 = LED off 1 = LED on
2	O	LED1 (Red) Control 0 = LED off 1 = LED on
1	O	Hot Swap LED (Blue) Control 0 = LED off 1 = LED on
0	I	Handle Status 0 = Handle/Switch closed 1 = Handle/Switch open

Table 10-2: µRTM I2C I/O Extender Port Assignment

Per default (after power-up) all the I2C I/O ports are inputs.

External circuitry on the µRTM must ensure the proper function according to the µRTM I2C I/O Extender Port Assignment. E.g. the µRTM board logic must ensure that the Blue Hot Swap LED defaults to the ON state and that LED1 and LED2 default to the OFF state.

Therefore, the Blue Hot Swap LED should not be connected directly to the I2C I/O port. In general, it is recommended to use external LED drivers (controlled by the I2C I/O ports).

It is also recommended that the reset signal defaults to the active state and the enable signal defaults to the not-active state.

Please see the following example adding a single 74LVC06-type device (6x Inverter with open drain output).

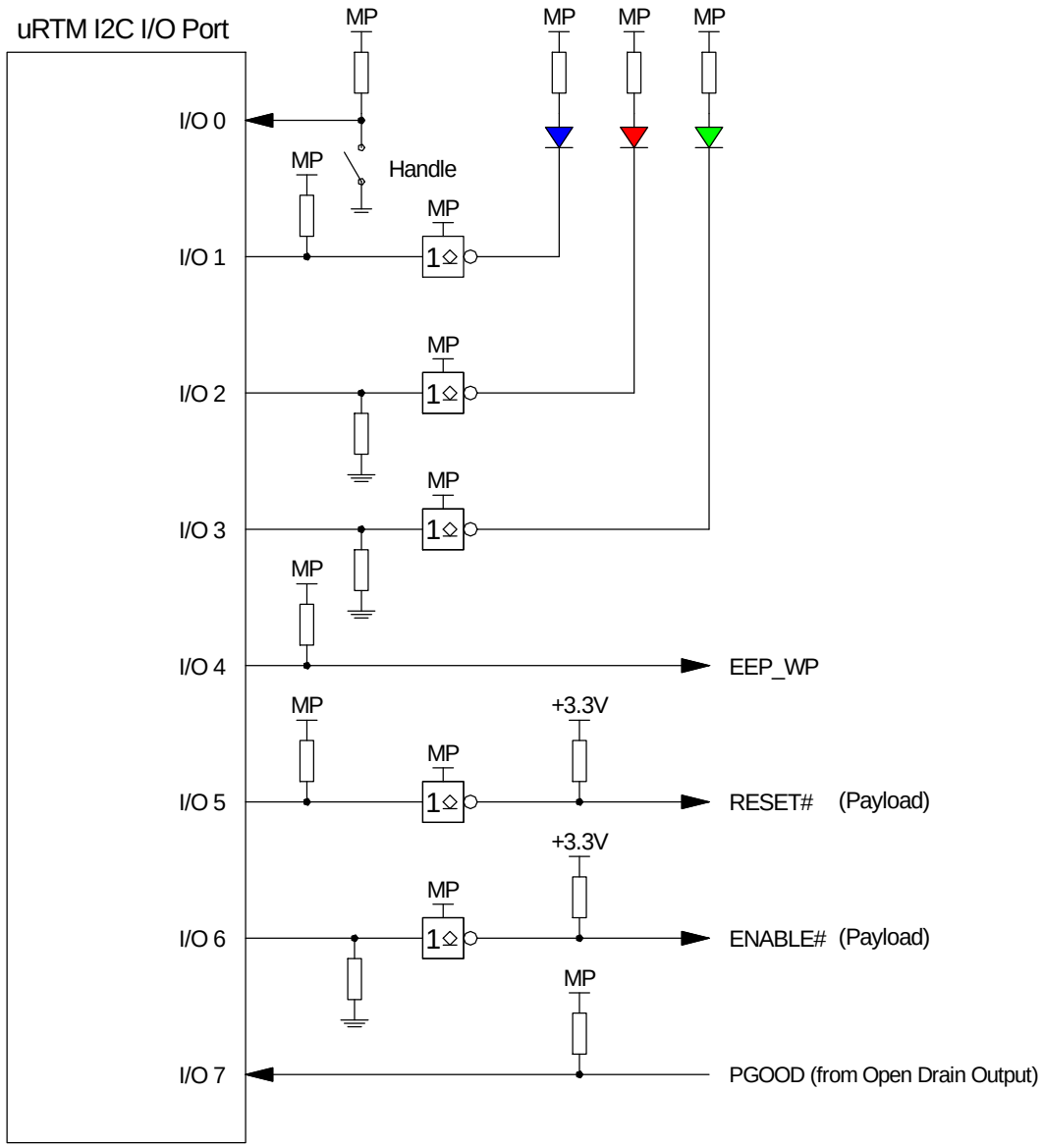


Figure 10-1: Example I2C I/O Extender Interface on µRTM

10.3 µRTM FRU Information Requirements

The EEPROM on the µRTM I2C bus must contain FRU information data for the µRTM.

The FRU information must include:

- Common Header
- Zone 3 Interface Compatibility Record

10.3.1 Common Header

The µRTM FRU information (Common Header) must start at EEPROM address 0h.

Offset	Length	Description
0	1	Common Header Format Version [7:4] Reserved. Write as 0h. [3:0] Format Version Number (Value 1h)
1	1	Internal Use Area Starting Offset (in multiples of 8 bytes) 00h indicates that this area is not present.
2	1	Chassis Info Area Starting Offset (in multiples of 8 bytes) 00h indicates that this area is not present.
3	1	Board Area Starting Offset (in multiples of 8 bytes) 00h indicates that this area is not present.
4	1	Product Info Area Starting Offset (in multiples of 8 bytes) 00h indicates that this area is not present.
5	3	Multi-Record Area Starting Offset (in multiples of 8 bytes) 00h indicates that this area is not present.
6	1	Value 00h
7	1	Common Header Checksum (zero checksum)

Table 10-3: µRTM FRU Common Header

10.3.2 Zone 3 Interface Compatibility Record

In the Multi-Record Area, the µRTM module must provide at least one Zone 3 Interface Compatibility Record defined as follows.

Offset	Length	Description
0	1	Record Type ID Value C0h (OEM)
1	1	[7:7] End of list. Set to one for the last record. [6:4] Reserved. Write as 0h. [3:0] Record format version (2h for this definition)
2	1	Record Length
3	1	Record Checksum Holds the zero checksum of the record
4	1	Header Checksum Holds the zero checksum of the header
5	3	Manufacturer ID 0x00315A, LSB first
8	1	PICMG Record ID Value 30h
9	1	Record Format Version Value 1h
10	1	Type of Interface Identifier 3h = OEM interface identifier
11	3	Interface Identifier Body Manufacturer ID (IANA) of the OEM that owns the definition of the interface. LS Byte first. 0x0071E3 (TEWS Technologies Private Enterprise Number)
14	4	Interface Identifier Body OEM-defined interface designator, 32 bits, LS Byte first 0x8DC0000 (0x8 = TAMC, 0xDC = 220)

Table 10-4: µRTM FRU Zone 3 Interface Compatibility Record

If any Zone 3 Interface Compatibility record in the µRTM's FRU information matches the Zone 3 Interface Compatibility record shown, the TAMC220 considers the µRTM to be compatible. Otherwise the TAMC220 considers the µRTM to be incompatible.

The Zone 3 Interface Compatibility records are considered as matching if the records are the same length and are identical from offset 9 to the end of the record. Otherwise the record is considered as not matching.

10.3.3 Sensor Data Records

The TAMC220 MMC supports an SDR for the µRTM Hot Swap Sensor and one LM75 temperature sensor on the µRTM, located in the TAMC220 FRU EEPROM. The handling of both sensors is completely in the hands of the TAMC220 MMC.