The Embedded I/O Company

TAMC532-TM

32x Gaussian Shaping MTCA.4 µRTM

Version 1.0

User Manual

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TAMC532-TM-10R

MTCA.4 Class A2.1 µRTM, Mid-Size front panel, 32 x Gaussian shaping amplifier, differential inputs

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	April 2015

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1 Product Description

The TAMC532-TM is a MTCA.4 compliant Micro Rear Transition Module for the TAMC532. Eight RJ45 connectors are used as input connectors for the 32 differential analog inputs of the TAMC532-TM.

Each of the 32 differential analog inputs is connected to its own filter block.

The filter block consists of an input Buffer with programmable gain, a Gaussian shaping amplifier with programmable shaping time and an output buffer with adjustable baseline shift. The Pole-Zero compensation at the input differentiator is adjustable by use of a digital potentiometer. This is ideal for readout of charge sensitive preamplifiers.

The baseline shift is useful if the input signal is always positive (or negative). It allows to increase the gain and to make better use of the ADC input voltage range.

All settings are common for groups of 8 inputs.

The output of the filter block is accessible by the AMC via Zone 3.

A Clock input is available in the TAMC532-TM front panel as well. A coaxial connector is used to feed the single-ended signal into the TAMC532-TM. After a single-ended to LVDS conversion, the signal is connected to Zone 3, RTM_CLK0.

Zone 3 pin assignment and the µRTM management implementation are MTCA.4 compliant and comply with Zone 3 Classification Recommendation according to Class A2.1.

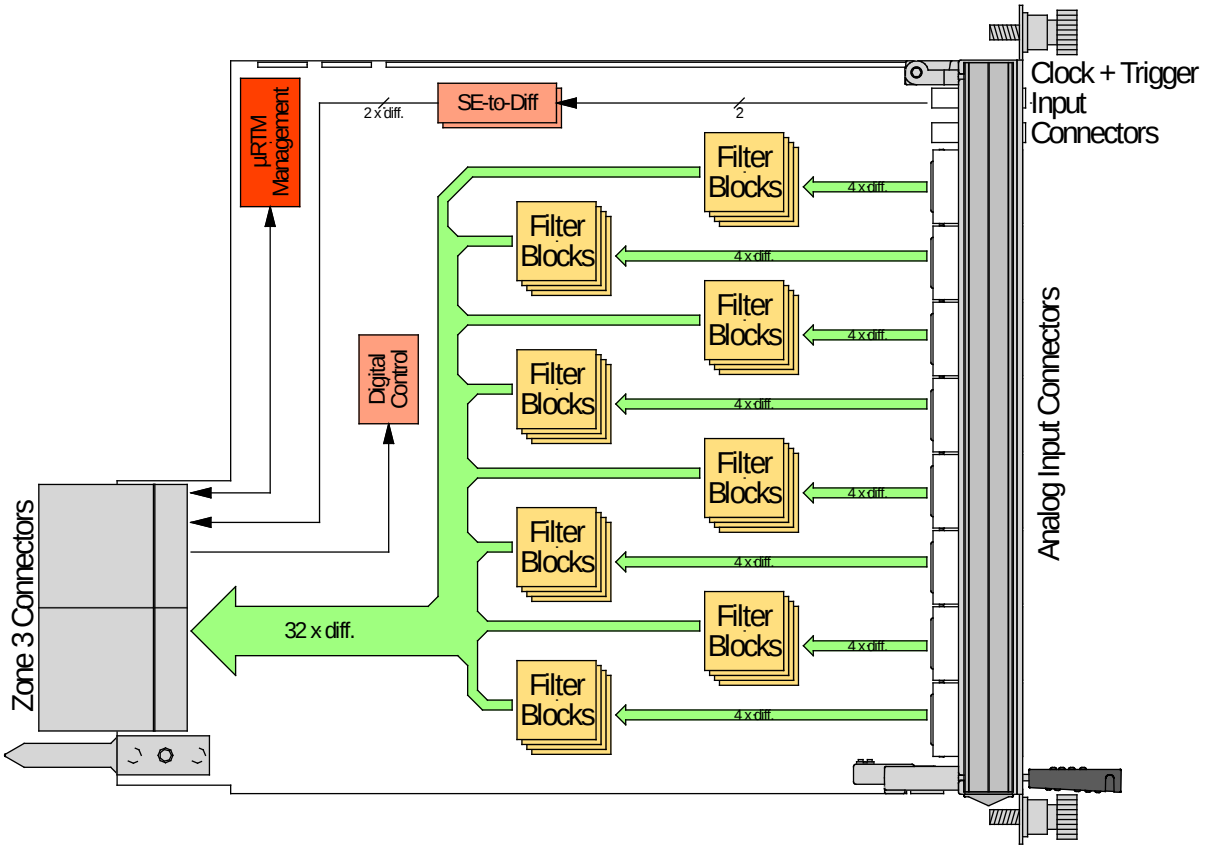

Figure 1-1 : Block Diagram

2 Technical Specification

AMC Interface		
Mechanical Interface	Rear Transition Module conforming to MTCA.4 Class A2.1 Module Type: Double Mid-Size Module (-10R)	
IPMI Support		
IPMI Version	1.5	
Front Panel LEDs	Blue Hot-Swap LED Red Failure Indication LED (LED1) Green Board OK (LED2)	
I2C Temperature Sensor	SE95, register compatible to LM75	
I2C EEPROM	M24C32 24AA025E48 (Unique-ID)	
Analog Inputs		
Connector	8 x RJ45	
Termination	100 Ohm differential	
Differential Voltage	±2.5V	
Common Mode Range	±3.8V	
Clock Input		
Connector	1 x MMCX	
Termination	50 Ohm	
Input voltage	0.2V – 3V (on-board AC-coupling)	
Trigger Input		
Connector	1 x MMCX	
Termination	50 Ohm	
Input voltage	0.2V – 3V (on-board AC-coupling)	
Physical Data		
Power Requirements	Management Power: 20mA typical @ +3.3V DC	
	Typical 1.5A @ +12V DC	
Temperature Range	Operating	0°C to +70°C
	Storage	0°C to +70°C
MTBF	169.000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	250 g	

Table 2-1 : Technical Specification

3 Handling and Operating Instructions

3.1 ESD Protection

The AMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done in an ESD/EOS protected Area.

3.2 Thermal Considerations

Forced air cooling is recommended during operation.
Without forced air cooling, damage to the device could occur.

3.3 Zone 3 I/O Voltage

Prior to inserting the TAMC532-TM into a system, make sure that the selected Zone 3 I/O voltage is compatible with the corresponding front AMC.

4 IPMI Support

The Front-AMC module provides a Module Management Controller (MMC) that performs health monitoring, hot-swap functionality and stores the Field Replaceable Unit (FRU) information. The MMC communicates via an Intelligent Platform Management Interface (IPMI) with superordinated IPMI controllers.

The TAMC532-TM is controlled by the Front-AMCs MMC and provides a temperature sensor, FRU information and management signals for hot swap handle status and LED control.

4.1 Temperature and Voltage Sensors

The MMC on the Front-AMC module monitors sensors on-board the TAMC532-TM and signals sensor events to the superordinated IPMI controller / shelf manager. Available sensors are listed in the table below.

Sensor Number	Signal Type	Thresholds	Signal Monitored
0	Event	-	Hot-swap switch
1	Temperature	lnr lcr lnc unc ucr unr	SE95

unr: upper non-recoverable, ucr: upper critical, unc: upper non-critical
lnr: lower non-recoverable, lcr: lower critical, lnc: lower non-critical

Table 4-1 : Temperature and Voltage Sensors

4.2 FRU Information

The TAMC532-TM stores the module FRU information in a non-volatile EEPROM. The actual FRU information data is shown below.

Area	Size (in Bytes)	Writeable
Common Header	8	no
Internal Use Area	0	no
Chassis Info Area	0	no
Board Info Area	variable	no
Product Info Area	variable	no
Multi Record Area		
Zone 3 Interface Compatibility Record	variable	yes

Table 4-2 : FRU Information

4.2.1 Board Info Area

Product Information	Value
Version	1
Language Code	0x00 - English
Manufacturer date/time	determined at manufacturing
Board manufacturer	TEWS TECHNOLOGIES GmbH
Board product name	TAMC532-TM
Board serial number	determined at manufacturing (see board label)
Board part number	TAMC532-TM-xxR -xx = -10

Table 4-3 : Board Info Area

4.2.2 Product Info Area

Product Information	Value
Version	1
Language Code	0x00 - English
Product manufacturer	TEWS TECHNOLOGIES GmbH
Product name	TAMC532-TM
Board part/model number	TAMC532-TM-xxR -xx = -10
Product version	V1.0 Rev. A (see board label)
Product serial number	determined at manufacturing (see board label)
Asset tag	= Product serial Number

Table 4-4 : Product Info Area

4.2.3 Multi Record Area

4.2.3.1 Zone 3 Interface Compatibility Record

Product Information	Value
Version	1
Type of Interface Identifier	0x03 - OEM Interface Identifier
Manufacturer ID (IANA) of the OEM	0x0071E3 (TEWS TECHNOLOGIES GmbH)
OEM-defined interface designator	0x82140000 (0x8 = TAMC, 0x214 = 532)

Table 4-5 : Zone 3 Interface Compatibility Record

If the Zone 3 Interface Compatibility record matches the Zone 3 Interface Compatibility record in the AMC, the AMC considers the µRTM to be compatible. Otherwise, the AMC considers the µRTM to be incompatible.

The Zone 3 Interface Compatibility records are considered as matching if the records are the same length and are identical from offset 9 to the end of the record. Otherwise the record is considered as not matching.

4.2.3.2 Module Current Requirements

As per µTCA.4 specification the TAMC532-TM current requirement must be included into the Front-AMC module's Module Current Requirement record.

5 Functional Description

5.1 Analog Input Channel

The TAMC532-TM provides 32 identical analog input channels with Gaussian shaper signal conditioning. Each input channel consists of:

- Input buffer
- Gaussian shaper
- Output buffer

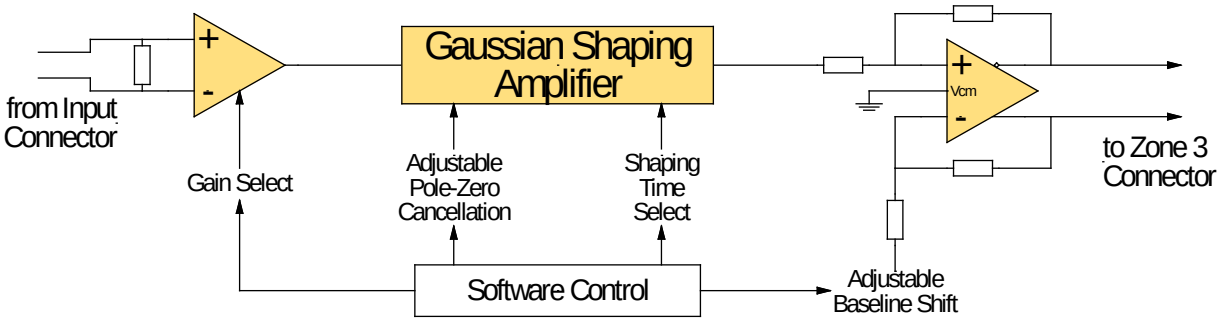

Figure 5-1 : Analog Input Channel

5.1.1 Input Buffer

An AD8130 differential receiver amplifier is used as input buffer. The differential input voltage range is ±2.5V. Selectable input buffer gains are 1, 2, 5 and 10.

Gain selection is done via the RCC, and common of groups of 8 channels.

Each input provides a differential 100 Ohm termination.

Differential input voltage range is ±2.5V max.

Common Mode input voltage range is ±3.8V max.

5.1.2 Gaussian Shaper

The Shaper consists of the parts:

- o The differentiator with Pole-Zero compensation
- o 1st second order Sallen-Key Filter
- o 2nd second order Sallen-Key Filter

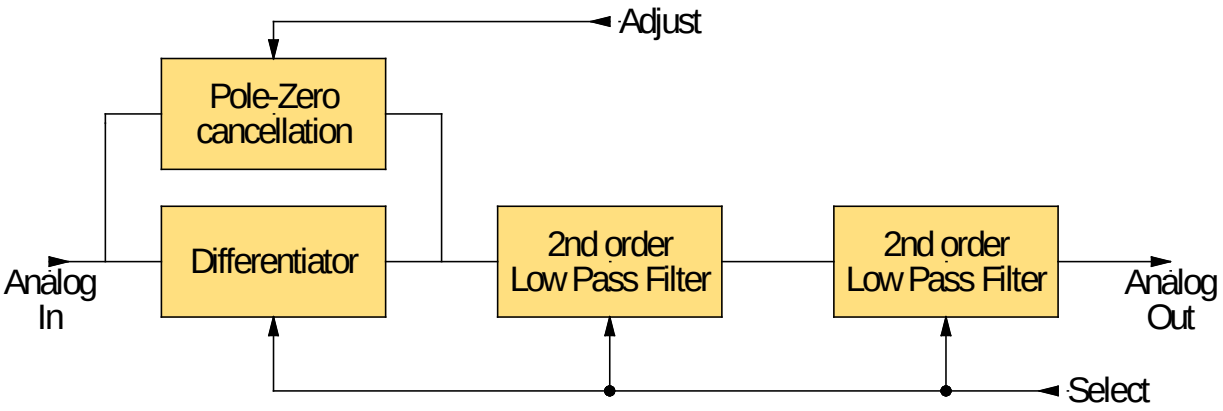

Figure 5-2 : Gaussian Shaper

The resistor setting for pole-zero cancellation is done via the RCC, and unique for each channel.

The time constants of differentiator and both low pass filters are adjusted according to selected filter time.

Filter time selection is done via the RCC and common for groups of 8 inputs.

Each second order Sallen-Key filter has a fixed gain of 3.3.

5.1.3 Output Buffer

A THS4504 fully differential operational amplifier is used as output buffer. The gain is fixed to 0.4, and the output common mode voltage is 0V.

ADCs have (nearly) always a bipolar input voltage range. In shaper applications, the signal is usually only positive or negative. As a result, the half ADC resolution is wasted in this case. To avoid this, a Baseline Shift is implemented at the output buffer.

The baseline shift adds an adjustable offset of up to ±1V to the differential output signal. This improves ADC resolution in applications with mainly positive or negative signals.

Baseline shifter setting is done via the RCC, and common for groups of eight channels.

The power-down pin of the THS4504 is used to keep all amplifiers disabled until they are enabled by the µRTM management and via the RCC.

5.2 Clock Input

The TAMC532-TM provides a 50 Ohm terminated, ac-coupled, single ended Input via coaxial connector for RTM_CLK0.

The clock is converted into an LVDS signal and connected to RTM_CLK0± at the Zone 3 interface. After Reset, the buffer has to be enabled from the AMC by writing to the appropriate RCC register.

5.3 Trigger Input

The TAMC532-TM provides a 50 Ohm terminated, ac-coupled, single ended Input via coaxial connector for the trigger input. Despite the ac-coupling, also dc-signals are supported after an initial edge.

The trigger is converted into an LVDS signal and connected to D8± at the Zone 3 interface. After Reset, the buffer has to be enabled from the AMC by writing to the appropriate RCC register.

5.4 Digital Control (RCC)

Control of the various adjustable settings of the TAMC532-TM is done via an RTM configuration controller (RCC). A simple I2C interface allows the AMC to take control over all RTM settings.

Zone 3 signals D3± are used to implement I^2C SCL (D3+) and SDA (D3-) signals.

RCC I^2C address is 0x84 for write, and 0x85 for read access. One-byte sub-addressing is used, i.e. the first byte written to the RCC must be the I^2C offset of the desired register. Unlimited subsequent write accesses to the whole register area are supported, so writing the complete register set with one I^2C instruction is possible.

I2C Offset	Description	Read / Write
0x00	Pole Zero Cancellation for Channel 0	r/w
0x01	Pole Zero Cancellation for Channel 1	
0x02	Pole Zero Cancellation for Channel 2	
0x03	Pole Zero Cancellation for Channel 3	
0x04	Pole Zero Cancellation for Channel 4	
0x05	Pole Zero Cancellation for Channel 5	
0x06	Pole Zero Cancellation for Channel 6	
0x07	Pole Zero Cancellation for Channel 7	
0x08	Pole Zero Cancellation for Channel 8	
0x09	Pole Zero Cancellation for Channel 9	
0x0A	Pole Zero Cancellation for Channel 10	
0x0B	Pole Zero Cancellation for Channel 11	
0x0C	Pole Zero Cancellation for Channel 12	
0x0D	Pole Zero Cancellation for Channel 13	
0x0E	Pole Zero Cancellation for Channel 14	

I2C Offset	Description	Read / Write
0x0F	Pole Zero Cancellation for Channel 15	
0x10	Pole Zero Cancellation for Channel 16	
0x11	Pole Zero Cancellation for Channel 17	
0x12	Pole Zero Cancellation for Channel 18	
0x13	Pole Zero Cancellation for Channel 19	
0x14	Pole Zero Cancellation for Channel 20	
0x15	Pole Zero Cancellation for Channel 21	
0x16	Pole Zero Cancellation for Channel 22	
0x17	Pole Zero Cancellation for Channel 23	
0x18	Pole Zero Cancellation for Channel 24	
0x19	Pole Zero Cancellation for Channel 25	
0x1A	Pole Zero Cancellation for Channel 26	
0x1B	Pole Zero Cancellation for Channel 27	
0x1C	Pole Zero Cancellation for Channel 28	
0x1D	Pole Zero Cancellation for Channel 29	
0x1E	Pole Zero Cancellation for Channel 30	
0x1F	Pole Zero Cancellation for Channel 31	
0x20	Baseline Shift Channel 0-7, High Byte	r/w
0x21	Baseline Shift Channel 0-7, Low Byte	
0x22	Baseline Shift Channel 8-15, High Byte	
0x23	Baseline Shift Channel 8-15, Low Byte	
0x24	Baseline Shift Channel 16-23, High Byte	
0x25	Baseline Shift Channel 16-23, Low Byte	
0x26	Baseline Shift Channel 24-31, High Byte	
0x27	Baseline Shift Channel 24-31, Low Byte	
0x28	Zone 3 Control	r/w
0x29	Input Gain Select	r/w
0x2A	Filter Frequency Select	r/w
0x2B	Firmware Version	ro
0x2C	Scratchpad Register A	r/w
0x2D	Scratchpad Register B	r/w
0x2E	Scratchpad Register C	r/w
0x2F	Scratchpad Register D	r/w

Table 5-1 : RCC register map

5.4.1 Pole-Zero Cancellation Register

A digital potentiometer with 256 taps in conjunction with series and parallel resistors is used to implement the pole-zero cancellation resistor. The effective resistance range is from 1k to 50k Ohm.

The effective resistor value can be calculated using the following formula:

R_{PZ} (Ohm) = (10^8 + 3.90625 * POT * 10^7) / (1.01*10^5 + POT * 390.625)

POT is defined as the integer of the Pole-Zero Cancellation Register.

Bit	Description	Reset Value
7:0	Value of POT (MSB first)	0x80

Table 5-2 : Pole-Zero Cancellation Register

5.4.2 Baseline Shift Register

Two registers, the High-Byte and the Low-Byte Register, are needed to control the Baseline Shifter.

The following formula can be used to calculate the baseline shift voltage:

$V_{BASELINE}$ (Volt) = DAC / 16384

DAC is defined as the integer of the 16bit binary “0 & High-Byte[6:0] & Low-Byte[7:0]”.

Bit	Description	Reset Value
7	Sign Bit 0 = positive baseline voltage 1 = negative baseline voltage	0x80
6:0	Bit[11:4] of DAC	

Table 5-3 : High-Byte Register

Bit	Description	Reset Value
7:4	Bit[3:0] of DAC	0x00
3:0	0000	

Table 5-4 : Low-Byte Register

5.4.3 Zone 3 Control Register

Bit	Description	Reset Value
7	Zone 3 Enable (Read only) 0 = disabled 1 = enabled All other bits of this register are 0 when this bit is 0. Zone 3 Enable is set to 1 by the AMCs MMC.	-
6	Reserved	0
5	Reserved	0
4	Option (J100) Enable 0 = disabled 1 = enabled	0
3	RTM_TRIG0 Enable 0 = Buffer disabled 1 = Buffer enabled	0
2	RTM_CLK0 Enable 0 = Buffer disabled 1 = Buffer enabled	0
1	Analog Output Enable 1 Output amplifier control for Analog Channels 1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 30, 31 0 = Output Amplifiers disabled (Class A1 compatibility) 1 = Output Amplifiers enabled	0
0	Analog Output Enable 0 Output amplifier control for all other Analog Channels 0 = Output Amplifiers disabled 1 = Output Amplifiers enabled	0

Table 5-5 : Zone 3 Control Register

5.4.4 Input Gain Select Register

Bit	Description	Reset Value
[7:6]	Input Gain for Channel 24-31: 00 = Gain 1 10 = Gain 2 01 = Gain 5 11 = Gain 10	00
[5:4]	Input Gain for Channel 16-23: 00 = Gain 1 10 = Gain 2 01 = Gain 5 11 = Gain 10	00
[3:2]	Input Gain for Channel 8-15: 00 = Gain 1 10 = Gain 2 01 = Gain 5 11 = Gain 10	00
[1:0]	Input Gain for Channel 0-7: 00 = Gain 1 10 = Gain 2 01 = Gain 5 11 = Gain 10	00

Table 5-6 : Input Gain Select Register

5.4.5 Filter Frequency Select Register

Bit	Description	Reset Value
[7:6]	Filter Frequency for Channel 24-31: 01 = 100ns 00 = 1µs 10 = 10µs 11 = 10µs	00
[5:4]	Filter Frequency for Channel 16-23: 01 = 100ns 00 = 1µs 10 = 10µs 11 = 10µs	00
[3:2]	Filter Frequency for Channel 8-15: 01 = 100ns 00 = 1µs 10 = 10µs 11 = 10µs	00
[1:0]	Filter Frequency for Channel 0-7: 01 = 100ns 00 = 1µs 10 = 10µs 11 = 10µs	00

Table 5-7 : Filter Frequency Select Register

5.5 JTAG

The TAMC532-TM has a JTAG capable device on-board that is connected to the Zone 3 JTAG interface. It is the RCC, an ATxmega256 with an instruction register length of 4.

Users shall take care to leave the RCC in JTAG bypass mode. Clearing or programming the RCC via JTAG is possible and will make the TAMC532-TM unusable until the RCC is correctly reprogrammed.

5.6 I2C Management Bus

The TAMC532-TM implements the following I2C devices / addresses on the µRTM I2C management bus:

Device Type	Device	I2C Address	
EEPROM	AT24C32	50h	1010000b
EEPROM	24AA025E48	51h	1010001b
Temperature Sensor	SE95	48h	1001000b
I2C I/O Extender	PCA8574A	3Eh	0111110b

Table 5-8 : µRTM I2C Devices

5.6.1 I2C I/O Extender

The TAMC532-TM provides an 8-Bit I2C I/O Extender device on the I2C management bus that is used for controlling certain management signals on the µRTM:

I/O Port Bit	I/O Direction	Function	Description
7	O	-	not used
6	O	0 = Enable signal not active 1 = Enable signal active	Payload (Zone 3) Enable Control
5	O	0 = Payload Reset# signal active 1 = Payload Reset# signal not active	Payload Reset Control
4	I	0 = Power Supply status is not Good 1 = Power Supply status is Good	Status of local Payload Power Supply
3	O	0 = LED off 1 = LED on	LED2 (Green) Control
2	O	0 = LED on 1 = LED off	LED1 (Red) Control
1	O	0 = LED on 1 = LED off	Hot Swap LED (Blue) Control
0	I	0 = Handle/Switch closed 1 = Handle/Switch open	Handle Status

Table 5-9 : µRTM I2C I/O Extender Port Assignment

6 Installation

This chapter contains general notes regarding installing the µRTM into a system.

6.1 Zone 3 I/O Voltage

Prior to inserting the TAMC532-TM into a system, make sure that the selected Zone 3 I/O voltage is compatible with the corresponding front AMC. Zone 3 I/O voltage is selected by changing the Jumper position of J1:

Jumper 1-2	Jumper 3-4	I/O Voltage
open	open	3.3V
installed	open	2.5V
open	installed	1.8V
installed	installed	1.5V

Table 6-1 : Zone 3 I/O Voltage selection (J1)

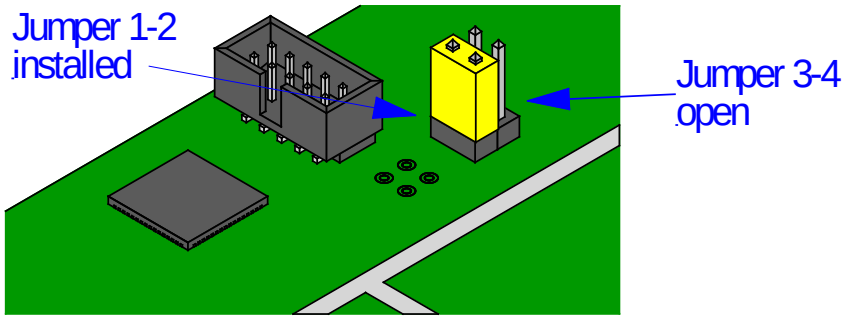

Figure 6-1 : Zone 3 I/O Voltage Selector (J1)

6.2 µRTM Installation

During insertion and extraction, the operational state of the AMC is visible via the blue LED in the AMCs front panel. The following table lists all valid combinations of Hot-swap handle position and blue LED status, including a short description of what's going on.

Blue LED / Handle	On	Off	Long Blink	Short Blink
Open (Pulled out)	**Extraction:** Module can be extracted **Insertion:** Module is waiting for closed Handle	Module is waiting for hot swap negotiation	-	Hot swap negotiation in progress (Extraction)
Closed (Pushed all way in)	Module is waiting for hot swap negotiation	Module is active (operating)	Hot swap negotiation in progress (Insertion)	-

Figure 6-2 : Hot-Swap states

6.2.1 Insertion

Typical insertion sequence:

1. Insert the µRTM module into its slot, with the board edges aligned to the card guides
2. Fasten the screws of the front plate, so the module cannot be pushed out by the Front-AMC if it is inserted afterwards
3. Make sure that the module handle is pushed into the inserted position
    a. Blue LED turns “ON.” (Module is ready to attempt activation by the system)
    b. Blue LED starts “Long Blink” (Hot Swap Negotiation / Module activation in progress)
    c. Blue LED turns “OFF”, and green LED turns “ON” (Module is ready and powered)

When the Blue LED does not go off but returns to the “ON” state, the µRTM FRU information is incompatible to the Front-AMC.

6.2.2 Extraction

Typical Extraction sequence:

1. Pull the module handle out ½ way
    a. Blue LED starts “Short Blink” (Hot Swap Negotiation in progress)
    b. Blue LED turns “ON” (Module is ready to be extracted)
2. Loosen the screws of the front plate
3. Pull the module handle out completely and extract the µRTM from the slot.

6.3 Zone 3 Keying

The TAMC532-TM provides the following male keying pin:

N	A Rotation	View into rear of µRTM	Voltage Levels
2	45	 white = clearance	0 – ±1V

6.4 Class A1 Compatibility

If the TAMC532-TM shall be used with a Class A1 compliant AMC, compatibility can be achieved if

- “Analog Output Enable 1” = 0.

7 Indicators

This chapter describes board indicators such as LEDs.

7.1 LED Indicators

For a quick visual inspection, the µRTM provides the following front panel LEDs.

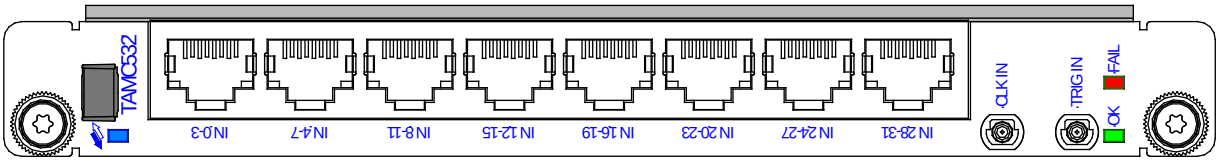

Figure 7-1 : Front Panel LED View

LED	Color	State	Description
HS	Blue	Off	No Power or µRTM is ready for normal operation
		Short Blink	Hot-Swap negotiation (extraction)
		Long Blink	Hot-Swap negotiation (insertion)
		On	µRTM is ready to attempt activation by the system or µRTM is ready to be extracted
FAIL	Red	Off	No fault
		On	Failure or out of service status
OK	Green	Off	µRTM is not powered up
		On	µRTM is powered and OK

Table 7-1 : Front Panel LEDs

8 I/O Connectors

This chapter provides information about user accessible on-board connectors.

8.1 Overview

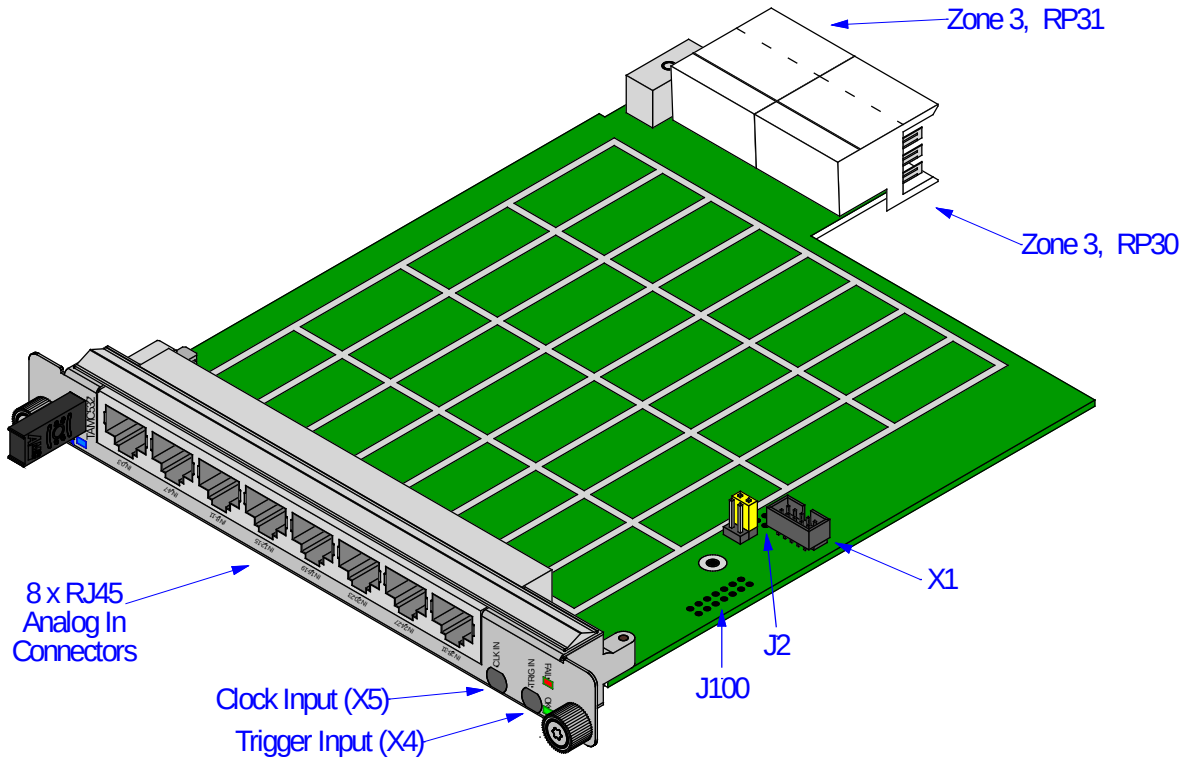

Figure 8-1 : Connector Overview

8.2 Board Connectors

8.2.1 Zone 3 Connectors

The TAMC532-TM provides two 30-pair ADF connectors (RP30 and RP31) at the Zone 3 Interface.

Pin-Count	30 contact pairs (60 signal contacts) + 30 GND pins
Connector Type	Advanced Differential Fabric (ADF) connector
Source & Order Info	Erni 204781 or compatible

8.2.1.1 RP30

ADF connector ground pins are not shown.

	A	B	C	D	E	F
1	PWR	PWR	PS#	SDA	TCK	TDO
2	PWR	PWR	MP	SCL	TDI	TMS
3	-	-	-	-	-	-
4	SDA	SCL	D4+	D4-	RTM_TRIG3+	RTM_TRIG3-
5	RTM_TRIG2+	RTM_TRIG2-			RTM_TRIG0+	RTM_TRIG0-
6	-	-	OUT0+	OUT0-	-	-
7	GND	GND	GND	GND	GND	GND
8	-	-	-	-	-	-
9	RTM_CLK0+	RTM_CLK0-	-	-	-	-
10	RTM_CLK1+	RTM_CLK1-	CH31+	CH31-	CH30+	CH30-

Table 8-1 : Zone 3 RP30 Connector Pin Assignment

8.2.1.2 RP31

ADF connector ground pins are not shown.

	A	B	C	D	E	F
1	CH29+	CH29-	CH28+	CH28-	CH27+	CH27-
2	CH26+	CH26-	CH25+	CH25-	CH24+	CH24-
3	CH23+	CH23-	CH22+	CH22-	CH21+	CH21-
4	CH20+	CH20-	CH19+	CH19-	CH18+	CH18-
5	CH17+	CH17-	CH16+	CH16-	CH15+	CH15-
6	CH14+	CH14-	CH13+	CH13-	CH12+	CH12-
7	CH11+	CH11-	CH10+	CH10-	CH9+	CH9-
8	CH8+	CH8-	CH7+	CH7-	CH6+	CH6-
9	CH5+	CH5-	CH4+	CH4-	CH3+	CH3-
10	CH2+	CH2-	CH1+	CH1-	CH0+	CH0-

Table 8-2 : Zone 3 RP31 Connector Pin Assignment

8.2.2 Analog In Connectors

The TAMC532-TM provides 8 RJ45 Connectors as analog input. Each RJ45 holds 4 differential analog inputs.

Pin-Count	8 x 8 Pins
Connector Type	Multi Port (8x) RJ45
Source & Order Info	FCI 10118064-5001310LF

8.2.2.1 In 0-3

Pin	Signal	Description
8	IN[0]+	Differential Analog Input 0
7	IN[0]-	
6	IN[1]+	Differential Analog Input 1
3	IN[1]-	
5	IN[2]+	Differential Analog Input 2
4	IN[2]-	
2	IN[3]+	Differential Analog Input 3
1	IN[3]-	

Table 8-3 : Pin Assignment X6-A (Analog In 0-3)

8.2.2.2 In 4-7

Pin	Signal	Description
8	IN[4]+	Differential Analog Input 4
7	IN[4]-	
6	IN[5]+	Differential Analog Input 8
3	IN[5]-	
5	IN[6]+	Differential Analog Input 6
4	IN[6]-	
2	IN[7]+	Differential Analog Input 7
1	IN[7]-	

Table 8-4 : Pin Assignment X6-B (Analog In 4-7)

8.2.2.3 In 8-11

Pin	Signal	Description
8	IN[8]+	Differential Analog Input 8
7	IN[8]-	
6	IN[9]+	Differential Analog Input 9
3	IN[9]-	
5	IN[10]+	Differential Analog Input 10
4	IN[10]-	
2	IN[11]+	Differential Analog Input 11
1	IN[11]-	

Table 8-5 : Pin Assignment X6-C (Analog In 8-11)

8.2.2.4 In 12-15

Pin	Signal	Description
8	IN[12]+	Differential Analog Input 12
7	IN[12]-	
6	IN[13]+	Differential Analog Input 13
3	IN[13]-	
5	IN[14]+	Differential Analog Input 14
4	IN[14]-	
2	IN[15]+	Differential Analog Input 15
1	IN[15]-	

Table 8-6 : Pin Assignment X6-D (Analog In 12-15)

8.2.2.5 In 16-19

Pin	Signal	Description
8	IN[16]+	Differential Analog Input 16
7	IN[16]-	
6	IN[17]+	Differential Analog Input 17
3	IN[17]-	
5	IN[18]+	Differential Analog Input 18
4	IN[18]-	
2	IN[19]+	Differential Analog Input 19
1	IN[19]-	

Table 8-7 : Pin Assignment X6-E (Analog In 16-19)

8.2.2.6 In 20-23

Pin	Signal	Description
8	IN[20]+	Differential Analog Input 20
7	IN[20]-	
6	IN[21]+	Differential Analog Input 21
3	IN[21]-	
5	IN[22]+	Differential Analog Input 22
4	IN[22]-	
2	IN[23]+	Differential Analog Input 23
1	IN[23]-	

Table 8-8 : Pin Assignment X6-F (Analog In 20-23)

8.2.2.7 In 24-27

Pin	Signal	Description
8	IN[24]+	Differential Analog Input 24
7	IN[24]-	
6	IN[25]+	Differential Analog Input 25
3	IN[25]-	
5	IN[26]+	Differential Analog Input 26
4	IN[26]-	
2	IN[27]+	Differential Analog Input 27
1	IN[27]-	

Table 8-9 : Pin Assignment X6-G (Analog In 24-27)

8.2.2.8 In 28-31

Pin	Signal	Description
8	IN[28]+	Differential Analog Input 28
7	IN[28]-	
6	IN[29]+	Differential Analog Input 29
3	IN[29]-	
5	IN[30]+	Differential Analog Input 30
4	IN[30]-	
2	IN[31]+	Differential Analog Input 31
1	IN[31]-	

Table 8-10: Pin Assignment X6-H (Analog In 28-31)

8.2.3 Clock Input Connector X5

Pin-Count	2 Pins
Connector Type	MMCX
Source & Order Info	Molex 73415-0963 or compatible

Pin	Signal	Description
Center	RTM_CLK0	Clock input
Shield	GND	Current return path / shield

Table 8-11: Pin Assignment X5 (Clock Input)

8.2.4 Trigger Input Connector X4

Pin-Count	2 Pins
Connector Type	MMCX
Source & Order Info	Molex 73415-0963 or compatible

Pin	Signal	Description
Center	RTM_CLK0	Clock input
Shield	GND	Current return path / shield

Table 8-12: Pin Assignment X4 (Trigger Input)

8.2.5 On-Board Connectors

8.2.5.1 X1 (RMC JTAG)

The dedicated RMC JTAG/ISP Header is intended for factory use only.

Pin-Count	10
Connector Type	10-pin 2mm box header
Source & Order Info	Molex 87832-1020

Pin	Signal	Description
1	TCK	Test Clock
2	GND	Ground
3	TDO	Test Data Output (TAP Controller: TDI)
4	VT_{REF}	Reference Voltage
5	TMS	Test Mode Select Input
6	nSRST	RMC RESET#
7	µRTM_MP	Connected to MP
8	nTRST	Connected to PENABLE#
9	TDI	Test Data Input (TAP Controller: TDO)
10	GND	Ground

Table 8-13: Pin Assignment X1 (RMC JTAG Header)

8.2.5.2 J2 (RMC Debug)

An unpopulated 2 x 2 through hole pin field is available to provide a debug interface for the management microcontroller if necessary.

Pin	Signal	Description
3	D+ / Tx	Depending on the µController programming, these pins may provide a USB or UART interface
1	D- / Rx	
2	µRTM_MP	+3.3V Management Power
4	GND	Ground

Table 8-14: Pin Assignment J2 (RMC Debug Header)

8.2.5.3 J100 (Option)

An unpopulated 7 x 2 through hole pin field is available that provides optional access to additional Zone 3 Signals.

Pin	Signal	Description
1	RTM_TRIG2+	Connected to Zone 3 D6±
2	RTM_TRIG2-	
3	GND	Ground
4	GND	
5	RTM_TRIG3+	Connected to Zone 3 D5±
6	RTM_TRIG3-	
7	+3.3V	+3.3V derived from Payload Power
8	OPTION_EN	Signal to enable / disable buffer, controlled by the RCC
9	RTM_CLK1+	Connected to Zone 3 RTM_CLK±
10	RTM_CLK1-	
11	GND	Ground
12	GND	
13	RTM_OUT0+	Can be connected to Zone 3 OUT0± by assembly option.
14	RTM_OUT0-	

Table 8-15: Pin Assignment J100 (Option)