The Embedded I/O Company

TEWS TECHNOLOGIES

TAMC532

32 x 12/14 Bit 50/75 Msps ADC for MTCA.4 Rear-I/O

Version 1.1

User Manual

Issue 1.1.0

September 2021

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TAMC532-10R

32 x 12 Bit 75 Msps ADC for MTCA.4 Rear-I/O

TAMC532-11R

32 x 14 Bit 50 Msps ADC for MTCA.4 Rear-I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Document History

Issue	Description	Date
1.0.0	Initial Issue	April 2015
1.0.1	- Changed PCIe Bar Endianness in Chapter 6.1.1 - Added DMA Descriptor Big Endian Model Note in Chapter 6.1.4 - Added information about auto-load sequence abort in chapter 5.2.1.2 - Modified I2C Bridge Status Register Information concerning Write and Read Data FIFO Counter - Added register address information to the register description tables throughout the document.	April 2015
1.0.2	- Added CSPT Data Endian Model mode in CSPT Unit [x] Control Register - Changed Bit Positions of WRS_SWR_DCNT and WRS_SRD_DCNT in I2C Bridge Control Register - Corrected the register names at offset 0x02 and 0x03 in Table 6-41 - Removed minor typo (Lower / Upper) in chapter 6.2.2.4 and 6.2.2.5	May 2015
1.0.3	- Added Information about minimum ADC sample Clock Frequency of 10MHz - Added Information about reset time after ADC sampling frequency change. - Added note about trigger edge sensitivity in CSPT Unit [x] Control Register - Added description about triggers in chapter ADC Data Acquisition - Updated Chapter “LED Indicators” - Added DCIRST_LOCKED in Module Status Register	July 2015
1.0.4	- BCC: o Updated ADC Setup Interface Control Register o Updated LMK Setup Interface Control Register o Added CPS Setup Interface Control Register - FPGA: o ADC SIPO Unit Disable added to the Module Control Register o ADC Loss Of Calibration Detected added to the Module Status Register	January 2016

Issue	Description	Date
1.1.0	Functional extension to V1.1 due to new FPGA firmware and general review of the document - Automatic Buffer Termination Disable functionality added in the CSPT Unit Control Register - Software controlled Buffer Termination added in the Application Command Register - Typo corrected in the title of the FPGA JTAG Connector Pin Assignment Table. - Typo correction in the description of the BCCs Si5338 Status Register and LMK_SCI of LMK04816 Status register: the description for value 0 and 1 was interchanged - Clarification in the description of the BCCs Miscellaneous Register: reserved state added to FPGA_IN0 and FPGA_IN1 - Correction of the Affected analog input paths of DIS_AMP_B in the BCCs ADC Input Amplifiers Control Register - All phrases related to the user-programmability of the FPGA are removed throughout the document. This better matches the fact that the TAMC532 is delivered with a factory programmed firmware. - Description of LEDs 1-4 revised and User Mode added - Jitter Attenuator Control Register removed from BCC, as the jitter attenuator has been removed. - Description of BCC Firmware Identification Register added - Added note for CSPT Unit memory interface synchronization requirement in chapter Application Control Register - Revised DDR3 Memory usage description in chapter 5.4	September 2021

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1 Product Description

The TAMC532 is an Advanced Mezzanine Card (AMC) according to MTCA.4 (MicroTCA Enhancements for Rear I/O and Precision Timing). 32 analog input channels allow sampling of analog signals with 75 Msps at 12 Bit resolution (optional 50 Msps at 14 Bit).

The TAMC532 utilizes Back-IO via Zone 3 to interface the ADCs with the signal conditioning located on the µRTM. This modular concept allows adapting the TAMC532 to nearly any analog input requirement without changing the AMC itself.

A very powerful on-board clocking structure enables using the TAMC532 in nearly all kind of clocking scenarios. A self-clocked application as well as synchronizing multiple TAMC532 is possible, allowing applications with up to several hundred simultaneous sampled channels.

Data readout is done via PCI-Express.

The on-board DRR3 memory is used for data buffering in triggered applications that require subsequent readout.

Up to eight backplane triggers are available, each configurable as input or output.

The TAMC532 is equipped with a powerful Kintex-7 FPGA for data acquisition and transfer. The Kintex-7 FPGA is configured with a firmware that provides a very functional readout system and full control over the numerous clocking and trigger options.

Operating temperature range is -0°C to +70°C.

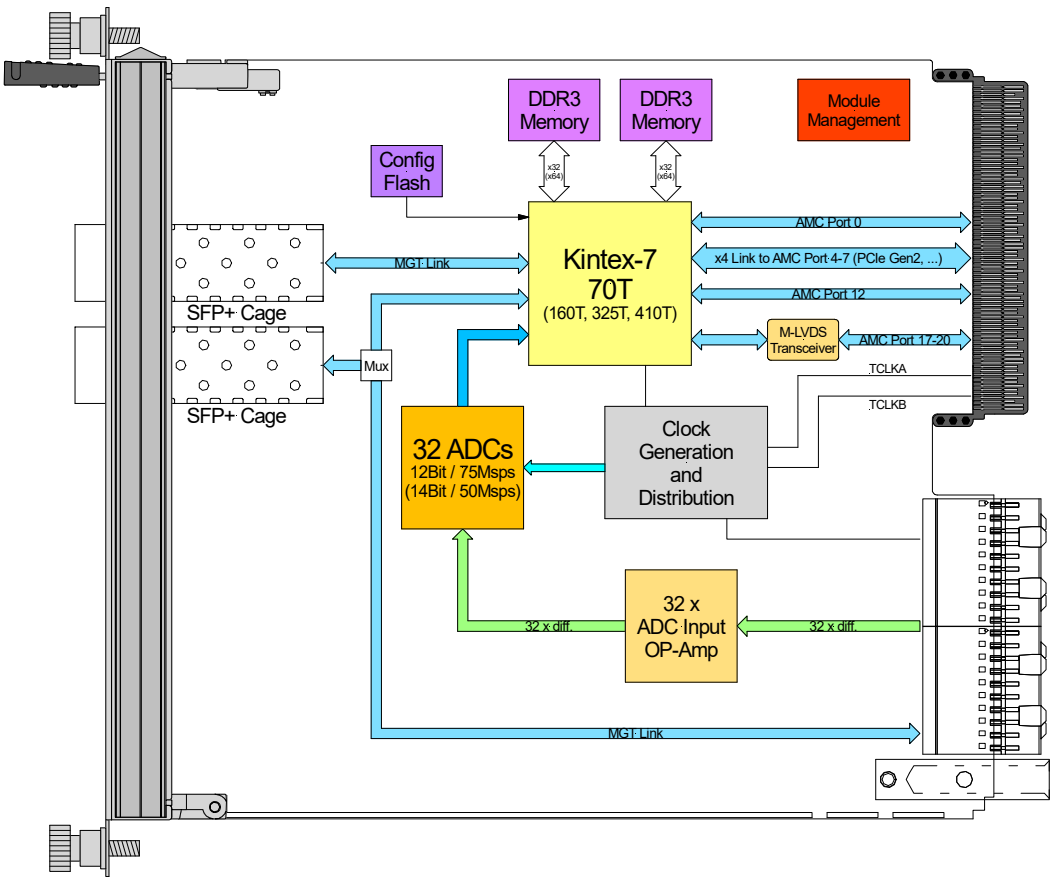

Figure 1-1 : Block Diagram

2 Technical Specification

AMC Interface		
Mechanical Interface	Advanced Mezzanine Card (AMC) Interface conforming to PICMG® AMC.0 R2.0 (Advanced Mezzanine Card Base Specification) Module Type: Double Mid-size Module	
Electrical Interfaces	AMC Port 4-7 AMC Port 17-20 via M-LVDS Transceivers TCLKA + B	
IPMI Support		
IPMI Version	1.5	
Front Panel LEDs	Blue Hot-Swap LED Red Failure Indication LED (LED1) Green Board OK / User LED (LED2)	
Main On-Board Devices		
FPGA	XC7K70T-1FBG676C or compatible	
DDR3 Memory	MT41J64M16LA or compatible	
Flash	N25Q256 or compatible	
ADC	TAMC532-10R : AD9637 (12 Bit resolution) TAMC532-11R : AD9257 (14 Bit resolution)	
Zone 3 I/O Interface		
Analog Input Voltage	0V ±1V (differential)	
Number of Channels	32	
I/O Connector	2 x 30pair ADF Connector according to MTCA.4	
Physical Data		
Power Requirements	Management Power: 70mA typical @ +3.3V DC	
	Payload Power: 2A typical @ +12V DC	
	max. Current Draw as per Module Current Requirements Record: 5A	
Temperature Range	Operating	0 °C to +70 °C
	Storage	0 °C to +70 °C
MTBF	272000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	385 g	

Table 2-1 : Technical Specification

3 Handling and Operating Instructions

3.1 ESD Protection

The AMC module is sensitive to static electricity. Packing, unpacking and all other module handling has to be done in an ESD/EOS protected Area.

3.2 Thermal Considerations

Forced air cooling is recommended during operation. Without forced air cooling, damage to the device can occur.

3.3 I/O Signaling Voltages

The FPGA I/O-Lines to the µRTM are directly connected to the FPGA I/O pins. The I/O voltage of these FPGA I/O pins is 2.5V maximum.

The FPGA I/O pins are NOT 3.3V or 5V tolerant.

4 IPMI Support

The AMC module provides a Module Management Controller (MMC) that performs health monitoring, hot-swap functionality and stores the Field Replaceable Unit (FRU) information. The MMC communicates via an Intelligent Platform Management Interface (IPMI).

4.1 Temperature and Voltage Sensors

The MMC monitors on-board sensors and signals sensor events to the superordinated IPMI controller / shelf manager. Available sensors are listed in the table below.

Sensor Number	Signal Type	Thresholds	Signal Monitored
0	Event	-	Hot-swap switch
1	Temperature	lnr lcr lnc unc ucr unr	Board Temp.
2		lnr lcr lnc unc ucr unr	RAM Temp.
3	Temperature	lnr lcr lnc unc ucr unr	FPGA Temp.
4	Voltage	lnr lcr lnc unc ucr unr	+12V (PWR)
5	Voltage	lnr lcr lnc unc ucr unr	+1V0
6	Voltage	lnr lcr lnc unc ucr unr	+1V5
7	Voltage	lnr lcr lnc unc ucr unr	+1V8

unr: upper non-recoverable, ucr: upper critical, unc: upper non-critical
lnr: lower non-recoverable, lcr: lower critical, lnc: lower non-critical

Table 4-1 : Temperature and Voltage Sensors

4.2 FRU Information

The MMC stores the module FRU information in a non-volatile EEPROM. Some of the records are writeable. If records are modified, the user is responsible for setting the proper checksums. The actual FRU information data is shown below.

Area	Size (in Bytes)	Writeable
Common Header	8	no
Chassis Info Area	0	no
Board Info Area	variable	no
Product Info Area	variable	no
Multi Record Area		
Module Current Requirements	variable	yes
AMC Point-to-Point Connectivity	variable	yes
Clock Configuration	variable	yes
Compatibility Record	variable	yes

Table 4-2 : FRU Information

4.2.1 Board Info Area

Product Information	Value
Version	1
Language Code	0x00 - english
Manufacturer date/time	determined at manufacturing
Board manufacturer	TEWS TECHNOLOGIES GmbH
Board product name	TAMC532
Board serial number	determined at manufacturing (see board label)
Board part number	TAMC532-xxR -xx = -10 / -11

Table 4-3 : Board Info Area

4.2.2 Product Info Area

Product Information	Value
Version	1
Language Code	0x00 - english
Product manufacturer	TEWS TECHNOLOGIES GmbH
Product name	TAMC532
Board part/model number	TAMC532-xxR -xx = -10 / -11
Product version	V1.0 Rev. A (see board label)
Product serial number	determined at manufacturing (see board label)
Asset tag	= Product serial Number

Table 4-4 : Product Info Area

4.2.3 Multi Record Area

4.2.3.1 Module Current Requirements

The “Current Draw” value holds the Payload Power (PWR) requirement of the AMC given as current requirement in units of 0.1A at 12V. The table below shows the factory default “Current Draw” value for this AMC module.

Product Information	Value
Current Draw	0x32 (5 A)

Table 4-5 : Module Current Requirements

The AMC’s MMC announces the current demand to the shelf manager. If the power budget for the AMC slot is smaller than this value, the shelf manager may not enable Payload power for the used slot.

4.2.3.2 AMC Point-to-Point Connectivity

The AMC module provides the following AMC Point-to-Point Connectivity Record Data.

Channel	Port	Link Type	Link Type Extension	Link Grouping ID	Asymmetric Match
0	0	AMC.2 Ethernet	1000BASE-BX Ethernet Link	Single Channel Link	Exact match
1	4	AMC.1 PCI Express	Gen 1 PCI Express, non-SSC	Single Channel Link	PCI Express Primary Port
		AMC.1 PCI Express	Gen 1 PCI Express, SSC	Single Channel Link	PCI Express Primary Port
		AMC.1 PCI Express	Gen 2 PCI Express, non-SSC	Single Channel Link	PCI Express Primary Port
		AMC.1 PCI Express	Gen 2 PCI Express, SSC	Single Channel Link	PCI Express Primary Port
2	4-7	AMC.1 PCI Express	Gen 1 PCI Express, non-SSC	Single Channel Link	PCI Express Primary Port
		AMC.1 PCI Express	Gen 1 PCI Express, SSC	Single Channel Link	PCI Express Primary Port
		AMC.1 PCI Express	Gen 2 PCI Express, non-SSC	Single Channel Link	PCI Express Primary Port
		AMC.1 PCI Express	Gen 2 PCI Express, SSC	Single Channel Link	PCI Express Primary Port

Table 4-6 : AMC Point-to-Point Connectivity

4.2.3.3 Clock Configuration

AMC FCLKA (CLK3) is used as the PCI Express Reference Clock.

Clock ID	Clock Features	Clock Family	Clock Accuracy	Clock Frequency
FCLKA	Clock Receiver, connected through PLL	PCI Express	PCI Express Gen 1	100 MHz nom.
	Clock Receiver, connected through PLL	PCI Express	PCI Express Gen 2	100 MHz nom.
TCLKA	Clock Receiver, connected through PLL	undefined	undefined	10kHz – 500MHz
	Clock Receiver, connected without PLL	Undefined	Undefined	10MHz – 50MHz
TCLKB	Clock Receiver, connected through PLL	Undefined	Undefined	10kHz – 500MHz
	Clock Receiver, connected without PLL	Undefined	Undefined	10MHz – 400MHz
	Clock Source with PLL	undefined	undefined	10kHz – 100MHz

Table 4-7 : Clock Configuration

4.2.4 Modifying FRU Records

Some of the records are writeable to allow adaption to certain systems. If records are modified, the user is responsible for setting the proper checksums.

5 Functional Description

This chapter gives an overview of the various functions of the TAMC532.

5.1 Overview

From a FPGA centric view, the TAMC532 can be divided into several functional blocks. The following subchapters provide a detailed description for each of these blocks.

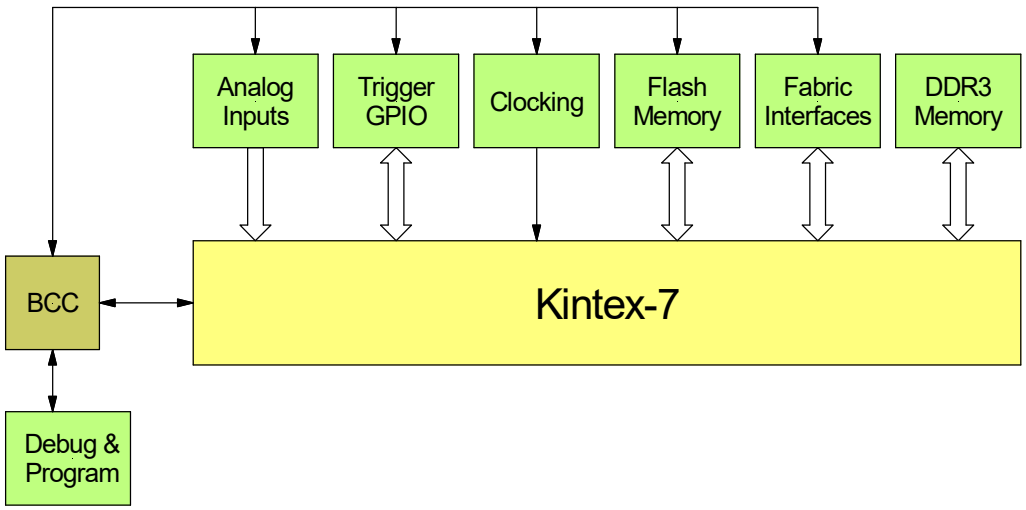

Figure 5-1 : Functional Block Diagram

5.2 FPGA

The heart of the TAMC532 is the Kintex-7 FPGA. It is configured with a firmware that provides a very functional readout system and control over the numerous clocking and trigger options.

5.2.1 Interrupt Handling

The firmware contains different functions or sub-components. For a simplified interrupt handling, the interrupt-relevant information of these components has been grouped within the Module Interrupt Status Register.

Interrupts are controlled via a two-stage technique: a Module Interrupt Global Enable Bit and separate Interrupt Source Enable Bits.

Different interrupt event information is registered within the Module Interrupt Status Register. Every interrupt source has a corresponding enable bit within the Module Interrupt Enable Register. When a specific interrupt occurs and if this specific interrupt is enabled, it is registered as Interrupt Status Register information.

Consequently, interrupts that are not enabled cannot be registered/captured within the Interrupt Status Register and got lost.

Bits inside the Interrupt Status Register can be cleared (Interrupt Acknowledge) by active-high bit writing (W1C). If a bit indicates a logical one it will be zero after such a write. If a bit indicates a logical zero it will remain at logical zero after such a write, meaning that it cannot be set by software.

The content of the Interrupt Status Register does not generate PCIe Interrupts without any control. If the Global Module Interrupt Enable Bit is not set, PCIe Interrupts are prohibited. In such a case, the Interrupt Status Register also operates as Interrupt Pending Register.

In accordance with PCIe requirements, legacy and MSI interrupt generation is supported. MSI-X is not supported.

In case of legacy interrupts, INTA interrupts are generated. In case of MSI interrupts, only a single vector will be used. Configuring MSI-X will cause that no interrupts are generated.

The module interrupt configuration usage information can be obtained via the Module Status Register.

5.2.2 DMA Controller

The design contains four different DMA Controllers *DMACs*, which operate and behave in the same way. Every DMA Controller has a separate register set to obtain status information and write control settings.

As long as a DMAC is not enabled, its logic is held in reset state and all status information is at default.

Besides, every DMAC provides a self-clearing SW reset to reset the logic and status information (instead of toggling the corresponding enable off and on).

After a DMAC is enabled (DMAC_EN), the controller performs an auto-load sequence of the Descriptor Information stored at the host memory address indicated by the Base Descriptor Address Register. The load sequence is aborted if the DMA Base Address Register is 0x00000000.

Consequently, the Base Descriptor Address Register should point to a valid Descriptor Address before enabling the DMA Controller.

Descriptor linked list reading continues until the last read DMA Descriptor does not provide an successor element (Next Descriptor Address is 0x00000000), the last descriptor has the EOL bit set or the internal descriptor queue buffer is full (256 elements pre-fetched).

The Descriptor Queue is filled successively; one after the other, meaning that one DMA descriptor is requested at a time (for internal handling of outstanding request).

Every request statically reads the first 3 DWs from the specified (host) memory address (via Base Descriptor Address Register or Next Descriptor Address). There is no sanity check on the read information. It is expected that the read information is in accordance with the specified DMA Descriptor Structure.

For future improvements every DMA Descriptor should consider the 4th reserved DW.

The current internal descriptor queue memory fill-level can be obtained by reading the corresponding DMA Controller status register (DMAC_DQ_SIZE).

A load sequence can also be initiated by writing into the Base Descriptor Address Register after the DMAC is enabled and if the internal buffer descriptor memory is not full (Descriptor Queue Size is 0xFF). The loaded Descriptor information is queued after the last Descriptor stored within the internal buffer.

The Base descriptor Address Register should not be write-accessed during auto-prefetching operations since this would initiate false Descriptor order.

Some more corresponding information is provided within the status register.

If an error occurs during reading descriptor information, bit DMAC_DQH_ECR is set. Conditions that cause such an error are: PCIe timeout, returned read length does not match the requested one or an erroneous completion is reported by the system.

The current descriptor host memory buffer size (DMAC_RDB_SIZE) is also provided as debugging option.

DMA Controller idle status indication is separated on two information bits, reflecting the internal structure: DMAC_AIF_IDLE (Application Interface Controller) and DMAC_DQH_IDLE (Descriptor Queue Handler).

The Application Interface Controller, which is connected to a specific CSPT Unit, signals idle when it is willing / ready to process DMA transmit data.

The Descriptor Queue Controller signals idle when it is not performing any descriptor load or update operation.

Consequently, if both idle states are concurrently asserted, the DMA Controller is in idle.

5.2.3 ADC Data Acquisition

Data acquisition is performed via four separate CSPT (Capture, Storage, Processing and Transmission) Units (A/B/C/D). These units are configured via independent configuration register sets.

Although a different configuration is possible for the CSPT Units, settings shall be the same for all units.

Every unit is linked to a specific physical ADC and a specific DMA Controller. The mapping is as follows:

- Unit A: ADC Channel #07 - #00, DMA Controller #0
- Unit B: ADC Channel #15 - #08, DMA Controller #1
- Unit C: ADC Channel #23 - #16, DMA Controller #2
- Unit D: ADC Channel #31 - #24, DMA Controller #3

CSPT Units are functional identical, meaning that the subsequent description is common for all.

The functional configuration of a unit is performed via a set of three registers: CSPT Control Register and CSPT Data Register #0 (Pre-Trigger Sample Count) and #1 (Post-Trigger Sample Count).

Note that the CSPT configuration should be defined (via writes into the defined registers) before any unit is enabled. In accordance with that, before changing the configuration, all units have to be disabled.

The CSPT unit applies a static data source mode (CSPT_DSM) and data acquisition mode (CSPT_DAM).

The data source mode defines that ADC data is stored within the on-board DDR3 memory (data sink). The memory content is in-turn used as source for DMA host transfers (data source). Consequently, the DDR3 memory is used as ADC data buffer.

The CSPT unit operates due to performance considerations on different memory (mapping afterwards).

- Unit A: ADC Channel #07 - #00, DDR3 Memory #0
- Unit B: ADC Channel #15 - #08, DDR3 Memory #0
- Unit C: ADC Channel #23 - #16, DDR3 Memory #1
- Unit D: ADC Channel #31 - #24, DDR3 Memory #1

The data acquisition mode allows selecting an amount of pre-trigger data stored and / or post-trigger data to be stored within the on-board DDR3 memory. Based on this technique, standard pre- and post-trigger as well as around-trigger data acquisition can be performed.

The Pre-Trigger Sample Count (CSPT_PRT_SC), resident within CSPT Data Register #0, defines the number of sample to be captured before the trigger. Whereas the Post-Trigger Sample Count (CSPT_POT_SC), resident within the CSPT Data Register #1, defines the number of sample to be captured after the trigger.

The sum of both values must not exceed the total memory depth to avoid data overwriting (refer table below).

Memory Depth	Maximum Sample Count per Channel
2x 256Mbyte (default)	8M
2x 512Mbyte (optionally)	16M
2x 1GByte (optionally)	32M

Table 5-1 : Maximum Sample Count per Channel

For pre-trigger data acquisition, the CSPT units start writing ADC channel data into the DDR3 memory after they are enabled. The memory is used as cyclic / ring buffer, oldest samples are replaced by current ones.

Caused by trigger input detection, either post-trigger data acquisition continues if data should be captured (CSPT_POT_SC not equal to 0x00000000) or the DMA data transfer comes next.

During post-trigger data acquisition, the CSPT units write ADC channel data into the DDR3 memory. Writing is performed until the defined sample count (CSPT_POT_SC) has been stored. Overwriting pre-trigger with post-trigger data is inhibited and results in an error reporting (CSPT_ERR, Application Status Register). Data is still valid in such cases and used for subsequent DMA data transfer.

Following the data acquisition phase, the DMA data transfer is performed, using the memory-stored data.

Under normal operation, the CSPT Units terminate the DMA Buffer that is currently used by the associate DMA Controller after the desired number of samples (sum of pre- and post-trigger sample count) has been transferred to the DMA Controller Buffer.

Caused by the automatic DMA Buffer termination (CSPT_ABT), all pending data is flushed from the DMA Controller Buffer and the current active DMA Buffer (Descriptor) is terminated, including signaling the selected interrupts.

In case that a Pseudo-Streaming Operation is desired, the CSPT Automatic Buffer Termination can be disabled. In consequence, a DMA Buffer (Descriptor) is only terminated if its memory space is exhausted. This allows filling a DMA/Host Memory Buffer with multiple CSPT acquisition cycles.

In this operation mode, buffer termination can be manually initiated by the CSPT Unit Software Buffer Termination command (CSPT_SW_BTERM).

The functional configuration registers are surrounded by a set of three application registers: Application Control Register, Application Command Register and Application Status Register.

These registers group (combine) additional CSPT control information and allow a concurrent appliance to the different CSPT units.

In order to simplify the data processing, the physical ADC input data is, irrespective of the adjusted incoming bit width (12 or 14 bit) extended to 16 bit (internal data processing vector width per channel).

This width extension applies a most-significant bit mapping technique, causing lower data bits to be zero. In accordance with that, the highest (left-most) ADC data bit is located at the highest (left-most) position. Lower ADC data bits follow in a descending order.

<table>
<tr><th>Internal Data Processing Vector (16 Bit)</th><th>12 Bit (-10R)</th><th>14 Bit (-11R)</th></tr>
<tr><td>15</td><td>11</td><td>13</td></tr>
<tr><td>14</td><td>10</td><td>12</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>6</td><td>2</td><td>4</td></tr>
<tr><td>5</td><td>1</td><td>3</td></tr>
<tr><td>4</td><td>0</td><td>2</td></tr>
<tr><td>3</td><td rowspan="4">Zero</td><td>1</td></tr>
<tr><td>2</td><td>0</td></tr>
<tr><td>1</td><td rowspan="2">Zero</td></tr>
<tr><td>0</td></tr>
</table>

Table 5-2 : ADC data alignment

The internal data processing vector width per channel is used for the Register Interface ADC Channel [xx] Data Register und the DMA data transfer via CSPT Units.

Data acquisition is initiated by stimulating the selected external trigger input (CSPT External Trigger) or via the software trigger input (CSPT Unit Software Trigger Input). The external input can be disabled while the software input is always available.

Note that the external trigger input is subdued an edge evaluation and level mode is not supported.

5.2.4 I2C Bridge

The I2C Bridge provides a simplified interface that allows performing standard byte reads and writes but also advanced write-read (read-after-write) transfers.

The bridge is based on an I2C master for the actual, physical I2C bus access, which in-turn is encapsulated by a register interface wrapper, providing the following function description.

Note that the I2C master is not multi-master capable.

As long as the I2C master is not enabled (I2C_MST_EN), its logic is held in reset state (register map values show default values) and all initiated operation are ignored.

During functional operation, different operations can be performed on a target I2C bus: Standard Write, Standard Read and Write-Read. Standard Write and Read are variations of the Write-Read Command.

The I2C Bridge Command Register contains corresponding self-clearing commands, to initiate I2C operations.

A bus operation can be initiated only if the I2C master is in its idle state (MST_IDLE). Operations initiated during its busy state are lost and will not been captured or queued for later processing.

The I2C Bridge Status Register provides information about the current functional state of an I2C master.

Write-Read Operation

A Write-Read is initiated via command WRS_OP_CMD within I2C Bridge Command Register.

This advanced I2C bus access technique allows writing a number of bytes (WRS_SWR_DCNT) followed by reading of a defined number of bytes (WRS_SRD_DCNT). So it is possible to combine a proceeding write and a subsequent read operation.

In case that any of this byte numbers is zero, the corresponding operation is not performed. Hence, the Write-Read operation behaves like a Standard Write if WRS_SRD_DCNT is 0x00 respectively behaves like a Standard Read if WRS_SWR_DCNT is 0x00.

Due to a Write-Read Command an I2C target access will be initiated if the I2C master is in idle state.

Irrespective of whether a write will be executed or only a read, an I2C STA (start-sequence) is generated to claim the bus. In case that both, a write and a read are executed, another STA (re-start) is generated between the two operations.

Following the STA sequence, the I2C slave is addressed, using the bus (I2C_BUS_NUM) and address information (I2C_DEV_NUM) provided within the I2C Bridge Command Register.

The successful addressing of the selected I2C slave is reported via DEV_DET inside the I2C Bridge Status Register. This information remains stable until the next I2C operation is initiated. The fault that the selected slave cannot be addressed causes the master to return to its idle state with the information is not set.

After successful addressing, the selected number of bytes to write is transferred if the corresponding number (WRS_SRD_DCNT) is not 0x00. It is expected that the slave acknowledges every write cycle (ACK). If the slave signals a not acknowledge (NACK), the I2C operation is aborted and an error is reported (DEV_OP_ERR).

Write data is read from the I2C Write Data FIFO. The I2C Bridge Status Register provides information about how many bytes are available for writing (WR_DFIFO_CFL).

If there are no bytes to read (WRS_SRD_DCNT is 0x0), processing ends. Otherwise a restart sequence with another addressing phase follows (same procedure as preceding the write operation).

Afterwards the selected number of bytes to read is requested (transferred) from the selected I2C slave.

Read data is stored within the I2C Read Data FIFO. Register I2C Bridge Status Register provides information about how many bytes are available for reading (RD_DFIFO_CFL). The master acknowledges every read (ACK), except the last one (NACK), to correctly terminate the read operation.

Every access will end by generating an I2C STO (stop-sequence) to release the bus.

Write and read data are provided respective obtained via 32 bit registers. Write data transmission selects the least significant register byte first, upper bytes follow in an ascending order. The same order is applied by storing read data.

For interrupt controlled processing the Module Interrupt Status Register is capable of signaling the end of an initiated I2C bus operation (I2C_BRDG_CP). Interrupt signalisation can be controlled through the Module Interrupt Enable Register (I2C_BRDG_CP_EN).

An interrupt is generated after an initiated operation is terminated and before the I2C master enters its idle state (MST_IDLE). In accordance to that, the fault of a loss of arbitration (BUS_ARBL) and/or erroneous operation (DEV_OP_ERR), will also result in an interrupt generation.

5.3 Board Configuration Controller (BCC)

The TAMC532 provides a board configuration controller (BCC) to support the following tasks:

- Power sequencing
- Level shifting for various signals
- Power-up configuration of on-board clocking resources
- Power-up configuration and direction control of on-board M-LVDS transceivers
- Power-up configuration of on-board ADCs

After power-up, the FPGA can gain access to the configuration interfaces of all on-board devices. Two I2C interfaces between FPGA and BCC (BCC-I2C and Configuration-I2C) are used for this purpose. If necessary, the BCC bridges the I2C traffic from the FPGA to the different device specific interfaces. On-board devices with I2C interfaces are directly accessible by the FPGA via Configuration I2C.

5.4 DDR3 Memory

Two Banks of DDR3 Memory with 32 Bit data bus each provide a total of 512Mbyte. This is sufficient for storing a total of 256Msamples, or 8Msamples from each ADC channel. At 10MHz sample frequency, the memory allows to make 800ms snapshots of all ADCs.

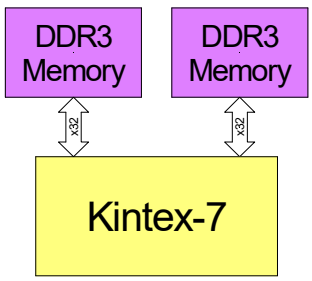

Figure 5-2 : DDR3 Memory Interfaces

5.5 Fabric Interfaces

The TAMC532 provides the following fabric interfaces:

- x4 Multi-Gigabit Link between FPGA and AMC Fat Pipe Region (e.g. AMC port 4-7)

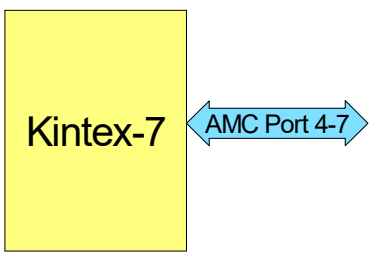

Figure 5-3 : Fabric Interfaces

5.5.1 PCI-Express

AMC Port 4-7 is directly connected to the FPGAs Multi-Gigabit Transceivers. This allows connecting the TAMC532 to a PCI-Express environment.

5.6 Flash Memory

The TAMC532 provides SPI flash devices that are used to store the FPGA firmware. After power-up, the FPGA automatically loads its firmware.

5.7 ADC Clocking

From a top level view, the ADC clocking structure of the TAMC532 provides 4 clock inputs and 9 clock outputs.

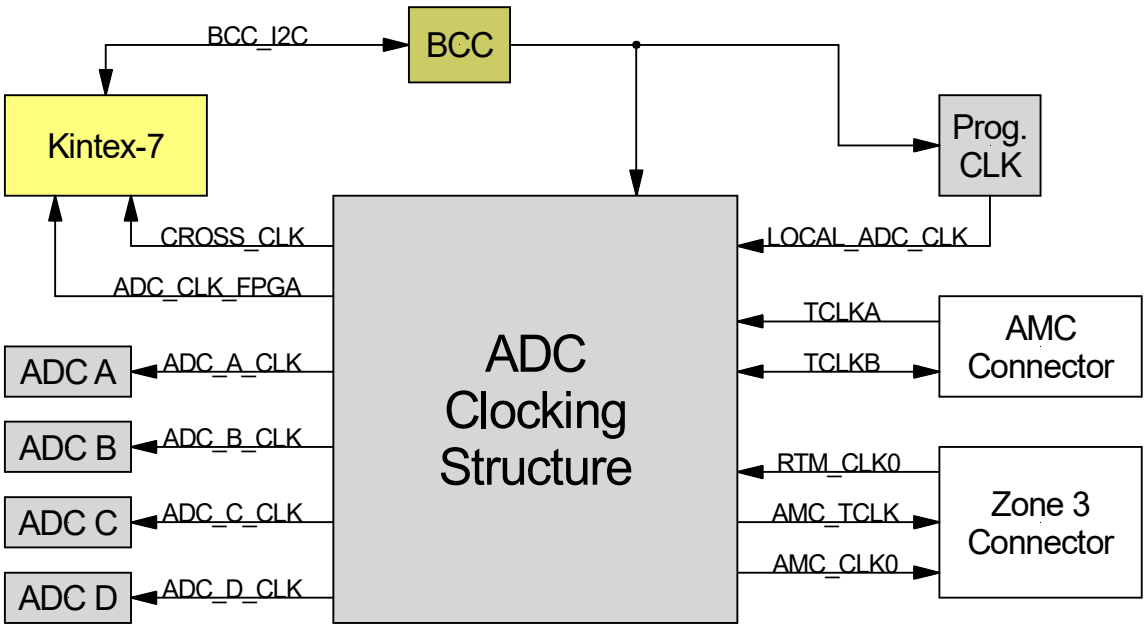

Figure 5-4 : ADC Clocking Overview

Clock sources are TCLKA and TCLKB from the AMC connector, RTM_CLK0 from Zone 3 Connector or the on-board generated LOCAL_ADC_CLK.

LOCAL_ADC_CLK is generated by a programmable clock source and 50MHz by default. It is possible to modify the frequency of this clock if necessary.

By default, all ADCs get the same phase aligned clock. If the input clock frequency is less than the minimum ADC input clock frequency (10MHz), the Clocking structure is able to up-scale the input frequency.

To compensate routing delays or to phase align several TAMC532, individual phase-shift and delay elements can be used for each of the ADC clocks.

Initial setup of the ADC Clocking Structure is done by the BCC. The FPGA can modify this setup by writing to the corresponding BCC registers via BCC_I2C.

The following figure shows a detailed view of the ADC Clocking Structure. The blue arrows indicate the control interfaces that are connected to the BCC.

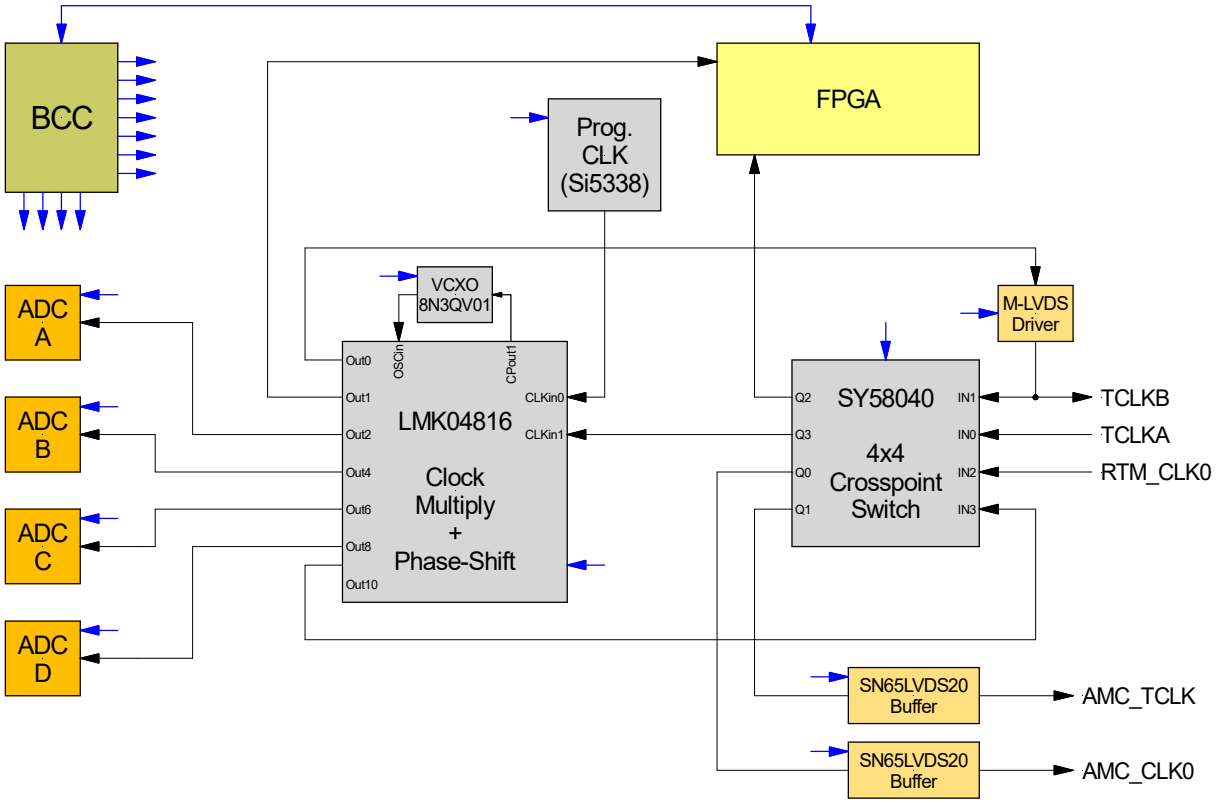

Figure 5-5 : ADC Clock Generation and Distribution Structure

5.7.1 Crosspoint Switch

The Crosspoint switch allows routing any signal from its 4 inputs to any of its 4 outputs. Configuration of the crosspoint switch is done via BCC.

5.7.2 LMK04806

The minimum Sampling Frequency of the ADCs is 10MHz. To support slower external clock sources, the LMK04816 can multiply the external clock to a frequency >10MHz using its dual PLL structure.

In addition, this dual PLL structure allows zero-delay operation with internal loopback. Zero-delay operation is important to guarantee a fixed phase relationship between the slow input frequency and the multiplied (fast) output frequency for the ADCs.

Due to the nature of the dual PLL structure, the input frequency has a low limit of 10kHz. To support any input frequency above 10kHz, the first PLL makes use of an in-system programmable VCXO. See chapter “Mandatory Devices” for the exact device type.

Using the PLLs is also necessary to make the full phase-shift capabilities of the LMK04816 working, which allow shifting the output clocks in up to 522 steps of half PLL-frequency. Each output can be shifted individually.

Bypassing the PLLs is also possible. In this mode, the clock at CLKin1 can be used to clock the ADCs directly.

An analog delay of up to 575ps (25ps step) is available for each output group, independent from the operational mode of the LMK04806.

5.7.3 VCXO

The VCXO frequency has to be an integer multiple of the input frequency.

5.7.4 ADCs

The ADCs itself have the capability to internally use a divided version of their input clock. By default this feature is disabled. The ADCs are directly using their input clocks.

5.7.5 TCLKB

By default, the output buffer of TCLKB is disabled. The User can enable the buffer by writing to the corresponding BCC register via BCC_I2C.

5.7.6 AMC_TCLK

Any of the four crosspoint switch inputs can be connected to AMC_TCLK. By default, the output buffer of AMC_TCLK is disabled. Only if ZONE3_EN is high, the User FPGA can enable the buffer by writing to the corresponding BCC register via BCC_I2C. If ZONE3_EN is going low the buffer is immediately disabled.

5.7.7 AMC_CLK0

Any of the four crosspoint switch inputs can be connected to AMC_CLK0. By default, the output buffer of AMC_CLK0 is disabled. Only if ZONE3_EN is high, the User can enable the buffer by setting the DIP Switch accordingly. If ZONE3_EN is going low the buffer is immediately disabled.

5.8 Trigger and GPIO

The TAMC532 provides access to several GPIO signals at the AMC Connector and the Zone 3 Interface. Each of these signals can be used as a trigger input.

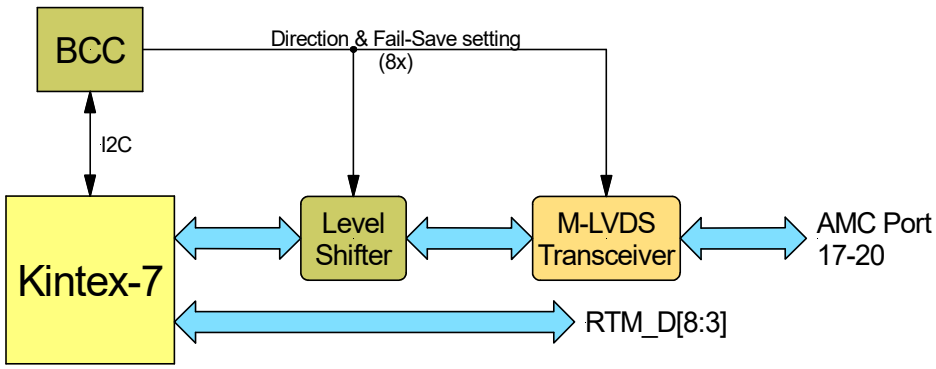

Figure 5-6 : M-LVDS I/O

AMC Port 17-20 Rx and Tx Differential Pairs are all routed to eight M-LVDS Transceivers that convert the differential signals to single ended signals. At power-up, the transceivers are all configured as inputs, “reading” the signal from the AMC backplane. If desired, each Transceiver can individually be reconfigured as output by the user. To save FPGA pins, the Output-enable signals of the M-LVDS transceivers are not directly connected to the FPGA. Instead, they are connected to the Board-Configuration-Controller (BCC), which is connected to the FPGA via an I2C interface.

Zone 3 signals D[8:3]± are directly connected to FPGA pins.

D[8:5]± are used as RTM Trigger Inputs [0:3]. The IO-Standard is LVDS.

D[4]± is not used, but connected to FPGA pins with 2.5V IO-voltage.

D[3]+ is used as SCL of the RTM I2C-Bus, 2.5V IO-voltage.

D[3]- is used as SDA of the RTM I2C-Bus, 2.5V IO-voltage.

5.9 Analog Inputs

The TAMC532 provides 32 differential analog inputs. An operational amplifier with unity gain is used for each analog input to shift the analog input signal to the common-mode voltage of the ADC.

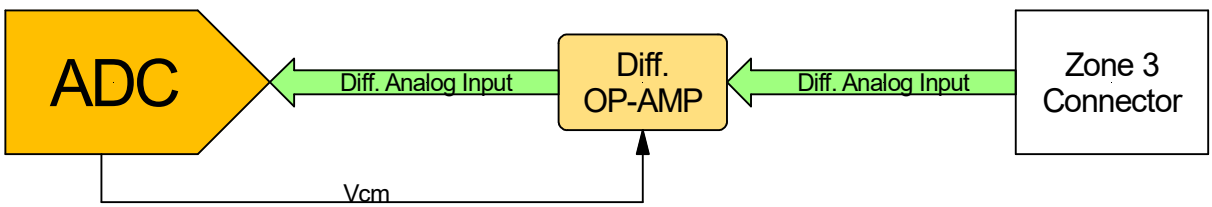

Figure 5-7 : Single Analog Input

Four Octal ADCs are used on the TAMC532, each combining eight ADCs into a single chip. As a result, only one data clock and one frame clock signal is needed to sample the serial data streams of 8 ADCs into the FPGA. As a side effect, all eight ADCs of a group use the same sample clock.

ADC Data is output as one serial double data rate stream per ADC. The resulting data rate is the product of sample rate and ADC resolution. Data format used is 2's Complement, MSB first.

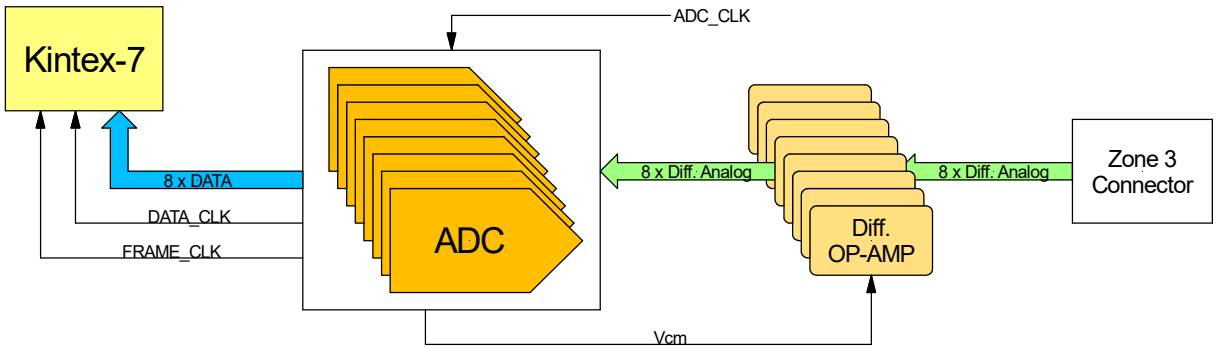

Figure 5-8 : 8 x Analog Input Group

To save power, all operational amplifiers are powered down when the ZONE3_EN signal is low. This includes the case that no or an incompatible µRTM is connected to the TAMC532.

5.9.1 ADC Sample Clock

The sample clock provided to the ADCs (ADC_CLK) has to be in the range of 10MHz to 50MHz. Depending on ADC resolution and FPGA Speed grade, sample frequencies above 50 MHz may be possible.

In each case, the ADCs have to be reset to guarantee proper operation after a clock change. It will take about 3*10^6 sample clock cycles to complete this reset. During reset, the ADCs deliver no or random data.

Changing the Frequency Set via the BCC (Frequency Adjustment Control Register) automatically re-initializes the ADCs, including the ADC reset.

5.9.2 Input Voltage Range

Each input is capable to digitize differential analog voltages of up to ±1V at a common mode voltage of 0V. I.e. that each of the two traces that build the differential pair is allowed to swing between the absolute voltages -0.5V and +0.5V measured against ground.

5.10 Debug

5.10.1 LEDs

4 LEDs are provided by the TAMC532, which are directly controlled by the FPGA. Additional LEDS display basic board Status Information.

For more information about the front-panel LEDs, please refer to chapter “LED Indicators”.

5.10.2 UART

The TAMC532 provides a UART on the Debug Connector. The UART is used by the MMC and provides IPMI related debug information at 38400 baud.

5.10.3 JTAG

The TAMC532 provides 4 different ways to gain access over the JTAG-Chain the Kintex-7 is part of. It can be accessed by:

(1) The Module Management Controller (MMC)

(2) the FPGA JTAG connector

(3) the Debug Connector

(4) the AMC connectors JTAG interface

When connecting a cable to one of the interfaces the chain is automatically connected to it. If multiple cables are connected, the cable with the highest priority is selected. E.g. the AMC Connectors JTAG Interface is only usable when no other cables are connected.

If a µRTM is connected via the Zone 3 connectors, also the µRTM JTAG devices are included into the JTAG chain. The DIP Switch can be used to exclude the µRTM from the AMCs JTAG chain.

5.11 Reset

A Reset signal is provided to the FPGA for 200ms after successful FPGA configuration.

5.12 µRTM Detection

If a compatible µRTM is detected, ZONE3_EN is set high to signal the existence of a compatible µRTM to the FPGA, and all Zone 3 Interfaces are enabled. When ZONE3_EN is going low, the FPGA disables all its Zone 3 interfaces.

6 Addressable Resources

This chapter describes system resources, such as memory mapping, register set and default interrupt request assignments.

6.1 FPGA

6.1.1 Structural Description

The firmware is separated into two main parts: the PCIe Framework Unit and the Application Logic Unit.

The PCIe Framework Unit provides an application logic front-end module. Components necessary to handle PCI Express traffic, the software registers, the bridge functionality and the ADC interfaces resident within this part. For ADC data transfer via DMA from the module into the host memory, the framework contains also four independent software-configurable scatter-gather DMA controllers.

The Application Logic Unit contains four components for capturing, storing, processing and transmitting (CSPT) ADC channel data. There is one component for one physical ADC. The components use on-board DDR3 memory for storing the data locally.

The PCIe accessible software register set provides fundamental control of the firmware function logic.

A register subset is used within the framework for reading module status information and controlling base functions. Another register subset is mapped into the application function unit.

Three separate bridge interfaces are included to allow accessing the different I2C busses on the TAMC532 (BCC, Payload and RTM). Every bridge interface owns an independent register set to stimulate the connect I2C master.

In addition, another bridge allows accessing the connected SPI flash device (optional feature). It is linked like the I2C masters above.

The below figure depicts this SOC structure on a component-based level.

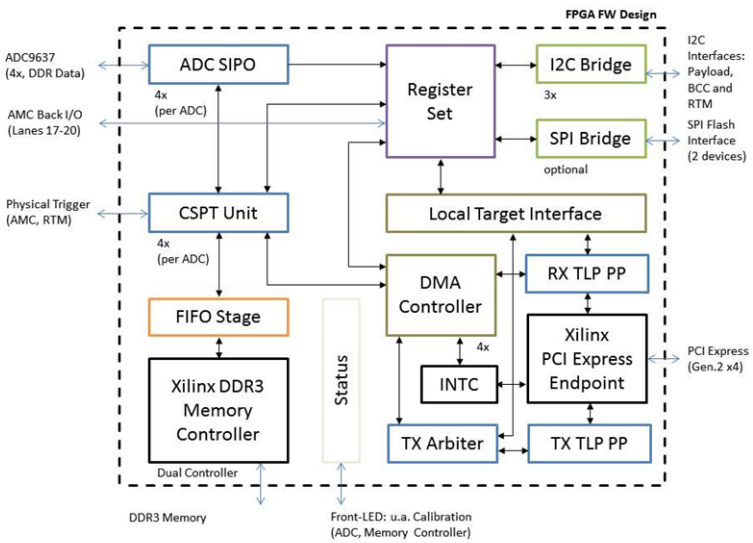

Figure 6-1 : TAMC532 Firmware SOC Structure

6.1.2 PCIe Configuration

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	8214 1498
0x04	Status		Command		Y	0480 000B
0x08	Class Code			Revision ID	N	068000 01
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 08
0x10	PCI Base Address 0 for Local Address Space 0				Y	FFFFF000
0x14	PCI Base Address 1 for Local Address Space 1				N	00000000
0x18	PCI Base Address 2 for Local Address Space 2				N	00000000
0x1C	PCI Base Address 3 for Local Address Space 3				N	00000000
0x20	PCI Base Address 4 for Local Address Space 4				N	00000000
0x24	PCI Base Address 5 for Local Address Space 5				N	00000000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	80xx 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00

Table 6-1 : PCIe Configuration Registers

Subsystem ID xx value encodes the module variant in a hexadecimal representation (TEWS definition).

BAR	Size (Byte)	Space	Prefetch	Port Width (Bit)	Endian Mode	Description
0	4k	MEM	No	32	Big	Module Register Space

Table 6-2 : PCIe Bar Overview

6.1.3 Register Interface

Single registers within the register space shall only be accessed (read or write) that is indicated size (column Size).

Offset to PCI Base Address	Register Name	Size (Bit)
0x00	Module Control Register	32
0x04	Module Status Register	32
0x08	Module Interrupt Enable Register	32
0x0C	Module Interrupt Status Register	32
0x10	ADC Channels [01, 00] Data Register	32
0x14	ADC Channels [03 ,02] Data Register	32
0x18	ADC Channels [05 ,04] Data Register	32
0x1C	ADC Channels [07 ,06] Data Register	32
0x20	ADC Channels [09, 08] Data Register	32
0x24	ADC Channels [11, 10] Data Register	32
0x28	ADC Channels [13, 12] Data Register	32
0x2C	ADC Channels [15, 14] Data Register	32
0x30	ADC Channels [17, 16] Data Register	32
0x34	ADC Channels [19, 18] Data Register	32
0x38	ADC Channels [21, 20] Data Register	32
0x3C	ADC Channels [23, 22] Data Register	32
0x40	ADC Channels [25, 24] Data Register	32
0x44	ADC Channels [27, 26] Data Register	32
0x48	ADC Channels [29, 28] Data Register	32
0x4C	ADC Channels [31, 30] Data Register	32
0x50	I2C Bridge Control Register	32
0x54	I2C Bridge Clock Divider Register	32
0x58	I2C Bridge Status Register	32
0x5C	I2C Bridge Command Register	32
0x60	I2C Bridge Write Data FIFO Interface Register	32
0x64	I2C Bridge Read Data FIFO Interface Register	32
0x68 : 0x7F	Reserved	-
0x80	DMA Controller #0 Control Register	32
0x84	DMA Controller #0 Status Register	32
0x88	DMA Controller #0 Base Descriptor Address Register	32
0x8C	DMA Controller #0 Current Memory Write Address Register	32
0x90	DMA Controller #1 Control Register	32
0x94	DMA Controller #1 Status Register	32
0x98	DMA Controller #1 Base Descriptor Address Register	32

Offset to PCI Base Address	Register Name	Size (Bit)
0x9C	DMA Controller #1 Current Memory Write Address Register	32
0xA0	DMA Controller #2 Control Register	32
0xA4	DMA Controller #2 Status Register	32
0xA8	DMA Controller #2 Base Descriptor Address Register	32
0xAC	DMA Controller #2 Current Memory Write Address Register	32
0xB0	DMA Controller #3 Control Register	32
0xB4	DMA Controller #3 Status Register	32
0xB8	DMA Controller #3 Base Descriptor Address Register	32
0xBC	DMA Controller #3 Current Memory Write Address Register	32
0xC0 : 0xFF	Reserved	-
0x100	Application Control Register (Application Control Register #0)	32
0x104	CSPT Unit A Control Register (Application Control Register #1)	32
0x108	CSPT Unit A Data Register #0 – Pre-Trigger Value (Application Control Register #2)	32
0x10C	CSPT Unit A Data Register #1 – Post-Trigger Value (Application Control Register #3)	32
0x110	Reserved	-
0x114	CSPT Unit B Control Register (Application Control Register #4)	32
0x118	CSPT Unit B Data Register #0 – Pre-Trigger Value (Application Control Register #5)	32
0x11C	CSPT Unit B Data Register #1 – Post-Trigger Value (Application Control Register #6)	32
0x120	Reserved	-
0x124	CSPT Unit C Control Register (Application Control Register #7)	32
0x128	CSPT Unit C Data Register #0 – Pre-Trigger Value (Application Control Register #8)	32
0x12C	CSPT Unit C Data Register #1 – Post-Trigger Value (Application Control Register #9)	32
0x130	Reserved	-
0x134	CSPT Unit D Control Register (Application Control Register #10)	32
0x138	CSPT Unit D Data Register #0 – Pre-Trigger Value (Application Control Register #11)	32
0x13C	CSPT Unit D Data Register #1 – Post-Trigger Value (Application Control Register #12)	32
0x140	Reserved	-
0x144 : 0x15F	Reserved	32

Offset to PCI Base Address	Register Name	Size (Bit)
0x160	Application Status Register (Application Status Register)	32
0x164	Application Command Register (Application Data Register)	32
0x168 : 0x1FB	Reserved	-
0x1FC	Firmware Identification Register	32

Table 6-3 : Module Register Space

6.1.3.1 Module Control Register (0x00)

Bit	Symbol	Description	Access	Reset Value
31 : 7	-	Reserved	R	0x0000
7 : 4	ADC_SIPO_DIS	ADC SIPO Unit Disable (ADC #3 … #0) For advanced control this bit allows enabling or disabling a specific ADC SIPO unit. Bit #4 corresponds with ADC SIPO Unit A Bit #5 corresponds with ADC SIPO Unit B Bit #6 corresponds with ADC SIPO Unit C Bit #7 corresponds with ADC SIPO Unit D Bit information mean: 0b0 = ADC SIPO Unit is enabled 0b1 = ADC SIPO Unit is disabled *Toggling one of this bits allows resetting the corresponding ADC SIPO Unit*	R/W	0x0
3 : 1	-	Reserved	R	0b000
0	MOD_INT_GE	Global Module Interrupt Enable The bit operates as master (module-wide) interrupt enable. If it is not set, the information within the Module Status Register are inhibited from generating PCIe Interrupts. Bit information mean: 0b0 = enable PCIe Interrupts 0b1 = disable PCIe Interrupts	R/W	0b0

Table 6-4 : Module Control Register (0x00)

6.1.3.2 Module Status Register (0x04)

Bit	Symbol	Description	Access	Reset Value
31 : 20	-	Reserved	R	0x0000
19 : 16	ADC_LOSS_DET	ADC Loss Of Calibration Detected Shows whether or not a loss of ADC calibration has been detected. Bit #16 corresponds with ADC SIPO Unit A Bit #17 corresponds with ADC SIPO Unit B Bit #18 corresponds with ADC SIPO Unit C Bit #19 corresponds with ADC SIPO Unit D Bit information mean: 0b0 = Loss of Calibration **not** detected 0b1 = Loss of Calibration detected	R/W1	0x0
15 : 13	-	Reserved	R	0
12	DCIRST_LOCKED	DCI Reset Locked Internal calibration requires resetting the DCI controller for correct multi-purpose I/O function. Bit information mean: 0b0 = DCI calibration in progress 0b1 = DCI calibrated *DCI calibration is required for correct functionality*	R	0
11 : 9	-	Reserved		0
8	Z3_EN	Zone 3 Enable Indicates whether Zone 3 is enabled (meaning that a MMC supported RTM is connected to the module) or not. Bit information mean: 0b0 = RTM not connected 0b1 = RTM connected *Information is provided by the MMC*	R	0
7 : 4	ADC_CAL_STAT	ADC Input Calibration State (ADC #3 … #0) Shows whether the ADC input SERDES logic has been calibrated on the ADC provided data and frame clock or not. Bit #4 corresponds with ADC SIPO Unit A Bit #5 corresponds with ADC SIPO Unit B Bit #6 corresponds with ADC SIPO Unit C Bit #7 corresponds with ADC SIPO Unit D Bit information mean: 0b0 = Calibration in progress/not completed 0b1 = Calibration completed	R	0
3	MOD_INT_MODE_MSI	Module Interrupt Mode MSI Indicates that the module uses MSI interrupts for interrupt generation. Bit information mean: 0b0 = MSI are not used 0b1 = MSI are used	R	0b0

Bit	Symbol	Description	Access	Reset Value
		Only a single MSI vector will be used		
2	MOD_INT_MODE_INT	Module Interrupt Mode INTA Indicates that the module uses legacy INTA interrupts for interrupt generation. Bit information mean: 0b0 = INTA are not used 0b1 = INTA are used	R	0b0
1	-	Reserved	R	0b0
0	MOD_INT_MODE_ERR	Module Interrupt Mode Error This error is signaled in case of an unsupported interrupt usage mode/mechanism. Bit information mean: 0b0 = Interrupts configured correctly (INTA/MSI) 0b1 = Interrupts configuration erroneous *No interrupts will be generated in case of an invalid interrupt configuration*	R	0b0

Table 6-5 : Module Status Register (0x04)

6.1.3.3 Module Interrupt Enable Register (0x08)

Bit	Symbol	Description	Access	Reset Value
31 : 24	-	Reserved	R	0x00
23	-	Reserved	R	0
22	DMAC_EOL_3_EN	DMA Controller #3 Descriptor End-Of-List Enable Controls whether an interrupt is generated after a descriptor has been processed / finalized that has the HI_EOL bit set. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
21	DMAC_DMF_3_EN	DMA Controller #3 Descriptor Data Memory Filled Enable Controls whether an interrupt is generated after a descriptor has been processed / finalized that has the HI_DMF bit set. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
20	DMAC_DDL_3_EN	DMA Controller #3 Descriptor Data Loaded Enable Controls whether an interrupt is generated after a descriptor has been loaded and queued that has the HI_DDL bit set. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
19	-	Reserved	R	0
18	DMAC_EOL_2_EN	DMA Controller #2 Descriptor End-Of-List Enable Controls whether an interrupt is generated after a descriptor has been processed / finalized that has the HI_EOL bit set. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
17	DMAC_DMF_2_EN	DMA Controller #2 Descriptor Data Memory Filled Interrupt Enable Controls whether an interrupt is generated after a descriptor has been processed / finalized that has the HI_DMF bit set.	R/W	0b0

Bit	Symbol	Description	Access	Reset Value
		Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation		
16	DMAC_DDL_2_EN	DMA Controller #2 Descriptor Data Loaded Enable Control whether an interrupt is generated after a descriptor has been loaded and queued that has the HI_DDL bit set. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
15	-	Reserved	R	0
14	DMAC_EOL_1_EN	DMA Controller #1 Descriptor End-Of-List Enable Controls whether an interrupt is generated after a descriptor has been processed / finalized that has the HI_EOL bit set. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
13	DMAC_DMF_1_EN	DMA Controller #1 Descriptor Data Memory Filled Enable Controls whether an interrupt is generated after a descriptor has been processed / finalized that has the HI_DMF bit set. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
12	DMAC_DDL_1_EN	DMA Controller #1 Descriptor Data Loaded Enable Controls whether an interrupt is generated after a descriptor has been loaded and queued that has the HI_DDL bit set. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
11	-	Reserved	R	0
10	DMAC_EOL_0_EN	DMA Controller #0 Descriptor End-Of-List Enable Controls whether an interrupt is generated after a descriptor has been processed / finalized that has the HI_EOL bit set.	R/W	0b0

Bit	Symbol	Description	Access	Reset Value
		Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation		
9	DMAC_DMF_0_EN	DMA Controller #0 Descriptor Data Memory Filled Enable Controls whether an interrupt is generated after a descriptor has been processed / finalized that has the HI_DMF bit set. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
8	DMAC_DDL_0_EN	DMA Controller #0 Descriptor Data Loaded Enable Controls whether an interrupt is generated after a descriptor has been loaded and queued that has the HI_DDL bit set. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
7 : 5	-	Reserved	R	0b000
4	I2C_BRDG_OCP_EN	I2C Bridge Operation Command Processed Enable Enable/disable interrupt generation after the end of the last initiated I2C operation on the selected I2C bus and target. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
3	-	Reserved	R	0b0
2	BCC_INTR_EN	BCC Interrupt Enable Enable/disable signalisation of BCC interrupt information. Bit setting means: 0b0 = disable interrupt generation 0b1 = enable interrupt generation	R/W	0b0
1 : 0	-	Reserved	R	0b00

Table 6-6 : Module Interrupt Enable Register (0x08)

6.1.3.4 Module Interrupt Status Register (0x0C)

Bit	Symbol	Description	Access	Reset Value
31 : 24	-	Reserved	R	0x00
23	-	Reserved	R	0
22	DMAC_EOL_3	DMA Controller #3 Descriptor End-Of-List A descriptor has been processed / finalized, which has the HI_EOL bit set. Bit information mean: 0b0 = default 0b1 = HI_EOL bit signalisation	R/W1C	0b0
21	DMAC_DMF_3	DMA Controller #3 Descriptor Data Memory Filled A descriptor has been processed / finalized, which has the HI_DMF bit set. Bit information mean: 0b0 = default 0b1 = HI_DMF bit signalisation	R/W1C	0b0
20	DMAC_DDL_3	DMA Controller #3 Descriptor Data Loaded A descriptor has been loaded and queued, which has the HI_DDL bit set. Bit information mean: 0b0 = default 0b1 = HI_DDL bit signalisation	R/W1C	0b0
19	-	Reserved	R	0
18	DMAC_EOL_2	DMA Controller #2 Descriptor End-Of-List A descriptor has been processed / finalized, which has the HI_EOL bit set. Bit information mean: 0b0 = default 0b1 = HI_EOL bit signalisation	R/W1C	0b0
17	DMAC_DMF_2	DMA Controller #2 Descriptor Data Memory Filled A descriptor has been processed / finalized, which has the HI_DMF bit set. Bit information mean: 0b0 = default 0b1 = HI_DMF bit signalisation	R/W1C	0b0
16	DMAC_DDL_2	DMA Controller #2 Descriptor Data Loaded A descriptor has been loaded and queued, which has the HI_DDL bit set. Bit information mean: 0b0 = default	R/W1C	0b0

Bit	Symbol	Description	Access	Reset Value
		0b1 = HI_DDL bit signalisation		
15	-	Reserved	R	0
14	DMAC_EOL_1	DMA Controller #1 Descriptor End-Of-List A descriptor has been processed / finalized, which has the HI_EOL bit set. Bit information mean: 0b0 = default 0b1 = HI_EOL bit signalisation	R/W1C	0b0
13	DMAC_DMF_1	DMA Controller #1 Descriptor Data Memory Filled A descriptor has been processed / finalized, which has the HI_DMF bit set. Bit information mean: 0b0 = default 0b1 = HI_DMF bit signalisation	R/W1C	0b0
12	DMAC_DDL_1	DMA Controller #1 Descriptor Data Loaded A descriptor has been loaded and queued, which has the HI_DDL bit set. Bit information mean: 0b0 = default 0b1 = HI_DDL bit signalisation	R/W1C	0b0
11	-	Reserved	R	0
10	DMAC_EOL_0	DMA Controller #0 Descriptor End-Of-List A descriptor has been processed / finalized, which has the HI_EOL bit set. Bit information mean: 0b0 = default 0b1 = HI_EOL bit signalisation	R/W1C	0b0
9	DMAC_DMF_0	DMA Controller #0 Descriptor Data Memory Filled A descriptor has been processed / finalized, which has the HI_DMF bit set. Bit information mean: 0b0 = default 0b1 = HI_DMF bit signalisation	R/W1C	0b0
8	DMAC_DDL_0	DMA Controller #0 Descriptor Data Loaded A descriptor has been loaded and queued, which has the HI_DDL bit set. Bit information mean: 0b0 = default 0b1 = HI_DDL bit signalisation	R/W1C	0b0

Bit	Symbol	Description	Access	Reset Value
7 : 5	-	Reserved	R	0b000
4	I2C_BRDG_OCP	I2C Bridge Operation Command Processed Signals the end of the last initiated I2C operation on the selected I2C bus and target. Bit information mean: 0b0 = default 0b1 = I2C Command Processed	R/W1C	0b0
3	-	Reserved	R	0b0
2	BCC_INTR	BCC Interrupt Enable Signalisation of BCC interrupt-information. Bit setting means: 0b0 = default 0b1 = BCC Interrupt (various information)	R/W1C	0b0
1 : 0	-	Reserved	R	0b00

Table 6-7 : Module Interrupt Status Register (0x0C)

6.1.3.5 ADC Channel [xx] Data Register

There are 16 equal-structured dual ADC Channel Data registers, showing the most-recent values of the 32 ADC inputs.

Register Offset = 0x10 + (#/2 * 0x4)

Bit	Symbol	Description	Access	Reset Value
31 : 16	ADC_CH	ADC Channel Data	R	0x0000
15 : 0	ADC_CH	The register bears the ADC channel data of two consecutive channels (2n, 2n +1). Irrespective of the ADC data output width (12 or 14 bit) the values are always most-significant bit aligned. *Left-most ADC Data Bit (12 or 14) is mapped onto either register bit #31 or Bit #15; remaining bits follow in descending order. In consequence of that the right-most register data bits are zero*	R	0x0000

Table 6-8 : ADC Channel [xx] Data Register

The reset value is shown before the ADC input calibration has been successfully performed.

The ADC Channel Data is always the last valid input obtained during successful ADC input calibration.

6.1.3.6 I2C Bridge Control Register (0x50)

Bit	Symbol	Description	Access	Reset Value
31 : 28	I2C_BUS_NUM	I2C Bus Number Selects one out of the available I2C busses that are connected to the FPGA. Bit setting means: 0x0 = BCC I2C Bus 0x1 = RTM I2C Bus (TEWS RTM Special) 0x2 = PL I2C Bus 0x3 = SFP Slot #0 0x4 = SFP Slot #1 Other settings are reserved and may result in an incorrect I2C Bridge Operation	R/W	0x0
27 : 20	I2C_DEV_NUM	I2C Device Number Defines the slave I2C device address on the selected I2C bus (I2C_BUS_NUM) to be the destination of an I2C operation *7-Bit addressing is supported only (A[6] : A[0])* *Device number is in LSB format, A[6] transmitted first on I2C bus*	R/W	0x00
19 : 12	WRS_SWR_DCNT	Write-Read Sequence Selected Write Data Count Selects the number of bytes to write during a Write-Read Sequence process. Bit setting means: 0x00 = 0 Byte 0x01 = 1 Byte … 0xFF = 255 Bytes *If 0x00 is selected, no write operation will be performed*	R/W	0x00
11 : 4	WRS_SRD_DCNT	Write-Read Sequence Selected Read Data Count Selects the number of bytes to read during a Write-Read Sequence process. Bit setting means: 0x00 = 0 Byte 0x01 = 1 Byte … 0xFF = 255 Bytes *If 0x00 is selected, no read operation will be performed*	R/W	0x00
3 : 1	-	Reserved	R	0b000
0	I2C_BRDG_EN	I2C Bridge Enable	R/W	0b0

Bit	Symbol	Description	Access	Reset Value
		Enables or disabled the I2C bridge. If the I2C is not enabled, its logic is held in reset state and will not react on any command. Bit setting means: 0b0 = disable Master 0b1 = enable Master		

Table 6-9 : I2C Bridge Control Register (0x50)

6.1.3.7 I2C Bridge Clock Divider Register (0x54)

Bit	Symbol	Description	Access	Reset Value
31 : 16	-	Reserved	R	0x0000
15 : 0	SCL_CDIV_VAL	SCL Clock Divider Value The value defines a divider that is applied on the internal processing clock (125 MHz) to derive the I2C SCL clock used during I2C master operations. SCL_{CLOCK} = 125 MHz / (SCL_CDIV_VAL / 2 +1) *Reset value causes 100 kHz SCL clock frequency*	R/W	0x04E2

Table 6-10 : I2C Bridge Clock Divider Register (0x54)

6.1.3.8 I2C Bridge Status Register (0x58)

Bit	Symbol	Description	Access	Reset Value
31 : 24	WR_DFIFO_CFL	Write Data FIFO Current Fill Level Reports the number of write data bytes currently stored within the Write Data FIFO. Bit information means: 0x00 = 0 bytes 0x01 = 1 byte … 0xFF = 255 bytes Internal data handling causes an increment and/or decrement of four bytes	R	0x00
23 : 16	RD_DFIFO_CFL	Read Data FIFO Current Fill Level Reports the number of read data bytes currently available for reading from the Read Data FIFO. Bit information means:	R	0x00

Bit	Symbol	Description	Access	Reset Value
		0x00 = 0 bytes 0x01 = 1 byte … 0xFF = 255 bytes		
15 : 14	-	Reserved	R	0b00
13	DEV_OP_ERR	Device Operation Erroneous Reports whether the last I2C operation has been performed successfully on the accessed I2C target or not. Bit information means: 0b0 = Operation terminated successfully 0b1 = Operation was erroneous (failed) *Information is persistent and cleared by an I2C operation*	R	0b0
12	BUS_ARBL	Bus Arbitration Lost Signals that the last I2C operation has not completed successfully (was interrupted) due to a loss of the I2C bus arbitration. Bit information means: 0b0 = Arbitration loss has not occurred 0b1 = Arbitration loss has occurred *Information is persistent and cleared by an I2C operation*	R	0b0
11 : 9	-	Reserved	R	0b000
8	DEV_DET	Device Detected Reports whether the I2C slave defined slave I2C device address has acknowledged the addressing. Bit information means: 0b0 = Acknowledge not detected 0b1 = Acknowledge detected *Information is persistent and cleared by an I2C operation*	R	0b0
7 : 6	-	Reserved	R	0b00
5	WRS_OP_IP	Write-Read Sequence in Progress Indicates that an I2C target read after write operation is currently been performed by the I2C master. Bit information means: 0b0 = No transfer in progress 0b1 = Transfer in progress *Information is signaled until the end of the transfer*	R	0b0

Bit	Symbol	Description	Access	Reset Value
4	BRDG_IDLE	Bridge Idle State Signals that the I2C bridge is in its idle state and ready / willing to process I2C bus commands. Bit information means: 0b0 = Master is Busy 0b1 = Master is Idle	R	0b0
3 : 1	-	Reserved	R	0b000
0	I2C_BUS_LS	I2C Bus Line State Shows the current detected line state. Bit information means: 0b0 = Line is idle 0b1 = Line is busy *Busy is reported after a I2C STA is detected until an I2C STO is detected*	R	0b0

Table 6-11 : I2C Bridge Status Register (0x58)

6.1.3.9 I2C Bridge Command Register (0x5C)

Bit	Symbol	Description	Access	Reset Value
31 : 12	-	Reserved	R	0x00000
11 : 9	-	Reserved	R	0b000
8	WRS_OP_CMD	Write-Read Operation Command The command allows performing a Read after Write sequence. The number of bytes to write first and read afterwards is configurable. *Write data is read from Transmit Data Register and read data is stored within the Receive Data Register* *Self-clearing command bit (reset by hardware)*	R0/W1	0b0
7 : 6	-	Reserved	R	0b00
5	RD_DFIFO_RST	Read Data FIFO Reset W1 writing clears the read data FIFO and resets its current fill level counter (RD_DFIFO_CFL) to zero. *Self-clearing command bit (reset by hardware)*	R0/W1	0b0
4	WR_DFIFO_RST	Write Data FIFO Reset W1 writing clears the write data FIFO and resets its current fill level counter (WR_DFIFO_CFL) to	R0/W1	0b0

Bit	Symbol	Description	Access	Reset Value
		zero. *Self-clearing command bit (reset by hardware)*		
3 : 1	-	Reserved	R	0b000
0	I2C_BRDG_RST	I2C Bridge Reset W1 writing resets the I2C bridge irrespective of a currently performed I2C operation. *Self-clearing command bit (reset by hardware)*	R0/W1	0b0

Table 6-12 : I2C Bridge Command Register (0x5C)

6.1.3.10 I2C Bridge Write Data FIFO Interface Register (0x60)

Bit	Symbol	Description	Access	Reset Value
31 : 0	WR_DFIFO_DREG	Write Data FIFO Data Register The register is connected to the write data FIFO input and register writes will fill the FIFO. Every write will increment its current fill level counter (WR_DFIFO_CFL)	R/W	0x00000000

Table 6-13 : I2C Bridge Write Data FIFO Interface Register (0x60)

6.1.3.11 I2C Bridge Read FIFO Data Register (0x64)

Bit	Symbol	Description	Access	Reset Value
31 : 0	RD_DFIFO_DREG	Read Data FIFO Data Register The register is connected to the read data FIFO output and register read will empty the FIFO. Every read will decrement its current fill level counter (RD_DFIFO_CFL)	R/W	0x00000000

Table 6-14 : I2C Bridge Read FIFO Data Register (0x64)

6.1.3.12 DMA Controller [x] Control Register

Register Offset = 0x80 + # * 0x10 , # = 0, 1, 2, 3

Bit	Symbol	Description	Access	Reset Value
31 : 4	-	Reserved	R	0x0000000
3 : 1	-	Reserved	R	0b0
0	DMAC_EN	DMA Controller Enable This includes prefetching DMA descriptors	R/W	0b0

Table 6-15 : DMA Controller [x] Control Register

Disabling the DMA Controller (DMAC_EN = 0) should only be done when the CSPT Units are not operating and while the DMA Controller is in idle state.

6.1.3.13 DMA Controller [x] Status Register

Register Offset = 0x84 + # * 0x10 , # = 0, 1, 2, 3

Bit	Symbol	Description	Access	Reset Value
31:16	DMAC_RDB_SIZE	Remaining Data Buffer Size Shows the remaining buffer size within the host memory, pointed by the current descriptor. *Size is given as integer DW number*	R	0x0000
15 : 8	DMAC_DQ_SIZE	Descriptor Queue Size Shows the number of locally stored / queued DMA descriptors within the DMA Controller *Size is given as integer number, incrementing by one for every Descriptor*	R	0x00
7	-	Reserved	R	0b0
6	DMAC_DQH_OOD	Descriptor Queue Handler Out-Of-Descriptors Error condition: No descriptor can be loaded. This state is the consequence of an descriptor load request from the Application Interface but there are no queued descriptors available and no Descriptor that can be loaded	R	0b0
5	DMAC_DQH_ECR	Descriptor Controller Handler Erroneous Completion Received Error condition: Descriptor data read failed. An error occurred while attempting to read	R	0b0

Bit	Symbol	Description	Access	Reset Value
		descriptor data from the host memory that was pointed by a Descriptor linked-list structure element		
4	DMAC_DQH_IDLE	Descriptor Queue Handler Idle Shows whether the Descriptor Queue Handler FSM is in idle state or not. This state is selected if • the descriptor initial / auto-load sequence has been performed and • the internal buffer descriptor memory is full (Descriptor Queue Size is 0xFF) or • an EOL has been found while pre-fetching a linked list	R	0b0
3 : 2	-	Reserved	R	0b00
1	DMAC_AIF_OOM	Application Interface Out-Of-Memory Error condition: No DMA data buffer available. This state is the consequence of an descriptor load request from a CSPT Unit but there are no queued descriptors available and no Descriptor that can be loaded	R	0b0
0	DMAC_AIF_IDLE	Application Interface Idle Shows whether the Application Interface FSM is ready / willing to accept input data for output DMA transfer	R	0b0

Table 6-16 : DMA Controller [x] Status Register

6.1.3.14 DMA Controller [x] Base Descriptor Address Register

Register Offest = 0x88 + # * 0x10 , # = 0, 1, 2, 3

Bit	Symbol	Description	Access	Reset Value
31:0	DMAC_BDA	Base Descriptor Address (Start of Linked List) Register writes cause a descriptor load sequence (stored / queued operation) if the descriptor memory is not full (not equal to 0xFF)	R/W	0x00000000

Table 6-17 : DMA Controller [x] Base Descriptor Address Register

6.1.3.15 DMA Controller [x] Current Memory Write Address Register

Register Offset = 0x8C + # * 0x10 , # = 0, 1, 2, 3

Bit	Symbol	Description	Access	Reset Value
31:0	DMAC_CMWRA	Current Memory Write Address Shows the host memory address within the currently active descriptor pointed host memory window, used for the next memory write	R/W	0x00000000

Table 6-18 : DMA Controller [x] Current Descriptor Address Register

6.1.3.16 Application Control Register (0x100)

Bit	Symbol	Description	Access	Reset Value
31:16	Reserved	-	R	0x0000
15:12	FLED_USER	Front LED User Output Determines the LED output states (on/off) of the Front LEDs if Front LED User Mode is selected. Bit #12 corresponds with LED 1 Bit #13 corresponds with LED 2 Bit #14 corresponds with LED 3 Bit #15 corresponds with LED 4 Bit setting means: 0b0 = LED off 0b1 = LED on	R/W	0x0
11:9	Reserved	-	R	0b000
8	FLED_MODE	Front LED Mode Determines whether the Front-LEDs operate in Status Mode or in User Mode. 0b0 = Status Mode (indicating Board Status Information) 0b1 = User Mode (indication User LED output)	R/W	0
7:4	Reserved	-	R	0x0
3 : 0	CSPT_EN	CSPT Unit x Enable This setting controls the ADC Channel Data input processing / transmission into the host memory. Bit #0 corresponds with CSPT Unit A Bit #1 corresponds with CSPT Unit B Bit #2 corresponds with CSPT Unit C Bit #3 corresponds with CSPT Unit D Bit setting means: 0b1 = enable 0b0 = disable	R/W	0x0

Table 6-19 : Application Control Register (0x100)

In Status Mode (FLED_MODE=0), which is the default after reset, the front panel LEDs 1-4 display board status information as described in chapter “LED Indicators”.

Setting FLED_MODE to 1, activating User Mode for the LEDs, provides full software control of LED 1-4 via FLED_USER of this register. Writes to FLED_USER only have effect when FLED:MODE is 1.

Internal CSPT Unit memory interface synchronization requires that the CSPT Units that share an memory interface (A and B or C and D) are both disabled before enabling either of them or both.

6.1.3.17 CSPT Unit [x] Control Register

Register Offset = 0x104 + (# * 0x10) , # = 0, 1, 2, 3

Bit	Symbol	Description	Access	Reset Value
31:24	Reserved	-	R	0x000
23:17	Reserved	-	R	0b000
16	CSPT_DEM	CSPT Data Endian Model Controls the ADC data path endianness to the DMA controller. Bit setting means: 0b0 = Normal 0b1 = Endian-Conversion	R/W	0b0
15 : 12	CSPT_TP	CSPT Trigger Polarity Allows adjusting the polarity of the selected External Trigger input (CSPT_ET). Bit setting means: 0x0 = Rising Edge 0x1 = Falling Edge	R/W	0x0
11 : 8	CSPT_ET	CSPT External Trigger Selects one out of the available External Trigger inputs. 0x1 = RTM D5 (Differential) 0x2 = RTM D6 (Differential) 0x3 = RTM D7 (Differential) 0x4 = RTM D8 (Differential) 0x5 = AMC Port 17 Rx 0x6 = AMC Port 17 Tx 0x7 = AMC Port 18 Rx 0x8 = AMC Port 18 Tx 0x9 = AMC Port 19 Rx 0xA = AMC Port 19 Tx 0xB = AMC Port 20 Rx 0xC = AMC Port 20 Tx Other settings are reserved and result in a trigger de-activation (off-state). *RTM D3 and RTM D4 (both differential) have been removed for compliance with TEWS RTM* *External trigger inputs are edge evaluated and level mode is not supported.*	R/W	0x0
7 : 5	Reserved	-	R	0x0

Bit	Symbol	Description	Access	Reset Value
4	CSPT_ABT_DIS	CSPT Automatic Buffer Termination Disable Controls the end-of-transfer DMA buffer handling. Bit setting means: 0b0 = Flush DMA data and terminate current DMA Descriptor after the number of configured samples (sum of pre- and post-trigger samples) has been queued for DMA transfer 0b1 = Do not flush DMA data and keep using the current DMA descriptor buffer *Disabling the automatic buffer termination requires manual flushing (CSPT_SW_BTERM) if the acquired amount of data does not match the buffer size.*	R/W	0
3 : 0	Reserved	-	R	0x0

Table 6-20 : CSPT Unit [x] Control Register

6.1.3.18 CSPT Unit [x] Data Register #0 – Pre-Trigger Sample Count

Register Offset = 0x108 + (# * 0x10) , # = 0, 1, 2, 3

Bit	Symbol	Description	Access	Reset Value
31:0	CSPT_PRT_SC	Pre-Trigger Sample Count Defines the number of samples to capture/transmit in pre-trigger data acquisition mode. *Must consider the memory depth*	R/W	0x00000000

Table 6-21 : CSPT Unit [x] Data Register #0 – Pre-Trigger Sample Count

6.1.3.19 CSPT Unit [x] Data Register #1 – Post-Trigger Sample Count

Register Offset = 0x10C + (# * 0x10) , # = 0, 1, 2, 3

Bit	Symbol	Description	Access	Reset Value
31:0	CSPT_POT_SC	Post-Trigger Sample Count Defines the number of samples to capture/transmit in post-trigger data acquisition mode. *Must consider the memory depth*	R/W	0x00000000

Table 6-22 : CSPT Unit [x] Data Register #1 – Post-Trigger Sample Count

6.1.3.20 Application Status Register (0x160)

Bit	Symbol	Description	Access	Reset Value
31 : 16	-	Reserved	R	0x0000
15 : 12	CSPT_ERR	CSPT Unit Error State General error information, used to signal one of the following two conditions: • ADC Data Overwrite Protection Activated • Trigger detected while CSPT Unit was not idle (missed trigger) Bit information mean: 0b0 = CSPT Unit is functional 0b1 = CSPT Unit signals error condition *Cleared when corresponding CSPT Unit is disabled*	R	0x0

Bit	Symbol	Description	Access	Reset Value
11 : 8	CSPT_ACT	CSPT Unit Active State Indicates that a CSPT Unit is currently processing / transmitting ADC Channel. Bit information mean: 0b0 = CSPT Unit is not active (idle) 0b1 = CSPT Unit is active	R	0x0
7 : 4	CSPT_RDY	CSPT Unit Ready State Indicates that a CSPT Unit is ready to accept a trigger input. Bit information mean: 0b0 = CSPT Unit is not ready 0b1 = CSPT Unit is ready	R	0x0
3 : 2	-	Reserved	R	0b00
1 : 0	MCC_STAT	Memory Controller Calibration State DDR3 Memory Controller Calibration States Bit #0 refers to DDR3 Memory Controller #0 Bit #1 refers to DDR3 Memory Controller #1 Bit information mean: 0b0 = Memory Controller is not Calibrated 0b1 = Memory Controller is Calibrated *Only if both Memory Controller are calibrated, the module is functional*	R	0b00

Table 6-23 : Application Status Register (0x160)

For all CSPT related, 4 bits or a nibble occupying, settings in this register, each bit of the nibble is assigned to a specific CSPT-Unit:

- Bit #3 corresponds with CSPT Unit D
- Bit #2 corresponds with CSPT Unit C
- Bit #1 corresponds with CSPT Unit B
- Bit #0 corresponds with CSPT Unit A

6.1.3.21 Application Command Register (0x164)

Bit	Symbol	Description	Access	Reset Value
31:12	Reserved	-	R	0x000000
11 : 8	CSPT_SW_BTERM	CSPT Unit Software Buffer Termination W1 writing flushes pending DMA data and terminates the current DMA descriptor of the DMA Controller linked to the CSPT Unit. *Self-clearing command bit (reset by hardware)* *Only affective while CSPT Unit is in idle state.* *CSPT Unit will get out of Idle for command processing.* *The corresponding DMA Controller will only flush and terminate the current DMA Buffer if there is any data in the pipeline.*	W1/R0	0
7 : 4	CSPT_SW_RST	CSPT Unit Software Reset W1 writing resets the corresponding regardless if it is enabled or not. *Self-clearing command bit (reset by hardware)*	W1/R0	0x0
3 : 0	CSPT_SW_TRIG	CSPT Unit Software Trigger Input W1 writing initiates / triggers a DMA operation cycle if the corresponding unit is enabled. *Self-clearing command bit (reset by hardware)*	W1/R0	0x0

Table 6-24 : Application Command Register (0x164)

For all CSPT related, 4 bits or a nibble occupying, settings in this register, each bit of the nibble is assigned to a specific CSPT-Unit:

- Bit #3 corresponds with CSPT Unit D
- Bit #2 corresponds with CSPT Unit C
- Bit #1 corresponds with CSPT Unit B
- Bit #0 corresponds with CSPT Unit A

6.1.3.22 Firmware Identification Register (0x1FC)

Bit	Symbol	Description	Access	Reset Value
31:24	FW_MAJ_VER	Firmware Major Version	R	0x00
23 : 16	FW_MIN_VER	Firmware Minor Version	R	0x00
15 : 8	FW_REV	Firmware Revision	R	0x00
7 : 0	FV_BLD_CNT	Firmware Build Count	R	0x00

Table 6-25 : Firmware Identification Register (0x1FC)

6.1.4 DMA Descriptors

DMA Descriptors uses four instruction double words (32 bit) with the structure shown below.

The instruction DWs are placed in an ascending order in the host memory and may not violate a 4k address boundary.

The Instruction DWs shall apply Big Endian Model within the host memory for correct usage.

Offset to PCI Base Address	Symbol	Description	Size (Bit)
0x0	IDW_0	Control Data	32
0x4	IDW_1	Next Descriptor Address	32
0x8	IDW_2	Data Memory Address	32
0xC	IDW_3	Reserved	32

6.1.4.1 DMA Descriptor Control DW

Bit	Symbol	Description	Access	Reset Value
31 : 16	DESCR_DBUF_SIZE	Data Buffer Size Indicates the size of the data memory range in the host memory. *Size is given as integer DW number*	R/W	0x0000
15 : 8	-	Reserved	R	0x00
7:5	-	Reserved	R	0b000
4	DESCR_HI_DDL	Descriptor Data Load Host Interrupt An interrupt is signaled after the descriptor instruction data have been loaded and queued. Bit setting means: 0b1 = enable interrupt generation 0b0 = disable interrupt generation	R/W	0b0
3 : 2	-	Reserved	R	0b00
1	DESCR_HI_DMF	Data Memory Filled Host Interrupt An interrupt is signaled after the descriptor has been processed / finalized (loading respectively switching to its successor). Bit setting means: 0b1 = enable interrupt generation 0b0 = disable interrupt generation *The interrupt is issued concurrently to the data submission*	R/W	0b0

Bit	Symbol	Description	Access	Reset Value
0	DESCR_HI_EOL	End-of-List Host Interrupt An interrupt is signaled after the descriptor has been processed / finalized. Bit setting means: 0b1 = enable interrupt generation 0b0 = disable interrupt generation *The interrupt may coincident with a Data Memory Filled interrupt*	R/W	0b0

Table 6-26 : DMA Descriptor Control DW

6.1.4.2 DMA Descriptor Next Descriptor Address

Bit	Symbol	Description	Access	Reset Value
31 : 0	DESCR_NDA	Next Descriptor Address Address of the next (linked-list) descriptor	R/W	0x00000000

Table 6-27 : DMA Descriptor Next Descriptor Address

6.1.4.3 DMA Descriptor Data Memory Address

Bit	Symbol	Description	Access	Reset Value
31 : 0	DESCR_DBUF_ADDR	Data Memory Address Address of the data buffer within the host memory. *The address and boundary must be DW aligned*	R/W	0x00000000

Table 6-28 : DMA Descriptor Data Memory Address

6.1.4.4 Reserved

Bit	Symbol	Description	Access	Reset Value
31 : 0	-	Reserved	R	0x00000000

Table 6-29 : Reserved

6.2 Board Configuration Controller (BCC)

The Board Configuration Controller provides power-up configuration of all on-board resources. Two I2C interfaces to the FPGA allow reconfiguring nearly all on-board resources at runtime.

6.2.1 BCC-I2C

The BCC-I2C bus contains only two I2C devices: The FPGA and the BCC. It is used for basic board configuration. If further control is needed, the Configuration-I2C bus can be used.

The I2C device address of the BCC target is 0b1101000 on BCC-I2C Bus.

Register Address	Register Name	Size (Bit)
0x00	LMK04816 Status Register	8
0x01	SI5338 Status Register	8
0x02	Rx/Tx Diff-Pair Control 17 Register	8
0x03	Rx/Tx Diff-Pair Control 18 Register	8
0x04	Rx/Tx Diff-Pair Control 19 Register	8
0x05	Rx/Tx Diff-Pair Control 20 Register	8
0x06	SFP Control Register	8
0x07	SPI Control Register	8
0x08	Jitter Attenuator Control Register	8
0x09	Miscellaneous Register	8
0x0A	Configuration DIP Switches Register	8
0x0B	ADC Input Amplifiers Control Register	8
0x0C	Frequency Adjustment Control Register	8
0x0D : 0xFB	Reserved	-
0xFC	Firmware Identification Register (Major ID)	8
0xFD	Firmware Identification Register (Minor ID)	8
0xFE	Firmware Identification Register (Revision)	8
0xFF	Firmware Identification Register (Build Count)	8

Table 6-30 : BCC Target Register Space

6.2.1.1 LMK04816 Status Register (0x00)

Bit	Symbol	Description	Access	Reset Value
7:5	-	Reserved	R	0b000
4	LMK_SLD	LMK Status Lock Detect Indicates the physical status of the LMK status lock detect pin. Bit information mean: 0b0 = PLL1 DLD and/or PLL2 DLD not asserted 0b1 = both LMK PLLs have locked *Both PLLs should have locked for a deterministic ADC operation (under default configuration)*	R	0b0
3	-	Reserved	R	0b0
2:0	LMK_SCI	LMK Status CLKIN2/1/0 Indicates the physical status of the LMK clock input pin (#2, #1 and #0). Bit 0 corresponds with Clock Input #0 (loop-back clock input or externally sourced clock input) Bit 1 corresponds with Clock Input #1 (on-board generated ADC clock provided by SI5338) Bit 2 corresponds with Clock Input #2 (not used) Bit information is equivalent for all inputs: 0b1 = Loss-of-Signal detected 0b0 = Signal input detected *For a deterministic ADC operation clock input #1 should signal an input, bit #0/#2 are irrespective (under default configuration)*	R	0b000

Table 6-31 : LMK04816 Status Register (0x00)

6.2.1.2 SI5338 Status Register (0x01)

Bit	Symbol	Description	Access	Reset Value
7:5	-	Reserved	R	0b000
4	SCG_INTR	System Clock Generator SI5338 Interrupt Request Indicates the physical status of the SI5338 interrupt request pin. Bit information mean: 0b0 = Interrupt request not asserted 0b1 = Interrupt request asserted *Under normal conditions no interrupt request should be asserted*	R	0b0
3:1	-	Reserved	R	0b000
0	UCG_INTR	User Clock Generator SI5338 Interrupt Request Indicates the physical status of the SI5338 interrupt request pin. Bit information mean: 0b0 = Interrupt request not asserted 0b1 = Interrupt request asserted *Under normal conditions no interrupt request should be asserted*	R	0b0

Table 6-32 : SI5338 Status Register (0x01)

6.2.1.3 AMC Rx/Tx Differential Pair [x] Control Register

There are four different registers with the same below structure. Every of these registers allow controlling one of the AMC port #17, #18, #19 and #20 connected LVDS buffers.

Register Offset = 0x02 + (# - 17) , # = 17, 18, 19, 20

Bit	Symbol	Description	Access	Reset Value
7:5	-	Reserved	R	0b000
4	MLVDS_FSS	MLVDS Failsafe Select Controls the fail-safe selection (type 1 or type 2 receiver input) of the AMC port MLVDS buffer. Bit setting cause: 0b0 = Disable Failsafe Receiver (Type 1 Receiver) 0b1 = Enable Failsafe Receiver (Type 2 Receiver)	R/W	0b0
3:2	-	Reserved	R	0b00
1	MLVDS_TX_DP_EN	TX Differential Pair Enable Controls the driver functionality of the AMC port MLVDS buffer TX differential pair output. Bit setting cause: 0b0 = Disable TX Differential Output 0b1 = Enable TX Differential Output *MLVDS device resist multiple drivers on the same node*	R/W	0b0
0	MLVDS_RX_DP_EN	RX Differential Pair Enable Controls the driver functionality of the AMC port MLVDS buffer RX differential pair output. Bit setting cause: 0b0 = Disable RX Differential Output 0b1 = Enable RX Differential Output *MLVDS device resist multiple drivers on the same node*	R/W	0b0

Table 6-33 : AMC Rx/Tx Differential Pair [x] Control Register

6.2.1.4 SFP Control Register (0x06)

Bit	Symbol	Description	Access	Reset Value
7:6	SFP1_RS	Rate Select SFP #1 Controls the state of the SFP #1 Rate Select pins. Bit 7 corresponds with RS Input #1 Bit 6 corresponds with RS Input #0 Bit setting is common for both pins and cause: *Effect depends on plugged SPF module*	R	0b00
5	-	Reserved	R	0b0
4	SFP1_TX_DIS	TX Disable SFP #1 Affects the SPF #1 TX output disable pin. 0b0 = Pin set to low-level 0b1 = Pin set to high-level	R/W	0b0
3:2	SFP0_RS	Rate Select SFP #0 Controls the state of the SFP #0 Rate Select pins. Bit 3 corresponds with RS Input #1 Bit 2 corresponds with RS Input #0 Bit setting is common for both pins and cause: 0b0 = Pin set to low-level 0b1 = Pin set to high-level *Effect depends on plugged SPF module*	R/W	0b00
1	-	Reserved	R	0b0
0	SFP0_TX_DIS	TX Disable SFP #0 Affects the SPF #0 TX output disable pin. 0b0 = Pin set to low-level 0b1 = Pin set to high-level	R/W	0b0

Table 6-34 : SFP Control Register (0x06)

6.2.1.5 SPI Control Register (0x07)

Bit	Symbol	Description	Access	Reset Value
7:5	-	Reserved	R	0x0
3:2	-	Reserved	R	0b00
1:0	SPI_FSC	SPI Flash Selection Control Determines the FPGA SPI Flash selection (linkage) for configuration and other accesses. Bit setting means: 0b00 = Selection is based on FPGA RS Pins 0b01 = Static SPI #0 Selection 0b10 = Static SPI #1 Selection 0b11 = Both SPI Flashes are disconnected	R/W	0b00

Table 6-35 : SPI Control Register (0x07)

6.2.1.6 Miscellaneous Register (0x09)

Bit	Symbol	Description	Access	Reset Value
7:6	FPGA_IN_1	RTM Turn-Off Signalisation Sets output of FPGA Input 1 which affects differential outputs RTM OUT #0 and #1. Bit setting means: 0b00 = tristate 0b10 = drive-low 0b11 = drive-high 0b01 = reserved *(DESY Feature)*	R/W	0b00
5:4	FPGA_IN_0	RTM Turn-Off Signalisation Sets output of FPGA Input 0 which affects differential outputs RTM OUT #0 and #1. Bit setting means: 0b00 = tristate 0b10 = drive-low 0b11 = drive-high 0b01 = reserved *(DESY Feature)*	R/W	0b00
3:2	-	Reserved	R	0b00
1	TCLKB_OUT_EN	TCLKB Output Enable Controls the LVDS output driver enable for TCLKB that is sourced by LMK04816. Bit setting means: 0b0 = output driver disabled 0b1 = output driver enabled	R/W	0b0
0	CONFIG_I2C_EN	Configuration I2C Bus Enable Enables or disables the FPGA configuration I2C bus access. Bit setting means: 0b0 = disabled 0b1 = enabled *FPGA is decoupled by default to allow BCC I2C configuration after power-up*	R/W	0b0

Table 6-36 : Miscellaneous Register (0x09)

6.2.1.7 Configuration DIP Switches Register (0x0A)

Bit	Symbol	Description	Access	Reset Value
7:4	-	Reserved	R	0x0
3 : 0	CFG_DIP_SW	BCC Configuration DIP Switch Settings Allows obtaining the current setting of the BCC configuration DIP switches Bit 3 corresponds with DIP Switch 3 Bit 2 corresponds with DIP Switch 2 Bit 1 corresponds with DIP Switch 1 Bit 0 corresponds with DIP Switch 0 Bit information means: 0b0 = enabled 0b1 = disabled	R	0bxxxx

Table 6-37 : Configuration DIP Switches Register (0x0A)

6.2.1.8 ADC Input Amplifiers Control Register (0x0B)

Bit	Symbol	Description	Access	Reset Value
7	DIS_AMP_D1	OP Amplifier ADC D1 Disable Bit Adjusts whether the analogue Operation Amplifier s for ADC D1 are disabled or enabled. Affected analog input paths: [28] Bit information means: 0b0 = enabled 0b1 = disabled *Setting is only effective if MMC signals a compatible RTM*	R/W	0b0
6	DIS_AMP_D	OP Amplifier ADC D Disable Bit Adjusts whether the analogue Operation Amplifier s for ADC D are disabled or enabled. Affected analog input paths: [24 25 26 27 29 30 31] Bit setting means: 0b0 = enabled 0b1 = disabled *Setting is only effective if MMC signals a compatible RTM*	R/W	0b0
5	DIS_AMP_C1	OP Amplifier ADC C1 Disable Bit Adjusts whether the analogue Operation Amplifier s for ADC C1 are disabled or enabled. Affected analog input paths: [16 22] Bit setting means: 0b0 = enabled	R/W	0b0

Bit	Symbol	Description	Access	Reset Value
		0b1 = disabled *Setting is only effective if MMC signals a compatible RTM*		
4	DIS_AMP_C	OP Amplifier ADC C Disable Bit Adjusts whether the analogue Operation Amplifier s for ADC C are disabled or enabled. Affected analog input paths: [17 18 19 20 21 23] Bit setting means: 0b0 = enabled 0b1 = disabled *Setting is only effective if MMC signals a compatible RTM*	R/W	0b0
3	DIS_AMP_B1	OP Amplifier ADC B1 Disable Bit Adjusts whether the analogue Operation Amplifier s for ADC B1 are disabled or enabled. Affected analog input paths: [10] Bit setting means: 0b0 = enabled 0b1 = disabled *Setting is only effective if MMC signals a compatible RTM*	R/W	0b0
2	DIS_AMP_B	OP Amplifier ADC B Disable Bit Adjusts whether the analogue Operation Amplifier s for ADC B are disabled or enabled. Affected analog input paths: [8 9 11 12 13 14 15] Bit setting means: 0b0 = enabled 0b1 = disabled *Setting is only effective if MMC signals a compatible RTM*	R/W	0b0
1	DIS_AMP_A1	OP Amplifier ADC A1 Disable Bit Adjusts whether the analogue Operation Amplifier s for ADC A1 are disabled or enabled. Affected analog input paths: [4] Bit setting means: 0b0 = enabled 0b1 = disabled *Setting is only effective if MMC signals a compatible RTM*	R/W	0b0
0	DIS_AMP_A	OP Amplifier ADC A Disable Bit Adjusts whether the analogue Operation Amplifier s for ADC A are disabled or enabled. Affected analog input paths: [0 1 2 3 5 6 7]	R/W	0b0

Bit	Symbol	Description	Access	Reset Value
		Bit setting means: 0b0 = enabled 0b1 = disabled *Setting is only effective if MMC signals a compatible RTM*		

Table 6-38 : ADC Input Amplifiers Control Register (0x0B)

6.2.1.9 Frequency Adjustment Control Register (0x0C)

Bit	Symbol	Description	Access	Reset Value
7:4	-	Reserved	R	0b00
6:5	FREQ_ADJ_CM	Frequency Adjustment Control Mode Selects one of the frequency control modes that adjust the ADC clock input path. Bit setting means: 0b00 = Frequency Sets Mode 0b10 = User Other settings are reserved and may result in an incorrect functionality	R/W	0b00
3:2	-	Reserved	R	0b00
1:0	FREQ_SET_SEL	Frequency Set Number Bit setting means: 0b00 = Set #0, ADCs operate with 50 MHz 0b01 = Set #1, ADCs operate with 10 MHz 0b10 = Set #2, ADCs operate with 75 MHz* 0b11 = Set #3, ADCs operate with TCLKA After a Frequency Set change, the ADCs are reset to guarantee proper ADC operation. This reset takes app. 3*10^6 sample clocks, or 300ms at 10MHz sample clock to complete. During reset, the ADCs deliver no or random data. Take care that TCLKA provides a stable clock of min. 10MHz before switching FREQ_SET_SEL to 0b11. *75MHz operation is not supported by 14-Bit ADCs	R	0b00

Table 6-39 : Frequency Adjustment Control Register (0x0C)

6.2.1.10 BCC Firmware Identification Register (0xFC)

Bit	Symbol	Description	Access	Reset Value
31:24	FW_MAJ_VER	BCC Firmware Major Version	R	0x00
23 : 16	FW_MIN_VER	BCC Firmware Minor Version	R	0x00
15 : 8	FW_REV	BCC Firmware Revision	R	0x00
7 : 0	FV_BLD_CNT	BCC Firmware Build Count	R	0x00

Table 6-40 : BCC Firmware Identification Register (0xFC)

6.2.2 Configuration-I2C

The Configuration-I2C bus provides full control over all on-board devices and can be used if the configuration possibilities provided by the BCC-I2C interface are not sufficient.

Access to this I2C bus from the FPGA has to be enabled using the BCC-I2C bus (set CONFIG_I2C_EN bit).

Besides the FPGA, the Configuration-I2C bus contains the following devices:

- Si5338 (0b1110001)
- Si5338 (0b1110000)
- M24C32 (0b1010000)
- 8N3QV01 (0b1101110)
- BCC Bridge (0b1101000)

6.2.2.1 BCC Bridge Register Space

Register Address	Register Name	Size (Bit)
0x00	ADC Setup Interface Control Register	8
0x01	ADC Setup Interface Status Register	8
0x02	ADC Interface Lower Target Address Register	8
0x03	ADC Interface Upper Target Address Register	8
0x04	ADC Interface Read Data	8
0x05	ADC Interface Write Data	8
0x06 : 0x0F	Reserved	8
0x10	LMK Setup Interface Control Register	8
0x11	LMK Setup Interface Status Register	8
0x12	LMK Setup Interface Read Data [7: 0]	8
0x13	LMK Setup Interface Read Data [15: 8]	8
0x14	LMK Setup Interface Read Data [23: 16]	8
0x15	LMK Setup Interface Read Data [31: 24]	8
0x16	LMK Setup Interface Write Data [7: 0]	8
0x17	LMK Setup Interface Write Data [15: 8]	8
0x18	LMK Setup Interface Write Data [23: 16]	8
0x19	LMK Setup Interface Write Data [31: 24]	8
0x1A : 0x1F	Reserved	-
0x20	CPS Setup Interface Control Register	8
0x21	CPS Setup Interface Status Register	8
0x22	CPS Setup Interface Read Data	8
0x23	CPS Setup Interface Write Data	8
0x24 : 0xFF	Reserved	-

Table 6-41 : BCC Bridge Register Space

6.2.2.2 ADC Setup Interface Control Register (0x00)

Bit	Symbol	Description	Access	Reset Value
7:6	-	Reserved	R	0x0
5:4	ADC_DEV_SEL	ADC Device Selection Determines which ADC is target of an access-operation. Bit setting means: 0b00 = ADC A 0b01 = ADC B 0b10 = ADC C 0b11 = ADC D	R/W	0b00
3:2		Reserved	R	0b00
1:0	ADC_RW_REQ	ADC Read/Write Request Write the following data to initiate the selected I/O request on the selected ADC: 0b01 = write request 0b10 = read request When read, Bit information means: 0b00 = no request in processing 0b01 = write request in progress 0b10 = read request in progress others = reserved *These are self-clearing command bits after request is processed*	R/W	0b0

Table 6-42 : ADC Setup Interface Control Register (0x00)

6.2.2.3 ADC Setup Interface Status Register (0x01)

Bit	Symbol	Description	Access	Reset Value
7:1	-	Reserved	R	0b000000
0	ADC_SIF_RDY	ADC Setup Interface Ready Indicates whether the selected ADC Setup Interface is willing/ready to process read/write commands or not. Bit information means: 0b0 = Busy 0b1 = Ready	R	0b0

Table 6-43 : ADC Setup Interface Status Register (0x01)

6.2.2.4 ADC Setup Interface Lower Target Address Register (0x02)

Bit	Symbol	Description	Access	Reset Value
7:0	ADC_LADDR	ADC Lower Target Register Address The register content defines together with ADC Setup Interface Upper Target Address Register the accessed ADC register address for reads or writes	R/W	0x00

Table 6-44 : ADC Setup Interface Lower Target Address Register (0x02)

6.2.2.5 ADC Setup Interface Upper Target Address Register (0x03)

Bit	Symbol	Description	Access	Reset Value
7:0	ADC_UADDR	ADC Upper Target Register Address The register content defines together with ADC Setup Interface Lower Target Address Register the accessed ADC register address for reads or writes	R/W	0x00

Table 6-45 : ADC Setup Interface Upper Target Address Register (0x03)

6.2.2.6 ADC Setup Interface Read Data (0x04)

Bit	Symbol	Description	Access	Reset Value
7:0	ADC_RD_DATA	ADC Read Data Shows the last data obtained during a read operation on the selected ADC. *Cleared after read operations*	R	0x00

Table 6-46 : ADC Setup Interface Read Data (0x04)

6.2.2.7 ADC Setup Interface Write Data (0x05)

Bit	Symbol	Description	Access	Reset Value
7:0	ADC_WR_DATA	ADC Read Data Stores the write data byte to be used by write operations on the selected ADC	R/W	0x00

Table 6-47 : ADC Setup Interface Write Data (0x05)

6.2.2.8 LMK Setup Interface Control Register (0x10)

Bit	Symbol	Description	Access	Reset Value
7:4	-	Reserved	R	0x0
3:2		Reserved	R	0b00
1:0	LMK_RW_REQ	LMK Read/Write Request Write the following data to initiate the selected I/O request on the LMK: 0b01 = write request 0b10 = read request When read, Bit information means: 0b00 = no request in processing 0b01 = write request in progress 0b10 = read request in progress others = reserved *These are self-clearing command bits after request is processed*	R/W	0b0

Table 6-48 : LMK Setup Interface Control Register (0x10)

6.2.2.9 LMK Setup Interface Status Register (0x11)

Bit	Symbol	Description	Access	Reset Value
7:1	-	Reserved	R	0b000000
0	LMK_SIF_RDY	LMK Setup Interface Ready Indicates whether the selected LMK Setup Interface is willing/ready to process read/write commands or not. Bit information means: 0b0 = Busy 0b1 = Ready	R	0b0

Table 6-49 : LMK Setup Interface Status Register (0x11)

6.2.2.10 LMK Read Data Register [x]

There are four registers to store the 32 bit read data provided by the LMK. The subsequent structure is command for all registers.

Register Offset = 0x12 + # , # = 0, 1, 2, 3

Bit	Symbol	Description	Access	Reset Value
7:0	LMK_RD_DATA	LMK Read Data Shows the last data DW obtained during a read operation on the LMK	R/W	0x00

Table 6-50 : LMK Read Register [x]

The LMKs register-address to read from is specified by writing the following into the LMK Write Data Registers:

- #0 = 0x1F
- #1 = LMK register address to read from
- #2 = 0x00
- #3 = 0x00

The read data is separated on the different registers as follows:

- Register #0, Bits [7: 0]
- Register #1, Bits [15: 8]
- Register #2, Bits [23:16]
- Register #3, Bits [31:24]

6.2.2.11 LMK Write Data Register [x]

There are four registers to store the 32 bit write data for the LMK. The subsequent structure is command for all registers.

Register Offset = 0x16 + # , # = 0, 1, 2, 3

Bit	Symbol	Description	Access	Reset Value
7:0	LMK_WR_DATA	LMK Write Data Stores the write data DW to be used by write operations on the selected ADC	R/W	0x00

Table 6-51 : LMK Write Register [x]

The read data is separated on the different registers as follows:

- Register #0, Bits [7: 0]
- Register #1, Bits [15: 8]
- Register #2, Bits [23:16]
- Register #3, Bits [31:24]

Bits [4:0] carry the register-address information. Refer to the LMK-manual for more details.

6.2.2.12 CPS Setup Interface Control Register (0x20)

Bit	Symbol	Description	Access	Reset Value
7:2	-	Reserved	R	0b000000
1:0	CPS_RW_REQ	CPS Write Request Initiate a write request on the CPS (Cross Point Switch): 0b00 = no request in processing 0b01 = write request in progress Others = reserved *Self-clearing command bits after request is processed*	R/W	0b00

Table 6-52 : CPS Setup Interface Control register (0x20)

6.2.2.13 CPS Setup Interface Status Register (0x21)

Bit	Symbol	Description	Access	Reset Value
7:1	-	Reserved	R	0b0000000
0	CPS_SIF_RDY	CPS Setup Interface Ready Indicates whether the selected CPS Setup Interface is willing/ready to process read/write commands or not. Bit information means: 0b0 = Busy 0b1 = Ready	R	0b0

Table 6-53 : CPS Setup Interface Read Data (0x21)

6.2.2.14 CPS Setup Interface Read Data (0x22)

Bit	Symbol	Description	Access	Reset Value
7:6	CPS_OP_3_IP	CPS Output 3 Input Shows the current configuration for CPS output #3. Bit information means: 0b00 = Input #0 0b01 = Input #1 0b10 = Input #2 0b11 = Input #3	R	0b00
5 : 4	CPS_OP_2_IP	CPS Output 2 Input Shows the current configuration for CPS output #2. Bit information means: 0b00 = Input #0 0b01 = Input #1 0b10 = Input #2 0b11 = Input #3	R	0b00
3 : 2	CPS_OP_1_IP	CPS Output 1 Input Shows the current configuration for CPS output #1. Bit information means: 0b00 = Input #0 0b01 = Input #1 0b10 = Input #2 0b11 = Input #3	R	0b00
1 : 0	CPS_OP_0_IP	CPS Output 0 Input Shows the current configuration for CPS output #0. Bit information means: 0b00 = Input #0 0b01 = Input #1 0b10 = Input #2 0b11 = Input #3	R	0b00

Table 6-54 : CPS Setup Interface Read Data (0x22)

6.2.2.15 CPS Setup Interface Write Data (0x23)

Writing into this register sets new configuration data for one CPS output.

Bit	Symbol	Description	Access	Reset Value
7 : 6	-	Reserved	R	0b00
5 : 4	CPS_COP_IO	CPS Configuration Output I/O Selects the CPS output to be configured. Bit setting means: 0b00 = Output #0 0b01 = Output #1 0b10 = Output #2 0b11 = Output #3	R/W	0b00
3 : 2	-	Reserved	R	0b00
1 : 0	CPS_CIP_IO	CPS Configuration Input I/O Selects the CPS input to be assigned to configuration output. Bit information means: 0b00 = Input #0 0b01 = Input #1 0b10 = Input #2 0b11 = Input #3	R/W	0b00

Table 6-55 : CPS Setup Interface Write Data (0x23)

7 Board Configuration

This chapter describes aspects of board configuration prior to board installation.

7.1 Overview

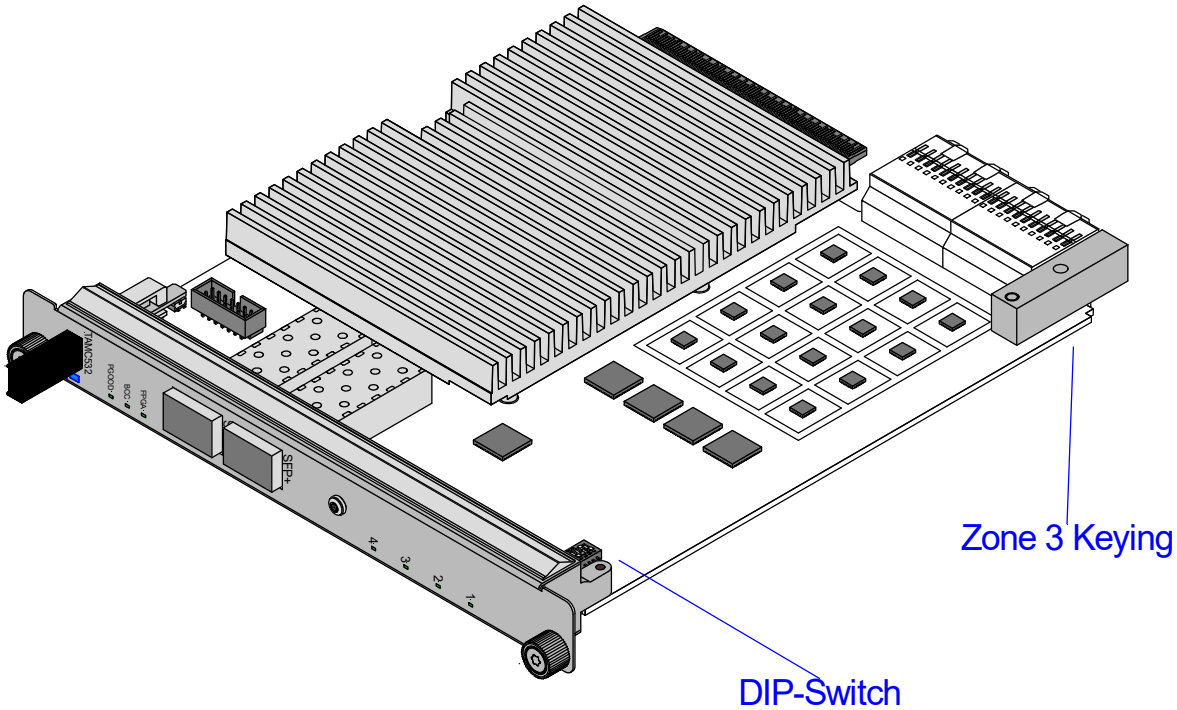

Figure 7-1 : Board Configuration Overview

7.2 Zone 3 Keying Pin

The TAMC532 provides the following female Zone 3 keying module:

N	A Rotation	View	Voltage Levels
0	NA	 View from the µRTM to the rear of the AMC white = clearance	-

Table 7-1 : Zone 3 Keying Pin

The keying module on the TAMC532 is just for alignment purposes, not for actual keying. This is due to the fact that the voltage levels on the TAMC532 Zone 3 interface do not match with any of the existing key definitions.

7.3 DIP-Switch

This DIP-Switch provides the following configuration options.

Switch No.	Switch Position	Description
1	ON	µRTM is excluded from the AMCs JTAG Chain
	OFF	µRTM is included in the AMCs JTAG Chain (*)
2	ON	Reserved
	OFF	
3	ON	Zone 3 AMC_CLK0 is enabled
	OFF	Zone 3 AMC_CLK0 is disabled (*)
4	ON	Reserved
	OFF	

Table 7-2 : DIP-Switch

(*) factory default setting

8 Installation

This chapter contains general notes regarding installing the AMC module into a system.

8.1 AMC Module Installation

During insertion and extraction, the operational state of the AMC is visible via the blue LED in the AMCs front panel. The following table lists all valid combinations of Hot-swap handle position and blue LED status, including a short description of what's going on.

Blue LED / Handle	On	Off	Long Blink	Short Blink
Open (Pulled out)	**Extraction:** Module can be extracted **Insertion:** Module is waiting for closed Handle	Module is waiting for hot swap negotiation	-	Hot swap negotiation in progress (Extraction)
Closed (Pushed all way in)	Module is waiting for hot swap negotiation	Module is active (operating)	Hot swap negotiation in progress (Insertion)	-

Figure 8-1 : Hot-Swap states

8.1.1 Insertion

Typical insertion sequence:

1. Insert the ACM module into its slot, with the board edges aligned to the card guides
2. Make sure that the module handle is pushed into the inserted position
    a. Blue LED turns "ON." (Module is ready to attempt activation by the system)
    b. Blue LED starts "Long Blink" (Hot Swap Negotiation / Module activation in progress)
    c. Blue LED turns "OFF", and green LED turns "ON" (Module is ready and powered)

When the Blue LED does not go off but returns to the "ON" state, the module FRU information is invalid or the system cannot provide the power requested by the AMC module.

8.1.2 Extraction

Typical Extraction sequence:

1. Pull the module handle out ½ way
    a. Blue LED starts "Short Blink" (Hot Swap Negotiation in progress)
    b. Blue LED turns "ON" (Module is ready to be extracted)
2. Pull the module handle out completely and extract the AMC module from the slot.

8.2 µRTM Module Installation

8.2.1 µRTM Insertion

1. Make sure that the front AMC is fastened to the MTCA.4 system
2. Simply insert the µRTM into the MTCA.4 system (slot must match for the front AMC) and fasten the µRTM to the MTCA.4 system
3. Close the µRTM Hot-Swap handle (if not already closed right from the start)
4. Wait until the blue Hot-Swap LED goes off and the green LED goes on

If the blue Hot-Swap LED stays active and the green LED stays off, the µRTM has been considered as incompatible to the front AMC (e.g. missing FRU information in µRTM EEPROM)

8.2.2 µRTM Extraction

1. Normal Operating (green LED is on, blue Hot-Swap LED is off)
2. Pull the µRTM Hot-Swap handle
3. Wait until the green LED goes off and the blue Hot-Swap LED shows activity
4. Wait until the blue Hot-Swap LED is permanently on
5. Unfasten the µRTM from the MTCA.4 system
6. Pull the µRTM from the MTCA.4 system (handle still pulled)

9 LED Indicators

For a quick visual inspection, the AMC module provides the following front panel LEDs.

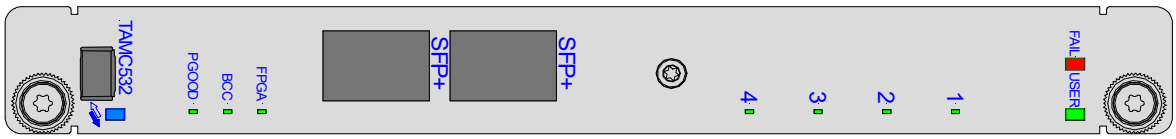

Figure 9-1 : Front Panel LED View

LED	Color	State	Description
HS	Blue	Off	No Power or Module is ready for normal operation
		Short Blink	Hot-Swap negotiation (extraction)
		Long Blink	Hot-Swap negotiation (insertion)
		On	Module is ready to attempt activation by the system or Module is ready to be extracted
FAIL	Red	Off	No fault
		On	Failure or out of service status
USER	Green	On	Board is powered-up and no fault is detected by the MMC

Table 9-1 : Basic MicroTCA LEDs

LED	Color	State	Description
PGOOD	Green	Off	On-Board Power Supplies are turned off
		On	On-Board Power Supplies are all turned on and ok
BCC	Green	Off	waiting for Payload Power
		Slow blink	Power-Supplies are on, Board configuration is in progress
		On	Board is powered up and configured
FPGA	Green	Off	FPGA is not configured or configuration failed
		On	FPGA has successfully configured

Table 9-2 : Board Status LEDs

Prior to FPGA configuration, the BCC controls the LEDs 1-4 to signal status information about the ongoing board initialization.

LED	State	BCC Status Information
4 : 1	0x0	Idle / Reset
	0x1	System Clock Generator Initialization in Progress
	0x2	User Clock Generator Initialization in Progress
	0x3	VCO Device Controller Initialization in Progress
	0x4	CPS Device Controller Initialization in Progress
	0x5	LMK Device Controller Initialization in Progress
	0x6	ADC A Initialization in Progress
	0x7	ADC B Initialization in Progress
	0x8	ADC C Initialization in Progress
	0x9	ADC D Initialization in Progress

Table 9-3 : Front Panel LEDs 1-4 (BCC controlled)

After successful board and FPGA configuration, the FPGA controls the LEDs. The following table provides a description of the LEDs 1-4 in Status Mode, which is default after power-up or reset.

LED	Color	State	Description
1	Green	any	CSPT Unit Activity Visualises whether the CSPT Units (A, B, C or D) are currently in idle state or not. On = CSPT Unit A, B, C or D is processing a data acquisition and transmission operation Off = All CSPT Units A, B, C and D are in idle state
2	Green	any	Memory Controller Calibration On = Memory Controller #0 and #1 functional Off = Memory Controller #0 and/or #1 **not** functional *The firmware processing functionality (application logic) should only be used if the Memory Controller Subsystem is in functional state*
3	Green	any	ADC Calibration Indicates whether the ADC input stage logic has been calibrated to the physical ADC data and frame clock or not. On = ADC Data Channel A, B, C and D calibrated Off = ADC Data Channel A, B, C and D **not** calibrated *The firmware processing functionality (application logic) should only be used if the ADC input stage has been calibrated*

LED	Color	State	Description
4	Green	any	Keep-Alive LED Signaling that the PCIe Subsystem is operating and that its reset has been de-asserted. Hence, the firmware is in operation state.

Table 9-4 : Front Panel LEDs 1-4 (Status Mode)

It is possible to change the behavior of LEDs 1-4 by selecting the User Mode in the Application Control Register. In User Mode, the LEDs are under software control. See the Application Control Register description for more details.

10 I/O Connectors

This chapter provides information about user accessible on-board connectors

10.1 Overview

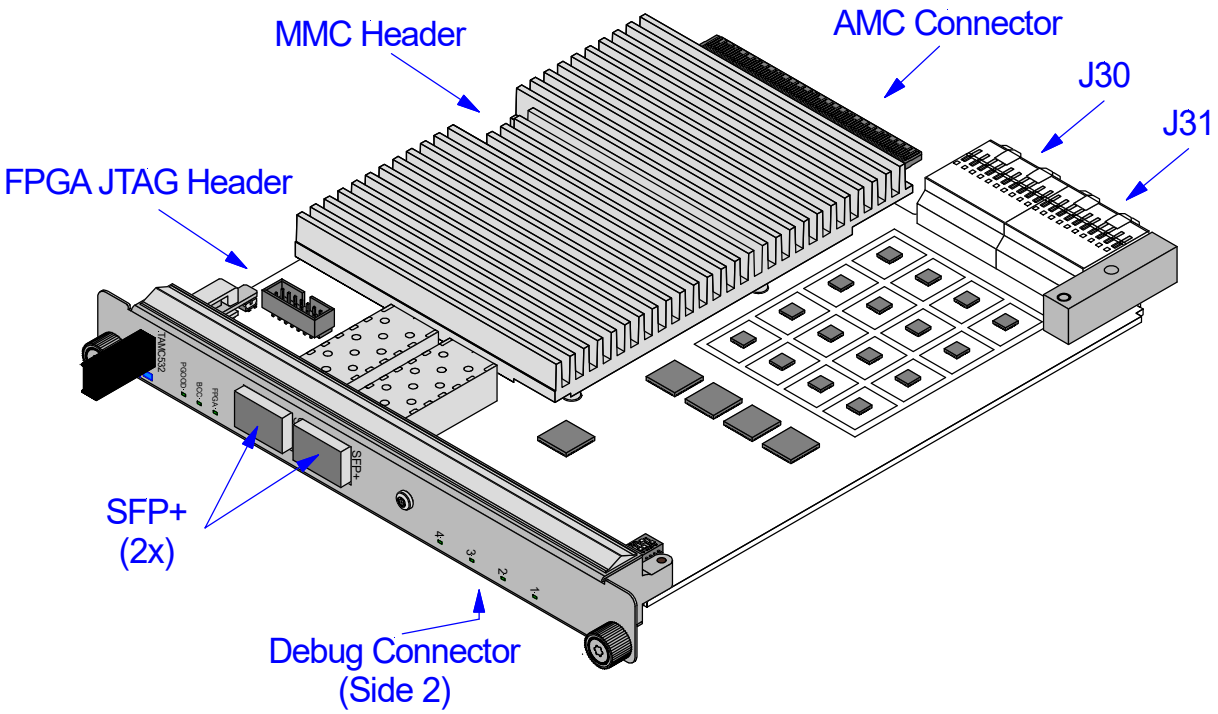

Figure 10-1 : Connector Overview

10.2 Zone 3 Connectors

The TAMC532 provides two 30-pair ADF connectors (J30 and J31) that build the Zone 3 Interface according to Class A2.1.

Pin-Count	30 contact pairs (60 signal contacts) + 30 GND pins
Connector Type	Advanced Differential Fabric (ADF) connector
Source & Order Info	Erni 973028 or compatible

10.2.1 J30

ADF connector ground pins are not shown.

	A	B	C	D	E	F
1	PWR	PWR	PS#	SDA	TCK	TDO
2	PWR	PWR	MP	SCL	TDI	TMS
3	SFP-CLK+	SFP-CLK-	SFP-Rx+	SFP-Rx-	SFP-Tx+	SFP-Tx-
4	D3+	D3-	D4+	D4-	D5+	D5-
5	D6+	D6-	D7+	D7-	D8+	D8-
6	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
7	GND	GND	GND	GND	GND	GND
8	AMC_CLK0+	AMC_CLK0-	-	-	-	-
9	RTM_CLK0+	RTM_CLK0-	-	-	-	-
10	-	-	CH31+	CH31-	CH30+	CH30-

Table 10-1 : Zone 3 J30 Connector Pin Assignment

10.2.2 J31

ADF connector ground pins are not shown.

	A	B	C	D	E	F
1	CH29+	CH29-	CH28+	CH28-	CH27+	CH27-
2	CH26+	CH26-	CH25+	CH25-	CH24+	CH24-
3	CH23+	CH23-	CH22+	CH22-	CH21+	CH21-
4	CH20+	CH20-	CH19+	CH19-	CH18+	CH18-
5	CH17+	CH17-	CH16+	CH16-	CH15+	CH15-
6	CH14+	CH14-	CH13+	CH13-	CH12+	CH12-
7	CH11+	CH11-	CH10+	CH10-	CH9+	CH9-
8	CH8+	CH8-	CH7+	CH7-	CH6+	CH6-
9	CH5+	CH5-	CH4+	CH4-	CH3+	CH3-
10	CH2+	CH2-	CH1+	CH1-	CH0+	CH0-

Table 10-2 : Zone 3 J31 Connector Pin Assignment

10.3 SFP+ Connectors

The pin assignment of the SFP+ connectors follows the SFP+ specification.

Pin	Signal	I/O	Description
1	VeeT	-	Ground
2	Tx Fault	Output	Transmitter Fault Indication
3	Tx Disable	Input	Transmitter Disable
4	SDA	I/O	I2C Data
5	SCL	Input	I2C Clock
6	ABS	Output	Module Absent
7	RS 0	Input	Receiver Bandwidth Select 0
8	LOS	Output	Loss Of Signal
9	RS 1	Input	Receiver Bandwidth Select 1
10	VeeT	-	Ground
11	VeeT	-	Ground
12	RD-	Input	Receive Data Output-
13	RD+	Input	Receive Data Output+
14	VeeT	-	Ground
15	VccR	Output	+3.3 Volt
16	VccT	Output	+3.3 Volt
17	VeeT	-	Ground
18	TD+	Output	Transmit Data Input+
19	TD-	Output	Transmit Data Input-
20	VeeT	-	Ground

Table 10-3 : SFP+ Connector Pin Assignment

10.4 FPGA JTAG Connector

The FPGA JTAG Connector allows direct connection to a Xilinx Platform Cable USB

Pin-Count	14
Connector Type	14-pin 2mm box header
Source & Order Info	Molex 87832-1420

Pin	Signal	Module I/O	Description
1	n.c.	-	Not used
2	V_{REF}	Output	IO Reference Voltage
3	GND	-	Ground
4	TMS	Input	Test Mode Select Input
5	GND	-	Ground
6	TCK	Input	Test Clock
7	GND	-	Ground
8	TDO	Output	Test Data Output
9	GND	-	Ground
10	TDI	Input	Test Data Input
11	GND	-	Ground
12	n.c	-	Not used
13	PGND	Input	Programmer present detection
14	n.c.	-	Not used

Table 10-4 : FPGA JTAG Connector Pin Assignment

10.5 Debug Connector

The Debug connector is located on Side 2 of the TAMC532, and allows direct connection of the TEWS program and debug box TA900.

Pin-Count	20
Connector Type	20-pin, 1mm FPC (Flexible Printed Circuit)
Source & Order Info	AMP 2-487951-0 / 2-84953-0 Molex 0522072060

Mating Flexible Printed Circuits: 20 mm (isolated length):

Adapt-Elektronik, 280-1.0-B-20-200-5-5-10-10)

Pin	Signal	Module I/O	Description
1	DBG_PRSNT#	Input	External Debug Hardware is connected / present
2	JTAG_VIO	Output	JTAG Reference I/O Voltage (+3.3V)
3	TDO	Output	JTAG Chain Test Data Output
4	GND	-	Ground
5	TDI	Input	JTAG Chain Test Data Input
6	TMS	Input	JTAG Chain Test Mode Select Input
7	GND	-	Ground
8	TCK	Input	JTAG Chain Test Clock
9	GND	-	Ground
10	PL_RX	Input	Not used
11	PL_VIO	Output	FPGA UART Reference I/O Voltage (+1.5V)
12	PL_TX	Output	Not used
13	GND	-	Ground
14	MMC_RX	Input	MMC UART Receive Data
15	MMC_VIO	Output	MMC UART Reference I/O Voltage (+3.3V / MP)
16	MMC_TX	Output	MMC UART Transmit Data
17	GND	-	Ground
18	3.3V	Output	+3.3Volt
19	USER_VIO	Output	User signal Reference I/O Voltage (+1.5V)
20	USER#	I/O	User signal connected to the FPGA. A Pullup (app. 3k) is located on the TAMC532

Table 10-5 : Debug Connector Pin Assignment

10.6 AMC Connector

This is an excerpt from the AMC-connector pin assignment. Only the user available signals are listed.

Pin	Signal	Function
15	Rx0-	AMC port 0 Connected to Lane 2 of MGT_BANK_115
14	Rx0+	
12	Tx0-	
11	Tx0+	
48	Rx4-	AMC port 4 Connected to Lane 3 of MGT_BANK_116
47	Rx4+	
45	Tx4-	
44	Tx4+	
54	Rx5-	AMC port 5 Connected to Lane 2 of MGT_BANK_116
53	Rx5+	
51	Tx5-	
50	Tx5+	
63	Rx6-	AMC port 6 Connected to Lane 1 of MGT_BANK_116
62	Rx6+	
60	Tx6-	
59	Tx6+	
69	Rx7-	AMC port 7 Connected to Lane 0 of MGT_BANK_116
68	Rx7+	
66	Tx7-	
65	Tx7+	
81	FCLKA-	PCIe Ref.-Clock Connected to CLK0 of MGT_BANK_116
80	FCLKA+	
78	TCLKB-	Differential Clock Input or Output
77	TCLKB+	
75	TCLKA-	Differential Clock Input
74	TCLKA+	

Pin	Signal	Function
111	Rx12-	AMC Port 12 Connected to Lane 1 of MGT_BANK_115
112	Rx12+	
114	Tx12-	
115	Tx12+	
141	Rx17-	Connected to M-LVDS Transceiver
142	Rx17+	
144	Tx17-	Connected to M-LVDS Transceiver
145	Tx17+	
141	Rx18-	Connected to M-LVDS Transceiver
142	Rx18+	
144	Tx18-	Connected to M-LVDS Transceiver
145	Tx18+	
141	Rx19-	Connected to M-LVDS Transceiver
142	Rx19+	
144	Tx19-	Connected to M-LVDS Transceiver
145	Tx19+	
141	Rx20-	Connected to M-LVDS Transceiver
142	Rx20+	
144	Tx20-	Connected to M-LVDS Transceiver
145	Tx20+	
165	TCK	JTAG Interface
166	TMS	
168	TDO	
169	TDI	

Table 10-6: AMC Connector Pin Assignment

10.7 MMC Header

The dedicated MMC JTAG/ISP Header is for factory use only.

Pin-Count	10
Connector Type	10-pin 2mm box header
Source & Order Info	Molex 87832-1020

Pin	Signal	Module I/O	Description
1	TCK	Input	Test Clock
2	GND	-	Ground
3	TDO	Output	Test Data Output (TAP Controller: TDI)
4	VT_{REF}	-	Reference Voltage
5	TMS	Input	Test Mode Select Input
6	nSRST	Input	MMC RESET#
7	n.c.	-	Connected to MP
8	nTRST	Input	Connected to PENABLE#
9	TDI	Input	Test Data Input (TAP Controller: TDO)
10	GND	-	Ground

Table 10-7 : MMC Header Pin Assignment, factory use only

MMC Header is reserved for factory use. Do not plug anything to this header-field.