The Embedded I/O Company

TEWS TECHNOLOGIES

TAMC631

Spartan-6 AMC with FMC Module Slot

Version 1.0

User Manual

Issue 1.0.4

May 2012

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TAMC631-10R

XC6SLX25T-2, 256 MB DDR3, Mid-Size front panel

TAMC631-11R

same as TAMC631-10R but Full-Size front panel

TAMC631-12R

XC6SLX75T-2, 256 MB DDR3, Mid-Size front panel

TAMC631-13R

same as TAMC631-12R but Full-Size front panel

TAMC631-14R

XC6SLX100T-2, 256 MB DDR3, Mid-Size front panel

TAMC631-15R

same as TAMC631-14R but Full-Size front panel

TAMC631-16R

XC6SLX15T-2, 256 MB DDR3, Mid-Size front panel

TAMC631-17R

same as TAMC631-16R but Full-Size front panel

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	October 2010
1.0.1	Added Variants -14R, -15R, -16R, -17R *4. IPMI Support*: Completely rewritten *5.4 Configuration*: Added note that JTAG-capable hardware is needed, added note about VCCO voltages and blank configuration devices *5.4.3 Selecting the Configuration Source*: Added note about “Enable BitStream Compression” for LX150T devices *5.5.2 Programmable Clock Generator*: Changed the default clock frequencies *5.6.1 DDR3 SDRAM*: Updated Table 5-11: DDR3 SDRAM Part History Various minor changes and rephrasings	February 2011
1.0.2	*Table 5 9: Programmable Clock:* Corrected USER_CLK1 to 62.5 MHz	June 2011
1.0.3	Added *6.3 Troubleshooting* Added *Appendix A* (generic user constraint file)	December 2011
1.0.4	Added *4.2.4.3 Clock Configuration* *4.2.4.1 Module Current Requirements*: Rewritten and elaborated how to estimate the power requirements for a user design.	May 2012

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1 Product Description

The TAMC631 is a standard single Mid-Size or Full-Size AMC.1 Type 1 module providing a user configurable XC6SLX25T-2, XC6SLX75T-2, XC6SLX100T-2 or XC6SLX150T-2 Spartan-6 FPGA. The Spartan-6's PCIe Endpoint Block is connected to AMC port 4. The TAMC631 variants with XC6SLX75T, XC6SLX100T and XC6SLX150T FPGA also provide connections to AMC port 0 and 1.

For flexible front I/O solutions the TAMC631 provides a VITA 57.1 FMC Module slot with a low-pin count connector, allowing active and passive signal conditioning. All FMC I/O lines are directly connected to the FPGA, which maintains the flexibility of the SelectIO technology of the Spartan-6 FPGA. The low-pin count interface includes one multi-gigabit link.

The FPGA is connected to two banks of 128 Mbytes, 16 bit wide DDR3 SDRAM. The SDRAM-interface uses the hardwired internal Memory Controller Blocks of the Spartan-6.

The FPGA is configured by a platform flash which is programmable via a JTAG header. The JTAG header also supports readback and on-chip debugging of the FPGA design (using Xilinx "ChipScope"). An SPI-EEPROM can be used as alternative configuration source or for user data storage. The TAMC631 is delivered with blank configuration flashes.

A programmable clock generator (5 KHz – 500 MHz) supplies up to three different clock frequencies to the FPGA. The clock generator settings are programmable via JTAG and are stored in an EEPROM. In addition two differential reference clocks are available from the FMC slot to the FPGA.

User applications for the TAMC631 with XC6SLX25T-2 and XC6SLX75T-2 FPGA can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com. The larger FPGA densities require a full licensed ISE Design Suite.

TEWS offers an FPGA Development Kit (TAMC631-FDK) which consists of a well documented basic example design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TAMC631. It implements a DMA capable PCIe endpoint with interrupt support, register mapping, DDR3 memory access and basic I/O to the FMC slot. It comes as a Xilinx ISE project with source code and as ready-to-download bitstream.

Please note: The basic example design requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (can be downloaded from www.xilinx.com, a 30 day evaluation license is available).

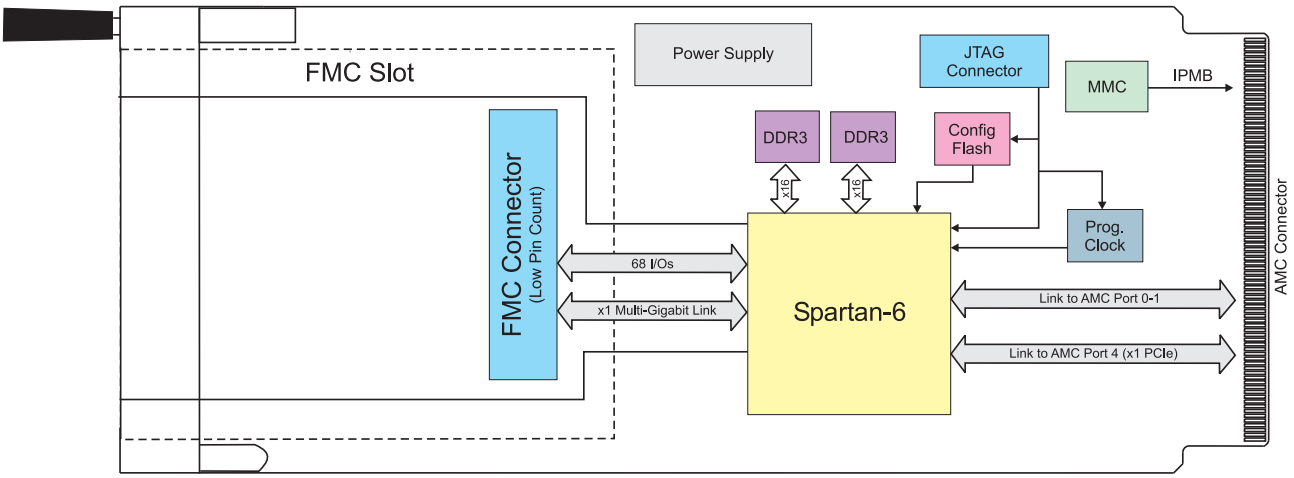

Figure 1-1 : Block Diagram

2 Technical Specification

AMC Interface	
Mechanical Interface	Advanced Mezzanine Card (AMC) Interface conforming to PICMG® AMC.0 R2.0 (Advanced Mezzanine Card Base Specification) Module Type: Single Mid-size module (-10R, -12R, -14R, -16R) Module Type: Single Full-size module (-11R, -13R, -15R, -17R)
Electrical Interface	PICMG® AMC.1 R1.0 PCIe single lane (x1) port (AMC.1 Type 1 compliant) Spartan-6 GTPs connected to AMC port 0 and 1 (not on -10R & -11R)
IPMI	
IPMI Version	1.5
Front Panel LEDs	Blue Hot-Swap LED Red Failure Indication LED (LED1) Green Board OK / User LED (LED2)
On Board Devices	
PCIe Endpoint	Spartan-6 PCI Express Endpoint Block
User configurable FPGA	Spartan-6 (Xilinx) TAMC631-10R, -11R: XC6SLX25T-2 TAMC631-12R, -13R: XC6SLX75T-2 TAMC631-14R, -15R: XC6SLX100T-2 TAMC631-16R, -17R: XC6SLX150T-2
Configuration Flash	XCF32P (Xilinx) Revision A modules: TAMC631-10R / -11R: XCF16P
SPI-Flash	MP25P64 (Micron) 64 Mbit (can be used for FPGA configuration) Revision A modules: MP25P32
DDR3 RAM	MT41J64M16 (Micron) 64 Meg x 16 Bit
Programmable Clock Generator	5V9885 (IDT)
I/O Interface	
I/O Connector	FMC low pin count slot according to VITA 57.1 (FPGA Mezzanine Card (FMC) Standard)
User Defined Signals	34 differential or 68 single-ended I/O plus 2 differential Clocks
Multi-Gigabit-Interfaces	1 gigabit data plus gigabit reference clock

Physical Data		
Power Requirements	Depends on FPGA design. 300 mA typical @ +12V DC (Payload Power, Blank FPGA) 35 mA typical @ +3.3V DC (Management Power) Additional power is used by the FMC. 4.5A as per Module Current Requirement	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	260 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	102 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instruction

3.1 ESD Protection

The TAMC631 is sensitive to static electricity. Packing, unpacking and all other handling of the TAMC631 has to be done in an ESD/EOS protected Area.

3.2 Thermal Considerations

Forced air cooling is recommended during operation. Without forced air cooling, damage to the device can occur.

3.3 I/O Signaling Voltages

The FPGA I/O-Lines to the FMC Slot are directly connected to the FPGA I/O pins. The I/O voltage of these FPGA I/O pins is 3.3V maximum.

The FPGA I/O pins are NOT 5V tolerant.

3.4 TAMC631 Mid-size Option Usage Restrictions

Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module with its component height violation can be used in the system. Otherwise damage to the TAMC631 or the slot it is used in may occur!

Refer to the chapter “Using FMCs with Mid-size faceplates” for details.

3.5 Voltage Limits on FMCs

The AMC.0 specification limits the voltages on AMC modules. These limits also apply to mounted FMCs.

Refer to the chapter “Voltage Limits on FMC Modules” for details.

4 IPMI Support

The TAMC631 provides a Module Management Controller (MMC) that performs health monitoring, hot-swap functionality and stores the Field Replaceable Unit (FRU) information. The MMC communicates via an Intelligent Platform Management Interface (IPMI).

4.1 Temperature and Voltage Sensors

The MMC monitors on board sensors and signals sensor events to the superordinated IPMI controller / shelf manager.

Sensor Number	Signal Type	Thresholds[1]	Signal Monitored
0	Event	-	Hot-swap switch
1	Temperature	lcr lnc unc ucr	LM75 #1
2	Temperature	lcr lnc unc ucr	LM75 #2
3	Voltage	lcr lnc unc ucr	+12V (PWR)
4	Voltage	lcr lnc unc ucr	+12V (FMC)
5	Voltage	lcr lnc unc ucr	+5V
6	Voltage	lcr lnc unc ucr	+1.8V

Table 4-1 : Temperature and Voltage Sensors

4.2 FRU Information

The MMC stores the module FRU information in a non-volatile EEPROM. Some of the records are writeable to allow adapting the TAMC631 to the user FPGA designs. If records are modified, the user is responsible to set the proper checksums.

Area	Size (in Bytes)	Writeable
Common Header	8	no
Internal Use Area	72	yes
Chassis Info Area	0	no
Board Info Area	variable	no
Product Info Area	variable	no
Multi Record Area	variable	see below
Module Current Requirements	variable	yes
AMC Point-to-Point Connectivity	variable	yes
Clock Configuration	variable	yes

Table 4-2 : FRU Information

[1] unr: upper non-recoverable, ucr: upper critical, unc: upper non-critical lnc: lower non-critical, lcr: lower critical, lnr: lower non-recoverable

4.2.1 Internal Use Area

The TAMC631 uses the Internal Use Area to store default FMC-slot settings for the case that a module is present, but no valid FRU information is found. The value of “Fallback-Voltage for VADJ” determines what happens in this case. If the “Fallback-Voltage for VADJ” is set to 0x0000, the module won’t turn on. Any other value sets VADJ to “Fallback-Voltage for VADJ” * 10mV, as long this value is within the range defined by Minimum VADJ and Maximum VADJ. Example: 0x00FA = 250 * 10mV = 2.5V.

Product Information	Value
Internal Use Format Version	1
TEWS IUA Format-Version	0x01
Present FMC Slots	0x01 – FMC-slot #0
Fallback-Voltage for VADJ	0x0000 – if no valid FMC-FRU is found, the TAMC631 won’t turn on.
Minimum VADJ	0x0078 – 1200mV for TAMC631
Maximum VADJ	0x014A – 3300mV for TAMC631

Table 4-3 : Internal Use Area

The whole Internal Use Area is writeable, but if changes become necessary, only the Fallback-Voltage for VADJ should be altered.

4.2.2 Board Info Area

Product Information	Value
Version	1
Language Code	0x00 - English
Manufacturer date/time	determined at manufacturing
Board manufacturer	TEWS TECHNOLOGIES GmbH
Board product name	TAMC631
Board serial number	determined at manufacturing (see board label)
Board part number	TAMC631-xxR

Table 4-4 : Board and Product Info Area

-xx = -10R / -11R / -12R / -13R / -14R / -15R / -16R / -17R

4.2.3 Product Info Area

Product Information	Value
Version	1
Language Code	0x00 - English
Product manufacturer	TEWS TECHNOLOGIES GmbH
Product name	TAMC631
Board part/model number	TAMC631-xxR
Product version	V1.0 Rev. A (see board label)
Product serial number	determined at manufacturing (see board label)
Asset tag	= Product serial Number

Table 4-5 : Board and Product Info Area

-xx = -10R / -11R / -12R / -13R / -14R / -15R / -16R / -17R

4.2.4 Multi Record Area

4.2.4.1 Module Current Requirements

The “Current Draw” value holds the Payload Power (PWR) requirement of the AMC given as current requirement in units of 0.1A at 12V. The table below shows the factory default “Current Draw” value.

Product Information	Value
Current Draw	0x2D (4.5 A)

Table 4-6 : Module Current Requirements

The MMC adds the FMC Current Requirement (if present) to the AMC’s “Current Draw” and announces the result as current demand to the shelf manager. If the power budget for the AMC slot is smaller than this value, the shelf manager may not enable Payload power for the used slot.

If required, the “Current Draw” value in the Module Current Requirements record may be modified to a value that falls within the given power budget. **Make sure that the modified value still satisfies the AMC module power requirements for the actual FPGA content!**

Use the following formula to calculate the actual current requirement:

$$I_{DRAW} = \frac{P_{BOARD} + (P_{FPGA} + P_{IO}) \cdot 1.2}{12V}$$

Use the Xilinx XPower Analyzer (XPA) to estimate the power requirement for the actual FPGA design. Use the “Total” value of the “Supply Power (W)” results in the Summary View of the XPA as P_{FPGA}. The XPA does not account static I/O power (P_{IO}), this must be considered separately. P_{BOARD} is the static power consumption of the AMC module (refer to the Technical Specification table). The “1.2“ is a factor that accommodates losses in the on board power supplies.

For the TAMC631 P_{BOARD} is 4W.

With the calculated current requirement the “Current Draw” value would be:

$$CurrentDraw = \frac{I_{DRAW}}{10}$$

In the case that no valid FRU information is found in the FMC EEPROM, the AMC's Module Current Requirement record must also cover the current draw of the FMC. In this case also refer to the chapter "VADJ".

4.2.4.2 AMC Point-to-Point Connectivity

The TAMC631's Spartan-6 FPGA allows implementing a wide range of interfaces (Serial RapidIO, PCI-Express, Gig.-Eth., SAS, SATA, XAUI, etc.). The MMC stores a Connectivity Record for each interface that is implemented by the TAMC631. By default, the MMC of the TAMC631 stores the following Connectivity Records:

- Single x1 2.5 Gbps PCI-Express Link on AMC Port 4
- 2x GbE Links on AMC Ports 0-1 (not on TAMC631 with Spartan-6 LX25T)

Channel	Port	Link Type	Link Type Extension	Link Grouping ID	Asymmetric Match
0	4	AMC.1 PCI Express	Gen 1 PCI Express, non-SSC	Single Channel Link	matches with 10
		AMC.1 PCI Express	Gen 1 PCI Express, SSC	Single Channel Link	matches with 10
1	0	AMC.2 Ethernet	1000BASE-BX Ethernet Link	Single Channel Link	exact match
2	1	AMC.2 Ethernet	1000BASE-BX Ethernet Link	Single Channel Link	exact match

Table 4-7 : AMC Point-to-Point Connectivity

4.2.4.3 Clock Configuration

AMC FCLKA should be used as the PCI Express Reference Clock.

Clock ID	Clock Features	Clock Family	Clock Accuracy	Clock Frequency
FCLKA	Clock Receiver, connected through PLL	PCI Express	PCI Express Gen 1	100 MHz nom

Table 4-8 : Clock Configuration

4.2.5 Modifying FRU Records

Some of the records are writeable to allow adapting the TAMC631 to user FPGA designs. If records are modified, the user is responsible to set the proper checksums.

5 Functional Description

5.1 FPGA Block Diagram

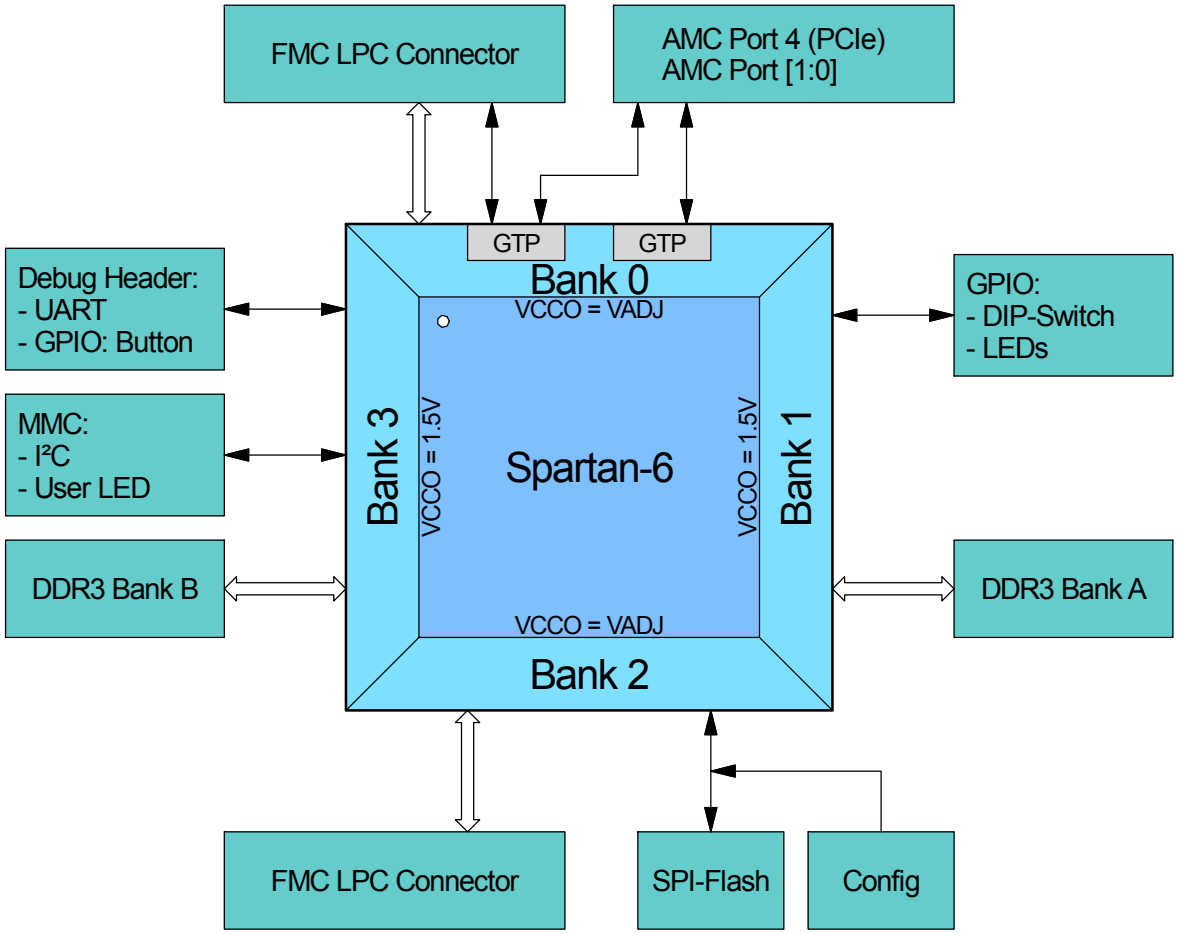

Figure 5-1 : FPGA Block Diagram

5.2 FPGA

The FPGA is a Spartan-6 LX25T-2, LX75T-2, LX100T-2 or LX150T-2 FPGA. Each Spartan-6 FPGA in a FGG484 package provides two Memory Controller Blocks and an Endpoint Block for PCI Express.

Spartan-6	Slices	Flip-Flops	DSP48A1 Slices	Block RAM (Kb)	CMTs	GTP Transceivers
LX25T	3.758	30.064	38	936	2	2
LX75T	11.662	93.296	132	3.096	6	4
LX100T	15.822	126.576	180	4.824	6	4
LX150T	23.038	184.304	180	4.824	6	4

Table 5-1 : TAMC631 FPGA Feature Overview

The board supports JTAG or master serial mode configuration, the latter from a Platform Flash or an SPI-Flash. The FPGA is equipped with 4 I/O banks and 2 (LX25T) or 4 (75LXT, LX100T, LX150T) GTP transceivers.

Bank	V_{CCO}	V_{REF}	Signals	Remarks
Bank 0	VADJ	VREF_A_M2C	LA[00…16]	
Bank 1	1.5V	0.75V	DDR3 Bank A	+GPIO
Bank 2	VADJ	VREF_A_M2C	LA[17…33]	+Configuration
Bank 3	1.5V	0.75V	DDR3 Bank B	+GPIO
GTP Bank	**Description**			**Remarks**
Bank 101	AMC Backplane (PCIe Endpoint Block) FMC DP0			
Bank 123	AMC Backplane			not with LX25T

Table 5-2 : FPGA Bank Usage

All FMC I/O lines are directly connected to the FPGA-pins. Refer to the Xilinx UG381: *Spartan-6 FPGA SelectIO Resources User Guide* for SelectIO interface signal standards, slew rate control and current drive strength capabilities.

The FPGA's VCCAUX is connected to the 3.3V supply.

5.3 Gigabit Transceiver (GTPs)

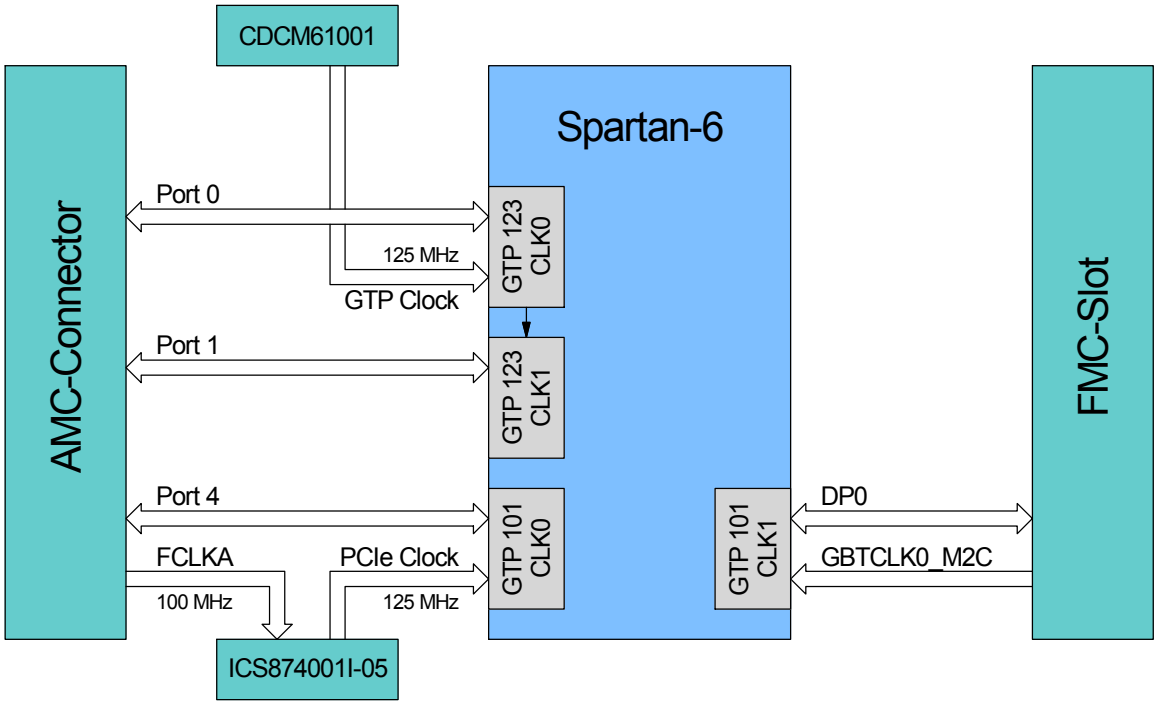

Figure 5-2 : GTP Block Diagram

The TAMC631 provides up to 4 GTPs (also referred to as Multi Gigabit Transceiver (MGT)):

- One GTP is wired to the AMC port 4. This is the GTP preferred by the Spartan-6 PCI Express Endpoint Block.
- One GTP is wired to the FMC LPC connector (DP0)

The XC6SLX75T, XC6SLX100T and XC6SLX150T options provide two additional GTPs:

- Two GTPs are wired to AMC port 0 & 1

GTP	Signal	FPGA Pins	Connected to
MGT0_101	MGTTX	B6 / A6	AMC port 4, (normally used for PCIe)
	MGTRX	D7 / C7	
MGT1_101	MGTTX	B8 / A8	FMC DP0
	MGTRX	D9 / C9	
MGT0_123	MGTTX	B14 / A14	AMC port 0
	MGTRX	D13 / C13	
MGT1_123	MGTTX	B16 / A16	AMC port 1
	MGTRX	D15 / C15	

Table 5-3 : Gigabit Transceiver Connections

The GTP clock MGT0_101 is derived from the 100 MHz AMC fabric clock with a Jitter Attenuator designed for the use in PCI Express systems.

The GTP clock MGT1_101 is directly connected to the FMC's GBTCLK0_M2C signal.

The GTP clock MGT0_123 is generated by a low-jitter clock generator. GTP clock MGT1_123 can share the GTP clock MGT0_123.

GTP	Signal	FPGA Pins	Connected to
MGT0_101	MGTREFCLK	A10 / B10	125 MHz (derived from FLCKA)
MGT1_101	MGTREFCLK	C11 / D11	GBTCLK0_M2C
MGT0_123	MGTREFCLK	A12 / B12	125 MHz
MGT1_123	MGTREFCLK	E12 / F12	n.c.

Table 5-4 : Multi Gigabit Transceiver Reference Clocks

5.4 Configuration

The FPGA can be configured by the following sources:

- Platform Flash
- SPI-Flash
- JTAG

The configuration flash can be selected with a DIP-switch; alternatively, JTAG configuration is always available. Both flashes use the Master Serial / SPI configuration mode and are programmed via JTAG; the SPI-Flash uses the indirect SPI programming mode. To change the TAMC631 programming, JTAG-capable hardware is needed (i.e. the Xilinx Platform Cable USB II).

On delivery the configuration devices are blank.

The configuration pins are located in I/O-bank 2 that is supplied with VADJ. While the configuration signals are routed through level shifters, Xilinx doesn't guarantee a successful configuration with a VCCO_2 lower than 2.5V (refer i.e. to Xilinx AR# 34510).

A green on board "DONE"-LED is lit when the FPGA is configured. If the FPGA is not configured, the red front panel out-of-service status LED remains lit.

5.4.1 Configuration DIP-Switch

The Configuration DIP-Switch allows to select the configuration flash (Platform Flash or SPI) and to configure the JTAG-chain. The Configuration DIP-Switch is located on the back side of the TAMC631.

Switch	Signal	Description
S1	ON	Include FPGA and Platform Flash in JTAG-chain
	OFF	Bypass FPGA and Platform Flash
S2	ON	Include Clock Generator in JTAG-chain
	OFF	Bypass Clock Generator
S3	ON	Include FMC-slot in JTAG-chain if a FMC is installed
	OFF	Bypass FMC-slot
S4	ON	Configure FPGA from SPI-Flash
	OFF	Configure FPGA from Platform Flash

Table 5-5 : Configuration DIP-Switch Settings

5.4.2 JTAG

For direct FPGA configuration, FPGA readback or in-system diagnostics with ChipScope, the JTAG Header can be used to access the JTAG-chain. The JTAG-chain can be extended to include the FMC-Slot, so JTAG capable FMCs can be used.

The JTAG-chain is accessible from the JTAG Header, the Debug Connector or from the AMC backplane JTAG port (option). These are connected in parallel, so only one connection should be made to avoid signal contentions.

To ease the use of the JTAG-chain, it can be partitioned into segments. Each segment can be separately held inactive and thereby excluded ("bypassed") from the chain. In this way it is possible to target a specific

JTAG device which makes the use of the .svf generating software more convenient. It also allows masking the on board JTAG devices when a JTAG-device on a mounted FMC is targeted.

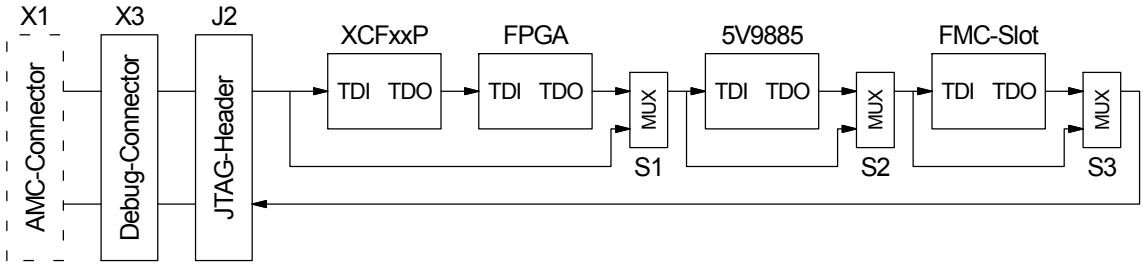

Figure 5-3 : JTAG-Chain Segmentation

The first segment contains the FPGA and the configuration device. The second segment contains the clock generator. The third segment contains the FMC-Slot. The latter segment is only activated when a FMC is installed (PRSNT_M2C# is asserted). Selection of these segments is controlled by a DIP-Switch.

Switch	Signal	Description
S1	ON	Include FPGA and Platform Flash in JTAG-chain
	OFF	Bypass FPGA and Platform Flash
S2	ON	Include Clock Generator in JTAG-chain
	OFF	Bypass Clock Generator
S3	ON	Include FMC-slot in JTAG-chain if FMC is installed
	OFF	Bypass FMC-slot

Table 5-6 : Configuration DIP-Switch S1-S3 Settings

Devices in inactive segments are held in the Test-Logic-Reset State. The FPGA/configuration device segment and the clock generator segment are active by default.

5.4.3 Selecting the Configuration Source

Besides direct JTAG configuration the TAMC631 provides two configuration sources: a platform flash and a SPI-Flash. Both devices share common pins, so a selection must be made. It is made with the SPI Enable Switch (S4). If it is set OFF, the platform flash is selected as configuration source, if it is set ON, the SPI-Flash is selected for configuration.

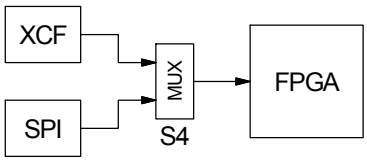

Figure 5-4 : Configuration Source Selection

This selection can be overridden by the MMC to enable code updates and revision selection via IPMI.

After the FPGA configuration is done, the SPI-Flash is always user accessible, regardless of the SPI Enable Switch setting to enable the user to use it in a design, i.e. for data or code storage.

Switch	Signal	Description
S4	ON	Configure FPGA from SPI-Flash
	OFF	Configure FPGA from Platform Flash

Table 5-7 : Configuration DIP-Switch S4 Settings

For module variants with LX150T FPGA the "Enable BitStream Compression" Generate Programming File-option must be used when the platform flash shall be the configuration source. This is necessary since the platform flash is too small to hold the uncompressed FPGA configuration bitstream. Refer to Xilinx UG380: *Spartan-6 FPGA Configuration User Guide*. Depending on the actual design, the compression may not suffice. In this case the SPI-Flash must be used as configuration source.

5.5 Clocking

5.5.1 Clock Sources

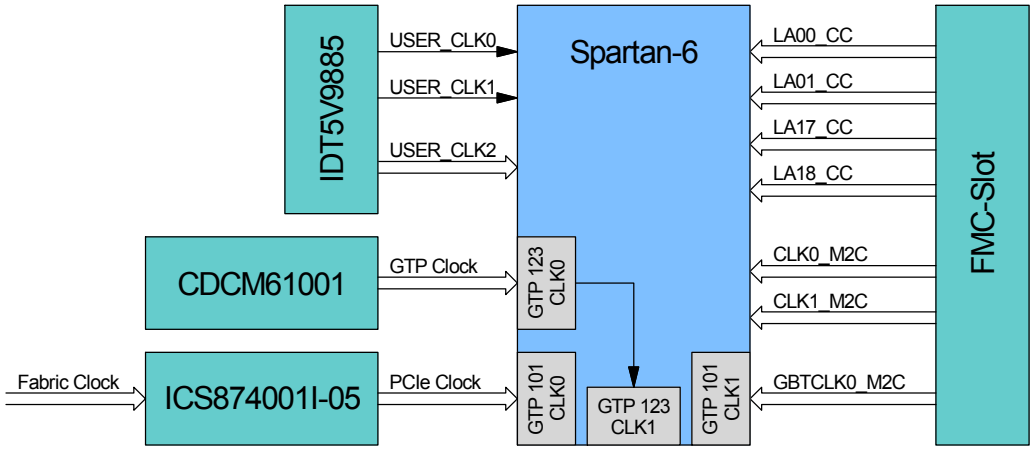

Figure 5-5 : FPGA Clock Sources

The TAMC631 uses 4 main clock sources:

- 3 user programmable clocks (2 single-ended, 1 differential), provided by an IDT5V9885 programmable clock generator. These clocks are connected to global clock pins of the Spartan-6 FPGA. The IDT5V9885 is JTAG programmable, allowing to change the default clock values.
- Clocks provided by the FMC slot. These clocks are connected to global clock pins of the Spartan-6 FPGA, except GBTCLK0_M2C, which is connected to a GTP reference clock input.
- 100 MHz AMC fabric clock, converted to 125 MHz (default) by an ICS874001I-05 PCI Express jitter-attenuator. This clock is connected to a GTP reference clock input.
- 125 MHz (default), provided by a CDCM61001 low-jitter clock generator. This clock is connected to a GTP reference clock input.

The following table lists the available clock sources on the TAMC631:

FPGA Clock-Pin Name	FPGA Pin Number	Source	Description
MGTREFCLK0_101	A10 / B10	FCLKA (100 MHz AMC fabric clock) through PCI Express Jitter Attenuator	125 MHz (default)
MGTREFCLK1_101	C11 / D11	GBTCLK0_M2C	depends on FMC
MGTREFCLK0_123	A12 / B12	Low-Jitter Clock Generator	125 MHz (default)
MGTREFCLK1_123	E12 / F12	n.c.	-
IO_L30N_GCLK0	AB13	IDT5V9885 clock generator: USER_CLK0	User programmable single-ended clock. Can be used as configuration clock. Refer to the next chapter for default value
IO_L30P_GCLK1	Y13	IDT5V9885 clock generator: USER_CLK1	User programmable single-ended clock. Refer to the next chapter for default value
IO_L29N_GCLK2	U12	FMC low pin count connector: LA17_ CC	Depends on FMC
IO_L29P_GCLK3	T12		
IO_L37N_GCLK12	F16	FMC low pin count connector: CLK0_M2C	Depends on FMC
IO_L37P_GCLK13	E16		
IO_L36N_GCLK14	F15	IDT5V9885 clock generator: USER_CLK2	User programmable differential clock. Refer to the next chapter for default value
IO_L36P_GCLK15	F14		
IO_L35N_GCLK16	G11	FMC low pin count connector: LA01_ CC	depends on FMC
IO_L35P_GCLK17	H12		
IO_L34N_GCLK18	F10	FMC low pin count connector: LA00_CC	depends on FMC
IO_L34P_GCLK19	G9		
IO_L31P_GCLK31	AA12	FMC low pin count connector: LA18_ CC	depends on FMC
IO_L31N_GCLK30	AB12		
IO_L32P_GCLK29	Y11	FMC low pin count connector: CLK1_M2C	depends on FMC
IO_L32N_GCLK28	AB11		

Table 5-8 : Available FPGA clocks

AMC FCLKA (CLK3) is connected to the FPGA via a PCIe jitter-attenuator that scales the Clock from 100 MHz up to 125 MHz and reduces the Clock Jitter. The PCI-Express Interface works with Spread-Spectrum Clock (SSC) and non SSC PCI-Express Reference Clocks.

5.5.2 Programmable Clock Generator

The TAMC631 provides a user programmable IDT5V9885 clock generator. The clock generator allows changing the user-clocks to specific application needs.

IDT supplies the “IDT Programmable Clock” programming software, which can be used to change the clock settings. The input of the clock generator is a 40 MHz on board oscillator. The default clock settings are:

IDT Pin	Frequency	FPGA Pin	Description
REFIN	40 MHz	-	Clock generator reference clock
OUT1	-	-	Unused, not connected to the FPGA
OUT 2	20 MHz	AB13	USER_CLK0, can be used as CCLK.
OUT 3	62.5 MHz	Y13	USER_CLK1
OUT 4	166.67 MHz	F14 / F15	USER_CLK2, differential
OUT 5	-	-	Unused, not connected to the FPGA
OUT 6	-	-	Unused, not connected to the FPGA

Table 5-9 : Programmable Clock

When changing the clock settings, the following rule must be observed:

The clock generator device offers 4 configuration sets. These must be identical; otherwise the device will load invalid configuration data on power up.

When USER_CLK0 is used as configuration Clock (CCLK), it should be no more than 20 MHz, as this is the maximum frequency for read operations on the SPI-Flash.

For an instruction on how to reprogram the clock generator, refer to chapter “6.1 Clock Generator Configuration”.

5.6 Memory

The TAMC631 is equipped with two banks of 128 Mbytes, 16 bit wide DDR3 SDRAM and one 64-Mbit non-volatile SPI-Flash[2]. The SPI-Flash can also be used as configuration memory.

5.6.1 DDR3 SDRAM

The TAMC631 provides two MT41J64M16 (96-ball) DDR3 memory components. They are accessible through the Memory Controller Block hard-IPs in bank 1 and bank 3 of the Spartan-6 FPGA, using SSTL15 signaling.

The memory component’s CS# is fixed to GND. The address bits A14 and A13 are memory address expansion bits.

[2] Revision A modules: 32 MBit

Signal	DDR Bank A FPGA Pin	DDR Bank B FPGA Pin	I/O Standard	Termination	Memory Device	
					Pin	Name
A0	H21	K2	SSTL15_II	49.9Ω V_{TT}	N3	A0
A1	H22	K1	SSTL15_II	49.9Ω V_{TT}	P7	A1
A2	G22	K5	SSTL15_II	49.9Ω V_{TT}	P3	A2
A3	J20	M6	SSTL15_II	49.9Ω V_{TT}	N2	A3
A4	H20	H3	SSTL15_II	49.9Ω V_{TT}	P8	A4
A5	M20	M3	SSTL15_II	49.9Ω V_{TT}	P2	A5
A6	M19	L4	SSTL15_II	49.9Ω V_{TT}	R8	A6
A7	G20	K6	SSTL15_II	49.9Ω V_{TT}	R2	A7
A8	E20	G3	SSTL15_II	49.9Ω V_{TT}	T8	A8
A9	E22	G1	SSTL15_II	49.9Ω V_{TT}	R3	A9
A10	J19	J4	SSTL15_II	49.9Ω V_{TT}	L7	A10/AP
A11	H19	E1	SSTL15_II	49.9Ω V_{TT}	R7	A11
A12	F22	F1	SSTL15_II	49.9Ω V_{TT}	N7	A12/BCN
A13	G19	J6	SSTL15_II	49.9Ω V_{TT}	T3	NC/A13
A14	F20	H5	SSTL15_II	49.9Ω V_{TT}	T7	NC/A14
BA0	K17	J3	SSTL15_II	49.9Ω V_{TT}	M2	BA0
BA1	L17	J1	SSTL15_II	49.9Ω V_{TT}	N8	BA1
BA2	K18	H1	SSTL15_II	49.9Ω V_{TT}	M3	BA2
RAS#	K21	M5	SSTL15_II	49.9Ω V_{TT}	J3	RAS#
CAS#	K22	M4	SSTL15_II	49.9Ω V_{TT}	K3	CAS#
WE#	K19	H2	SSTL15_II	49.9Ω V_{TT}	L3	WE#
CS#	-	-	-	100Ω GND	L2	CS#
RESET#	H18	E3	LVCMOS15	4.7kΩ GND	T2	RESET#
CKE	F21	F2	SSTL15_II	4.7kΩ GND	K9	CKE
ODT	J22	L6	SSTL15_II	49.9Ω V_{TT}	K1	ODT
DQ0	R20	R3	SSTL15_II	ODT	E3	DQ0
DQ1	R22	R1	SSTL15_II	ODT	F7	DQ1
DQ2	P21	P2	SSTL15_II	ODT	F2	DQ2
DQ3	P22	P1	SSTL15_II	ODT	F8	DQ3
DQ4	L20	L3	SSTL15_II	ODT	H3	DQ4
DQ5	L22	L1	SSTL15_II	ODT	H8	DQ5
DQ6	M21	M2	SSTL15_II	ODT	G2	DQ6
DQ7	M22	M1	SSTL15_II	ODT	H7	DQ7
DQ8	T21	T2	SSTL15_II	ODT	D7	DQ8
DQ9	T22	T1	SSTL15_II	ODT	C3	DQ9
DQ10	U20	U3	SSTL15_II	ODT	C8	DQ10
DQ11	U22	U1	SSTL15_II	ODT	C2	DQ11
DQ12	W20	W3	SSTL15_II	ODT	A7	DQ12

Signal	DDR Bank A FPGA Pin	DDR Bank B FPGA Pin	I/O Standard	Termination	Memory Device	
					Pin	Name
DQ13	W22	W1	SSTL15_II	ODT	A2	DQ13
DQ14	Y21	Y2	SSTL15_II	ODT	B8	DQ14
DQ15	Y22	Y1	SSTL15_II	ODT	A3	DQ15
LDQS	N20	N3	DIFF_SSTL15_II	ODT	F3	LDQS
LDQS#	N22	N1	DIFF_SSTL15_II	ODT	G3	LDQS#
UDQS	V21	V2	DIFF_SSTL15_II	ODT	C7	UDQS
UDQS#	V22	V1	DIFF_SSTL15_II	ODT	B7	UDQS#
LDM	N19	N4	SSTL15_II	ODT	E7	LDM
UDM	P20	P3	SSTL15_II	ODT	D3	UDM
CK	K20	K4	DIFF_SSTL15_II	100Ω	J7	CK
CK#	L19	K3	DIFF_SSTL15_II		K7	CK#
RZQ	F18	R7	SSTL15_II	100Ω GND	-	-
ZIO	P19	W4	SSTL15_II	open	-	-

Table 5-10: DDR3 SDRAM Interface

For details regarding the DDR3 SDRAM interface, please refer to the DDR3 SDRAM datasheet and the Xilinx UG388: *Spartan-6 FPGA Memory Controller User Guide*.

The following table contains the exact memory component part number for a specific TAMC631 module version. This is important when using the Memory Interface Generator (MIG). If a device is not in the MIG list of supported devices, a custom part must be created in the MIG.

Module Version	DDR3 Device
TAMC631 V1.0 Rev.A	MT41J64M16LA-187E
since TAMC631 V1.0 Rev.B	MT41J64M16JT-15E IT

Table 5-11: DDR3 SDRAM Part History

5.6.2 SPI-Flash

The TAMC631 provides a Numonyx M25P64 64-Mbit serial Flash memory[3], which can be used as FPGA configuration source. After configuration, it is always accessible from the FPGA, so it also can be used for code or user data storage.

The SPI-EEPROM is connected via voltage translators. Choose an I/O standard appropriate to VADJ.

SPI-Signal	Bank	V_{CCO}	Pin	Description
C	2	VADJ	Y20	Serial Clock (CCLK)
D	2	VADJ	AB20	Serial Data input (MOSI)
Q	2	VADJ	AA20	Serial Data output (DIN)
S#	2	VADJ	AA3	Chip Select (CS0_B)

Table 5-12: FPGA SPI-Flash Connections

5.7 FMC Module Slot

Instead of a front I/O connector, the TAMC631 offers an FPGA Mezzanine Card (FMC) module slot. This allows a wide range of connectors to be used with the TAMC631 and customer specific I/O solutions can be easily applied with the TAMC631.

The FMC standard is described in: VITA 57.1, available at www.vita.com/fmc.

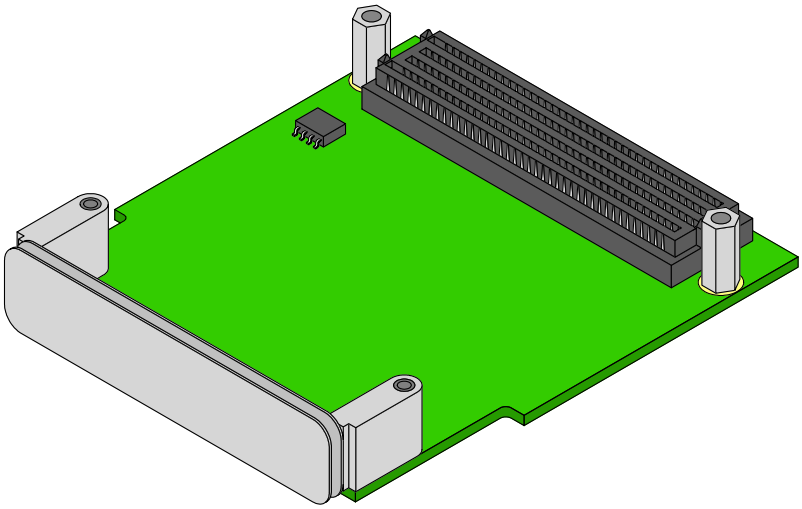

Figure 5-6 : A FMC Module

The FMC module can adapt the TAMC631 to various I/O standards, either mechanical (connector) or electrical.

[3] Revision A modules: 32-Mbit

The TAMC631 implements the Low Pin Count (LPC) option of the VITA 57.1 specification. It offers the full set of connectivity options for the Low Pin Count option:

- 68 single-ended or 34 differential user defined signals
- 1 GTP link
- 1 GTP reference clock
- 2 differential clocks

Signal	Bank	Pin	Signal	Bank	Pin
LA00_P_CC	0	G9	LA00_N_CC	0	F10
LA01_P_CC	0	H12	LA01_N_CC	0	G11
LA02_P	0	B2	LA02_N	0	A2
LA03_P	0	B3	LA03_N	0	A3
LA04_P	0	C4	LA04_N	0	A4
LA05_P	0	E5	LA05_N	0	E6
LA06_P	0	D4	LA06_N	0	D5
LA07_P	0	G8	LA07_N	0	F9
LA08_P	0	F7	LA08_N	0	F8
LA09_P	0	H10	LA09_N	0	H11
LA10_P	0	H14	LA10_N	0	G15
LA11_P	0	C17	LA11_N	0	A17
LA12_P	0	B18	LA12_N	0	A18
LA13_P	0	D17	LA13_N	0	C18
LA14_P	0	C19	LA14_N	0	A19
LA15_P	0	G16	LA15_N	0	F17
LA16_P	0	B20	LA16_N	0	A20
LA17_P_CC	2	T12	LA17_N_CC	2	U12
LA18_P_CC	2	AA12	LA18_N_CC	2	AB12
LA19_P	2	Y5	LA19_N	2	AB5
LA20_P	2	AA4	LA20_N	2	AB4
LA21_P	2	AA14	LA21_N	2	AB14
LA22_P	2	AA8	LA22_N	2	AB8
LA23_P	2	AA6	LA23_N	2	AB6
LA24_P	2	T7	LA24_N	2	U6
LA25_P	2	Y7	LA25_N	2	AB7
LA26_P	2	Y15	LA26_N	2	AB15
LA27_P	2	AA18	LA27_N	2	AB18
LA28_P	2	Y9	LA28_N	2	AB9
LA29_P	2	R13	LA29_N	2	T14
LA30_P	2	AA16	LA30_N	2	AB16
LA31_P	2	W12	LA31_N	2	Y12
LA32_P	2	V17	LA32_N	2	W18

Signal	Bank	Pin	Signal	Bank	Pin
LA33_P	2	Y17	LA33_N	2	AB17
CLK0_M2C_P	0	E16	CLK0_M2C_N	0	F16
CLK1_M2C_P	2	Y11	CLK1_M2C_N	2	AB11
GBTCLK0_M2C_P	101	C11	GBTCLK0_M2C_N	101	D11
DP0_M2C_P	101	D9	DP0_M2C_N	101	C9
DP0_C2M_P	101	B8	DP0_C2M_N	101	A8

Table 5-13: FMC-Interface

Refer to chapter “X2 FMC LPC Connector” for the FMC LPC Connector pinout.

The geographic address pins GA[0:1] are wired to a default of “00”. The FMC’s PRSNT_M2C# and I²C signals are also connected to the FPGA. Refer to “Additional User-I/O”.

The TAMC631 supports the maximum current for each FMC supply, as defined for a Low Pin Count module slot.

Supply Voltage	Range	Max Amps
VADJ	1.2V - 3.3V	2
VREF_A_M2C	0V - 3.3V	1mA
3.3V	3.3V	3
12V	12V	1
3.3VAUX	3.3V	20mA

Table 5-14: FMC-Supplies

5.7.1 VADJ

If a FMC is present, the TAMC631 reads the FRU information from the FMC’s I²C-EEPROM to determine how VADJ has to be set. It uses the value in the “Nominal Voltage” field in the “DC Load” record for VADJ.

If a FMC is present, but no valid FRU information is found (because the EEPROM on the FMC is empty or it has no EPPROM installed), the TAMC631 uses its “Fallback-Voltage for VADJ” setting that is stored in the Internal Use Area of the TAMC631 FRU information. To avoid damage to a plugged in FMC, the “Fallback-Voltage for VADJ” is set to “0x0000” by default, which means that the module will not turn on.

When no valid FRU information is found, the AMC’s Module Current Requirement record must also cover the current draw of the FMC. Eventually the record must be modified, refer to the chapter “Module Current Requirement”.

If no FMC is present, the TAMC631 is turned on, with a VADJ set to 1.8V.

5.8 GPIO

The TAMC631 has some general purpose I/O connected to the FPGA. The recommended signaling standard is LVCMOS15.

Signal	Bank	V_{CCO}	Pin	Description
GPIO_SW0	1	1.5V	J16	4x DIP-switch
GPIO_SW1			J17	
GPIO_SW2			C20	
GPIO_SW3			C22	
GPIO_LED0	1	1.5V	N16	4x green on board LEDs
GPIO_LED1			P16	
GPIO_LED2			M17	
GPIO_LED3			M18	
GPIO_BUT	3	1.5V	C1	1x push-button (not installed on board, accessible via debug-connector)

Table 5-15: FPGA General Purpose I/O

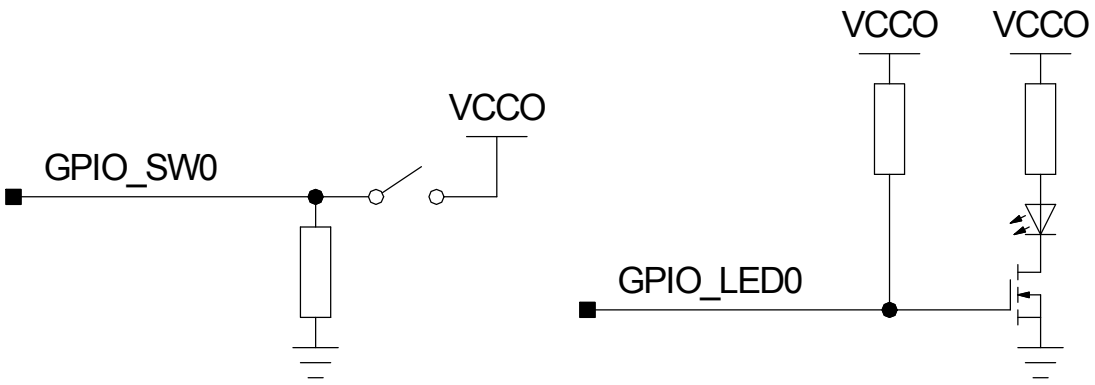

Figure 5-7 : FPGA General Purpose I/O

5.9 Additional User-I/O

The additional user-I/O is composed of debug signals and a couple of signals to the MMC and the FMC. Choose an I/O standard appropriate to the V_{CCO} of a particular I/O pin.

Signal	Bank	V_{CCO}	Pin	Description
UART_RxD	3	1.5V	P5	accessible via debug-connector
UART_TxD			P4	
USER_LED_CTRL	3	1.5V	AA1	Connected to MMC, pulled to MP, use as open-collector. When high, USER_LED is edge sensitive. When low, USER_LED is level sensitive

Signal	Bank	V_{CCO}	Pin	Description
USER_LED	3	1.5V	AA2	Connected to MMC, pulled to MP, use as open-collector. Controls the AMC “USER” front panel LED2. When edge sensitive, a rising or falling edge of USER_LED triggers the MMC to turn off the USER LED in the front panel for app. 100ms. When level sensitive it directly controls the USER LED.
RESET_n	3	1.5V	Y3	Payload reset from MMC. The RESET# signal stays low for approx. 200ms after Payload Power is turned on.
SCL	3	1.5V	F3	I2C to MMC This I2C-interface is for future use.
SDA			E4	
PRSNT_M2C#	2	VADJ	AA10	FMC present
SCL_FMC	3	1.5V	D1	I2C to FMC The I2C to the FMC allows accessing the I2C-EEPROM on the FMC. This I2C-bus is shared with the MMC.
SDA_FMC			D2	

Table 5-16: FPGA Additional User I/O

5.10 On Board Indicators

For a quick visual inspection, the TAMC631 offers three mandatory AMC front panel LEDs.

LED	Color	State	Description
HS	Blue	Off	No Power or module is powered
		Short Blink	Hot-Swap negotiation (extraction)
		Long Blink	Hot-Swap negotiation (insertion)
		On	Module is ready to be powered or module is ready to be unpowered
FAIL	Red	Off	No fault
		On	Failure or out of service status, i.e. FPGA is not configured
USER	Green	Off	Design dependent, can be controlled by the FPGA. Refer to “Additional User-I/O”
		On	
		Blink	

Table 5-17: Front Panel LEDs

The TAMC631 provides a couple of board-status LEDs. These include Power-Good and FPGA-DONE status:

Indicator	Color	Position	Description
Power Good C2M	Green	On board	Power Good Carrier Card Indicates that the VADJ, 12P0V and 3P3V supplies are within tolerance
Power Good AMC	Green	On board	AMC Power Good Power Good for the whole TAMC631
DONE	Green	On board	FPGA DONE-Pin LED Indicates successful FPGA configuration

Table 5-18: Board-Status LEDs

The AMC “USER” front panel LED2 is controllable by the FPGA. In addition the TAMC631 provides 4 GPIO LEDs:

Indicator	Color	FPGA Pin	Position	Description
USER_LED	Green	AA2	Front Panel	User controlled LED, function depends on user application and USER_LED_CTRL
GPIO_LED	Green	N16, P16, M17, M18	On board	FPGA GPIO LEDs

Table 5-19: User LEDs

5.11 Thermal Management

Power dissipation is design dependent. Main factors are device utilization, frequency and GTP-transceiver usage. Use the Xilinx XPower Estimator (XPE) or XPower Analyzer to determine if additional cooling requirements as forced air cooling apply. Forced air cooling is recommended during operation.

The Spartan-6 FPGA has a heatsink mounted (Fischer Elektronik ICK S 18 x 18 x 6,5). The heatsink provides a R_{TH} of 7.1 K/W without air flow, with an additional 1.3 K/W for the mounting hardware.

6 Design Help

6.1 Clock Generator Configuration

6.1.1 File Creation

The IDT5V9885C programmable clock generator can be programmed via the JTAG-Chain. IDT supplies the „*IDT Programmable Clock*“ programming software, which supports the export of the .svf file needed by the JTAG programming algorithms.

To use this .svf file, the FPGA and the configuration device must be bypassed and the TAMC631 must not be connected to a JTAG-capable FMC. The clock generator must be the only active segment of the JTAG-chain.

6.1.2 Using the iMPACT GUI for Clock Programming

The basic procedure to program the IDT5V9885C via the iMPACT GUI is to open iMPACT and initialize the chain (it is assumed that a Xilinx Platform Cable USB is used). iMPACT will then ask for a BSDL-file. Browse to the IDT5V9885C's BSDL-file and select it. The *IDT Programmable Clock*'s output file can now be assigned as new configuration file and can be played with “Execute XSVF/SVF”.

- Plug a Platform Cable USB into the JTAG Header
- Create a new project
- “Initialize Chain”
- Select the BSDL-File for the IDT5V9885C
- Right-click the IDT5V9885C-symbol and select “Assign New Configuration File…”
- Browse to the *IDT Programmable Clock* .svf output file
- Right-click the IDT5V9885C-symbol and select “Execute XSVF/SVF”
- Close iMPACT.

6.2 Example Design

User applications for the TAMC631 can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com.

TEWS offers an FPGA Development Kit (TAMC631-FDK) which consists of a well documented basic example design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TAMC631. It implements a DMA capable PCIe endpoint with interrupt support, register mapping, DDR3 memory access and basic I/O to the FMC slot. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream. This example design can be used as a starting point for own projects.

The basic example design requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (downloadable from www.xilinx.com, a 30 day evaluation license is available) or can be licensed separately. It will not work with the free ISE WebPACK.

6.3 Troubleshooting

6.3.1 The board does not power up

Symptoms:

- The front panel blue hot-swap LED and the red “Fail” LED remain lit.
- The on board “Power Good C2M” and “Power Good AMC” LEDs stay off.

Possible Cause:

1) An FMC without valid EEPROM content is mounted, and the MMC is not able to set VADJ. To avoid potential hardware damage, the board does not power up.
   A solution is to manually set the VADJ as described in chapter “Internal Use Area”.
2) The module current requirements including the FMC exceed the system limits. There are several possibilities to solve this issue:
   a) Remove other AMCs from the system
   b) Use a different power-supply with higher wattage
   c) Modify the “Current Draw” value in the Multi record Area, as described in chapter “Module Current Requirements”

6.3.2 The FPGA does not configure

Symptoms:

- The front panel red “Fail” LED remains lit.
- The on board “DONE” LED stays off.

Possible Cause:

1) If the Configuration Clock Rate for the FPGA bitstream generation is left at the Xilinx default setting of 2 MHz, it may take up to 30 seconds until the FPGA configuration is finished.
   Change the Configuration Rate in the Xilinx ISE Design Suite to archive a faster FPGA configuration.
2) The configuration source is empty or the wrong configuration source is selected.
   Make sure that you programmed your bitstream into the desired configuration source, and select the correct configuration source as described in chapter “Selecting the Configuration Source”. Remember that the TAMC631 is delivered with blank configuration devices.

7 Installation

7.1 AMC Module Insertion & Hot-Swap

7.1.1 Insertion

Typical insertion sequence:

Handle	Blue LED	Description
Open (Full extracted)	OFF	Insert Module into slot
Open (Full extracted)	ON	Module is ready to attempt activation
Closed (Pushed all way in)	Long Blink	Hot-Swap Negotiation
Closed (Pushed all way in)	OFF	Module is ready & powered

Table 7-1 : AMC Module Insertion

When the blue LED does not go off, but returns to the “ON” state, the module FRU information is invalid or the carrier cannot provide the necessary power.

If the blue LED is off, but the red front panel out-of-service status LED remains lit, the FPGA may not be configured.

7.1.2 Extraction

Typical Extraction sequence:

Handle	Blue LED	Description
Pulled out 1/2	OFF	Request Hot-Swap
Pulled out 1/2	Short Blink	Hot-Swap Negotiation
Pulled out 1/2	ON	Module is ready to be extracted
Open (Full extracted)	ON	Extract Module from slot

Table 7-2 : AMC Module Extraction

7.2 Installation of an FMC Module

Before installing an FMC module, be sure that the power supply for the TAMC631 is turned off.

The components are Electrostatic Sensitive Devices (ESD). Use an anti-static mat connected to a wristband when handling or installing the components.

7.3 Using FMCs with Mid-size faceplates

The TAMC631 places the FMC directly at the AMC faceplate. A TAMC631 Mid-size faceplate provides a cut-out to ease the installation of the FMC to the TAMC631. Pins of FMC I/O-connectors that protrude on the Side 2 (the “back side”) of the FMC may still touch the AMC front panel. This is a potential hazardous electrical problem, depending on the I/O circuitry used.

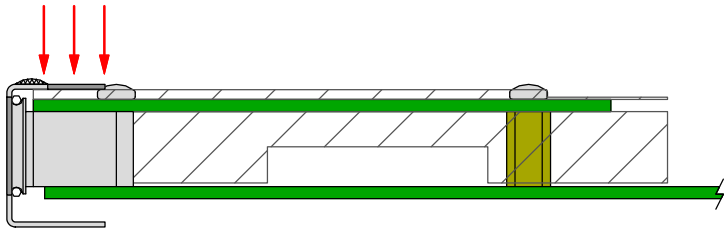

Figure 7-1 : Using FMCs with Mid-size faceplates

It is within the responsibility of the user to carefully check if a specific FMC can be used on a mid-size TAMC631. If you are not sure if the available spacing to conductive parts of the FMC is sufficient, it is strongly recommended to use a TAMC631 with full-size front panel.

7.4 Voltage Limits on FMC Modules

The AMC.0 specification limits the voltages on AMC modules to following thresholds:

	DC voltage	AC voltage
Positive	+27V	+27V peak
Negative	-15V	-15V peak

Table 7-3 : Voltage Limits on FMC Modules

For FMC modules using voltages (including I/O voltages) that exceed these thresholds, an additional insulation to adjacent modules or carrier boards becomes necessary.

8 Pin Assignment – I/O Connector

8.1 Overview

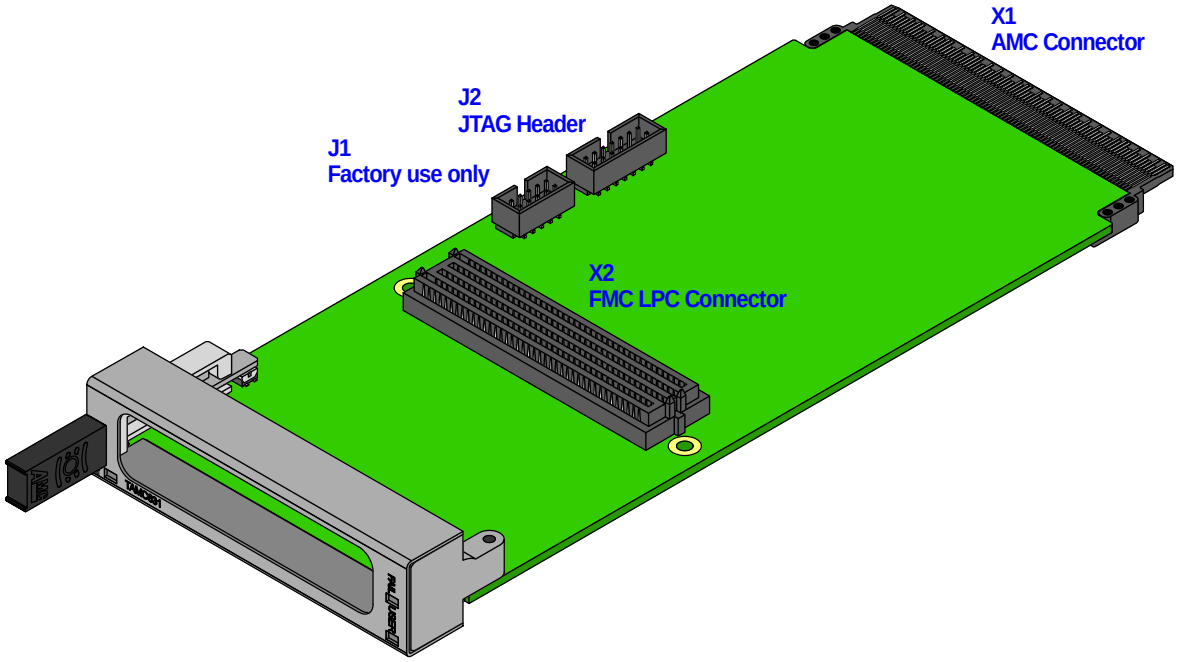

Figure 8-1 : Connector Positions

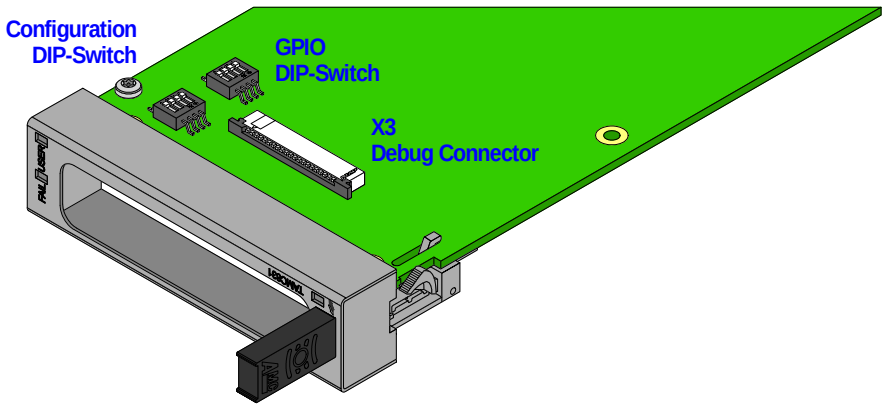

Figure 8-2 : Connector and DIP-switch Positions

8.2 I/O Circuitry

All FMC I/O lines are directly connected to the FPGA-pins. Together with the adjustable V_{CCO} and V_{REF} this maintains the flexibility of the SelectIO technology of the Spartan-6 FPGA. Refer to UG381: *Spartan-6 FPGA SelectIO Resources User Guide* for SelectIO interface signal standards, slew rate control and current drive strength capabilities.

8.2.1 Differential Signaling

As defined in the FMC specification, the TAMC631 expects the AC-coupling for DP signals to be placed on the FMC. The board traces are routed with 50Ω single-ended and 100Ω differential impedance.

8.3 J2 JTAG Header

This header directly connects a JTAG interface cable to the JTAG pins of the FPGA for readback and on-chip debugging of the FPGA design. The pinout of this header matches the pinout of the Xilinx Platform Cable USB II. This allows the direct usage of Xilinx software-tools like Chipscope or iMPACT with the Platform Cable USB II. The connector is a 2mm dual row shrouded header.

Pin	Signal	Description
1	NC	Not Connected
2	V_{REF}	JTAG Reference Voltage (3.3V)
3	GND	Ground
4	TMS	Test Mode Select Input
5	GND	Ground
6	TCK	Test Clock
7	GND	Ground
8	TDO	Test Data Output (TAP Controller: TDI)
9	GND	Ground
10	TDI	Test Data Input (TAP Controller: TDO)
11	GND	Ground
12	TRST#	Not Connected on Platform Cable USB II, used for Test Logic Reset TRST# on the TAMC631
13	NC	JTAG pseudo ground. Optional. Not connected on the TAMC631
14	NC	HALT_INIT_WP signal. Optional. Not connected on the TAMC631

Table 8-1 : Pin Assignment JTAG Header J2

8.4 X1 AMC-Connector

This is an excerpt from the AMC-connector pin assignment. Only the user available signals are listed.

Pin	Signal	Description
11	Tx0+	AMC port 0 (normally used for GbE0) Not for TAMC631 with XC6S25T
12	Tx0-	
14	Rx0+	
15	Rx0-	
20	Tx1+	AMC port 1 (normally used for GbE1) Not for TAMC631 with XC6S25T
21	Tx1-	
23	Rx1+	
24	Rx1-	
44	Tx4+	AMC port 4 (normally used for PCIe)
45	Tx4-	
47	Rx4+	
48	Rx4-	
80	FCLKA+	Fabric Clock (100MHz)
81	FCLKA-	

Table 8-2 : Pin Assignment AMC Connector X1

8.5 X2 FMC LPC Connector

The TAMC631 provides a full Low Pin Count interface. The connector is a Samtec #ASP-134603-01.

Pin	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_M2C	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3.3V AUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3.3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3.3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3.3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3.3V	GND	NC	NC

Table 8-3 : Pin Assignment FMC-Connector X2

8.6 X3 Debug-Connector

Pin	Signal	I/O	Description
1	JTAG SEL	O	A 1.2k pullup to 3.3 Volt is located on the TAMC631
2	3.3V	O	JTAG reference I/O voltage
3	TDO	O	Test Data Output
4	GND	-	Ground
5	TDI	I	Test Data Input
6	TMS	I	Test Mode Select Input
7	GND	-	Ground
8	TCK	I	Test Clock
9	GND	-	Ground
10	UART_RxD	I	FPGA UART Receive Data
11	1.5V	O	UART reference I/O voltage
12	UART_TxD	O	FPGA UART Transmit Data
13	GND	-	Ground
14	MMC_RxD	I	MMC UART Receive Data
15	MP	O	UART reference I/O voltage
16	MMC_TxD	O	MMC UART Transmit Data
17	GND	-	Ground
18	3.3V	O	+3.3 Volt
19	1.5V	O	User signal reference I/O voltage
20	GPIO_BUT	I	User signal connected to the FPGA, A 10k pullup to 1.5 Volt is located on the TAMC631

Table 8-4 : Pin Assignment Debug Connector X3

9 Appendix A

This appendix provides a generic user constraint file for the Spartan-6 FPGA.

```
## ################################################################################################ ##
##                                          TEWS TECHNOLOGIES                                       ##
## ################################################################################################ ##
##
##   Project Name    : TAMC631 Complete Pinning
##   File Name       : tamc631_complete.ucf
##   Target Device   : -
##   Design Tool     : Xilinx ISE Design Suite 12.2, Embedded Edition
##   Simulation Tool : Xilinx ISIM included in Design Tool
##
##   Description     : The files lists all FPGA pins that are connected on the TAMC631
##
##   Owner           : TEWS TECHNOLOGIES GmbH
##                     Am Bahnhof 7
##                     D-25469 Halstenbek
##
##                     Tel.: +49 / (0)4101 / 4058-0
##                     Fax.: +49 / (0)4101 / 4058-19
##                     e-mail: support@tews.com
##
##                     Copyright (c) 2011
##                     TEWS TECHNOLOGIES GmbH
##
##   History         :
##       Version   1 : (SE, 15.07.2010)
##                     Initial Version
##       Version   2 : (RR, 06.08.2010)
##                     Comments, typos & some minor corrections:
##                       * Moved HSWAPEN_N to Prohibited Pins as this is not a usable signal
##                       * Added VREF & GTP prohibits
##                       * Rearranged & resorted GPIO / Debug / MMC signals, removed duplicates
##                       * Added default timing constraints for USER & M2C-Clocks
##                       * Added comments (s.b. & "pin location for reference only")
##                       * Added "Configuration / User Storage" section
##                       * Corrected LAx pinning (after pin-swapping in the layout process)
##       Version   3 : (RR, 22.09.2010)
##                       * Added USER_LED_CTRL
##                       * Corrected RZQ/ZIO pin locations
##                       * Typo correction
##       Version   4 : (SE, 29.10.2010)
##                       * Updated timing constraint for USER_CLK1
##                       * Updated timing constraint for USER_CLK2
##                       * Added MCB_PERFORMANCE constraint
##       Version   5 : (RR, 01.02.2011)
##                       * net "DDRx_RESET_n" iostandard = LVCMOS15; # 1,5V
##       Version   6 : (RR, 19.12.2011)
##                       * Changed the iostandard of the nets SDA_FMC & SCL_FMC from I2C to
##                         LVCMOS15
##
##
##   Comments        : VADJ varies from 0V to 3.3V. Hence the pins with VCCO = VADJ must be set
##                     to an appropriate IO standard that reflects the real VADJ value. These
##                     pins get, as a placeholder, the LVCMOS12 standard, as this will most
##                     likely throw a warning as a reminder.
##                     The constraints for the GTP-transceiver and the MCB are for reference
##                     only. Replace them with the constraints valid for your GTP / MCB
##                     implementation (i.e. the .ucf from the core generator output).
##
## ################################################################################################ ##


## ################################################################################################ ##
## Section: Miscellaneous
## ################################################################################################ ##

## Set basic device information
```

```
# VCCAUX is set to 3.3 by hardware
config vccaux = 3.3;

## Prohibited Pins

# Prohibited Pins that are used for device initialization
config prohibit                   = AA21; # M0
config prohibit                   = Y19;  # M1
config prohibit                   = C3;   # HSWAPEN_N
config prohibit                   = Y4;   # INIT_B

# Prohibited Pins that are used as VREF
config prohibit                   = D3;   # Bank 0
config prohibit                   = A5;   # Bank 0
config prohibit                   = G13;  # Bank 0
config prohibit                   = D19;  # Bank 0

config prohibit                   = F19;  # Bank 1
config prohibit                   = D22;  # Bank 1
config prohibit                   = R19;  # Bank 1

config prohibit                   = V15;  # Bank 2
config prohibit                   = U13;  # Bank 2
config prohibit                   = AB10; # Bank 2
config prohibit                   = Y8;   # Bank 2

config prohibit                   = P8;   # Bank 3
config prohibit                   = M8;   # Bank 3
config prohibit                   = K8;   # Bank 3
config prohibit                   = B1;   # Bank 3

# GTP Transceiver
config prohibit                   = E12;  # BANK 123
config prohibit                   = F12;  # BANK 123


## ##################################################################################################### ##
## Section: Configuration / User Storage
## ##################################################################################################### ##

# These pins are used for configuration. After configuration these pins can be used to access
# the SPI-EEPROM

# I/O Standard
net "CCLK"                        iostandard = LVCMOS12;      # VADJ
net "MOSI"                        iostandard = LVCMOS12;      # VADJ
net "DIN"                         iostandard = LVCMOS12;      # VADJ
net "CSO_B"                       iostandard = LVCMOS12;      # VADJ

# Pin Location constraints
net "CCLK"                        loc = Y20;                  # BANK 2
net "MOSI"                        loc = AB20;                 # BANK 2
net "DIN"                         loc = AA20;                 # BANK 2
net "CSO_B"                       loc = AA3;                  # BANK 2


## ##################################################################################################### ##
## Section: Clocking
## ##################################################################################################### ##

# I/O Standard
net "CCLK_USER_CLK0"              iostandard = LVCMOS15;      # VADJ

net "USER_CLK1"                   iostandard = LVCMOS15;      # VADJ

net "USER_CLK2_P"                 iostandard = LVDS_25;       # VADJ
net "USER_CLK2_N"                 iostandard = LVDS_25;       # VADJ


# Pin Location constraints
net "CCLK_USER_CLK0"              loc = AB13;                 # BANK 2, 20 MHz (default)

net "USER_CLK1"                   loc = Y13;                  # BANK 2, 62.5 MHz (default)
```

```
net "USER_CLK2_P"                 loc = F14;                # BANK 0, 166.67 MHz (default)
net "USER_CLK2_N"                 loc = F15;                # BANK 0


# Differential Termination
net "USER_CLK2_P"                 diff_term = TRUE;
net "USER_CLK2_N"                 diff_term = TRUE;


# Clock constraints
net "CCLK_USER_CLK0" tnm_net = "CCLK_USER_CLK0";
timespec "TS_CCLK_USER_CLK0" = period "CCLK_USER_CLK0"  50 ns high 50 %;

net "USER_CLK1" tnm_net = "USER_CLK1";
timespec "TS_USER_CLK1" = period "USER_CLK1"  16 ns high 50 %;

net "USER_CLK2_P" tnm_net = "USER_CLK2";
timespec "TS_USER_CLK2" = period "USER_CLK2"   6 ns high 50 %;


## ##############################################################################################
## Section: Debug Signals
## ##############################################################################################

# I/O Standard
net "UART_RxD"                    iostandard = LVCMOS15;      # 1,5V
net "UART_TxD"                    iostandard = LVCMOS15;      # 1,5V


# Pin Location constraints
net "UART_RxD"                    loc = P5;                 # BANK 3
net "UART_TxD"                    loc = P4;                 # BANK 3


## ##############################################################################################
## Section: MMC Interface
## ##############################################################################################

# I/O Standard
net "RESET_n"                     iostandard = LVCMOS15;      # 1,5V

net "USER_LED"                    iostandard = LVCMOS15;      # 1,5V
net "USER_LED_CTRL"               iostandard = LVCMOS15;      # 1,5V

net "SCL"                         iostandard = LVCMOS15;      # 1,5V
net "SDA"                         iostandard = LVCMOS15;      # 1,5V


# Pin Location constraints
net "RESET_n"                     loc = Y3;                 # BANK 3

net "USER_LED"                    loc = AA2;                # BANK 3
net "USER_LED_CTRL"               loc = AA1;                # BANK 3

net "SCL"                         loc = F3;                 # BANK 3
net "SDA"                         loc = E4;                 # BANK 3


## ##############################################################################################
## Section: General Purpose I/O
## ##############################################################################################

# I/O Standard
net "GPIO_SW[*]"                  iostandard = LVCMOS15;      # 1,5V
net "GPIO_LED[*]"                 iostandard = LVCMOS15;      # 1,5V
net "GPIO_BUT"                    iostandard = LVCMOS15;      # 1,5V


# Pin Location constraints
net "GPIO_SW0"                    loc = J16;                # BANK 1
net "GPIO_SW1"                    loc = J17;                # BANK 1
net "GPIO_SW2"                    loc = C20;                # BANK 1
```

```
net "GPIO_SW3"                  loc = C22;                # BANK 1

net "GPIO_LED0"                 loc = N16;                # BANK 1
net "GPIO_LED1"                 loc = P16;                # BANK 1
net "GPIO_LED2"                 loc = M17;                # BANK 1
net "GPIO_LED3"                 loc = M18;                # BANK 1

net "GPIO_BUT"                  loc = C1;                 # BANK 3


## ############################################################################################## ##
## Section: FMC Connector
## ############################################################################################## ##

# I/O Standards
# Note: VAdjust varies from 0V to 3.3V. Hence LVCMOS has been chosen as general purpose standard
#       which must be set in an appropriate manner. (1.2V has been arbitrarily chosen)

net "FMC_PRESENT_n"             iostandard = LVCMOS12;    # VADJ

net "SCL_FMC"                   iostandard = LVCMOS15;    # 1,5V
net "SDA_FMC"                   iostandard = LVCMOS15;    # 1,5V

net "LAx_P[*]"                  iostandard = LVCMOS12;    # VADJ
net "LAx_N[*]"                  iostandard = LVCMOS12;    # VADJ

net "CLK0_M2C_P"                iostandard = LVDS_25;     # VADJ
net "CLK0_M2C_N"                iostandard = LVDS_25;     # VADJ
net "CLK1_M2C_P"                iostandard = LVDS_25;     # VADJ
net "CLK1_M2C_N"                iostandard = LVDS_25;     # VADJ


# Differential Termination
net "CLK0_M2C_P"                diff_term = TRUE;
net "CLK0_M2C_N"                diff_term = TRUE;
net "CLK1_M2C_P"                diff_term = TRUE;
net "CLK1_M2C_N"                diff_term = TRUE;


# Clock constraints (replace with your own)
net "CLK0_M2C_P" tnm_net = "CLK0_M2C_P";                  # 100 MHz
timespec "TS_CLK0_M2C_P" = period "CLK0_M2C_P"  10  ns high 50 %;

net "CLK1_M2C_P" tnm_net = "CLK1_M2C_P";                  # 100 MHz
timespec "TS_CLK1_M2C_P" = period "CLK1_M2C_P"  10  ns high 50 %;


# Pin Location Constrains
net "FMC_PRESENT_n"             loc = AA10;               # BANK 2

net "SCL_FMC"                   loc = D1;                 # BANK 3
net "SDA_FMC"                   loc = D2;                 # BANK 3

net "LAx_P[0]"                  loc = G9;                 # BANK 0
net "LAx_P[1]"                  loc = H12;                # BANK 0
net "LAx_P[2]"                  loc = B2;                 # BANK 0
net "LAx_P[3]"                  loc = B3;                 # BANK 0
net "LAx_P[4]"                  loc = C4;                 # BANK 0
net "LAx_P[5]"                  loc = E5;                 # BANK 0
net "LAx_P[6]"                  loc = D4;                 # BANK 0
net "LAx_P[7]"                  loc = G8;                 # BANK 0
net "LAx_P[8]"                  loc = F7;                 # BANK 0
net "LAx_P[9]"                  loc = H10;                # BANK 0
net "LAx_P[10]"                 loc = H14;                # BANK 0
net "LAx_P[11]"                 loc = C17;                # BANK 0
net "LAx_P[12]"                 loc = B18;                # BANK 0
net "LAx_P[13]"                 loc = D17;                # BANK 0
net "LAx_P[14]"                 loc = C19;                # BANK 0
net "LAx_P[15]"                 loc = G16;                # BANK 0
net "LAx_P[16]"                 loc = B20;                # BANK 0
net "LAx_P[17]"                 loc = T12;                # BANK 2
net "LAx_P[18]"                 loc = AA12;               # BANK 2
net "LAx_P[19]"                 loc = Y5;                 # BANK 2
```

```
net "LAx_P[20]"                 loc = AA4;              # BANK 2
net "LAx_P[21]"                 loc = AA14;             # BANK 2
net "LAx_P[22]"                 loc = AA8;              # BANK 2
net "LAx_P[23]"                 loc = AA6;              # BANK 2
net "LAx_P[24]"                 loc = T7;               # BANK 2
net "LAx_P[25]"                 loc = Y7;               # BANK 2
net "LAx_P[26]"                 loc = Y15;              # BANK 2
net "LAx_P[27]"                 loc = AA18;             # BANK 2
net "LAx_P[28]"                 loc = Y9;               # BANK 2
net "LAx_P[29]"                 loc = R13;              # BANK 2
net "LAx_P[30]"                 loc = AA16;             # BANK 2
net "LAx_P[31]"                 loc = W12;              # BANK 2
net "LAx_P[32]"                 loc = V17;              # BANK 2
net "LAx_P[33]"                 loc = Y17;              # BANK 2

net "LAx_N[0]"                  loc = F10;              # BANK 0
net "LAx_N[1]"                  loc = G11;              # BANK 0
net "LAx_N[2]"                  loc = A2;               # BANK 0
net "LAx_N[3]"                  loc = A3;               # BANK 0
net "LAx_N[4]"                  loc = A4;               # BANK 0
net "LAx_N[5]"                  loc = E6;               # BANK 0
net "LAx_N[6]"                  loc = D5;               # BANK 0
net "LAx_N[7]"                  loc = F9;               # BANK 0
net "LAx_N[8]"                  loc = F8;               # BANK 0
net "LAx_N[9]"                  loc = H11;              # BANK 0
net "LAx_N[10]"                 loc = G15;              # BANK 0
net "LAx_N[11]"                 loc = A17;              # BANK 0
net "LAx_N[12]"                 loc = A18;              # BANK 0
net "LAx_N[13]"                 loc = C18;              # BANK 0
net "LAx_N[14]"                 loc = A19;              # BANK 0
net "LAx_N[15]"                 loc = F17;              # BANK 0
net "LAx_N[16]"                 loc = A20;              # BANK 0
net "LAx_N[17]"                 loc = U12;              # BANK 2
net "LAx_N[18]"                 loc = AB12;             # BANK 2
net "LAx_N[19]"                 loc = AB5;              # BANK 2
net "LAx_N[20]"                 loc = AB4;              # BANK 2
net "LAx_N[21]"                 loc = AB14;             # BANK 2
net "LAx_N[22]"                 loc = AB8;              # BANK 2
net "LAx_N[23]"                 loc = AB6;              # BANK 2
net "LAx_N[24]"                 loc = U6;               # BANK 2
net "LAx_N[25]"                 loc = AB7;              # BANK 2
net "LAx_N[26]"                 loc = AB15;             # BANK 2
net "LAx_N[27]"                 loc = AB18;             # BANK 2
net "LAx_N[28]"                 loc = AB9;              # BANK 2
net "LAx_N[29]"                 loc = T14;              # BANK 2
net "LAx_N[30]"                 loc = AB16;             # BANK 2
net "LAx_N[31]"                 loc = Y12;              # BANK 2
net "LAx_N[32]"                 loc = W18;              # BANK 2
net "LAx_N[33]"                 loc = AB17;             # BANK 2

net "CLK0_M2C_P"                loc = E16;              # BANK 0
net "CLK0_M2C_N"                loc = F16;              # BANK 0
net "CLK1_M2C_P"                loc = Y11;              # BANK 2
net "CLK1_M2C_N"                loc = AB11;             # BANK 2


# GTP Connection
# These are pin locations that are for reference only. Replace this with the constraints that are
# valid for your GTP-Transceiver implementation.

# Clock Constraints
net "GBTCLK0_M2C_P"             loc = C11;              # BANK 101
net "GBTCLK0_M2C_N"             loc = D11;              # BANK 101

# Pin Constrains for Lane 1
net "DP0_C2M_P"                 loc = B8;               # BANK 101
net "DP0_C2M_N"                 loc = A8;               # BANK 101
net "DP0_M2C_P"                 loc = D9;               # BANK 101
net "DP0_M2C_N"                 loc = C9;               # BANK 101


## ############################################################################################## ##
## Section: Extended Options Region
```

```
## ############################################################################################################ ##

# These are pin locations that are for reference only. Replace this with the constraints that are
# valid for your PCIe / GTP-Transceiver implementation.

# Clock Constraints
net "PCIe_125M_P"                 loc = A10;                # BANK 101
net "PCIe_125M_N"                 loc = B10;                # BANK 101

# Pin Constrains for Lane 0
net "PCIe_TX0_P"                  loc = B6;                 # BANK 101
net "PCIe_TX0_N"                  loc = A6;                 # BANK 101
net "PCIe_RX0_P"                  loc = D7;                 # BANK 101
net "PCIe_RX0_N"                  loc = C7;                 # BANK 101


## ############################################################################################################ ##
## Section: Common Options Region
## ############################################################################################################ ##

# In larger devices a second GTP tile is available
# These are pin locations that are for reference only. Replace this with the constraints that are
# valid for your GTP-Transceiver implementation.

# Clock Constraints
net "MGT0_125M_P"                 loc = A12;                # BANK 123
net "MGT0_125M_N"                 loc = B12;                # BANK 123

# Pin Constrains for Lane 0
net "MGT_TX0_P"                   loc = B14;                # BANK 123
net "MGT_TX0_N"                   loc = A14;                # BANK 123
net "MGT_RX0_P"                   loc = D13;                # BANK 123
net "MGT_RX0_N"                   loc = C13;                # BANK 123

# Pin Constrains for Lane 1
net "MGT_TX1_P"                   loc = B16;                # BANK 123
net "MGT_TX1_N"                   loc = A16;                # BANK 123
net "MGT_RX1_P"                   loc = D15;                # BANK 123
net "MGT_RX1_N"                   loc = C15;                # BANK 123


## ############################################################################################################ ##
## Section: DDR3 Memory Controller
## ############################################################################################################ ##

# General MCB constraints
config MCB_PERFORMANCE = STANDARD;


# These are pin locations that are for reference only. Replace this with the constraints that are
# valid for your MCB implementation.

# MCB 1, I/O Termination
net "DDRA_DQ[*]"                  in_term = none;
net "DDRA_DQS_P"                  in_term = none;
net "DDRA_DQS_N"                  in_term = none;
net "DDRA_UDQS_P"                 in_term = none;
net "DDRA_UDQS_N"                 in_term = none;

# MCB 1, I/O Standards
net "DDRA_DQ[*]"                  iostandard = SSTL15_II;     # 1,5V
net "DDRA_A[*]"                   iostandard = SSTL15_II;     # 1,5V
net "DDRA_BA[*]"                  iostandard = SSTL15_II;     # 1,5V
net "DDRA_DQS_P"                  iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRA_UDQS_P"                 iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRA_DQS_N"                  iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRA_UDQS_N"                 iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRA_CK_P"                   iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRA_CK_N"                   iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRA_CKe"                    iostandard = SSTL15_II;     # 1,5V
net "DDRA_RAS_n"                  iostandard = SSTL15_II;     # 1,5V
net "DDRA_CAS_n"                  iostandard = SSTL15_II;     # 1,5V
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net "DDRA_WE_n"                 iostandard = SSTL15_II;     # 1,5V
net "DDRA_ODT"                  iostandard = SSTL15_II;     # 1,5V
net "DDRA_RESET_n"              iostandard = LVCMOS15;      # 1,5V
net "DDRA_DM"                   iostandard = SSTL15_II;     # 1,5V
net "DDRA_UDM"                  iostandard = SSTL15_II;     # 1,5V
net "DDRA_RZQ"                  iostandard = SSTL15_II;     # 1,5V
net "DDRA_ZIO"                  iostandard = SSTL15_II;     # 1,5V

# MCB 1, Pin Location Constraints for Clock, Masks, Address, and Controls
net "DDRA_A[0]"                 loc = "H21";                # BANK 1
net "DDRA_A[10]"                loc = "J19";                # BANK 1
net "DDRA_A[11]"                loc = "H19";                # BANK 1
net "DDRA_A[12]"                loc = "F22";                # BANK 1
net "DDRA_A[1]"                 loc = "H22";                # BANK 1
net "DDRA_A[2]"                 loc = "G22";                # BANK 1
net "DDRA_A[3]"                 loc = "J20";                # BANK 1
net "DDRA_A[4]"                 loc = "H20";                # BANK 1
net "DDRA_A[5]"                 loc = "M20";                # BANK 1
net "DDRA_A[6]"                 loc = "M19";                # BANK 1
net "DDRA_A[7]"                 loc = "G20";                # BANK 1
net "DDRA_A[8]"                 loc = "E20";                # BANK 1
net "DDRA_A[9]"                 loc = "E22";                # BANK 1
net "DDRA_BA[0]"                loc = "K17";                # BANK 1
net "DDRA_BA[1]"                loc = "L17";                # BANK 1
net "DDRA_BA[2]"                loc = "K18";                # BANK 1
net "DDRA_CAS_n"                loc = "K22";                # BANK 1
net "DDRA_CK_P"                 loc = "K20";                # BANK 1
net "DDRA_CK_N"                 loc = "L19";                # BANK 1
net "DDRA_CKe"                  loc = "F21";                # BANK 1
net "DDRA_LDM"                  loc = "N19";                # BANK 1
net "DDRA_DQ[0]"                loc = "R20";                # BANK 1
net "DDRA_DQ[10]"               loc = "U20";                # BANK 1
net "DDRA_DQ[11]"               loc = "U22";                # BANK 1
net "DDRA_DQ[12]"               loc = "W20";                # BANK 1
net "DDRA_DQ[13]"               loc = "W22";                # BANK 1
net "DDRA_DQ[14]"               loc = "Y21";                # BANK 1
net "DDRA_DQ[15]"               loc = "Y22";                # BANK 1
net "DDRA_DQ[1]"                loc = "R22";                # BANK 1
net "DDRA_DQ[2]"                loc = "P21";                # BANK 1
net "DDRA_DQ[3]"                loc = "P22";                # BANK 1
net "DDRA_DQ[4]"                loc = "L20";                # BANK 1
net "DDRA_DQ[5]"                loc = "L22";                # BANK 1
net "DDRA_DQ[6]"                loc = "M21";                # BANK 1
net "DDRA_DQ[7]"                loc = "M22";                # BANK 1
net "DDRA_DQ[8]"                loc = "T21";                # BANK 1
net "DDRA_DQ[9]"                loc = "T22";                # BANK 1
net "DDRA_LDQS_P"               loc = "N20";                # BANK 1
net "DDRA_LDQS_N"               loc = "N22";                # BANK 1
net "DDRA_ODT"                  loc = "J22";                # BANK 1
net "DDRA_RAS_n"                loc = "K21";                # BANK 1
net "DDRA_RESET_n"              loc = "H18";                # BANK 1
net "DDRA_UDM"                  loc = "P20";                # BANK 1
net "DDRA_UDQS_P"               loc = "V21";                # BANK 1
net "DDRA_UDQS_N"               loc = "V22";                # BANK 1
net "DDRA_WE_n"                 loc = "K19";                # BANK 1
net "DDRA_RZQ"                  loc = "F18";                # BANK 1
net "DDRA_ZIO"                  loc = "P19";                # BANK 1

# MCB 3, I/O Termination
net "DDRB_DQ[*]"                in_term = none;
net "DDRB_DQS_P"                in_term = none;
net "DDRB_DQS_N"                in_term = none;
net "DDRB_UDQS_P"               in_term = none;
net "DDRB_UDQS_N"               in_term = none;

# MCB 3, I/O Standards
net "DDRB_DQ[*]"                iostandard = SSTL15_II;     # 1,5V
net "DDRB_A[*]"                 iostandard = SSTL15_II;     # 1,5V
net "DDRB_BA[*]"                iostandard = SSTL15_II;     # 1,5V
net "DDRB_DQS_P"                iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRB_UDQS_P"               iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRB_DQS_N"                iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRB_UDQS_N"               iostandard = DIFF_SSTL15_II;# 1,5V
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net "DDRB_CK_P"                 iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRB_CK_N"                 iostandard = DIFF_SSTL15_II;# 1,5V
net "DDRB_CKe"                  iostandard = SSTL15_II;     # 1,5V
net "DDRB_RAS_n"                iostandard = SSTL15_II;     # 1,5V
net "DDRB_CAS_n"                iostandard = SSTL15_II;     # 1,5V
net "DDRB_WE_n"                 iostandard = SSTL15_II;     # 1,5V
net "DDRB_ODT"                  iostandard = SSTL15_II;     # 1,5V
net "DDRB_RESET_n"              iostandard = LVCMOS15;      # 1,5V
net "DDRB_DM"                   iostandard = SSTL15_II;     # 1,5V
net "DDRB_UDM"                  iostandard = SSTL15_II;     # 1,5V
net "DDRB_RZQ"                  iostandard = SSTL15_II;     # 1,5V
net "DDRB_ZIO"                  iostandard = SSTL15_II;     # 1,5V

# MCB 3, Pin Location Constraints for Clock, Masks, Address, and Controls
net "DDRB_A[0]"                 loc = "K2";                 # BANK 3
net "DDRB_A[10]"                loc = "J4";                 # BANK 3
net "DDRB_A[11]"                loc = "E1";                 # BANK 3
net "DDRB_A[12]"                loc = "F1";                 # BANK 3
net "DDRB_A[1]"                 loc = "K1";                 # BANK 3
net "DDRB_A[2]"                 loc = "K5";                 # BANK 3
net "DDRB_A[3]"                 loc = "M6";                 # BANK 3
net "DDRB_A[4]"                 loc = "H3";                 # BANK 3
net "DDRB_A[5]"                 loc = "M3";                 # BANK 3
net "DDRB_A[6]"                 loc = "L4";                 # BANK 3
net "DDRB_A[7]"                 loc = "K6";                 # BANK 3
net "DDRB_A[8]"                 loc = "G3";                 # BANK 3
net "DDRB_A[9]"                 loc = "G1";                 # BANK 3
net "DDRB_BA[0]"                loc = "J3";                 # BANK 3
net "DDRB_BA[1]"                loc = "J1";                 # BANK 3
net "DDRB_BA[2]"                loc = "H1";                 # BANK 3
net "DDRB_CAS_n"                loc = "M4";                 # BANK 3
net "DDRB_CK_P"                 loc = "K4";                 # BANK 3
net "DDRB_CK_N"                 loc = "K3";                 # BANK 3
net "DDRB_CKe"                  loc = "F2";                 # BANK 3
net "DDRB_LDM"                  loc = "N4";                 # BANK 3
net "DDRB_DQ[0]"                loc = "R3";                 # BANK 3
net "DDRB_DQ[10]"               loc = "U3";                 # BANK 3
net "DDRB_DQ[11]"               loc = "U1";                 # BANK 3
net "DDRB_DQ[12]"               loc = "W3";                 # BANK 3
net "DDRB_DQ[13]"               loc = "W1";                 # BANK 3
net "DDRB_DQ[14]"               loc = "Y2";                 # BANK 3
net "DDRB_DQ[15]"               loc = "Y1";                 # BANK 3
net "DDRB_DQ[1]"                loc = "R1";                 # BANK 3
net "DDRB_DQ[2]"                loc = "P2";                 # BANK 3
net "DDRB_DQ[3]"                loc = "P1";                 # BANK 3
net "DDRB_DQ[4]"                loc = "L3";                 # BANK 3
net "DDRB_DQ[5]"                loc = "L1";                 # BANK 3
net "DDRB_DQ[6]"                loc = "M2";                 # BANK 3
net "DDRB_DQ[7]"                loc = "M1";                 # BANK 3
net "DDRB_DQ[8]"                loc = "T2";                 # BANK 3
net "DDRB_DQ[9]"                loc = "T1";                 # BANK 3
net "DDRB_LDQS_P"               loc = "N3";                 # BANK 3
net "DDRB_LDQS_N"               loc = "N1";                 # BANK 3
net "DDRB_ODT"                  loc = "L6";                 # BANK 3
net "DDRB_RAS_n"                loc = "M5";                 # BANK 3
net "DDRB_RESET_n"              loc = "E3";                 # BANK 3
net "DDRB_UDM"                  loc = "P3";                 # BANK 3
net "DDRB_UDQS_P"               loc = "V2";                 # BANK 3
net "DDRB_UDQS_N"               loc = "V1";                 # BANK 3
net "DDRB_WE_n"                 loc = "H2";                 # BANK 3
net "DDRB_RZQ"                  loc = "R7";                 # BANK 3
net "DDRB_ZIO"                  loc = "W4";                 # BANK 3
```