The Embedded I/O Company

TAMC651

Spartan-6 FPGA AMC for MTCA.4 Rear-I/O

Version 1.0

User Manual

Issue 1.0.2

April 2015

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TAMC651-10R

XC6SLX45T-2 FPGA, 128 MB DDR3, Mid-Size front panel

TAMC651-11R

Same as TAMC651-10R but Full-Size front panel

TAMC651-12R

XC6SLX100T-2 FPGA, 128 MB DDR3, Mid-Size front panel

TAMC651-13R

Same as TAMC651-12R but Full-Size front panel

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	September 2011
1.0.1	(1) Added Power Requirements to Technical Specification Table (2) Added MTBF to Technical Specification Table (3) Some additions in Clock Signal Planning chapter (4) Added Note regarding µRTM EEPROM Write Protect implementation (5) Generic FPGA User Constraint File (UCF) updated	December 2011
1.0.2	- Added DDR3 SDRAM Alternative Part - Modified Tables in Board-I/O / Zone 3 Interface / Pin Assignment	April 2015

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1 Product Description

The TAMC651 is a double Mid-Size AMC providing a user programmable FPGA and a Zone 3 interface for µRTM Rear-I/O according to MTCA.4.

The user programmable FPGA is a Xilinx Spartan-6 LX45T/LX100T device. Both a Xilinx Platform-Flash and a serial SPI Flash are available as FPGA configuration memory.

128 MB of 16 bit wide DDR3 memory is provided, utilizing a Spartan-6 integrated Memory-Controller-Block.

AMC port 4 is used for a PCI Express x1 link that utilizes the Spartan-6 integrated PCI Express Endpoint Block.

AMC ports 12-15 (point-to-point) and AMC ports 17-20 (multi-point) are connected to FPGA I/O pins via on-board M-LVDS transceivers.

One of the Spartan-6 GTP transceivers utilizes a SFP interface available at the front plate.

The TAMC651 provides a multi-output programmable clock generator and a 4 In / 4 Out clock crosspoint-switch.

46 differential pair FPGA I/Os and two of the Spartan-6 GTP transceivers are connected to the Zone 3 interface (µRTM).

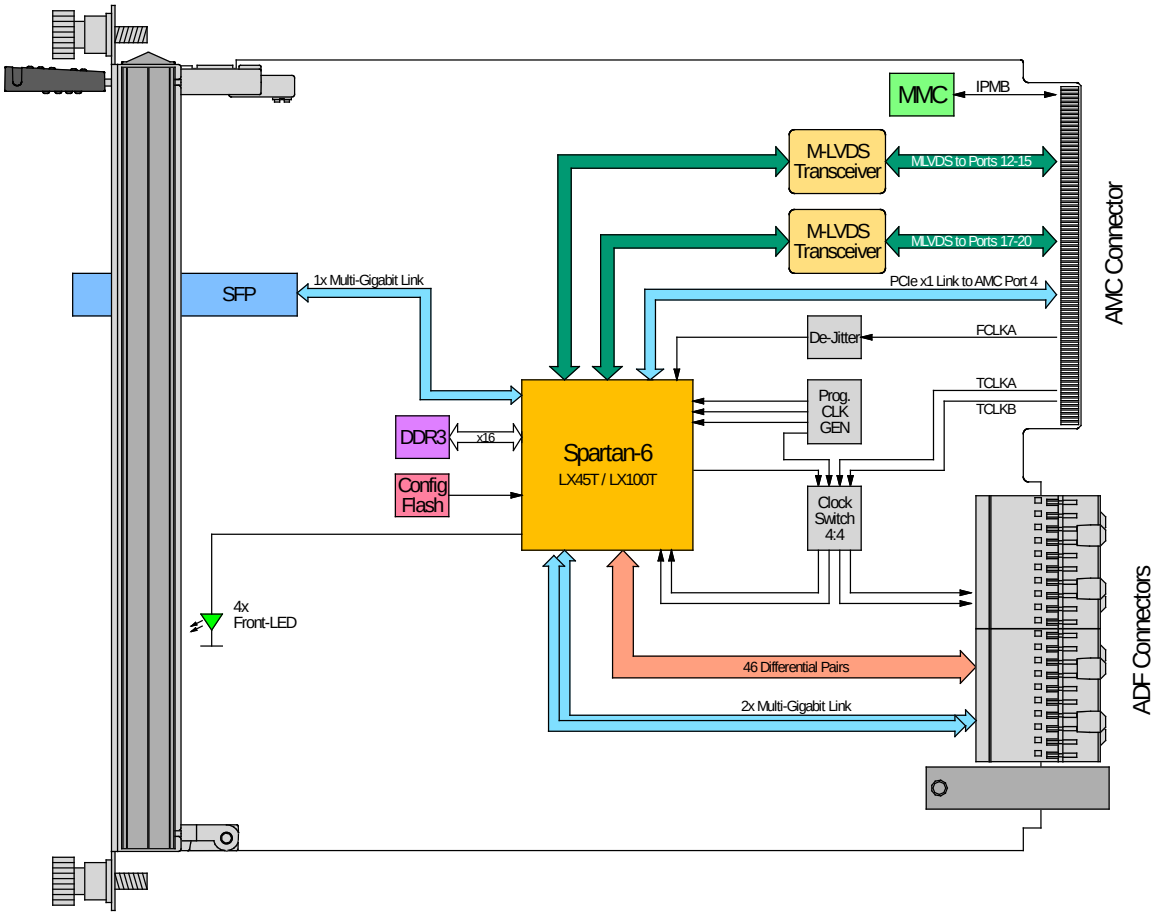


Figure 1-1 : TAMC651 Block Diagram

2 Technical Specification

AMC Interface		
Mechanical Interface	Advanced Mezzanine Card (AMC) Interface conforming to PICMG® AMC.0 R2.0 (Advanced Mezzanine Card Base Specification) and PICMG® MTCA.4 (MicroTCA Enhancements for Rear-I/O and Precision Timing) Module Type: TAMC651-10R/-12R: Double Mid-size Module Module Type: TAMC651-11R/-13R: Double Full-size Module	
Electrical Interface	Port 4	PICMG® AMC.1 R1.0 PCIe single lane (x1) port (AMC.1 Type 1 compliant)
	Ports 12-15	MLVDS Transceiver Point-to-Point (controlled by FPGA I/O)
	Ports 17-20	MLVDS Transceiver Multi-Point (controlled by FPGA I/O)
	TCLKA, TCLKB	Connected to Clock Crosspoint-Switch Inputs
IPMI Support		
IPMI Version	1.5	
AMC.0 Front Panel LEDs	Blue Hot-Swap LED Red Failure Indication LED (LED1) Green User LED (LED2)	
Main On-Board Devices		
MMC	Atmel ATmega1281-16MU	
PCIe Endpoint	Spartan-6 FPGA PCI Express Endpoint Block	
User Programmable FPGA	TAMC651-10R/-11R: Xilinx XC6SLX45T-2FGG484I TAMC651-12R/-13R: Xilinx XC6SLX100T-2FGG484I	
FPGA Configuration Flash	Xilinx XCF32PFSG48C	
SPI Serial Flash	Numonyx M25P64-VME6	
PCIe Jitter Attenuator	IDT ICS874001I-05	
Programmable Clock Generator	Silicon Labs Si5338B-A-GM	
LVDS Crosspoint-Switch	Micrel SY89540UMY	
M-LVDS Transceiver	National DS91M040TSQ	
DDR3 Memory	16-bit wide 128 Mbyte DDR3 Memory, connected to Spartan-6 FPGA Memory Controller Block (MT41J64M16LA-187E-IT, MT41K64M16TW-107-IT:J or compatible)	
I/O Interface		
Front I/O	SFP Port (connected to Spartan-6 FPGA GTP Transceiver Port)	

	4x general purpose LED (controlled by FPGA I/O)	
SFP Port	SFP Connector	Molex 74441-001
	SFP Cage	Molex 74754-0103
Zone 3 Interface I/O	46x LVDS differential pairs (connected to FPGA I/O) 2x LVDS differential Reference Clock (coming from Crosspoint-Switch) 2x Spartan-6 FGPA GTP transceiver ports FPGA I/O Bank Supply 2.5V	
Zone 3 Interface Connectors	2x ERNI Ermet ZD ADF 30-pair 973028	
Zone 3 Interface Key	Tyco 5223986-1 N = 1 (LVDS)	
JTAG Header	Molex 87832-1420	
MMC Header	Molex 87832-1020	
Physical Data		
Power Requirements	Management Power: 52mA peak @ +3.3V DC	
	Payload Power: Depends on FPGA application 0.64A @ +12V DC with TPLD004 example running in idle (TAMC651-10R)	
	max. Current Draw as per Module Current Requirements record: 4.5A	
Temperature Range	Operating	-40°C to +85°C
	Storage	-40°C to +85°C
MTBF	283739 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	212 g	

Table 2-1 : Technical Specification

3 Handling and Operating Instructions

3.1 ESD Protection

The AMC module is sensitive to static electricity. Packing, unpacking and all other module handling has to be done in an ESD/EOS protected Area.

3.2 Thermal Considerations

Forced air cooling is recommended during operation. Without forced air cooling, damage to the device can occur.

3.3 I/O Signaling Voltages

The Zone 3 I/O-Lines are directly connected to FPGA I/O pins.
The I/O voltage of these FPGA I/O pins is 3.95V maximum.

The FPGA I/O pins are NOT 5V tolerant.

4 IPMI Support

The AMC module provides a Module Management Controller (MMC) that performs health monitoring, hot-swap functionality and stores the Field Replaceable Unit (FRU) information. The MMC communicates via an Intelligent Platform Management Interface (IPMI).

4.1 Temperature and Voltage Sensors

The MMC monitors on-board sensors and signals sensor events to the superordinated IPMI controller / shelf manager. Available sensors are listed in the table below.

Sensor Number	Signal Type	Thresholds	Signal Monitored
0	**Event**	**-**	**Hot-swap switch**
1	**Temperature**	**lnr lcr lnc unc ucr unr**	**Board Temp.**
2	**Temperature**	**lnr lcr lnc unc ucr unr**	**Board Temp.**
3	**Voltage**	**lnr lcr lnc unc ucr unr**	**+12V (PWR)**
4	**Voltage**	**lnr lcr lnc unc ucr unr**	**+5V**
5	**reserved**	**reserved**	**reserved**
6	**Voltage**	**lnr lcr lnc unc ucr unr**	**+1.8V**
7	**Event**	**-**	**RTM Hot-Swap**
8	**Temperature**	**lnr lcr lnc unc ucr unr**	**RTM Temp.**

unr: upper non-recoverable, ucr: upper critical, unc: upper non-critical
lnr: lower non-recoverable, lcr: lower critical, lnc: lower non-critical

Table 4-1 : Temperature and Voltage Sensors

The following on-board power supplies are monitored by the MMC via a digital power good signal: +1.2V, 1.5V, 2.5V, 3.3V.

4.1.1 Sensor Locations

The following figure shows the location of the TAMC651 physical sensors.

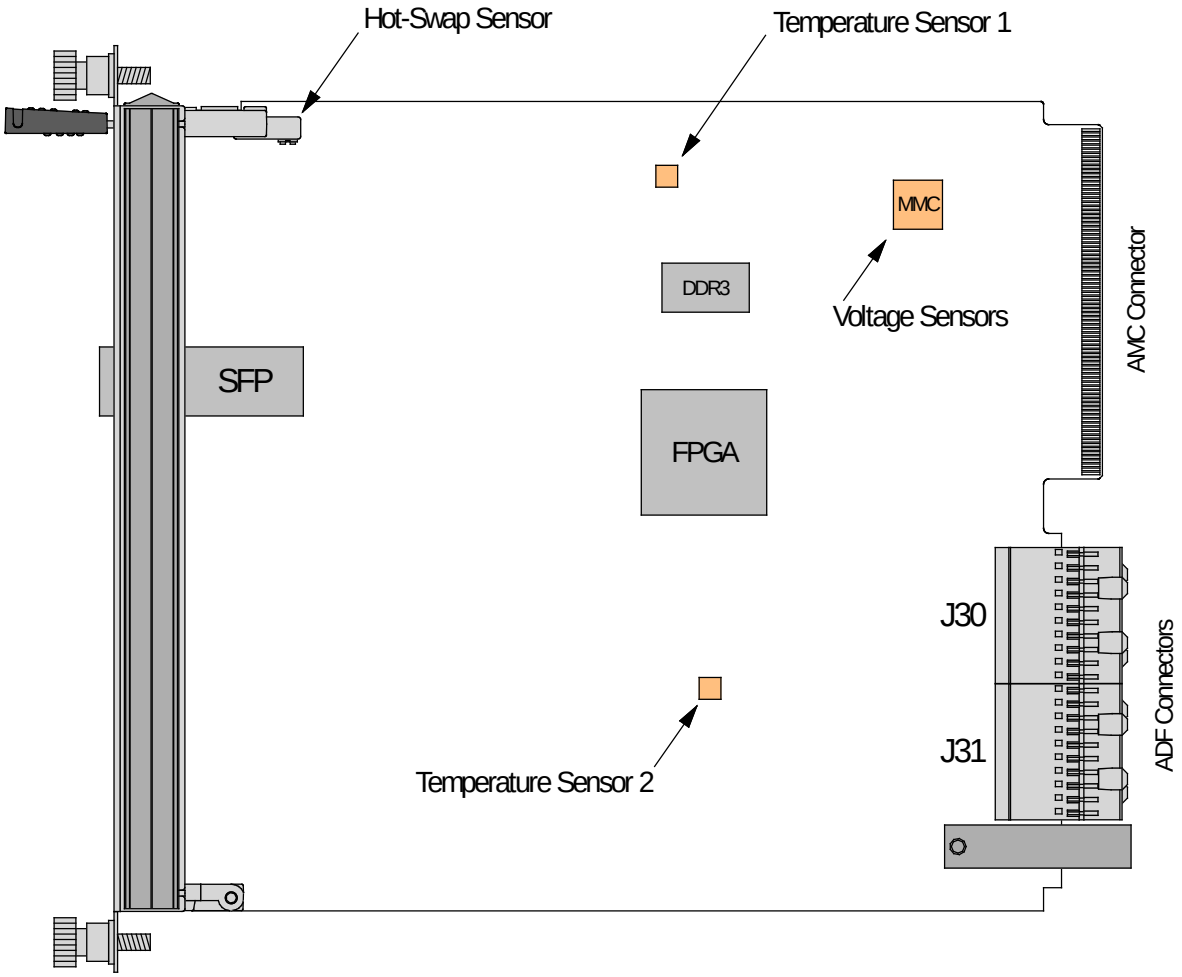


Figure 4-1 : Sensor Locations

4.2 FRU Information

The MMC stores the module FRU information in a non-volatile EEPROM. Some of the records are writeable. If records are modified, the user is responsible for setting the proper checksums. The actual FRU information data is indicated below.

Area	Size (in Bytes)	Writeable
Common Header	**8**	**no**
Chassis Info Area	**0**	**no**
Board Info Area	**variable**	**no**
Product Info Area	**variable**	**no**
Multi Record Area		
Module Current Requirements	**variable**	**yes**
AMC Point-to-Point Connectivity	**variable**	**yes**
Clock Configuration	**variable**	**yes**
Zone 3 Interface Compatibility	**variable**	**yes**

Table 4-2 : FRU Information

4.2.1 Board Info Area

Product Information	Value
Version	**1**
Language Code	**0x00 - English**
Manufacturer date/time	**determined at manufacturing**
Board manufacturer	**TEWS TECHNOLOGIES GmbH**
Board product name	**TAMC651**
Board serial number	**determined at manufacturing (see board label)**
Board part number	**TAMC651-xxR** **-xx = -10 / -11 / -12 / -13**

Table 4-3 : Board Info Area

4.2.2 Product Info Area

Product Information	Value
Version	**1**
Language Code	**0x00 - English**
Product manufacturer	**TEWS TECHNOLOGIES GmbH**
Product name	**TAMC651**
Board part/model number	**TAMC651-xxR** **-xx = -10 / -11 / -12 / -13**
Product version	**V1.0 Rev. C (see board label)**
Product serial number	**determined at manufacturing (see board label)**
Asset tag	**= Product serial Number**

Table 4-4 : Product Info Area

4.2.3 Multi Record Area

4.2.3.1 Module Current Requirements

The “Current Draw” value holds the Payload Power (PWR) requirement of the module (including the optional µRTM) given as current requirement in units of 0.1A at 12V.

The AMC module announces the value of “Current Draw” as current demand to the shelf manager. If the allocated power budget for the actual AMC slot is smaller than this value, the shelf manager may not enable Payload power for this slot. If required, the “Current Draw” value in the Module Current Requirements record may be modified to a value that falls within the given power budget. Make sure that the modified value still satisfies the AMC module power requirements for both the AMC module (with the actual FPGA implementation) and the mounted µRTM.

Product Information	Value
Current Draw	**0x2D (4.5 A)**

Table 4-5 : Module Current Requirements

4.2.3.2 AMC Point-to-Point Connectivity

The AMC module provides the following AMC Point-to-Point Connectivity Record Data.

Channel	Port	Link Type	Link Type Extension	Link Grouping ID	Asymmetric Match
0	**4**	**AMC.1 PCI Express**	**Gen 1 PCI Express, non-SSC**	**Single Channel Link**	**PCI Express Primary Port**
		AMC.1 PCI Express	**Gen 1 PCI Express, SSC**	**Single Channel Link**	**PCI Express Primary Port**

Table 4-6 : AMC Point-to-Point Connectivity

Since the protocol and channel configuration for the MLVDS transceiver interface on AMC ports 12-15 and 17-20 is user application dependent, there are no pre-configured channel or link descriptors stored for AMC ports 12-15 and 17-20.

4.2.3.3 Clock Configuration

AMC FCLKA is used as the PCI Express Reference Clock. TCLKA and TCLKB are connected to inputs of the on-board clock crosspoint-switch.

Clock ID	Clock Features	Clock Family	Clock Accuracy	Clock Frequency
FCLKA	**Clock Receiver, connected through PLL**	**PCI Express**	**PCI Express Gen 1**	**100 MHz nom.**
TCLKA	**Clock Receiver, Not connected through PLL**	**unspecified**		
TCLKB	**Clock Receiver, Not connected through PLL**	**unspecified**		

Table 4-7 : Clock Configuration

4.2.3.4 Zone 3 Interface Compatibility

The Zone 3 Interface Compatibility data of AMC and µRTM must match for the µRTM to be considered as compatible.

Parameter		Setting
Type of Interface Identifier		**OEM**
Interface Identifier	**Manufacturer ID (IANA)**	**TEWS Technologies GmbH Private Enterprise Number 0x0071E3**
	OEM defined Interface Designator	**0x828B0000 (0x8 = TAMC, 0x28B = 651)**

Table 4-8 : Zone 3 Interface Compatibility

4.2.4 Modifying FRU Records

Some of the records are writeable to allow adaption to certain systems. If records are modified, the user is responsible for setting the proper checksums.

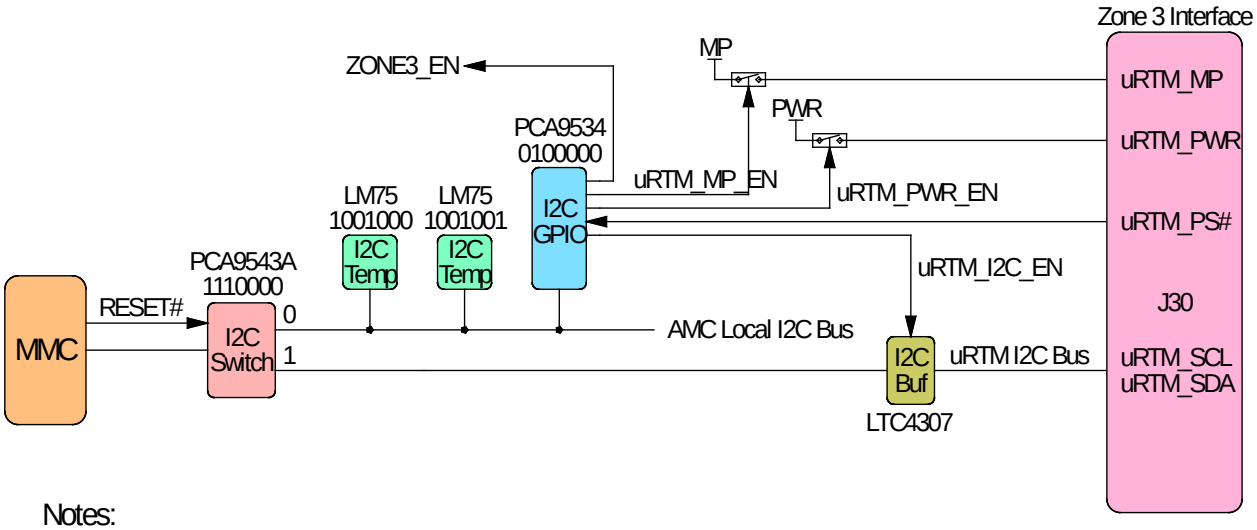
5 Local I2C Management Bus

This chapter describes the TAMC651 local I2C management bus controlled by the TAMC651 MMC.

The chapter is merely intended for the MMC firmware designer (not for the user).

5.1 Overview

The figure below shows the MMC controlled local I2C management bus of the TAMC651.



Notes:
I2C Addresses 1110000 and 1110001 are reserved by the TAMC651.
These I2C Addresses must not be used by the uRTM.

Figure 5-1 : AMC Local I2C Management Bus

The following I2C devices are addressable by the TMAC651 MMC.

I2C Address	I2C Device
70h (1110000b)	**PCA9543A I2C Bus Switch**
48h (1001000b)	**First LM75 I2C Temperature Sensor**
49h (1001001b)	**Second LM75 I2C Temperature Sensor**
20h (0100000b)	**PCA9535 8-bit GPIO Extender**

Table 5-1 : Local I2C Management Bus Device Overview

5.2 I2C Bus Switch

The TAMC651 provides a PCA9543A I2C bus switch to decouple the AMC local I2C management bus from the µRTM I2C management bus.

The TAMC651 MMC local I2C management bus directly connects to the upstream port of the PCA9543A I2C bus switch. The AMC local I2C management bus is located on downstream port 0 and the µRTM I2C management bus is located on downstream port 1 of the PCA9543A I2C bus switch (decoupled by an additional I2C bus buffer as per MTCA.4).

5.3 I2C Temperature Sensors

The TAMC651 provides two LM75 temperature sensors on local I2C management bus 0.

I2C addresses are 48h and 49h.

Please see the LM75 device documentation for details.

5.4 I2C I/O Extender

The TAMC651 provides an 8-bit PCA9534 GPIO extender on local I2C management bus 0.

The following MMC controlled µRTM related management signals/functions are implemented on the AMC module's PCA9534.

I/O Port	I/O Direction	Signal	Description
7	I	RTM_I2C_RDY	µRTM I2C buffer ready status Ready goes high when the buffer is enabled and connection is established.
6	I	RTM_PWR_ERR#	µRTM PWR load switch status Active low. Indicating under voltage.
5	I	RTM_MP_ERR#	µRTM MP load switch failure status Active low. Indicating over current, under voltage or over temperature.
4	O	ZONE3_EN	Zone 3 Interface Enable 0 = Zone 3 Interface Disable 1 = Zone 3 Interface Enable
3	O	RTM_I2C_EN	µRTM I2C Bus Buffer Enable 0 = Disable µRTM I2C Bus 1 = Enable µRTM I2C Bus
2	O	RTM_PWR_EN	µRTM Payload Power Enable 0 = Disable µRTM PWR 1 = Enable µRTM PWR
1	O	RTM_MP_EN	µRTM Management Power Enable 0 = Disable µRTM MP 1 = Enable µRTM MP
0	I	RTM_PS#	µRTM Present Detection 0 = µRTM is present 1 = µRTM is not present

Table 5-2 : AMC I2C I/O Extender Port Assignment

The µRTM present detect signal (RTM_PS#) is directly connected to the RTM_PS# pin on the Zone 3 interface.

After detecting a µRTM, the MMC firmware may enable the µRTM management power by setting RTM_MP_EN.

The µRTM payload power should only be enabled after a successful Zone 3 Interface Compatibility check.

The Zone 3 interface enable signal integrates the µRTM JTAG chain into the TAMC651 JTAG chain. The signal also connects to an FPGA I/O pin. The FPGA application may use this signal to enable/disable drivers for the Zone 3 interface.

Simplified example sequence:

- Wait for µRTM present detection
- Enable µRTM management power
- Check µRTM management power load switch status
- Enable µRTM I2C bus buffer
- Check µRTM I2C bus buffer status
- Read µRTM FRU data
- Check Zone 3 Interface compatibility
- Monitor µRTM Hot-Swap handle (via µRTM I2C bus)
- Control µRTM Front LEDs (via µRTM I2C bus)
- If Zone 3 interface is compatible and µRTM hot-swap handle is closed enable µRTM payload power
- Check µRTM payload power load switch status
- Control µRTM Front LEDs (via µRTM I2C bus)
- Continue monitoring the µRTM hot-swap handle (via µRTM I2C bus) and µRTM present status

6 Functional Description

This chapter gives a brief overview of the various AMC module functions.

6.1 AMC Interface

6.1.1 Overview

AMC-Connector	Backplane	TAMC651
Port 4	PCIe / SRIO	PCIe x1 Link Connected to Spartan-6 FPGA PCIe Endpoint Block
Port 12-15	Point-2-Point links	Connected to FPGA I/O via M-LVDS transceivers
Port 17-20	Multi-Point bus for Triggers, Clocks, Interlocks	Connected to FPGA I/O via M-LVDS transceivers
TCLKA	TCLKA+/-	Connected to on-board Clock Cross-Point-Switch input
TCLKB	TCLKB+/-	Connected to on-board Clock Cross-Point-Switch input
FCLKA	FCLKA+/-	PCIe Reference Clock Connected to FPGA GTP transceiver via an on-board PCI Express Jitter Attenuator
JTAG	TCK, TMS, TDI, TDO	One Option for controlling the TAMC651 JTAG Chain
I2C	SCL_L, SDA_L	Connected to MMC
Management	PS0#, PS1#, GA[0:2], ENABLE#	Used for module management
Power Supply	MP, PWR, GND	Used as power supplies The MMC also controls on-board load switches to gate MP and PWR to the Zone 3 interface.

Table 6-1 : AMC Interface Overview

6.1.1.1 Point-to-Point Links

AMC backplane ports 12-15 are connected to DS91M040 M-LVDS transceivers. There is one bi-directional M-LVDS transceiver line for each port RX pair and one bi-directional M-LVDS transceiver line for each port TX pair.

The digital LVTTL/LVCMOS communication interface of the M-LVDS transceivers is connected to FPGA I/O pins.

The TAMC651 provides a 100R termination resistor for each of the 8 M-LVDS differential RX and TX pairs of AMC ports 12-15.

6.1.1.2 Multi-Point Links

AMC backplane ports 17-20 are connected to DS91M040 M-LVDS transceivers. There is one bi-directional M-LVDS transceiver line for each port RX pair and one bi-directional M-LVDS transceiver line for each port TX pair.

The digital LVTTL/LVCMOS communication interface of the M-LVDS transceivers is connected to FPGA I/O pins.

The receive data signals are mapped to global clock FPGA pins.

The TAMC651 does not provide any termination resistors on the 8 M-LVDS differential RX and TX pairs of AMC ports 17-20.

6.1.2 PCI-Express Interface

AMC port 4 is connected to one of the FPGA GTP transceivers supporting the Spartan-6 integrated PCIe Endpoint-Block.

The user programmable FPGA application implements the PCI Express x1 interface and also defines the addressable resources like registers, etc.

AMC FLCKA is used as the reference clock for the FPGA PCIe GTP transceiver. A Configuration DIP-Switch provides an option for multiplying FCLKA by 5:4 (default) or by 1. With the 100 MHz FCLKA for PCIe, the PCIe GTP transceiver reference clock is 125 MHz by default.

6.1.3 M-LVDS Transceiver Interface

The TAMC651 provides M-LVDS transceivers at AMC ports 12-15 (point-to-point) and AMC ports 17-20 (multi-drop).

Four National Semiconductor DS91M040 Quad M-LVDS transceivers are used on the TAMC651. Two for AMC ports 12-15 (point-to-point) and two for the AMC ports 17-20 (multi-point). Each DS91M040 device provides four M-LVDS transceivers (covering two AMC ports with TX and RX), two receiver type selection inputs and a general chip enable input.

The TAMC651 provides a 100 Ohm termination resistor for the M-LVDS lines on AMC ports 12-15 (point-to-point). The TAMC651 does not provide any termination resistor on the M-LVDS lines on AMC ports 17-20 (multi-point).

The line interface of the M-LVDS transceivers is directly connected to the appropriate pins on the AMC connector (no AC coupling). The digital communication signals of the M-LVDS transceivers are connected to FPGA I/O pins. The receive data signals for AMC ports 17-20 are connected to global clock FPGA pins.

The following figure shows one of the four M-LVDS transceivers, the one used for AMC ports 12 & 13 (termination resistors not shown). The M-LVDS interface for AMC ports 14 & 15, 17 & 18, 19 & 20 is build accordingly.

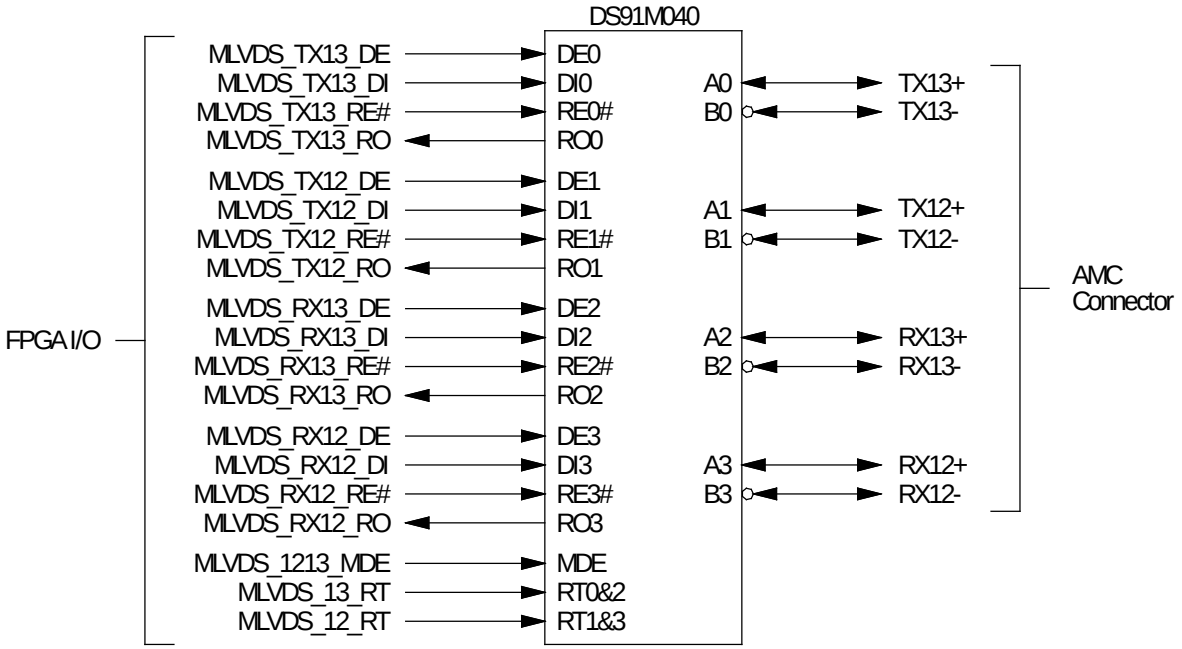


Figure 6-1 : M-LVDS Transceiver for AMC Ports 12 & 13

The following tables show the signal/pin assignments for AMC ports 12 and 13.

AMC Port	DS91M040	FPGA				
	Pin	Bank	Pin	Signal	I/O Std.	Dir
RX12	RE0#	1	M21	MLVDS_RX12_RE#	LVCMOS25	Out
	RO0		P21	MLVDS_RX12_RO		In
	DI0		U22	MLVDS_RX12_DI		Out
	DE0		M22	MLVDS_RX12_DE		Out
TX12	RE1#		N15	MLVDS_TX12_RE#		Out
	RO1		P18	MLVDS_TX12_RO		In
	DI1		W22	MLVDS_TX12_DI		Out
	DE1		N16	MLVDS_TX12_DE		Out
RX13	RE2#		M17	MLVDS_RX13_RE#		Out
	RO2		P19	MLVDS_RX13_RO		In
	DI2		V22	MLVDS_RX13_DI		Out
	DE2		M18	MLVDS_RX13_DE		Out
TX13	RE3#		N20	MLVDS_TX13_RE#		Out
	RO3		P17	MLVDS_TX13_RO		In
	DI3		Y22	MLVDS_TX13_DI		Out
	DE3		M16	MLVDS_TX13_DE		Out

Table 6-2 : M-LVDS Interface Data Transfer Signals (AMC Ports 12 & 13)

DS91M040	FPGA				
Pin	Bank	Pin	Signal	I/O Std.	Dir
MDE	3	J7	MLVDS_12_13_MDE	LVCMOS15	Out
RT1&3		H4	MLVDS_12_RT		Out
RT0&2		G4	MLVDS_13_RT		Out

Table 6-3 : M-LVDS Interface Device Control Signals (AMC Ports 12 & 13)

Signal	Description
MLVDS_xx_yy_MDE	Master Device Enable 0: M-LVDS Transceiver disabled (default) 1: M-LVDS Transceiver enabled
MLVDS_xx_RT	Receiver Type 0: Type 1 Receiver Inputs 1: Type 2 Receiver Inputs See DS91M040 documentation.
MLVDS_xx_RE#	Receiver Enable 0: Receiver enabled 1: Receiver disabled
MLVDS_xx_RO	Receiver Output (Data to FPGA input)
MLVDS_xx_DI	Driver Input (Data from FPGA output)
MLVDS_xx_DE	Driver Enable 0: Driver disabled (default) 1: Driver enabled

Table 6-4 : M-LVDS Interface Signal Description

Please see the “User Programmable FPGA” chapter for all FPGA pin/signal assignments of the M-LVDS interface.

6.2 Clocking Scheme

The figure below shows the main TAMC651 clocking scheme.

More details are available in the appropriate device sub-chapters.

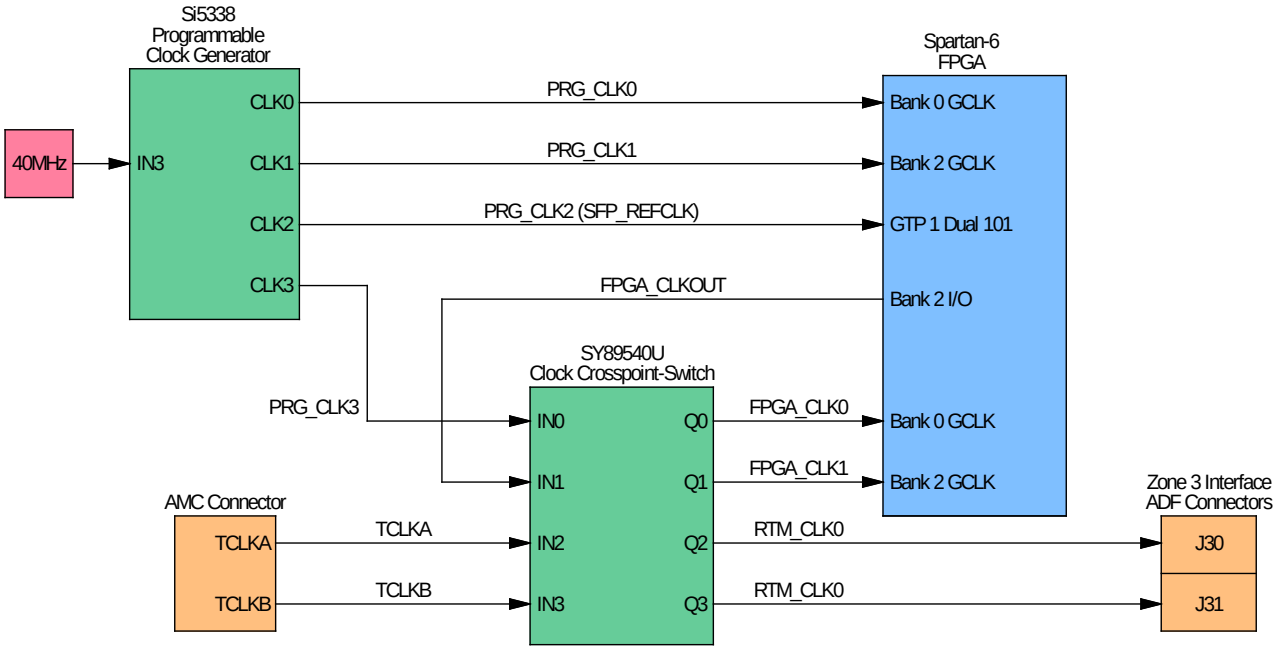


Figure 6-2 : Main Clocking Scheme

6.2.1 On-board Oscillators

The TAMC651 provides two fix on-board oscillators.

A 40 MHz oscillator is used as the clock source for the Si5338 programmable clock generator.

A 62.5 MHz oscillator is connected to the FPGA GCLK0/USER_CCLK pin.

6.2.2 AMC Backplane Clocks

The following table shows the TAMC651 relevant AMC backplane clock signals.

AMC-Connector	Backplane	TAMC651
Port 17-20	**Triggers, Clocks, Interlocks**	**Bidirectional differential signals. Connected to the line interface of on-board M-LVDS Transceivers. The digital interface receives signals of the M-LVDS transceivers are connected to clock capable pins of the Spartan-6 FPGA.**
TCLKA		**TCLKA (connected to on-board clock crosspoint-switch input.**
TCLKB		**TCLKB (connected to on-board clock crosspoint-switch input.**
FCLKA		**PCIe-Clock (connected to the input of an on-board PCI Express Clock Jitter Attenuator. The output is connected to the PCIe GTP reference clock input).**

Table 6-5 : AMC Backplane Clocks

6.2.3 PCI Express Clock Jitter Attenuator

The TAMC651 provides an IDT ICS874001I-05 Jitter Attenuator for the AMC FCLKA clock, which is used as the GTP transceiver reference clock for the Spartan-6 PCI-Express Endpoint Block.

The ICS874001I-05 Jitter Attenuator is configurable by an on-board Configuration DIP-Switch to either multiply the 100 MHz FCLKA signal by 5:4 (resulting in a 125 MHz GTP reference clock for PCIe) or by 1 (resulting in a 100 MHz GTP reference clock for PCIe).

6.2.4 Programmable Clock Generator

The TAMC651 provides the Silicon Labs Si5338 Programmable Clock Generator.

The Clock Source for the Si5338 is a 40 MHz oscillator on IN3.

The Si5338 I2C address is set to 70h (1110000b).

The clock generator allows adapting the clock outputs to specific application needs. The Si5338 could be re-configured by the FPGA application via a dedicated I2C bus interface. Silicon Labs supplies the “ClockBuilder” software tool which can be used to build the Si5338 register settings.

The Si5338 interrupt output is also available on an FPGA pin.

Input	Si5338	TAMC651
IN1/2	CLKIN/CLKINB	Not used IN1 unconnected, IN2 0R resistor to GND
IN3	CLKIN	Sourced by on-board 40 MHz Oscillator
IN4	I2C LSB	Pulldown resistor
IN5/6	FDBK/FDBKB	Not used IN5 unconnected, IN6 connected to GND

Table 6-6 : Programmable Clock Generator Inputs

Output Port	Output Level	Clock Signal Name	Clock Destination	Factory Pre-Configuration
0	LVDS (Output supply is 2.5V)	PRG_CLK0	FPGA Bank 0 GCLK15(P), GCLK14(N)	100 MHz
1		PRG_CLK1	FPGA Bank 2 GCLK3(P), GCLK2(N)	150 MHz
2		PRG_CLK2 (SFP_REFCLK)	FPGA GTP Transceiver SFP Reference Clock	125 MHz
3		PRG_CLK3	Clock Crosspoint-Switch Input Port 0	62.5 MHz

Table 6-7 : Programmable Clock Generator Outputs

Si5338		FPGA					
Pin	Label	Bank	Pin	Signal	I/O Std.	Dir	Output Type
12	SCL	1	R20	CLKGEN_SCL	LVCMOS25	Out	Drive low or High-Z
19	SDA		R19	CLKGEN_SDA		InOut	Drive low or High-Z
8	INTR		P16	CLKGEN_INT		In	

Table 6-8 : Programmable Clock Generator Control & Status Pins

Please see the Si5338 data sheet regarding the Si5338 configuration and status.

6.2.5 Clock Crosspoint-Switch

The TAMC651 provides an on-board Micrel SY89540 Precision Low Jitter 4x4 LVDS Crosspoint-Switch for clock distribution.

The SY89540U provides four clock inputs, four clock outputs and a control interface.

The following table shows the SY89540U clock connections.

LVDS is used for all input and output ports.

Input Port	Clock Signal Name	Clock Source (LVDS)
0	PRG_CLK3	Si5338 Output Port 3
1	FPGA_CLKOUT	FPGA Bank 2 Pins R11 (P), T11 (N)
2	AMC_TCLKA	AMC connector / backplane
3	AMC_TCLKB	AMC connector / backplane
Output Port	**Clock Signal Name**	**Clock Destination (LVDS)**
0	FPGA_CLK0	FPGA Bank 0 GCLK17(P), GCLK16(N)
1	FPGA_CLK1	FPGA Bank 2 GCLK29(P), GCLK28(N)
2	RTM_CLK0	Zone 3 connector / interface
3	RTM_CLK1	Zone 3 connector / interface

Table 6-9 : Clock Crosspoint-Switch Port Clock Mapping

There is no quiescence action for the LVDS clock signals that are driven towards the Zone 3 interface (µRTM). If the AMC payload power is on, these DC coupled LVDS clock signals are always driven by the AMC (towards the µRTM).

The SY89540U Clock Crosspoint-Switch is programmable (configurable) via FPGA /O Pins. Via the control interface the FPGA application is able to map any of the four output ports to any of the four input ports.

SY89540U		FPGA				
Pin	Label	Bank	Pin	Signal	I/O Std.	Dir
18	SIN0	1	R17	CLKSW_SIN0	LVCMOS25	Out
19	SIN1		R16	CLKSW_SIN1		
38	SOUT0		R15	CLKSW_SOUT0		
37	SOUT1		T21	CLKSW_SOUT1		
5	CONF		T20	CLKSW_CONF		
7	LOAD		T17	CLKSW_LOAD		

Table 6-10: Clock Crosspoint-Switch Control Pin Mapping

Please see the SY89540U data sheet regarding SY89540U configuration details.

6.2.6 GTP Reference Clocks

PCI-Express

See “PCI Express Clock Jitter Attenuator”.

SFP

One of the Si5338 Programmable Clock Generator outputs is used as the reference clock for the Spartan-6 GTP transceiver that is implements the SFP interface.

Default configuration for the SFP/GTP reference clock is 125 MHz.

If the FPGA application re-configures the Si5338 with any impact for the clock output used for the SFP/GTP transceiver, the Spartan-6 SFP/GTP transceiver logic may require certain reset actions.

µRTM

If GTP transceivers are used on the Zone 3 interface, the µRTM must provide the GTP reference clocks for these Spartan-6 GTP transceivers.

The TAMC651 provides AC coupling capacitors on the GTP reference clocks.

The GTP reference clocks provided by the µRTM must meet or exceed the reference clock characteristics as specified in the Spartan-6 data sheet.

6.3 User Programmable FPGA

6.3.1 Xilinx Documentation

The Spartan-6 FPGA documentation is available on the Xilinx website (www.xilinx.com).

The following list shows relevant Spartan-6 data sheets and user guides.

- **Spartan-6 FPGA Data Sheet: DC and Switching Characteristics (DS162)**
- Spartan-6 FPGA LX and LXT Production Errata (EN148)
- Spartan-6 FPGA Configuration User Guide (UG380)
- **Spartan-6 FPGA SelectIO Resources User Guide (UG381)**
- **Spartan-6 FPGA Clocking Resources User Guide (UG382)**
- Spartan-6 FPGA Block RAM Resources User Guide (UG383)
- Spartan-6 FPGA Configurable Logic Block User Guide (UG384)
- Spartan-6 FPGA Packaging and Pinouts (UG385)
- Spartan-6 FPGA GTP Transceivers (UG386)
- Spartan-6 FPGA Memory Controller User Guide (UG388)
- Spartan-6 FPGA Power Management User Guide (UG394)

6.3.2 FPGA Device Overview

The TAMC651 provides a Xilinx Spartan-6 user programmable FPGA.

The actual device depends on the TAMC651 board option.

The following table shows a brief comparison of the TAMC651 FPGA device options.

Board option		TAMC651-10R/-11R	TAMC651-12R/-13R
FGPA Device		XC6SLX45T-2-FGG484I	XC6SLX100T-2-FGG484I
Logic Cells		43661	101261
Configurable Logic Blocks (CLBs)	Slices	6822	15822
	Flip-Flops	54576	126576
	Distributed RAM (Kb)	401	976
DSP48A1 Slices		58	180
Block Ram Blocks (a 18 Kb)		116	268
CMTs (2 DCM, 1 PLL)		4	4
Memory Controller Blocks (used)		2 (1)	2 (1)
PCIe Endpoint Blocks		1	1
GTP Transceivers		4	4
I/O Banks		4	4
Max User I/O		296	296

Table 6-11: Spartan-6 LX45T LX100T Comparison

6.3.3 FPGA Power Supplies and I/O Bank Overview

VCCINT = 1.2V, VCCAUX = 3.3V

FPGA I/O Bank	VCCO	Main Usage
0	2.5V	Zone 3 I/O Interface Differential Pairs [16:00]
1	2.5V	AMC Port MLVDS Interface
2	2.5V	Zone 3 I/O Interface Differential Pairs [45:17]
3	1.5V	DDR3 Memory Interface, General Purpose Signals

Table 6-12 : FPGA I/O Bank Overview

The Spartan-6 GTP Dual Tiles are located within FPGA bank 0.

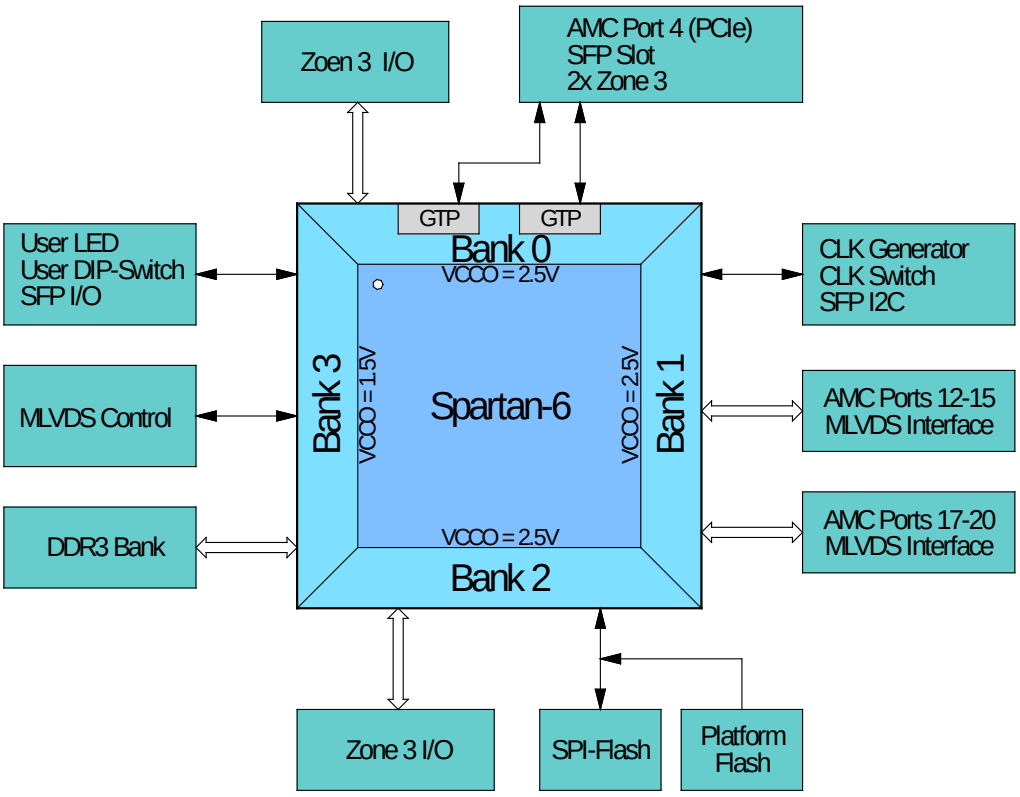


Figure 6-3 : FPGA Block Diagram

6.3.4 FPGA Pin Assignment

The following table shows the TAMC651 FPGA pin assignment.

Ground pins are not shown.

	Zone 3 Interface
	AMC MLVDS Interface
	DDR3 Memory Interface
	SFP Interface
	Clock Signals
	Clock Control
	GPIO | Miscellaneous | Debug Signals

Pin	Bank	Region	Pin-Label	Board Signal
C3	0	TL	IO_L1P_HSWAPEN_0	On-board pullup resistor
D3	0	TL	IO_L1N_VREF_0	+0.9V
D4	**0**	**TL**	**IO_L2P_0**	**RTM_DP[03]_P**
D5	**0**	**TL**	**IO_L2N_0**	**RTM_DP[03]_N**

B2	0	TL	IO_L3P_0	RTM_DP[01]_P
A2	0	TL	IO_L3N_0	RTM_DP[01]_N
E5	0	TL	IO_L4P_0	RTM_DP[02]_P
E6	0	TL	IO_L4N_0	RTM_DP[02]_N
B3	0	TL	IO_L5P_0	RTM_DP[00]_P
A3	0	TL	IO_L5N_0	RTM_DP[00]_N
C4	0	TL	IO_L6P_0	RTM_DP[04]_P
A4	0	TL	IO_L6N_0	RTM_DP[04]_N
F7	0	TL	IO_L7P_0	RTM_DP[07]_P
F8	0	TL	IO_L7N_0	RTM_DP[07]_N
C5	0	TL	IO_L8P_0	Not connected
A5	0	TL	IO_L8N_VREF_0	+0.9V
A6	101	NA	MGTTXN0_101	PCIe_TX_N
B6	101	NA	MGTTXP0_101	PCIe_TX_P
B9	101	NA	MGTAVCCPLL0_101	+1.2V_GTP
B10	101	NA	MGTREFCLK0N_101	PCIe_REFCLK_N
A10	101	NA	MGTREFCLK0P_101	PCIe_REFCLK_P
C7	101	NA	MGTRXN0_101	PCIe_RX_N
D7	101	NA	MGTRXP0_101	PCIe_RX_P
E9	101	NA	MGTRREF_101	GTP_CAL_REF
C9	101	NA	MGTRXN1_101	SFP_RX_N
E8	101	NA	MGTAVTTRCAL_101	GTP_CAL
D9	101	NA	MGTRXP1_101	SFP_RX_P
D12	101	NA	MGTAVCCPLL1_101	+1.2V_GTP
D11	101	NA	MGTREFCLK1N_101	SFP_REFCLK_N
C11	101	NA	MGTREFCLK1P_101	SFP_REFCLK_P
A8	101	NA	MGTTXN1_101	SFP_TX_N
B8	101	NA	MGTTXP1_101	SFP_TX_P
G8	0	TL	IO_L32P_0	RTM_DP[06]_P
F9	0	TL	IO_L32N_0	RTM_DP[06]_N
H10	0	TL	IO_L33P_0	RTM_DP[05]_P
H11	0	TL	IO_L33N_0	RTM_DP[05]_N
G9	0	TL	IO_L34P_GCLK19_0	RTM_DP[16]_P
F10	0	TL	IO_L34N_GCLK18_0	RTM_DP[16]_N
H12	0	TL	IO_L35P_GCLK17_0	FPGA_CLK0_P
G11	0	TL	IO_L35N_GCLK16_0	FPGA_CLK0_N
F14	0	TR	IO_L36P_GCLK15_0	PRG_CLK0_P
F15	0	TR	IO_L36N_GCLK14_0	PRG_CLK0_N
E16	0	TR	IO_L37P_GCLK13_0	RTM_DP[15]_P
F16	0	TR	IO_L37N_GCLK12_0	RTM_DP[15]_N

H13	0	TR	IO_L38P_0	AMC_ZONE3_EN
G13	0	TR	IO_L38N_VREF_0	+0.9V
A14	123	NA	MGTTXN0_123	GTP0_DAT_A2R_P
B14	123	NA	MGTTXP0_123	GTP0_DAT_A2R_N
B13	123	NA	MGTAVCCPLL0_123	+1.2V_GTP
B12	123	NA	MGTREFCLK0N_123	GTP0_CLK_R2A_N
A12	123	NA	MGTREFCLK0P_123	GTP0_CLK_R2A_P
C13	123	NA	MGTRXN0_123	GTP0_DAT_R2A_N
D13	123	NA	MGTRXP0_123	GTP0_DAT_R2A_P
C15	123	NA	MGTRXN1_123	GTP1_DAT_R2A_N
D15	123	NA	MGTRXP1_123	GTP1_DAT_R2A_P
E13	123	NA	MGTAVCCPLL1_123	+1.2V_GTP
F12	123	NA	MGTREFCLK1N_123	GTP1_CLK_R2A_N
E12	123	NA	MGTREFCLK1P_123	GTP1_CLK_R2A_P
A16	123	NA	MGTTXN1_123	GTP1_DAT_A2R_N
B16	123	NA	MGTTXP1_123	GTP1_DAT_A2R_P
H14	0	TR	IO_L49P_0	RTM_DP[10]_P
G15	0	TR	IO_L49N_0	RTM_DP[10]_N
C17	0	TR	IO_L50P_0	RTM_DP[08]_P
A17	0	TR	IO_L50N_0	RTM_DP[08]_N
G16	0	TR	IO_L51P_0	RTM_DP[09]_P
F17	0	TR	IO_L51N_0	RTM_DP[09]_N
D18	0	TR	IO_L62P_0	Not connected
D19	0	TR	IO_L62N_VREF_0	+0.9V
B18	0	TR	IO_L63P_SCP7_0	RTM_DP[13]_P
A18	0	TR	IO_L63N_SCP6_0	RTM_DP[13]_N
C19	0	TR	IO_L64P_SCP5_0	RTM_DP[11]_P
A19	0	TR	IO_L64N_SCP4_0	RTM_DP[11]_N
B20	0	TR	IO_L65P_SCP3_0	RTM_DP[14]_P
A20	0	TR	IO_L65N_SCP2_0	RTM_DP[14]_N
D17	0	TR	IO_L66P_SCP1_0	RTM_DP[12]_P
C18	0	TR	IO_L66N_SCP0_0	RTM_DP[12]_N
A21	NA	NA	TCK	FPGA_TCK
E18	NA	NA	TDI	FPGA_TDI
D20	NA	NA	TMS	FPGA_TMS
G17	NA	NA	TDO	FPGA_TDO
F18	1	RT	IO_L1P_A25_1	MLVDS_TX19_RE_N
F19	1	RT	IO_L1N_A24_VREF_1	MLVDS_TX19_DE
H16	1	RT	IO_L9P_1	MLVDS_TX17_RE_N
H17	1	RT	IO_L9N_1	MLVDS_TX17_DE

B21	1	RT	IO_L10P_1	MLVDS_RX19_DE
B22	1	RT	IO_L10N_1	MLVDS_RX19_DI
J16	1	RT	IO_L19P_1	MLVDS_RX15_RE_N
J17	1	RT	IO_L19N_1	MLVDS_RX15_DE
C20	1	RT	IO_L20P_1	MLVDS_RX19_RE_N
C22	1	RT	IO_L20N_1	MLVDS_RX20_DI
L15	1	RT	IO_L21P_1	MLVDS_TX15_RO
K16	1	RT	IO_L21N_1	MLVDS_RX14_RO
D21	1	RT	IO_L28P_1	MLVDS_RX20_DE
D22	1	RT	IO_L28N_VREF_1	MLVDS_TX19_DI
G19	1	RT	IO_L29P_A23_M1A13_1	MLVDS_RX17_RE_N
F20	1	RT	IO_L29N_A22_M1A14_1	MLVDS_TX20_RE_N
H18	1	RT	IO_L30P_A21_M1RESET_1	MLVDS_TX18_RE_N
H19	1	RT	IO_L30N_A20_M1A11_1	MLVDS_TX18_DE
F21	1	RT	IO_L31P_A19_M1CKE_1	MLVDS_TX20_DE
F22	1	RT	IO_L31N_A18_M1A12_1	MLVDS_RX17_DI
E20	1	RT	IO_L32P_A17_M1A8_1	MLVDS_RX20_RE_N
E22	1	RT	IO_L32N_A16_M1A9_1	MLVDS_TX20_DI
J19	1	RT	IO_L33P_A15_M1A10_1	MLVDS_RX14_RE_N
H20	1	RT	IO_L33N_A14_M1A4_1	MLVDS_RX18_RE_N
K19	1	RT	IO_L34P_A13_M1WE_1	MLVDS_TX15_RE_N
K18	1	RT	IO_L34N_A12_M1BA2_1	MLVDS_TX14_DE
G20	1	RT	IO_L35P_A11_M1A7_1	MLVDS_RX17_DE
G22	1	RT	IO_L35N_A10_M1A2_1	MLVDS_RX18_DI
K17	1	RT	IO_L36P_A9_M1BA0_1	MLVDS_TX14_RE_N
L17	1	RT	IO_L36N_A8_M1BA1_1	MLVDS_TX14_RO
H21	1	RT	IO_L37P_A7_M1A0_1	MLVDS_RX18_DE
H22	1	RT	IO_L37N_A6_M1A1_1	MLVDS_TX17_DI
K20	1	RT	IO_L38P_A5_M1CLK_1	MLVDS_TX15_DE
L19	1	RT	IO_L38N_A4_M1CLKN_1	MLVDS_RX15_RO
J20	1	RT	IO_L39P_M1A3_1	MLVDS_RX14_DE
J22	1	RT	IO_L39N_M1ODT_1	MLVDS_TX18_DI
M20	1	RT	IO_L40P_GCLK11_M1A5_1	MLVDS_TX17_RO
M19	1	RT	IO_L40N_GCLK10_M1A6_1	MLVDS_TX18_RO
K21	1	RT	IO_L41P_GCLK9_IRDY1_M1RASN_1	MLVDS_RX18_RO
K22	1	RT	IO_L41N_GCLK8_M1CASN_1	MLVDS_RX17_RO
P20	1	RB	IO_L42P_GCLK7_M1UDM_1	MLVDS_TX20_RO
N19	1	RB	IO_L42N_GCLK6_TRDY1_M1LDM_1	MLVDS_TX19_RO
L20	1	RB	IO_L43P_GCLK5_M1DQ4_1	MLVDS_RX20_RO
L22	1	RB	IO_L43N_GCLK4_M1DQ5_1	MLVDS_RX19_RO

M21	1	RB	IO_L44P_A3_M1DQ6_1	MLVDS_RX12_RE_N
M22	1	RB	IO_L44N_A2_M1DQ7_1	MLVDS_RX12_DE
N20	1	RB	IO_L45P_A1_M1LDQS_1	MLVDS_TX13_RE_N
N22	1	RB	IO_L45N_A0_M1LDQSN_1	MLVDS_RX14_DI
P21	1	RB	IO_L46P_FCS_B_M1DQ2_1	MLVDS_RX12_RO
P22	1	RB	IO_L46N_FOE_B_M1DQ3_1	MLVDS_RX15_DI
R20	1	RB	IO_L47P_FWE_B_M1DQ0_1	CLKGEN_SCL
R22	1	RB	IO_L47N_LDC_M1DQ1_1	MLVDS_TX14_DI
T21	1	RB	IO_L48P_HDC_M1DQ8_1	CLKSW_SOUT1
T22	1	RB	IO_L48N_M1DQ9_1	MLVDS_TX15_DI
U20	1	RB	IO_L49P_M1DQ10_1	PAYLOAD_RST_N
U22	1	RB	IO_L49N_M1DQ11_1	MLVDS_RX12_DI
V21	1	RB	IO_L50P_M1UDQS_1	MMC_SDA
V22	1	RB	IO_L50N_M1UDQSN_1	MLVDS_RX13_DI
W20	1	RB	IO_L51P_M1DQ12_1	UART_TXD
W22	1	RB	IO_L51N_M1DQ13_1	MLVDS_TX12_DI
Y21	1	RB	IO_L52P_M1DQ14_1	UART_RXD
Y22	1	RB	IO_L52N_M1DQ15_1	MLVDS_TX13_DI
P19	1	RB	IO_L53P_1	MLVDS_RX13_RO
R19	1	RB	IO_L53N_VREF_1	CLKGEN_SDA
M16	1	RB	IO_L58P_1	MLVDS_TX13_DE
N15	1	RB	IO_L58N_1	MLVDS_TX12_RE_N
U19	1	RB	IO_L59P_1	MMC_SCL
T20	1	RB	IO_L59N_1	CLKSW_CONF
N16	1	RB	IO_L60P_1	MLVDS_TX12_DE
P16	1	RB	IO_L60N_1	CLKGEN_INT
M17	1	RB	IO_L61P_1	MLVDS_RX13_RE_N
M18	1	RB	IO_L61N_1	MLVDS_RX13_DE
R15	1	RB	IO_L70P_1	CLKSW_SOUT0
R16	1	RB	IO_L70N_1	CLKSW_SIN1
P17	1	RB	IO_L71P_1	MLVDS_TX13_RO
P18	1	RB	IO_L71N_1	MLVDS_TX12_RO
R17	1	RB	IO_L72P_1	CLKSW_SIN0
T17	1	RB	IO_L72N_1	CLKSW_LOAD
T19	1	RB	IO_L73P_1	SFP_SCL
T18	1	RB	IO_L73N_1	SFP_SDA
V19	1	RB	IO_L74P_AWAKE_1	Not connected
V20	1	RB	IO_L74N_DOUT_BUSY_1	Not connected
U17	NA	NA	VFS	Tied to ground
P15	NA	NA	RFUSE	Tied to ground

T16	NA	NA	VBATT	Tied to ground
AA22	NA	NA	SUSPEND	Tied to ground
V18	2	NA	CMPCS_B_2	Not connected
AB21	2	NA	DONE_2	FPGA configuration logic
Y20	2	BR	IO_L1P_CCLK_2	FPGA configuration logic
AA21	2	BR	IO_L1N_M0_CMPMISO_2	On-board pullup resistor
V17	2	BR	IO_L2P_CMPCLK_2	RTM_DP[34]_P
W18	2	BR	IO_L2N_CMPMOSI_2	RTM_DP[34]_N
AA20	2	BR	IO_L3P_D0_DIN_MISO_MISO1_2	FPGA configuration logic
AB20	2	BR	IO_L3N_MOSI_CSI_B_MISO0_2	FPGA configuration logic
U16	2	BR	IO_L4P_2	RTM_DP[38]_P (2)
V15	2	BR	IO_L4N_VREF_2	+0.9V
W17	2	BR	IO_L5P_2	RTM_DP[37]_P
Y18	2	BR	IO_L5N_2	RTM_DP[37]_N
AA14	2	BR	IO_L6P_2	RTM_DP[45]_P
AB14	2	BR	IO_L6N_2	RTM_DP[45]_N
Y16	2	BR	IO_L17P_2	RTM_DP[40]_P
W15	2	BR	IO_L17N_2	RTM_DP[40]_N
V13	2	BR	IO_L18P_2	RTM_DP[44]_P
W13	2	BR	IO_L18N_2	RTM_DP[44]_N
R13	2	BR	IO_L12P_D1_MISO2_2	RTM_DP[42]_P
T14	2	BR	IO_L12N_D2_MISO3_2	RTM_DP[42]_N
Y19	2	BR	IO_L13P_M1_2	On-board Pulldown resistor
AB19	2	BR	IO_L13N_D10_2	Not connected
AA18	2	BR	IO_L14P_D11_2	RTM_DP[36]_P
AB18	2	BR	IO_L14N_D12_2	RTM_DP[36]_N
Y17	2	BR	IO_L15P_2	RTM_DP[35]_P
AB17	2	BR	IO_L15N_2	RTM_DP[35]_N
U14	2	BR	IO_L16P_2	RTM_DP[38]_N (2)
U13	2	BR	IO_L16N_VREF_2	+0.9V
AA16	2	BR	IO_L19P_2	RTM_DP[39]_P
AB16	2	BR	IO_L19N_2	RTM_DP[39]_N
W14	2	BR	IO_L20P_2	RTM_DP[41]_P
Y14	2	BR	IO_L20N_2	RTM_DP[41]_N
Y15	2	BR	IO_L21P_2	RTM_DP[43]_P
AB15	2	BR	IO_L21N_2	RTM_DP[43]_N
R11	2	BR	IO_L22P_2	FPGA_CLKOUT_P
T11	2	BR	IO_L22N_2	FPGA_CLKOUT_N
T15	2	BR	IO_L23P_2	RTM_DP[38]_P
U15	2	BR	IO_L23N_2	RTM_DP[38]_N

T12	2	BR	IO_L29P_GCLK3_2	PRG_CLK1_P
U12	2	BR	IO_L29N_GCLK2_2	PRG_CLK1_N
Y13	2	BR	IO_L30P_GCLK1_D13_2	Not connected
AB13	2	BR	IO_L30N_GCLK0_USERCCLK_2	USER_CLK (62.5 MHz)
AA12	2	BL	IO_L31P_GCLK31_D14_2	RTM_DP[33]_P
AB12	2	BL	IO_L31N_GCLK30_D15_2	RTM_DP[33]_N
Y11	2	BL	IO_L32P_GCLK29_2	FPGA_CLK1_P
AB11	2	BL	IO_L32N_GCLK28_2	FPGA_CLK1_N
W12	2	BL	IO_L40P_2	RTM_DP[19]_P
Y12	2	BL	IO_L40N_2	RTM_DP[19]_N
AA10	2	BL	IO_L41P_2	RTM_DP[22]_N (2)
AB10	2	BL	IO_L41N_VREF_2	+0.9V
V11	2	BL	IO_L42P_2	RTM_DP[18]_P
W11	2	BL	IO_L42N_2	RTM_DP[18]_N
Y9	2	BL	IO_L43P_2	RTM_DP[25]_P
AB9	2	BL	IO_L43N_2	RTM_DP[25]_N
W10	2	BL	IO_L44P_2	RTM_DP[22]_P
Y10	2	BL	IO_L44N_2	RTM_DP[22]_N
AA8	2	BL	IO_L45P_2	RTM_DP[28]_P
AB8	2	BL	IO_L45N_2	RTM_DP[28]_N
T10	2	BL	IO_L46P_2	RTM_DP[17]_P
U10	2	BL	IO_L46N_2	RTM_DP[17]_N
Y7	2	BL	IO_L47P_2	RTM_DP[26]_P
AB7	2	BL	IO_L47N_2	RTM_DP[26]_N
W9	2	BL	IO_L48P_D7_2	RTM_DP[22]_P (2)
Y8	2	BL	IO_L48N_RDWR_B_VREF_2	+0.9V
AA6	2	BL	IO_L49P_D3_2	RTM_DP[30]_P
AB6	2	BL	IO_L49N_D4_2	RTM_DP[30]_N
U9	2	BL	IO_L50P_2	RTM_DP[20]_P
V9	2	BL	IO_L50N_2	RTM_DP[20]_N
T8	2	BL	IO_L57P_2	RTM_DP[24]_P
U8	2	BL	IO_L57N_2	RTM_DP[24]_N
V7	2	BL	IO_L58P_2	RTM_DP[23]_P
W8	2	BL	IO_L58N_2	RTM_DP[23]_N
R9	2	BL	IO_L59P_2	RTM_DP[21]_P
R8	2	BL	IO_L59N_2	RTM_DP[21]_N
W6	2	BL	IO_L60P_2	RTM_DP[31]_P
Y6	2	BL	IO_L60N_2	RTM_DP[31]_N
Y5	2	BL	IO_L62P_D5_2	RTM_DP[29]_P
AB5	2	BL	IO_L62N_D6_2	RTM_DP[29]_N

AA4	2	BL	IO_L63P_2	RTM_DP[32]_P
AB4	2	BL	IO_L63N_2	RTM_DP[32]_N
T7	2	BL	IO_L64P_D8_2	RTM_DP[27]_P
U6	2	BL	IO_L64N_D9_2	RTM_DP[27]_N
Y4	2	BL	IO_L65P_INIT_B_2	FPGA Configuration Logic
AA3	2	BL	IO_L65N_CSO_B_2	FPGA Configuration Logic
AB2	2	NA	PROGRAM_B_2	FPGA_PROGRAM_B
R7	3	LB	IO_L1P_3	On-board calibration resistor (DDR_RZQ)
P8	3	LB	IO_L1N_VREF_3	+0.75V
W4	3	LB	IO_L2P_3	Not connected (DDR_ZIO)
Y3	3	LB	IO_L2N_3	GPIO_SW[1]
T6	3	LB	IO_L7P_3	GPIO_SW[2]
T5	3	LB	IO_L7N_3	GPIO_SW[3]
V5	3	LB	IO_L8P_3	GPIO_SW[4]
V3	3	LB	IO_L8N_3	GPIO_LED[1]
P5	3	LB	IO_L9P_3	GPIO_LED[2]
P4	3	LB	IO_L9N_3	GPIO_LED[3]
AA2	3	LB	IO_L10P_3	GPIO_LED[4]
AA1	3	LB	IO_L10N_3	GPIO_BUT_N
N6	3	LB	IO_L23P_3	SFP_PS_N
N7	3	LB	IO_L23N_3	Not connected
U4	3	LB	IO_L24P_3	SFP_TX_DIS
T4	3	LB	IO_L24N_3	SFP_TX_FLT
P6	3	LB	IO_L25P_3	SFP_RX_BW
P7	3	LB	IO_L25N_3	SFP_RX_LOS
T3	3	LB	IO_L26P_3	LED2_CTRL
R4	3	LB	IO_L26N_3	LED2_CTRL_MODE
M7	3	LB	IO_L31P_3	Not connected
M8	3	LB	IO_L31N_VREF_3	+0.75V
Y2	3	LB	IO_L32P_M3DQ14_3	DDR_DQ[14]
Y1	3	LB	IO_L32N_M3DQ15_3	DDR_DQ[15]
W3	3	LB	IO_L33P_M3DQ12_3	DDR_DQ[12]
W1	3	LB	IO_L33N_M3DQ13_3	DDR_DQ[13]
V2	3	LB	IO_L34P_M3UDQS_3	DDR_UDQS_P
V1	3	LB	IO_L34N_M3UDQSN_3	DDR_UDQS_N
U3	3	LB	IO_L35P_M3DQ10_3	DDR_DQ[10]
U1	3	LB	IO_L35N_M3DQ11_3	DDR_DQ[11]
T2	3	LB	IO_L36P_M3DQ8_3	DDR_DQ[08]
T1	3	LB	IO_L36N_M3DQ9_3	DDR_DQ[09]
R3	3	LB	IO_L37P_M3DQ0_3	DDR_DQ[00]

R1	3	LB	IO_L37N_M3DQ1_3	DDR_DQ[01]
P2	3	LB	IO_L38P_M3DQ2_3	DDR_DQ[02]
P1	3	LB	IO_L38N_M3DQ3_3	DDR_DQ[03]
N3	3	LB	IO_L39P_M3LDQS_3	DDR_LDQS_P
N1	3	LB	IO_L39N_M3LDQSN_3	DDR_LDQS_N
M2	3	LB	IO_L40P_M3DQ6_3	DDR_DQ[06]
M1	3	LB	IO_L40N_M3DQ7_3	DDR_DQ[07]
L3	3	LB	IO_L41P_GCLK27_M3DQ4_3	DDR_DQ[04]
L1	3	LB	IO_L41N_GCLK26_M3DQ5_3	DDR_DQ[05]
P3	3	LB	IO_L42P_GCLK25_TRDY2_M3UDM_3	DDR_UDM
N4	3	LB	IO_L42N_GCLK24_M3LDM_3	DDR_LDM
M5	3	LT	IO_L43P_GCLK23_M3RASN_3	DDR_RAS_N
M4	3	LT	IO_L43N_GCLK22_IRDY2_M3CASN_3	DDR_CAS_N
M3	3	LT	IO_L44P_GCLK21_M3A5_3	DDR_A[05]
L4	3	LT	IO_L44N_GCLK20_M3A6_3	DDR_A[06]
M6	3	LT	IO_L45P_M3A3_3	DDR_A[03]
L6	3	LT	IO_L45N_M3ODT_3	DDR_ODT
K4	3	LT	IO_L46P_M3CLK_3	DDR_CK_P
K3	3	LT	IO_L46N_M3CLKN_3	DDR_CK_N
K2	3	LT	IO_L47P_M3A0_3	DDR_A[00]
K1	3	LT	IO_L47N_M3A1_3	DDR_A[01]
J3	3	LT	IO_L48P_M3BA0_3	DDR_BA[0]
J1	3	LT	IO_L48N_M3BA1_3	DDR_BA[1]
K6	3	LT	IO_L49P_M3A7_3	DDR_A[07]
K5	3	LT	IO_L49N_M3A2_3	DDR_A[02]
H2	3	LT	IO_L50P_M3WE_3	DDR_WE_N
H1	3	LT	IO_L50N_M3BA2_3	DDR_BA[2]
J4	3	LT	IO_L51P_M3A10_3	DDR_A[10]
H3	3	LT	IO_L51N_M3A4_3	DDR_A[04]
G3	3	LT	IO_L52P_M3A8_3	DDR_A[08]
G1	3	LT	IO_L52N_M3A9_3	DDR_A[09]
F2	3	LT	IO_L53P_M3CKE_3	DDR_CKE
F1	3	LT	IO_L53N_M3A12_3	DDR_A[12]
E3	3	LT	IO_L54P_M3RESET_3	DDR_RESET_N
E1	3	LT	IO_L54N_M3A11_3	DDR_A[11]
J6	3	LT	IO_L55P_M3A13_3	DDR_A[13]
H5	3	LT	IO_L55N_M3A14_3	DDR_A[14]
K7	3	LT	IO_L57P_3	Not connected
K8	3	LT	IO_L57N_VREF_3	+0.75V
H4	3	LT	IO_L58P_3	MLVDS_12_RT

G4	3	LT	IO_L58N_3	MLVDS_13_RT
D2	3	LT	IO_L59P_3	MLVDS_14_RT
D1	3	LT	IO_L59N_3	MLVDS_15_RT
F3	3	LT	IO_L60P_3	MLVDS_17_RT
E4	3	LT	IO_L60N_3	MLVDS_18_RT
H6	3	LT	IO_L80P_3	MLVDS_19_RT
G7	3	LT	IO_L80N_3	MLVDS_20_RT
J7	3	LT	IO_L81P_3	MLVDS_12_13_MDE
H8	3	LT	IO_L81N_3	MLVDS_14_15_MDE
F5	3	LT	IO_L82P_3	MLVDS_17_18_MDE
G6	3	LT	IO_L82N_3	MLVDS_19_20_MDE
C1	3	LT	IO_L83P_3	Not connected
B1	3	LT	IO_L83N_VREF_3	+0.75V
C10	101	NA	MGTAVCC_101	+1.2V_GTP
E10	123	NA	MGTAVCC_123	
D8	101	NA	MGTAVTTRX_101	
D14	123	NA	MGTAVTTRX_123	
A7	101	NA	MGTAVTTTX_101	
A15	123	NA	MGTAVTTTX_123	
F11	NA	NA	VCCAUX	+3.3V
G12	NA	NA		
H15	NA	NA		
H9	NA	NA		
K15	NA	NA		
L8	NA	NA		
M15	NA	NA		
N8	NA	NA		
R10	NA	NA		
R12	NA	NA		
R6	NA	NA		
U11	NA	NA		
V6	NA	NA		
J10	NA	NA	VCCINT	+1.2V
J12	NA	NA		
J14	NA	NA		
J8	NA	NA		
K11	NA	NA		
K13	NA	NA		
K9	NA	NA		
L10	NA	NA		

L12	NA	NA		
L14	NA	NA		
M11	NA	NA		
M13	NA	NA		
M9	NA	NA		
N10	NA	NA		
N12	NA	NA		
N14	NA	NA		
P11	NA	NA		
P13	NA	NA		
P9	NA	NA		
R14	NA	NA		
B19	0	NA	VCCO_0	+2.5V
B4	0	NA		
E17	0	NA		
F6	0	NA		
G10	0	NA		
G14	0	NA		
C21	1	NA	VCCO_1	+2.5V
E1	1	NA		
G21	1	NA		
J18	1	NA		
L16	1	NA		
L21	1	NA		
N18	1	NA		
R21	1	NA		
U18	1	NA		
W21	1	NA		
AA11	2	NA	VCCO_2	+2.5V
AA15	2	NA		
AA19	2	NA		
AA7	2	NA		
AB3	2	NA		
T13	2	NA		
T9	2	NA		
V12	2	NA		
V16	2	NA		
V8	2	NA		
W5	2	NA		
C2	3	NA	VCCO_3	+1.5V

F4	3	NA		
G2	3	NA		
J5	3	NA		
L2	3	NA		
L7	3	NA		
N5	3	NA		
R2	3	NA		
U5	3	NA		
W2	3	NA		

Table 6-13: FPGA Pin / Signal Assignment

6.3.5 FPGA I/O Signal Description

The following table describes the TAMC651 FPGA I/O signals.

Board Signal	Direction	Description
AMC Port MLVDS Interface		
MLVDS_12_13_MDE	Out	Master Enable signal for the MLVDS transceiver chips used for AMC ports 12-15 and 17-20. There are four MLVDS transceiver chips. Each MLVDS transceiver chip covers two AMC ports. On-board pulldown resistor. 0: MLVDS transceiver chip disabled (default) 1: MLVDS transceiver chip enabled
MLVDS_14_15_MDE	Out	
MLVDS_17_18_MDE	Out	
MLVDS_19_20_MDE	Out	
MLVDS_n_RT n = 12, 13, 14, 15, 17, 18, 19, 20	Out (8x)	Receiver Type for the MLVDS transceiver used for AMC ports 12-15 and 17-20. The receiver type is configurable per AMC port. On-board pulldown resistor. 0: Type 1 receiver input 1: Type 2 receiver input See the DS91M040 documentation for details
MLVDS_RXn_RE_N n = 12, 13, 14, 15, 17, 18, 19, 20	Out (8x)	Receiver enable control for AMC RX port 0: Receiver enabled 1: Receiver disabled
MLVDS_RXn_RO n = 12, 13, 14, 15, 17, 18, 19, 20	In (8x)	Receive data signal from AMC RX port
MLVDS_RXn_DE n = 12, 13, 14, 15, 17, 18, 19, 20	Out (8x)	Transmitter enable control for AMC RX port On-board pulldown resistor 0: Transmitter disabled (default) 1: Transmitter enabled
MLVDS_RXn_DI n = 12, 13, 14, 15, 17, 18,	Out (8x)	Transmit data signal to AMC RX port

19, 20		
MLVDS_TXn_RE_N n = 12, 13, 14, 15, 17, 18, 19, 20	Out (8x)	Receiver enable control for AMC TX port 0: Receiver enabled 1: Receiver disabled
MLVDS_TXn_RO n = 12, 13, 14, 15, 17, 18, 19, 20	In (8x)	Receive data signal from AMC TX port
MLVDS_TXn_DE n = 12, 13, 14, 15, 17, 18, 19, 20	Out (8x)	Transmitter enable control for AMC TX port On-board pulldown resistor 0: Transmitter disabled (default) 1: Transmitter enabled
MLVDS_TXn_DI n = 12, 13, 14, 15, 17, 18, 19, 20	Out (8x)	Transmit data signal to AMC TX port
Clock Signals		
USER_CLK	In	Fix 62.5 MHz on-board oscillator connected to GCLK0 May also be used as FPGA configuration clock source during FPGA configuration (appropriate divider setting required)
PRG_CLK0_P	In	Differential clock signal from Si5338 (Programmable Clock Generator) output 0
PRG_CLK0_N	In	
PRG_CLK1_P	In	Differential clock signal from Si5338 (Programmable Clock Generator) output 1
PRG_CLK1_N	In	
FPGA_CLK0_N	In	Differential clock signal from SY89540U (Clock Crosspoint-Switch) output 0
FPGA_CLK0_P	In	
FPGA_CLK1_P	In	Differential clock signal from SY89540U (Clock Crosspoint-Switch) output 1
FPGA_CLK1_N	In	
FPGA_CLKOUT_P	Out	Differential clock signal output connected to SY89540U (Clock Crosspoint-Switch) input 1
FPGA_CLKOUT_N	Out	
Clock Control Signals		
CLKGEN_SCL	Out (OD)	I2C clock signal connected to the Si5338 programmable clock generator pin Drive low or High-Z (not high)
CLKGEN_SDA	Out (OD)	I2C data signal connected to the Si5338 pin Drive low or High-Z (not high)
CLKGEN_INT	In	Si5338 programmable clock generator interrupt output 0: Interrupt output not active 1: Interrupt output active
CLKSW_SIN[1:0]	Out (2x)	Signal outputs connected to the appropriate control pins of the on-board Clock Crosspoint-Switch See the SY89540U documentation for details
CLKSW_SOUT[1:0]	Out (2x)	
CLKSW_LOAD	Out	
CLKSW_CONFIG	Out	
GTP Transceiver Signals		

PCIe_TX_P	Out	PCI Express Transmit Data
PCIe_TX_N	Out	
PCIe_RX_P	In	PCI Express Receive Data
PCIe_RX_N	In	
PCIe_REFCLK_P	In	PCI Express Reference Clock (from AMC FCLKA PCIe Clock De-Jitter Device)
PCIe_REFCLK_P	In	
SFP_TX_P	Out	SFP Interface Transmit Data
SFP_TX_N	Out	
SFP_RX_P	In	SFP Interface Receive Data
SFP_RX_N	In	
SFP_REFCLK_P	In	SFP Interface Reference Clock (from Si5338 Programmable Clock Generator)
SFP_REFCLK_P	In	
GTP0_DAT_A2R_P	Out	µRTM GTP 0 Interface Transmit Data (to Zone 3 Interface)
GTP0_DAT_A2R_N	Out	
GTP0_DAT_R2A_P	In	µRTM GTP 0 Interface Receive Data (from Zone 3 Interface)
GTP0_DAT_R2A_N	In	
GTP0_CLK_R2A_P	In	µRTM GTP 0 Interface Reference Clock (from Zone 3 Interface)
GTP0_CLK_R2A_P	In	
GTP1_DAT_A2R_P	Out	µRTM GTP 1 Interface Transmit Data (to Zone 3 Interface)
GTP1_DAT_A2R_N	Out	
GTP1_DAT_R2A_P	In	µRTM GTP 1 Interface Receive Data (from Zone 3 Interface)
GTP1_DAT_R2A_N	In	
GTP1_CLK_R2A_P	In	µRTM GTP 1 Interface Reference Clock (from Zone 3 Interface)
GTP1_CLK_R2A_P	In	
SFP Interface (Control/Status)		
SFP_SCL	Out (OD)	I2C clock signal of the SFP module/connector Drive low or High-Z (not high)
SFP_SDA	In/Out (OD)	I2C data signal of the SFP module/connector Drive low or High-Z (not high)
SFP_PS_N	In	Present signal of the SFP module/connector On-board pullup resistor Active low
SFP_TX_DIS	Out	Transmit Disable control signal for the SFP module/connector On-board pullup resistor
SFP_TX_FLT	In	Transmit Fault status signal of the SFP module/connector
SFP_RX_BW	Out	Receiver Bandwidth control signal for the SFP module/connector On-board pullup resistor
SFP_RX_LOS	In	Receiver Loss of Signal status signal from SFP module/connector

General Purpose | Miscellaneous | Debug Signals		
PAYLOAD_RST#	In	Payload reset signal (controlled by the MMC) 0: Payload reset active 1: Payload reset not active
GPIO_SW[1:4]	In (4x)	On-board user DIP Switch status 0: Switch position is off 1: Switch position is on
GPIO_LED[1:4]	Out (4x)	Front plate user LED control 0: LED off 1: LED on
GPIO_BUT_N	In	Debug Connector
UART_RXD	In	Debug Connector
UART_TXD	Out	Debug Connector
MMC_SCL	In	Drive low or High-Z (not high)
MMC_SDA	In/Out (OD)	Drive low or High-Z (not high)
LED2_CTRL	Out (OD)	AMC User LED Control On-board pullup resistor Drive low or High-Z (not high)
		Level control mode: 0: Green User LED off 1: Green User LED on
		Edge control mode: During normal operation the green User LED is on. An edge on LED2_CTRL turns the LED off for approx 100ms (LED flashes off, indicating activity)
LED2_CTRL_MODE	Out (OD)	AMC User LED Control Mode On-board pullup resistor Drive low or High-Z (not high) 0: Level control mode 1: Edge control mode (default)
FPGA Configuration and/or Serial SPI Flash Access		
FPGA_CCLK	Out	(after configuration) Serial SPI Flash Clock
FPGA_DIN	In	(after configuration) Data from serial SPI Flash
FPGA_MOSI	Out	(after configuration) Data to serial SPI Flash
FPGA_INIT_B	In/Out	Not for user application
FPGA_CSO_B	Out	(after configuration) Select signal for serial SPI Flash
FPGA_M0	In	Not for user application On-board pullup resistor
FPGA_M1	In	Not for user application On-board pulldown resistor
DDR3 Memory Interface		
DDR_RESET_N	Out	DDR3 Memory reset signal
DDR_CK_P	Out	DDR3 Memory differential clock signal

DDR_CK_N	Out	
DDR_RAS	Out	DDR3 Memory row address strobe signal
DDR_CAS	Out	DDR3 Memory column address strobe signal
DDR_WE#	Out	DDR3 Memory write enable signal
DDR_CKE	Out	DDR3 Memory clock enable signal
DDR_ODT	Out	DDR3 Memory on-die-termination signal
DDR_LDM	Out	DDR3 Memory data input mask signal for DQ[07:00]
DDR_UDM	Out	DDR3 Memory data input mask signal for DQ[15:08]
DDR_BA[2:0]	Out (3x)	DDR3 Memory bank address signals
DDR_A[14:00]	Out (15x)	DDR3 Memory address signals (A13, A14 are for future use)
DDR_LDQS_P	In/Out	DDR3 Memory differential data strobe signal for DQ[07:00]
DDR_LDQS_N	In/Out	
DDR_UDQS_P	In/Out	DDR3 Memory differential data strobe signal for DQ[15:08]
DDR_UDQS_N	In/Out	
DDR_DQ[15:00]	In/Out (16x)	DDR3 Memory data bus signals
Zone 3 Interface		
AMC_ZONE3_EN	In	Zone 3 Interface Enable indication (controlled by the MMC). FPGA code may disable/enable Zone 3 Interface Drivers accordingly. 0: Zone 3 Interface is not enabled 1: Zone 3 Interface is enabled
RTM_DP[45:00]_P	In/Out (46x)	Zone 3 interface I/O signals. Up to 46 differential pairs (up to 92 single-ended lines). Directly connected to the Zone 3 interface connectors. Differential pairs RTM_DP[00:16] are located in FPGA bank 0. Differential pairs RTM_DP[17:45] are located in FPGA bank 2. Routing lengths are matched per FPGA bank. Global clock capable differential pairs in the order of least internal restriction potential: RTM_DP[33], RTM_DP[15], RTM_DP[16]
RTM_DP[45:00]_N	In/Out (46x)	

Table 6-14: FPGA I/O Signal Description

Please see the generic FPGA User Constraint File in Appendix A for appropriate FPGA I/O Standard assignments.

6.3.6 Global Clock Pin Assignment

The following table shows the signal mapping for all 32 FPGA global clock pins.

FPGA Pin-Label	Bank	Region	Assigned Signal
IO_L30N_GCLK0_USERCCLK_2	2	BR	USER_CLK (fix 62.5 MHz Oscillator) Could also be used as configuration clock source (with FPGA internal divider active during configuration)
IO_L30P_GCLK1_D13_2	2	BR	Not used
IO_L29N_GCLK2_2	2	BR	PRG_CLK1 (differential clock signal from programmable clock generator)
IO_L29P_GCLK3_2	2	BR	
IO_L43N_GCLK4_M1DQ5_1	1	RB	MLVDS_RX19_RO (from AMC/MLVDS port interface)
IO_L43P_GCLK5_M1DQ4_1	1	RB	MLVDS_RX20_RO (from AMC/MLVDS port interface)
IO_L42N_GCLK6_TRDY1_M1LDM_1	1	RB	MLVDS_TX19_RO (from AMC/MLVDS port interface)
IO_L42P_GCLK7_M1UDM_1	1	RB	MLVDS_TX20_RO (from AMC/MLVDS port interface)
IO_L41N_GCLK8_M1CASN_1	1	RT	MLVDS_RX17_RO (from AMC/MLVDS port interface)
IO_L41P_GCLK9_IRDY1_M1RASN_1	1	RT	MLVDS_RX18_RO (from AMC/MLVDS port interface)
IO_L40N_GCLK10_M1A6_1	1	RT	MLVDS_TX18_RO(from AMC/MLVDS port interface)
IO_L40P_GCLK11_M1A5_1	1	RT	MLVDS_TX17_RO (from AMC/MLVDS port interface)
IO_L37N_GCLK12_0	0	TR	RTM_DP[15] (differential pair on the Zone 3 interface)
IO_L37P_GCLK13_0	0	TR	
IO_L36N_GCLK14_0	0	TR	PRG_CLK0 (differential clock signal from programmable clock generator)
IO_L36P_GCLK15_0	0	TR	
IO_L35N_GCLK16_0	0	TL	FPGA_CLK0 (differential clock signal from clock crosspoint-switch)
IO_L35P_GCLK17_0	0	TL	
IO_L34N_GCLK18_0	0	TL	RTM_DP[16] (differential pair on the Zone 3 interface)
IO_L34P_GCLK19_0	0	TL	
IO_L44N_GCLK20_M3A6_3	3	LT	No user clock signals mapped. Occupied by Spartan-6 MCB signals for the DDR3 Memory Interface
IO_L44P_GCLK21_M3A5_3	3	LT	
IO_L43N_GCLK22_IRDY2_M3CASN_3	3	LT	
IO_L43P_GCLK23_M3RASN_3	3	LT	
IO_L42N_GCLK24_M3LDM_3	3	LB	
IO_L42P_GCLK25_TRDY2_M3UDM_3	3	LB	

IO_L41N_GCLK26_M3DQ5_3	**3**	**LB**	
IO_L41P_GCLK27_M3DQ4_3	**3**	**LB**	
IO_L32N_GCLK28_2	**2**	**BL**	**FPGA_CLK1 (differential clock signal from clock crosspoint-switch)**
IO_L32P_GCLK29_2	**2**	**BL**	
IO_L31N_GCLK30_D15_2	**2**	**BL**	**RTM_DP[33] (differential pair on the Zone 3 interface)**
IO_L31P_GCLK31_D14_2	**2**	**BL**	

Table 6-15: FPGA Global Clock Pin Assignment

6.3.7 Clock Signal Planning

The following section provides important information regarding the Spartan-6 clocking resources and potential resource conflicts in the TAMC651 context.

This information should be noticed for designing TAMC651 compatible µRTM modules.

Please refer to the Xilinx Spartan-6 Clocking Resources User Guide (UG382), especially Chapter 1: Clocking Resources

6.3.7.1 Global Clock Buffer

Spartan-6 FPGA's are providing (up to) 32 global clock input pins and 16 internal global clock buffers. So there are less internal global clock buffers than potential external clock signals. Internal signals such as DCM/PLL clock outputs and BUFIO2 DIVCLK outputs may also require global clock buffers.

FPGA Banks 0 & 1

The global clock inputs in FPGA banks 0 & 1 are sharing eight internal global clock buffers. Since there are more potential external clock signals than global clock buffers, not all the signals connected to global clock pins in FPGA banks 0 & 1 could be used with global clock buffers at the same time.

The following table shows all global clock buffers available for the external clock signals of FPGA banks 0 & 1 and also the potential conflicts when mapping external or internal signals to the global clock buffers.

Each global clock buffer (BUFGMUX) is a 2:1 MUX providing two inputs I0 and I1. Each BUFGMUX (output) could be set to either input I0 or input I1.

Each BUFGMUX I0 input is connected to the I1 input of an adjacent BUFGMUX. E.g. Input I0 of BUFGMUX_X2Y1 and input I1 of BUFGMUX_X2Y2 could not be used independently, but only with the same signal.

Per row, only one of the signals listed could be connected to the global clock buffer inputs shown in the left column!

The right column (internal signals) applies if the DIVCLK output of a BUFIO2 regional clock buffer is used to drive clock inputs in the general FPGA logic (since this also requires a global clock buffer).

Note that internal DCM or PLL clock outputs may also require one or more global clock buffers.

The table may be used for planning the signal assignments to the various global clock buffer mux inputs. Chose one signal for each row, then for each BUFGMUX chose the input that should be used (I0 or I1).

Global Clock Buffer Mux Inputs available for FPGA banks 0 & 1	External Signals		Internal Signals (1)
	Direct mapping options	Indirect mapping options (via bank 1 BUFIO2)	BUFIO2 DIVCLK Output
BUFGMUX_X2Y1 (I0) BUFGMUX_X2Y2 (I1)	RTM_DP[16] (differential) RTM_DP[16]_P (single) MLVDS_TX17_RO	MLVDS_TX20_RO (BUFIO2_X4Y20)	BUFIO2_X2Y28 BUFIO2_X4Y20
BUFGMUX_X2Y2 (I0) BUFGMUX_X2Y1 (I1)	RTM_DP[16]_N (single) MLVDS_TX18_RO	MLVDS_TX19_RO (BUFIO2_X4Y21)	BUFIO2_X2Y29 BUFIO2_X4Y21
BUFGMUX_X2Y3 (I0) BUFGMUX_X2Y4 (I1)	FPGA_CLK0 (differential) MLVDS_RX18_RO	MLVDS_RX20_RO (BUFIO2_X4Y18)	BUFIO2_X2Y26 BUFIO2_X4Y18
BUFGMUX_X2Y4 (I0) BUFGMUX_X2Y3 (I1)	PRG_CLK0 (differential) MLVDS_TX20_RO	MLVDS_TX17_RO (BUFIO2_X3Y12)	BUFIO2_X4Y28 BUFIO2_X3Y12
BUFGMUX_X3Y5 (I0) BUFGMUX_X3Y6 (I1)	MLVDS_RX17_RO	MLVDS_RX19_RO (BUFIO2_X4Y19)	BUFIO2_X2Y27 BUFIO2_X4Y19
BUFGMUX_X3Y6 (I0) BUFGMUX_X3Y5 (I1)	MLVDS_TX19_RO	MLVDS_TX18_RO (BUFIO2_X3Y13)	BUFIO2_X4Y29 BUFIO2_X3Y13
BUFGMUX_X3Y7 (I0) BUFGMUX_X3Y8 (I1)	RTM_DP[15] (differential) RTM_DP[15]_P (single) MLVDS_RX20_RO	MLVDS_RX18_RO (BUFIO2_X3Y10)	BUFIO2_X4Y26 BUFIO2_X3Y10
BUFGMUX_X3Y8 (I0) BUFGMUX_X3Y7 (I1)	RTM_DP[15]_N (single) MLVDS_RX19_RO	MLVDS_RX17_RO (BUFIO2_X3Y11)	BUFIO2_X4Y27 BUFIO2_X3Y11

(1) Internal DCM or PLL clock outputs may also require one or more global clock buffers

Table 6-16: FPGA Banks 0 & 1 BUFGMUX Resources

For example:

PRG_CLK0 and MLVDS_TX20_RO provide a path to the global clock buffer inputs BUFGMUX_X2Y4 (I0) & BUFGMUX_X2Y3 (I1), but they could not both be mapped directly to the global clock buffers inputs.

However, if RTM_DP[16] and MLVDS_TX17_RO are not used with their dedicated global clock buffer inputs, MLVDS_TX20_RO may be mapped indirectly to global clock buffer inputs BUFGMUX_X2Y1 (I0) & BUFGMUX_X2Y2 (I1) by using the BUFIO2_X4Y20 buffer, while PRG_CLK0 is mapped directly to global clock buffer inputs BUFGMUX_X2Y4 (I0) & BUFGMUX_X2Y3 (I1).

FPGA Banks 2 & 3

The global clock inputs in FPGA banks 2 & 3 are also sharing eight internal BUFGMUX buffers. Since there are no external user clock signals assigned to the global clock pins of FPGA bank 3, there are no external signal conflicts regarding the BUFGMUX buffers for FPGA bank 2.

The following table shows how the external clock signals of FPGA bank 2 could be mapped to global clock buffers. Note that differential input signals are (by default) associated with the P pin of a differential pair.

The right column (internal signals) applies if the DIVCLK output of a BUFIO2 regional clock buffer is used to drive clock inputs in the general FPGA logic (since this also requires a global clock buffer).

Note that internal DCM or PLL clock outputs may also require one or more global clock buffers.

Each global clock buffer (BUFGMUX) is a 2:1 MUX providing two inputs I0 and I1. Each BUFGMUX output could be set to either input I0 or input I1.

Global Clock Buffer Mux Inputs available for FPGA banks 2 & 3	Associated FPGA Bank 2 Global Clock Pin	External Signals	Internal Signals [1]
		Direct mapping option	BUFIO2 DIVCLK Output
BUFGMUX_X2Y9 (I0) BUFGMUX_X2Y10 (I1)	GCLK3 (29P)	PRG_CLK1 (differential) (from Programmable Clock Generator)	BUFIO2_X3Y0
BUFGMUX_X2Y10 (I0) BUFGMUX_X2Y9 (I1)	GCLK2 (29N)	BUFG not used by external clock signal	BUFIO2_X3Y1
BUFGMUX_X2Y11 (I0) BUFGMUX_X2Y12 (I1)	GCLK1 (30P)	BUFG not used by external clock signal	BUFIO2_X3Y6
BUFGMUX_X2Y12 (I0) BUFGMUX_X2Y11 (I1)	GCLK31 (31P)	RTM_DP[33] (differential) RTM_DP[33]_P (single) (from Zone 3 Interface)	BUFIO2_X1Y0
BUFGMUX_X3Y13 (I0) BUFGMUX_X3Y14 (I1)	GCLK0 (30N)	USER_CLK (fix 62.5 MHz Oscillator)	BUFIO2_X3Y7
BUFGMUX_X3Y14 (I0) BUFGMUX_X3Y13 (I1)	GCLK30 (31N)	RTM_DP[33]_N (single) (from Zone 3 Interface)	BUFIO2_X1Y1
BUFGMUX_X3Y15 (I0) BUFGMUX_X3Y16 (I1)	GCLK29 (32P)	FPGA_CLK1 (differential) (from Clock Crosspoint-Switch)	BUFIO2_X1Y6
BUFGMUX_X3Y16 (I0) BUFGMUX_X3Y15 (I1)	GCLK28 (32N)	BUFG not used by external clock signal	BUFIO2_X1Y7

[1] Internal DCM or PLL clock outputs may also require one or more global clock buffers

Table 6-17: FPGA Banks 2 & 3 BUFGMUX Resources

6.3.7.2 Regional Clock Buffer

The TAMC651 Spartan-6 FPGA provides:

- Four I/O banks (0 … 3), each spanning an edge of the FPGA device
- Two clock regions per I/O bank
    - bank 0 regions TL (top left), TR (top right)
    - bank 1 regions RT (right top), RB (right bottom)
    - bank 2 regions BL (bottom left), BR (bottom right)
    - bank 3 regions LT (left top), LB (left bottom)
- Four global clock pins per clock region
- Four BUFIO2 regional clock buffers per clock region
- Two GTP Dual Tiles in FPGA bank 0 (one GTP Dual Tile per region)

A BUFIO2 regional clock buffer is required for:

- Global clock input signals
    - that should be used in a high-speed regional clock network, e.g. sampling data of a SDR or DDR data rate interface (DDR data rate interfaces require an additional BUFIO2)
    - that should directly connect to a PLL/DCM input
    - that should connect to an alternative global clock buffer
- Using a GTP component clock output in the FPGA user logic

Since all the four GTP transceivers are located in FPGA bank 0, both FPGA bank 0 global clock pin signals and GTP implementations are competing for a limited number of FPGA bank 0 BUFIO2 components for clock regions TL and TR.

The following table shows all BUFIO2 buffers available for FPGA bank 0 regions TL & TR, and the resources that could be used with a certain BUFIO2 buffer. **Only one resource listed could be used with the BUFIO2 buffer shown in the same row!**

The GTPCLKOUT signals shown are clock outputs of the FPGA GTP transceiver component towards the FPGA user logic. Please refer to the Spartan-6 GTP Transceivers User Guide (UG386) for more information.

Bank 0 Region	BUFIO2 ID	External Clock Signals		GTP Transceiver	
		Signal	Inverting BUFIO2	Function	Clock Output
TL	BUFIO2_X2Y26	FPGA_CLK0 (diff)	N	SFP	GTP Dual 0 GTPCLKOUT1[0]
		RTM_DP[15] (diff) RTM_DP15]_P (se)			
		RTM_DP[15]_N (se)	Y		
	BUFIO2_X2Y27	RTM_DP[15]_N (se)	N		GTP Dual 0 GTPCLKOUT1[1]
		FPGACLK0 (diff)	Y		
		RTM_DP[15] (diff) RTM_DP15]_P (se)			
	BUFIO2_X2Y28	RTM_DP[16] (diff) RTM_DP[16]_P (se)	N	PCIe	GTP Dual 0 GTPCLKOUT0[0]

		PRG_CLK0 (diff)			
		RTM_DP[16]_N (se)	Y		
	BUFIO2_X2Y29	RTM_DP[16]_N (se)	N		GTP Dual 0 GTPCLKOUT0[1]
		RTM_DP[16] (diff) RTM_DP[16]_P (se)	Y		
		PRG_CLK0 (diff)			
TR	BUFIO2_X4Y26	RTM_DP[15] (diff) RTM_DP[15]_P (se)	N	RTM1	GTP Dual 1 GTPCLKOUT1[0]
		FPGA_CLK0 (diff)			
		RTM_DP[15]_N (se)	Y		
	BUFIO2_X4Y27	RTM_DP[15]_N (se)	N		GTP Dual 1 GTPCLKOUT1[1]
		RTM_DP[15] (diff) RTM_DP[15]_P (se)	Y		
		FPGA_CLK0 (diff)			
	BUFIO2_X4Y28	PRG_CLK0 (diff)	N	RTM0	GTP Dual 1 GTPCLKOUT0[0
		RTM_DP[16] (diff) RTM_DP[16]_P (se)			
		RTM_DP[16]_N (se)	Y		
	BUFIO2_X4Y29	RTM_DP[16]_N (se)	N		GTP Dual 1 GTPCLKOUT0[1]
		PRG_CLK0 (diff)	Y		
		RTM_DP[16] (diff) RTM_DP[16]_P (se)			

Table 6-18: FPGA Bank 0 Clock Region Buffer Resources

For example:

BUFIO2_X2Y28 could be either used by:

- GTP PCIe component clock out GTPCLKOUT[0]
- RTM_DP[16] differential signal (or RTM_DP[16]_P single-ended signal) from the Zone 3 interface
- PRG_CLK0 differential clock signal from the on-board programmable clock generator
- RTM_DP[16]_N single-ended signal from the Zone 3 interface (the BUFIO2 could only be used in inverting mode with this signal)

E.g. if the PCIe GTP output clock 0 is required in the FPGA user logic, the RTM_DP[16] differential signal could not be used with the BUFIO2_X2Y28 component. The RTM_DP[16] differential signal may still be used for region TL with the BUFIO2_X2Y29 component if the PCIe GTP output clock 1 is not required in the FPGA user logic. Note that in this case the BUFIO2_X2Y29 component may only be used in inverting mode with the RTM_DP[16] signal (so to maintain clock-data relation in this case it might be necessary to connect the P line to the N pin and vice versa). The RTM_DP[16] signal may also be used with BUFIO2_X4Y28 (non-inverting) for clock region TR.

When the RTM_DP[] signals are used as a clock signal for a Spartan-6 regional I/O clock network, the related data lines must belong to the same clock region as the clock signal!

6.3.8 GTP Transceiver

The TAMC651 Spartan-6 FPGA provides four GTP transceivers.

The figure below shows the Spartan-6 GTP transceiver utilization on the TAMC651.

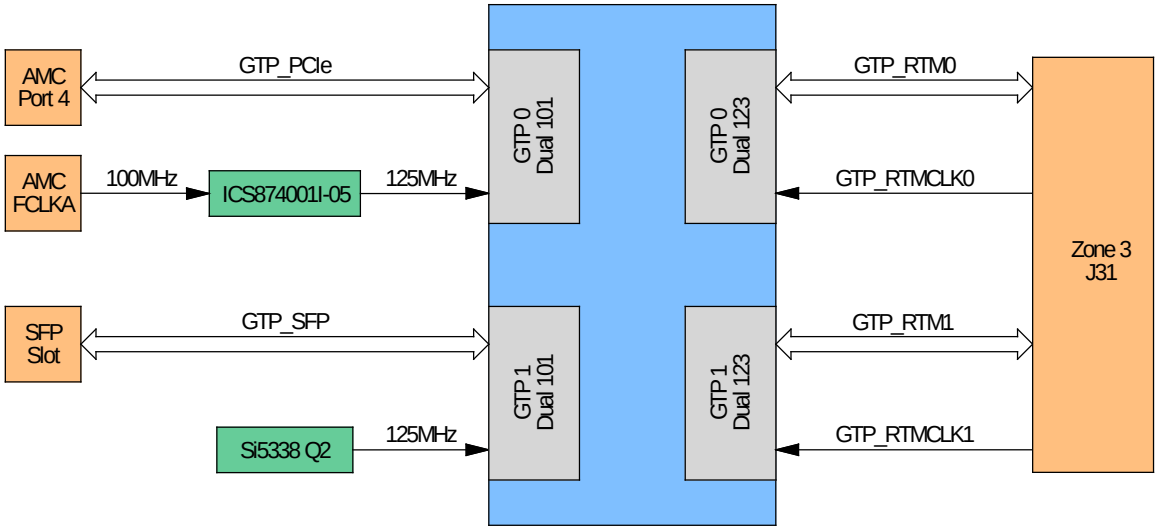


Figure 6-4 : Spartan-6 GTP Transceiver

GTP Channel Enumeration	Bank 0 GTP Dual	GTP Channel in Dual	GTP Usage		GTP Reference Clock Source
0	101	0	PCIe	AMC Port 4	AMC FCLKA via ICS874001I-05 Jitter Attenuator 125 MHz or 100 MHz
1		1	SFP	SFP Slot	From Si5338 Programmable Clock Generator Factory Pre-Configuration 125 MHz
2	123	0	RTM0	Zone 3 Interface	From µRTM
3		1	RTM1		

Table 6-19: Spartan GTP Transceiver

The TAMC651 provides AC coupling for all GTP signals (TX+/-, RX+/-, REFCLK+/-).

6.3.9 FPGA Memory Controller Block

The Spartan-6 Bank 1 Memory Controller Block is not used.

The Spartan-6 I/O Bank 3 Memory Controller Block is used for the DDR3 SDRAM Bank.

The TAMC651 provides one 128 Mbyte DDR3 SDRAM bank (16 bit data width).

Signal	DDR Bank FPGA Pin	I/O Standard	Termination	Memory Device	
				Pin	Name
A0	**K2**	**SSTL15_II**	**49.9Ω V_{TT}**	**N3**	**A0**
A1	**K1**	**SSTL15_II**	**49.9Ω V_{TT}**	**P7**	**A1**
A2	**K5**	**SSTL15_II**	**49.9Ω V_{TT}**	**P3**	**A2**
A3	**M6**	**SSTL15_II**	**49.9Ω V_{TT}**	**N2**	**A3**
A4	**H3**	**SSTL15_II**	**49.9Ω V_{TT}**	**P8**	**A4**
A5	**M3**	**SSTL15_II**	**49.9Ω V_{TT}**	**P2**	**A5**
A6	**L4**	**SSTL15_II**	**49.9Ω V_{TT}**	**R8**	**A6**
A7	**K6**	**SSTL15_II**	**49.9Ω V_{TT}**	**R2**	**A7**
A8	**G3**	**SSTL15_II**	**49.9Ω V_{TT}**	**T8**	**A8**
A9	**G1**	**SSTL15_II**	**49.9Ω V_{TT}**	**R3**	**A9**
A10	**J4**	**SSTL15_II**	**49.9Ω V_{TT}**	**L7**	**A10/AP**
A11	**E1**	**SSTL15_II**	**49.9Ω V_{TT}**	**R7**	**A11**
A12	**F1**	**SSTL15_II**	**49.9Ω V_{TT}**	**N7**	**A12/BCN**
A13	**J6**	**SSTL15_II**	**49.9Ω V_{TT}**	**T3**	**NC/A13**
A14	**H5**	**SSTL15_II**	**49.9Ω V_{TT}**	**T7**	**NC/A14**
BA0	**J3**	**SSTL15_II**	**49.9Ω V_{TT}**	**M2**	**BA0**
BA1	**J1**	**SSTL15_II**	**49.9Ω V_{TT}**	**N8**	**BA1**
BA2	**H1**	**SSTL15_II**	**49.9Ω V_{TT}**	**M3**	**BA2**
RAS#	**M5**	**SSTL15_II**	**49.9Ω V_{TT}**	**J3**	**RAS#**
CAS#	**M4**	**SSTL15_II**	**49.9Ω V_{TT}**	**K3**	**CAS#**
WE#	**H2**	**SSTL15_II**	**49.9Ω V_{TT}**	**L3**	**WE#**
CS#	**-**	**-**	**100Ω GND**	**L2**	**CS#**
RESET#	**E3**	**LVCMOS15**	**4.7kΩ GND**	**T2**	**RESET#**
CKE	**F2**	**SSTL15_II**	**4.7kΩ GND**	**K9**	**CKE**
ODT	**L6**	**SSTL15_II**	**49.9Ω V_{TT}**	**K1**	**ODT**
DQ0	**R3**	**SSTL15_II**	**ODT**	**E3**	**DQ0**
DQ1	**R1**	**SSTL15_II**	**ODT**	**F7**	**DQ1**
DQ2	**P2**	**SSTL15_II**	**ODT**	**F2**	**DQ2**
DQ3	**P1**	**SSTL15_II**	**ODT**	**F8**	**DQ3**
DQ4	**L3**	**SSTL15_II**	**ODT**	**H3**	**DQ4**
DQ5	**L1**	**SSTL15_II**	**ODT**	**H8**	**DQ5**
DQ6	**M2**	**SSTL15_II**	**ODT**	**G2**	**DQ6**

Signal	DDR Bank FPGA Pin	I/O Standard	Termination	Memory Device	
				Pin	Name
DQ7	**M1**	**SSTL15_II**	**ODT**	**H7**	**DQ7**
DQ8	**T2**	**SSTL15_II**	**ODT**	**D7**	**DQ8**
DQ9	**T1**	**SSTL15_II**	**ODT**	**C3**	**DQ9**
DQ10	**U3**	**SSTL15_II**	**ODT**	**C8**	**DQ10**
DQ11	**U1**	**SSTL15_II**	**ODT**	**C2**	**DQ11**
DQ12	**W3**	**SSTL15_II**	**ODT**	**A7**	**DQ12**
DQ13	**W1**	**SSTL15_II**	**ODT**	**A2**	**DQ13**
DQ14	**Y2**	**SSTL15_II**	**ODT**	**B8**	**DQ14**
DQ15	**Y1**	**SSTL15_II**	**ODT**	**A3**	**DQ15**
LDQS	**N3**	**DIFF_SSTL15_II**	**ODT**	**F3**	**LDQS**
LDQS#	**N1**	**DIFF_SSTL15_II**	**ODT**	**G3**	**LDQS#**
UDQS	**V2**	**DIFF_SSTL15_II**	**ODT**	**C7**	**UDQS**
UDQS#	**V1**	**DIFF_SSTL15_II**	**ODT**	**B7**	**UDQS#**
LDM	**N4**	**SSTL15_II**	**ODT**	**E7**	**LDM**
UDM	**P3**	**SSTL15_II**	**ODT**	**D3**	**UDM**
CK	**K4**	**DIFF_SSTL15_II**	**100Ω**	**J7**	**CK**
CK#	**K3**	**DIFF_SSTL15_II**		**K7**	**CK#**
RZQ	**R7**	**SSTL15_II**	**100Ω GND**	**-**	**-**
ZIO	**W4**	**SSTL15_II**	**open**	**-**	**-**

Table 6-20: FPGA Bank 3 MCB Interface (DDR3)

6.3.10 FPGA Configuration

Configuration Mode

The FPGA configuration mode is set fix to Master Serial/SPI by resistor configuration of the FPGA Mode pins. On the TAMC651 the FPGA is always the master of the serial configuration interface and provides the clock to the configuration memory device.

After power-up the FPGA device is blank and starts reading the configuration bitstream from the selected FPGA configuration memory device. When the FPGA has been configured properly, the on-board FPGA_DONE LED is set on.

Volatile direct FPGA configuration via the JTAG chain is always possible. The non-volatile FPGA configuration data source (Platform Flash or SPI Serial Flash) is selectable by the on-board Configuration DIP-Switch.

Configuration Options

The TAMC651 supports the following FPGA configuration options:

- Program FPGA directly via JTAG (volatile)
- FPGA reads configuration data from Platform Flash
- FPGA reads configuration data from SPI Serial Flash

All configuration options are using the TAMC651 JTAG chain which is accessible via the TAMC651 JTAG header. Connector and pin-out of the TAMC651 JTAG header matches that of the Xilinx Platform Cable USB II programmer. The Xilinx iMPACT software could be used for all configuration options.

JTAG (volatile)

For testing and debugging the FPGA may be configured directly via the TAMC651 JTAG chain.

Platform Flash

The TAMC651 provides the Xilinx XCF32PFSG48C Platform Flash device to store the FPGA bitstream.

On the TAMC651 the XCF32P device is used in serial slave mode.

The Platform-Flash device is directly programmable via the TAMC651 JTAG chain.

SPI Serial Flash

The TAMC651 provides the Numonyx M25P64-VME6 Serial SPI Flash device to store the FPGA bitstream.

The SPI-Flash device is indirectly programmable via the TAMC651 JTAG chain. The Xilinx iMPACT software will configure the FPGA with an application that programs the SPI Flash via FPGA I/O pins.

The FPGA configuration date source must be set to “SPI Flash” (Configuration DIP-Switch) for programming the SPI Serial Flash.

After configuration the user application may store user data in unused SPI Flash areas.

Configuration Clock

The FPGA configuration interface is synchronous to a configuration clock.

The TAMC651 supports using the FPGA internally generated configuration clock but does also provide an option for using the 62.5 MHz clock on the GCLK0 pin as configuration clock. For this option, an FPGA internal clock divider must be used. The clock divider is only active during configuration. The configuration clock source and rate (or divider) is selected in the ISE design software and is then integrated into the FPGA bitstream.

The TAMC651 has been successfully tested with an internal configuration clock setting of 26 MHz (+/-50%) and an external configuration clock setting of 62.5 MHz DIV 2 = 31.25 MHz. However, these are not guaranteed values. Guaranteed settings are 12 MHz (+/-50%) for the internal configuration clock source and 62.5 MHz DIV 4 = 15.625 MHz for the external configuration clock source.

Board Option	FPGA Device	FPGA Configuration Clock Rate	Approximate FPGA Configuration Time
Internal Configuration Clock Source			
TAMC651-10R/-11R	**XC6LX45T**	**12 MHz (+/-50%)**	**0.7 … 2.0 s**
TAMC651-12R/-13R	**XC6LX100T**		**1.5 … 4.5 s**
External Configuration Clock Source			
TAMC651-10R/-11R	**XC6LX45T**	**DIV 4 (15.625 MHz)**	**0.8 s**
TAMC651-12R/-13R	**XC6LX100T**		**1.7 s**

Table 6-21: FPGA Configuration Rate and Time

6.3.11 Thermal Management

When designing the FPGA logic project (prior to programming the FPGA or FPGA configuration devices), care must be taken regarding the FPGA power dissipation and junction temperature rating!

Exceeding the maximum junction temperature rating may damage the FPGA device!

The absolute maximum rating for the Spartan-6 (industrial temperature range) junction temperature is specified in the Xilinx “Spartan-6 DC and Switching Characteristics” data sheet (DS162).

Thermal specifications for the Spartan-6 FGG484 package are listed in the Spartan-6 “Packaging and Pinouts” user guide (UG385).

As stated in the Xilinx Spartan-6 Power Management user guide (UG394): To estimate the total power consumption (quiescent plus dynamic) for a specific design use one of the following tools:

- The XPower Power Estimator spreadsheet provides quick, approximate estimates, and does not require the design’s netlist
- The XPower Analyzer is delivered with the ISE Design Suite software and uses a netlist as input to provide more accurate estimates.

The TAMC651 provides the following Heatsink and thermal tape for the user programmable Xilinx Spartan-6 FPGA: Fischer Elektronik ICK S 18mm x 18mm x 6.5mm + WLFT 405 16mm x 16mm

6.4 DDR3 Memory Interface

The TAMC651 provides a 128 Mbyte (16 bit wide) DDR3 SDRAM memory.

The DDR3 SDRAM interface utilizes a hardwired internal Memory Controller Block of the Spartan-6 FPGA.

Initial device is a Micron MT41J64M16LA-187E-IT. The Micron MT41K64M16TW-107-IT:J has been added as an alternative part.

6.5 SFP Interface

The TAMC651 provides a standard SFP interface at the front plate.

One of the Spartan-6 GTP transceivers is used for the SFP data interface. Other SFP control and status signals are available as FPGA I/O.

One of the Si5338 Programmable Clock Generator outputs provides the reference clock for the Spartan-6 GTP transceiver that is used for the SFP interface.

6.6 Serial SPI Flash

The TAMC651 provides a Numonyx M25P64 64Mbit serial SPI Flash.

The SPI Flash signals are available on multi-purpose FPGA I/O pins that belong to the FPGA configuration interface during configuration and are available as User I/O after configuration.

SPI Flash		FPGA				
Signal	**Description**	**Bank**	**I/O Std.**	**Pin**	**Signal**	**Dir**
SPI_D	**SPI Data In**	**2 (VCCO 2.5V)**	**LVCMOS25**	**AB20**	**FPGA_MOSI**	**Out**
SPI_S#	**SPI Select**			**AA3**	**FPGA_CSO_B**	**Out**
SPI_Q	**SPI Data Out**			**AA20**	**FPGA_DIN**	**In**
SPI_C	**SPI Clock**			**Y20**	**FPGA_CCLK**	**Out**

Table 6-22: SPI Serial Flash Pin Mapping

The FPGA application may store user data in SPI Flash areas that are not used for storing FPGA configuration data.

6.7 Zone 3 (µRTM) Interface

TAMC651 Zone 3 Interface keynotes:

- Uses both J30 and J31 30-pair ADF receptacle connectors
- 46x differential User I/O (directly connected to Spartan-6 FPGA differential I/O pins)
- 2x differential Clock to µRTM (from AMC clock crosspoint-switch)
- 2x FPGA GTP Transceiver Link (µRTM provides the reference clocks)
- JTAG support

The voltage level for the µRTM user I/O signals is 2.5V (single-ended) or LVDS (differential). The signal level for the JTAG interface is 3.3V.

The differential user I/O signals of the Zone 3 interface signals are directly connected to the FPGA, without any further circuitry like termination networks. The Spartan-6 FPGA's internal termination-resistor capabilities could be used.

The reference clocks from the AMCs clock crosspoint switch are directly connected to the Zone 3 interface connectors (no AC coupling).

The AMC provides AC coupling capacitors for the (optionally) GTP reference clocks generated by the µRTM.

6.8 JTAG

The TAMC651 main JTAG chain features the following devices:

1. Xilinx Spartan-6 FPGA (TAMC651-10R/-11R: XC6SLX45T, TAMC651-12R/-13R: XC6SLX100T)
2. Xilinx Platform Flash (XCF32P)
3. µRTM JTAG chain (if Zone 3 interface is enabled)

The µRTM JTAG chain can always be bypassed by a Configuration DIP-Switch setting.

The TAMC651 provides several options for controlling the main JTAG chain.

Supported JTAG TAP controller interfaces are (in highest priority order):

1. JTAG Header (Xilinx Platform Cable USB II Programmer)
2. Debug Connector (TAMC651 bottom side)
3. TAMC651 MMC
4. AMC Slot

The Xilinx Platform Cable USB II programmer could be directly connected to the TAMC651 JTAG header.

See Board-I/O chapter for pin assignments and signal descriptions.

6.9 Debug Port

The TAMC651 provides a 20-pin debug (flex cable) connector on the back side.

The debug connector provides the following interfaces:

- JTAG chain access
- MMC UART interface (e.g. debug output)
- FPGA UART interface (depends on FPGA application)
- Push Button status

See Board-I/O chapter for pin assignment and signal description.

The TAMC651 debug port is compatible to the TEWS Technologies TA900 Program and Debug box.

7 Board Configuration

This chapter describes aspects of board configuration prior to board installation.

7.1 Overview

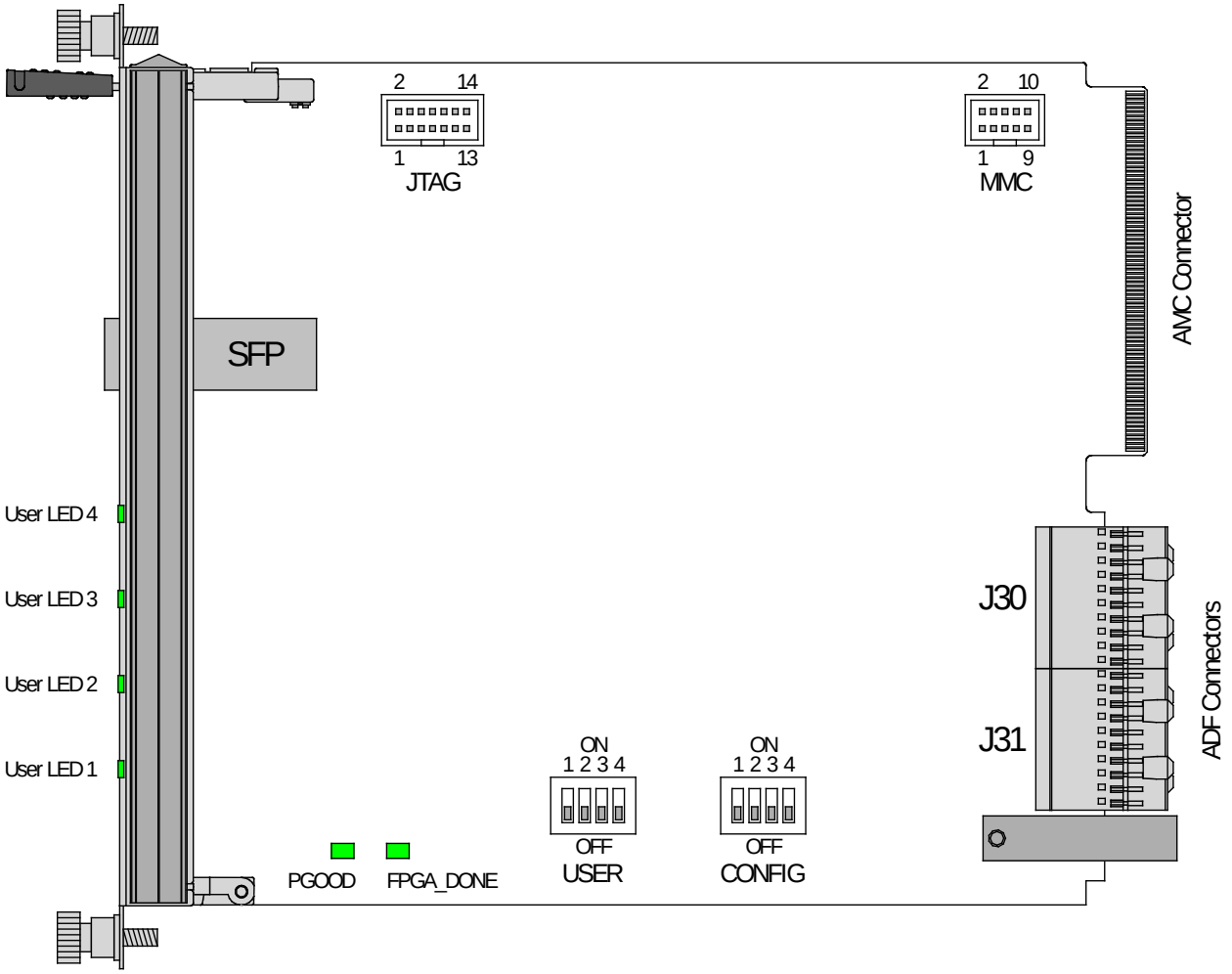


Figure 7-1 : Board Overview

7.2 DIP Switches

The TAMC651 provides two DIP-Switches that (if desired) must be set prior to board installation.

7.2.1 User DIP-Switch

The TAMC651 provides a four position user DIP-Switch, readable by the FPGA application.

Switch	FGPA				
	Bank	Pin	I/O Std.	Dir	Status
1	3 (VCCO 1.5V)	Y3	LVCMOS15	In	0: Switch is Off 1: Switch is On
2		T6			
3		T5			
4		V5			

Table 7-1 : User DIP-Switch

7.2.2 Configuration DIP-Switch

The TAMC651 provides a four position configuration DIP-Switch for general board configuration.

Switch	On	Off (default)
1	FPGA configuration data path set to SPI Flash	FPGA configuration data path set to Platform Flash
2	Force bypassing the µRTM JTAG Chain (even if the µRTM interface is enabled by the MMC)	Include µRTM JTAG Chain (if the µRTM interface is enabled by the MMC)
3	The PCIe REFCLK at the FPGA GTP Reference Clock Input is 1:1 FCLKA (100 MHz)	The PCIe REFCLK at the FPGA GTP Reference Clock Input is FCLKA (100 MHz) Multiplied by 5:4 (125 MHz)
4	Reserved	

Table 7-2 : Configuration DIP-Switch

7.3 FPGA Configuration Memory Programming

When powered-up in the system, the TAMC651 FPGA is initially blank and starts reading configuration data from the selected FPGA configuration memory device.

The TAMC651 provides two FPGA configuration memory options:

- a Xilinx Platform Flash (XCF32P in serial slave mode)
- a serial SPI Flash (M25P64)

The actual FPGA configuration memory device is selected by Configuration DIP-Switch position 1.

The TAMC651 is shipped with blank FPGA configuration memory devices.

The FPGA configuration memory device is programmable by the TAMC651 JTAG header. The TAMC651 JTAG header directly supports the Xilinx Platform Cable USB II. Typically, the TAMC651 FPGA configuration memory device is programmed by using the Xilinx iMPACT software, while the TAMC651 payload power is enabled (in-system).

The Xilinx Platform Flash is directly programmable via the JTAG interface. The Platform Flash is always programmable via the JTAG chain, regardless of the actually selected FPGA configuration memory device.

The serial SPI Flash is indirectly programmable via the FPGA JTAG interface. The Xilinx iMPACT software configures the FPGA with a support application that programs the SPI Flash via FPGA user I/O signals. The SPI Flash is only programmable if the SPI Flash is selected as the actual FPGA configuration memory device.

8 Board Installation

This chapter contains general notes regarding installing the AMC or µRTM module into the MTCA.4 system.

8.1 AMC Module Installation

During insertion and extraction, the operational state of the AMC is visible via the blue LED in the AMCs front panel. The following table lists all valid combinations of Hot-swap handle position and blue LED status, including a short description of what's going on.

Blue LED Handle	On	Off	Long Blink	Short Blink
Open (Pulled out)	**Extraction: Module can be extracted** **Insertion: Module is waiting for closed Handle**	**Module is waiting for hot swap negotiation**	**-**	**Hot swap negotiation in progress (Extraction)**
Closed (Pushed all way in)	**Module is waiting for hot swap negotiation**	**Module is active (operating)**	**Hot swap negotiation in progress (Insertion)**	**-**

Table 8-1 : Hot-Swap states

8.1.1 AMC Insertion

Typical insertion sequence:

1. Insert the ACM module into its slot, with the board edges aligned to the card guides
2. Make sure that the module handle is pushed into the inserted position
    a. Blue LED turns "ON." (Module is ready to attempt activation by the system)
    b. Blue LED starts "Long Blink" (Hot Swap Negotiation / Module activation in progress)
    c. Blue LED turns "OFF", and green LED turns "ON" (Module is ready and powered)

When the Blue LED does not go off but returns to the "ON" state, the module FRU information is invalid or the system cannot provide the power requested by the AMC module.

The green PGOOD on-board LED indicates if the TAMC651 payload power is enabled and considered within specification.

The green FPGA_DONE LED indicates successful FPGA configuration. The red front-plate LED indicates that the FPGA is not configured with a valid bitstream (Out-of-Service indication).

Please note that the TAMC651 is shipped with blank FPGA configuration memory devices, so the red LED will be lit on the first installation.

8.1.2 AMC Extraction

Typical Extraction sequence:

1. Pull the module handle out ½ way
    a. Blue LED starts “Short Blink” (Hot Swap Negotiation in progress)
    b. Blue LED turns “ON” (Module is ready to be extracted)
2. Pull the module handle out completely and extract the AMC module from the slot.

8.2 µRTM Module Installation

8.2.1 µRTM Insertion

1. Make sure that the TAMC651 (front AMC) is fastened to the MTCA.4 system
2. Simply insert the µRTM into the MTCA.4 system (slot must match for the front AMC) and fasten the µRTM to the MTCA.4 system
3. Close the µRTM Hot-Swap handle (if not already closed right from the start)
4. Wait until the blue Hot-Swap LED goes off and the green LED goes on

If the blue Hot-Swap LED stays active and the green LED stays off, the µRTM has been considered as incompatible to the TAMC651 (e.g. missing FRU information in µRTM EEPROM)

8.2.2 µRTM Extraction

1. Normal Operating (green LED is on, blue Hot-Swap LED is off)
2. Pull the µRTM Hot-Swap handle
3. Wait until the green LED goes off and the blue Hot-Swap LED shows activity
4. Wait until the blue Hot-Swap LED is permanently on
5. Unfasten the µRTM from the MTCA.4 system
6. Pull the µRTM from the MTCA.4 system (handle still pulled)

9 Board-I/O

This chapter provides information about board I/O like LEDs, DIP-Switches, Headers and Connectors.

9.1 Overview

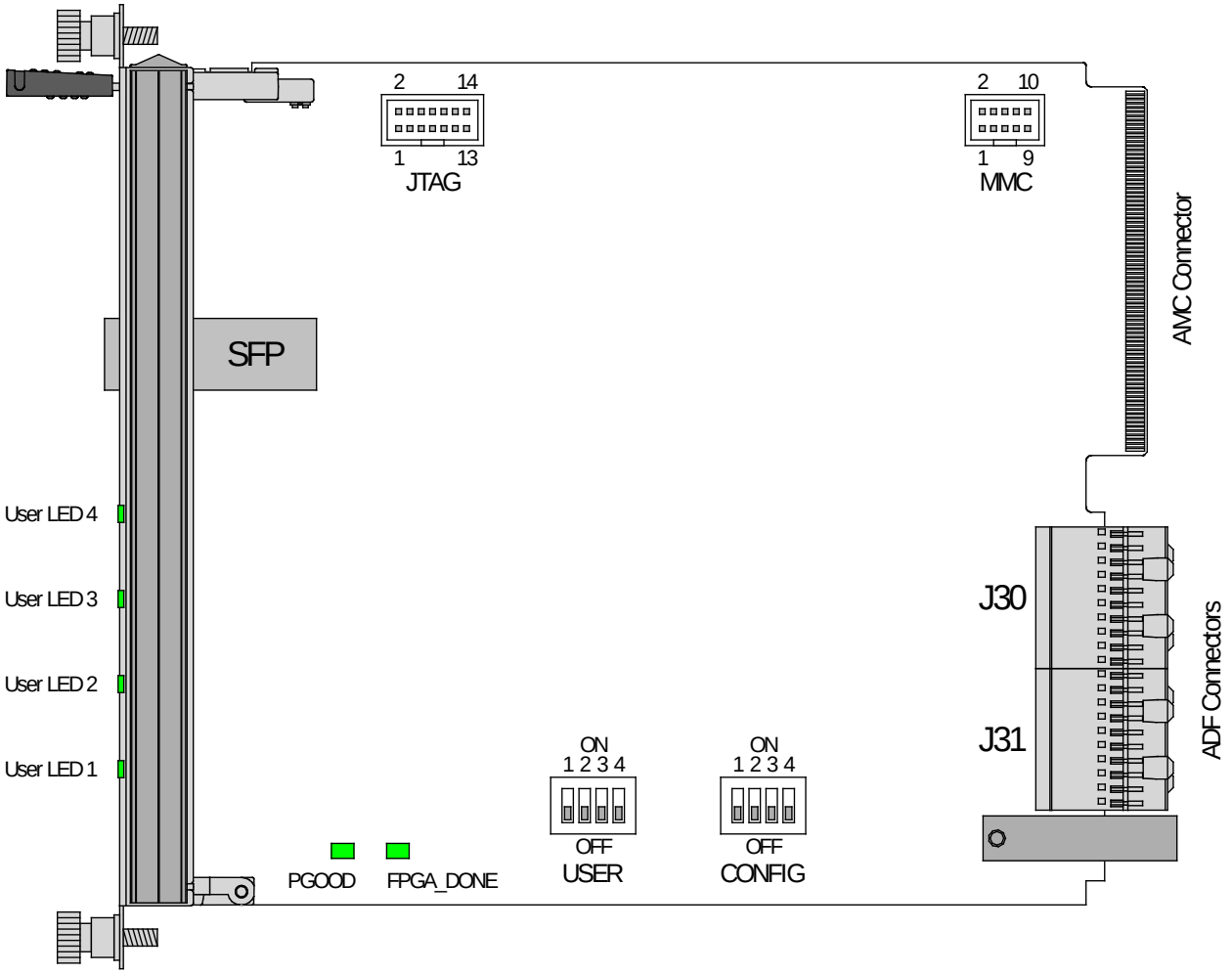


Figure 9-1 : Board I/O Overview

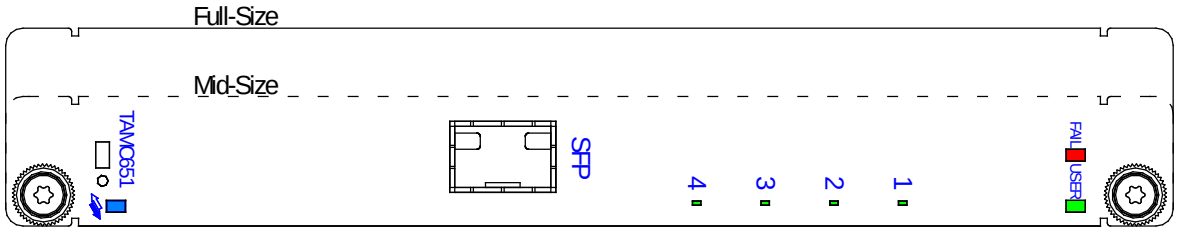


Figure 9-2 : Front Panel View

9.2 LEDs

9.2.1 Front-Plate User LEDs

LED	Color	State	Description
HS	**Blue**	**Off**	**No Power or Module is ready for normal operation**
		Short Blink	**Hot-Swap negotiation (extraction)**
		Long Blink	**Hot-Swap negotiation (insertion)**
		On	**Module is ready to attempt activation by the system or Module is ready to be extracted**
FAIL	**Red**	**Off**	**No fault**
		On	**Failure or out of service status**
USER	**Green**	**Off**	**FPGA Design dependent**
		On	
		Blink	

Table 9-1 : Front Panel LEDs (AMC.0)

As long as the FPGA is not configured with a valid bitstream, this is considered as an out of service status (FAIL LED = ON).

The TAMC651 is shipped with blank FPGA configuration memory devices, hence the FAIL LED defaults to the ON state for the first installation.

The front-plate user LEDs are controlled by the user FPGA application.

User LED	Color	FPGA				
		Bank	Pin	I/O Std.	Dir	Control
1	**green**	**3 (VCCO 1.5V)**	**V3**	**LVCMOS15**	**Out**	**0: LED Off (default by on-board pulldown resistor) 1: LED On**
2			**P5**			
3			**P4**			
4			**AA2**			

Table 9-2 : Front Panel User LEDs

9.2.2 On-board Status LEDs

Status LED	Color	Description
PGOOD	green	On if Power Good status is detected for all the following on-board power supplies: 1.2V, GTP_1.2V, 1.5V, 2.5V, 3.3V. Off otherwise.
FPGA_DONE		On if FPGA DONE output is high (FPGA has been configured with a valid bitstream) Off otherwise.

Table 9-3 : On-board Status LEDs

9.3 DIP Switches

9.3.1 User DIP-Switch

Switch	FGPA				
	Bank	Pin	I/O Std.	Dir	Status
1	3 (VCCO_3) (1.5V)	Y3	LVCMOS15	In	0: Switch is Off 1: Switch is On
2		T6			
3		T5			
4		V5			

Table 9-4 : User DIP-Switch

9.3.2 Configuration DIP-Switch

Switch	On	Off (default)
1	FPGA configuration data path set to SPI Flash	FPGA configuration data path set to Platform Flash
2	Force bypassing the µRTM JTAG Chain (even if the µRTM interface is enabled by the MMC)	Include µRTM JTAG Chain (if the µRTM interface is enabled by the MMC)
3	The PCIe REFCLK at the FPGA GTP Reference Clock Input is 1:1 FCLKA (100 MHz)	The PCIe REFCLK at the FPGA GTP Reference Clock Input is FCLKA (100 MHz) Multiplied by 5:4 (125 MHz)
4	Reserved	

Table 9-5 : Configuration DIP-Switch

9.4 Header

9.4.1 MMC Header

The dedicated MMC JTAG/ISP Header is for factory use only (MMC Firmware updates).

Pin-Count	**10**
Connector Type	**10-pin 2mm box header**
Source & Order Info	**K39010005** **(Molex 87832-1020)**

Pin	Signal	Description
1	**TCK**	**Test Clock**
2	**GND**	**Ground**
3	**TDO**	**Test Data Output (TAP Controller: TDI)**
4	**VT_{REF}**	**Reference Voltage**
5	**TMS**	**Test Mode Select Input**
6	**nSRST**	**MMC RESET#**
7	**n.c.**	**Connected to MP**
8	**nTRST**	**Connected to PENABLE#**
9	**TDI**	**Test Data Input (TAP Controller: TDO)**
10	**GND**	**Ground**

Table 9-6 : MMC Header

9.4.2 JTAG Header

The pinout of the JTAG chain header matches the pinout of the Xilinx Platform Cable USB II. This allows the direct usage of Xilinx software-tools like Chipscope or iMPACT with the Platform Cable USB II.

Pin-Count	**14**
Connector Type	**14-pin 2mm box header**
Source & Order Info	**K39014005** **(Molex 87832-1420)**

Pin	Signal	Description
1	**NC**	**Not Connected**
2	**V_{REF}**	**JTAG Reference Voltage (3.3V)**
3	**GND**	**Ground (Programmer Detect)**
4	**TMS**	**Test Mode Select Input**
5	**GND**	**Ground**
6	**TCK**	**Test Clock**
7	**GND**	**Ground**

Pin	Signal	Description
8	**TDO**	**Test Data Output (TAP Controller: TDI)**
9	**GND**	**Ground**
10	**TDI**	**Test Data Input (TAP Controller: TDO)**
11	**GND**	**Ground**
12	**NC**	**Not Connected**
13	**NC**	**Not Connected**
14	**NC**	**Not Connected**

Table 9-7 : JTAG Header

9.5 Debug Connector

Pin-Count	**20**
Connector Type	**20-pin, 1mm FPC (Flexible Printed Circuit) Connector**
Source & Order Info	**K39060207** **(AMP 2-487951-0 / 2-84953-0)** **(Molex 0522072060)**

Mating Flexible Printed Circuits: 20 mm (isolated length):
Adapt-Elektronik, 280-1.0-B-20-200-5-5-10-10)

Pin	Signal	**Description**
1	**DBG_PRSNT#**	**External Debug Hardware is connected / present**
2	**JTAG_VIO**	**JTAG Reference I/O Voltage (+3.3V)**
3	**TDO**	**JTAG Chain Test Data Output**
4	**GND**	**Ground**
5	**TDI**	**JTAG Chain Test Data Input**
6	**TMS**	**JTAG Chain Test Mode Select Input**
7	**GND**	**Ground**
8	**TCK**	**JTAG Chain Test Clock**
9	**GND**	**Ground**
10	**UART_RX**	**FPGA UART Receive Data**
11	**UART_VIO**	**FPGA UART Reference I/O Voltage (+2.5V)**
12	**UART_TX**	**FPGA UART Transmit Data**
13	**GND**	**Ground**
14	**MMC_RX**	**MMC UART Receive Data**
15	**MMC_VIO**	**MMC UART Reference I/O Voltage (MP)**
16	**MMC_TX**	**MMC UART Transmit Data**
17	**GND**	**Ground**

Pin	Signal	Description
18	**3.3V**	**+3.3 Volt**
19	**USER_VIO**	**User signal Reference I/O Voltage (+1.5V)**
20	**USER#**	**User signal connected to the FPGA. A weak Pullup (app. 10k) is located on the TAMC651**

Table 9-8 : Debug Connector

The TAMC651 debug connector is compatible with the TEWS Technologies TA900 Program and Debug Box.

9.6 AMC Interface

9.6.1 Connector Type

Pin-Count	170
Connector Type	AMC-Connector
Source & Order Info	Harting: ECPI0612001001

9.6.2 Pin Assignment

Ground Pins are not shown.

Pin	AMC.0 Signal	Signal Group	TAMC651 Usage
2	PWR	Power	Payload Power
3	PS1#	Management	Present Detection
4	MP	Power	Management Power
5	GA0	Management	Geographical Addressing
6	RSRVD6	Reserved	Not used / Not supported
8	RSRVD8		
9	PWR	Power	Payload Power
11	Tx0+	Port 0	Not used / Not supported
12	Tx0-		
14	Rx0+		
15	Rx0-		
17	GA1	Management	Geographical Addressing
18	PWR	Power	Payload Power
20	Tx1+	Port 1	Not used / Not supported
21	TX1-		
23	Rx1+		
24	Rx1-		
26	GA2	Management	Geographical Addressing
27	PWR	Power	Payload Power

Pin	AMC.0 Signal	Signal Group	TAMC651 Usage
29	Tx2+	Port 2	Not used / Not supported
30	Tx2-		
32	Rx2+		
33	Rx2-		
35	Tx3+	Port 3	Not used / Not supported
36	Tx3-		
38	Rx3+		
39	Rx3-		
41	ENABLE#	Management	Management Signal
42	PWR	Power	Payload Power
44	Tx4+	Port 4	PCIe x1 Link Spartan-6 PCIe Endpoint Block
45	Tx4-		
47	Rx4+		
48	Rx4-		
50	Tx5+	Port 5	Not used / Not supported
51	Tx5-		
53	Rx5+		
54	Rx5-		
56	SCL_L	Management	IPMB-L (Clock)
57	PWR	Power	Payload Power
59	Tx6+	Port 6	Not used / Not supported
60	Tx6-		
62	Rx6+		
63	Rx6-		
65	Tx7+	Port 7	Not used / Not supported
66	Tx7-		
68	Rx7+		
69	Rx7-		
71	SDA_L	Management	IPMB-L (Data)
72	PWR	Power	Payload Power
74	TCLKA+	TCLKA	Connected to Clock Switch Input
75	TCLKA-		
77	TCLKB+	TCLKB	Connected to Clock Switch Input
78	TCLKB-		
80	FCLKA+	FCLKA	PCIe Reference Clock. Connects to FPGA GTP via PCIe Jitter Attenuator.
81	FCLKA-		
83	PS0#	Management	Present Detection
84	PWR	Power	Payload Power

Pin	AMC.0 Signal	Signal Group	TAMC651 Usage
87	Rx8-	Port 8	Not used / Not supported
88	Rx8+		
90	Tx8-		
91	Tx8+		
93	Rx9-	Port 9	Not used / Not supported
94	Rx9+		
96	Tx9-		
97	Tx9+		
99	Rx10-	Port 10	Not used / Not supported
100	Rx10+		
102	Tx10-		
103	Tx10+		
105	Rx11-	Port 11	Not used / Not supported
106	Rx11+		
108	Tx11-		
109	Tx11+		
111	Rx12-	Port 12	Connected to FPGA via M-LVDS transceiver 100R on-board termination resistors for the differential pairs
112	Rx12+		
114	Tx12-		
115	Tx12+		
117	Rx13-	Port 13	Connected to FPGA via M-LVDS transceiver 100R on-board termination resistors for the differential pairs
118	Rx13+		
120	Tx13-		
121	Tx13+		
123	Rx14-	Port 14	Connected to FPGA via M-LVDS transceiver 100R on-board termination resistors for the differential pairs
124	Rx14+		
126	Tx14-		
127	Tx14+		
129	Rx15-	Port 15	Connected to FPGA via M-LVDS transceiver 100R on-board termination resistors for the differential pairs
130	Rx15+		
132	Tx15-		
133	Tx15+		
135	TCLKC-	TCLKC	Not used / Not supported
136	TCLKC+		
138	TCLKD-	TCLKD	Not used / Not supported
139	TCLKD+		
141	Rx17-	Port 17	Connected to FPGA via M-LVDS transceiver
142	Rx17+		

Pin	AMC.0 Signal	Signal Group	TAMC651 Usage
144	Tx17-		No on-board termination resistors
145	Tx17+		
147	Rx18-	Port 18	Connected to FPGA via M-LVDS transceiver No on-board termination resistors
148	Rx18+		
150	Tx18-		
151	Tx18+		
153	Rx19-	Port 19	Connected to FPGA via M-LVDS transceiver No on-board termination resistors
154	Rx19+		
156	Tx19-		
157	Tx19+		
159	Rx20-	Port 20	Connected to FPGA via M-LVDS transceiver No on-board termination resistors
160	Rx20+		
162	Tx20-		
163	Tx20+		
165	TCK	JTAG	JTAG Chain signals
166	TMS		
167	TRTS#		
168	TDO		
169	TDI		

Table 9-9 : AMC Connector Pin Assignment

9.7 SFP Interface

9.7.1 Connector Type

Pin-Count	20
Connector Type	SFP Connector
Source & Order Info	Molex 74441-0001 (or compatible)

9.7.2 Pin Assignment

Pin	Signal	Signal Description	TAMC651
1	**VeeT**	**Transmitter Ground**	**Ground**
2	**Tx Fault**	**Transmitter Fault Indication**	**FPGA I/O (input)**
3	**Tx Disable**	**Transmitter Disable**	**FPGA I/O (output)**
4	**MOD-DEF(2)**	**Module Definition 2 (SFP 2-wire data)**	**FPGA I/O (inout)**
5	**MOD-DEF(1)**	**Module Definition 1 (SFP 2-wire clock)**	**FPGA I/O (output)**

6	MOD-DEF(0)	Module Definition 0 (SFP present)	FPGA I/O (input)
7	Rate Select	Receiver Bandwidth Select	FPGA I/O (output)
8	LOS	Loss Of Signal	FPGA I/O (input)
9	VeeR	Receiver Ground	Ground
10	VeeR	Receiver Ground	Ground
11	VeeR	Receiver Ground	Ground
12	RD-	Receive Data Output-	FPGA GTP receiver
13	RD+	Receive Data Output+	
14	VeeR	Receiver Ground	Ground
15	VccR	Receiver Power	3.3V (/w filter)
16	VccT	Transmitter Power	3.3V (/w filter)
17	VeeT	Transmitter Ground	Ground
18	TD+	Transmit Data Input+	FPGA GTP transmitter
19	TD-	Transmit Data Input-	
20	VeeT	Transmitter Ground	Ground

Table 9-10: SFP Connector Pin Assignment

9.8 Zone 3 Interface

9.8.1 Zone 3 Mechanical Keying

The TAMC651 provides a female Zone 3 mechanical key as shown below.

The part number used is Tyco 5223986-1.

N	A Rotation in degrees	View	Voltage Levels
1	0	 View from the µRTM to the rear of the AMC white = clearance	LVDS

Table 9-11: Zone 3 Mechanical Keying

The µRTM must provide a matching male (plug) keypin!

9.8.2 Connector Type

The TAMC651 provides two 30-pair ADF connectors (J30 and J31) at the Zone 3 Interface.

Pin-Count	30 contact pairs (60 signal contacts) + 30 GND pins
Connector Type	Advanced Differential Fabric (ADF) connector
Source & Order Info	Erni: 973028

9.8.3 Pin Assignment

ADF connector ground pins are not shown.

	F	E	D	C	B	A
1	RTM_TDO	RTM_TCK	RTM_SDA	RTM_PS#	RTM_PWR	RTM_PWR
2	RTM_TMS	RTM_TDI	RTM_SCL	RTM_MP	RTM_PWR	RTM_PWR
3	DP_01-	DP_01+	DP_00-	DP_00+	RTM_CLK0-	RTM_CLK0+
4	DP_04-	DP_04+	DP_03-	DP_03+	DP_2-	DP_02+
5	DP_07-	DP_07+	DP_06-	DP_06+	DP_5-	DP_05+
6	DP_10-	DP_10+	DP_09-	DP_09+	DP_8-	DP_08+
7	DP_13-	DP_13+	DP_12-	DP_12+	DP_11-	DP_11+
8	DP_16-	DP_16+	DP_15-	DP_15+	DP_14-	DP_14+
9	DP_19-	DP_19+	DP_18-	DP_18+	DP_17-	DP_17+
10	DP_22-	DP_22+	DP_21-	DP_21+	DP_20-	DP_20+

Table 9-12: J30 Connector Pin Assignment

	F	E	D	C	B	A
1	DP_25-	DP_25+	DP_24-	DP_24+	DP_23-	DP_23+
2	DP_28-	DP_28+	DP_27-	DP_27+	DP_26-	DP_26+
3	DP_31-	DP_31+	DP_30-	DP_30+	DP_29-	DP_29+
4	DP_34-	DP_34+	DP_33-	DP_33+	DP_32-	DP_32+
5	DP_37-	DP_37+	DP_36-	DP_36+	DP_35-	DP_35+
6	DP_40-	DP_40+	DP_39-	DP_39+	DP_38-	DP_38+
7	DP_43-	DP_43+	DP_42-	DP_42+	DP_41-	DP_41+
8	RTM_CLK1-	RTM_CLK1+	DP_45-	DP_45+	DP_44-	DP_44+
9	GTP0_DAT_A2R-	GTP0_DAT_A2R+	GTP0_DAT_R2A-	GTP0_DAT_R2A+	GTP0_CLK0_R2A-	GTP0_CLK0_R2A+
10	GTP1_DAT_A2R-	GTP1_DAT_A2R+	GTP1_DAT_R2A-	GTP1_DAT_R2A+	GTP1_CLK1_R2A-	GTP1_CLK1_R2A+

Table 9-13: J31 Connector Pin Assignment

The following Zone 3 interface differential signals are connected to FPGA global clock pins:

- RTM_DP[15]
- RTM_DP[16]
- RTM_DP[33]

See Requirements for compatible µRTM Designs / User Signals / General I/O Signals / Clock and Data Signal Planning for details.

9.8.4 Signal Description

A2R: from-AMC-to-RTM (unidirectional)

R2A: from-RTM-to-AMC (unidirectional)

Signal	Direction	Level	Description
RTM_MP	A2R	3.3V	Management Power Enabled by AMC upon µRTM present detection
RTM_PS#	R2A	0V…3.3V	µRTM present detection. Connected to ground on the µRTM. MP (3.3V) pullup resistor on AMC.
RTM_PWR	A2R	10V…14V	Payload Power Enabled by AMC during insertion process (successful compatibility check required)
RTM_TMS	A2R	3.3V	JTAG Mode Signal
RTM_TCK	A2R	3.3V	JTAG Clock Signal
RTM_TDI	A2R	3.3V	JTAG Data (start of µRTM JTAG Chain)
RTM_TDO	R2A	3.3V	JTAG Data (end of µRTM JTAG Chain)
RTM_SCL	A2R	3.3V	I2C Management Bus Clock
RTM_SDA	I/O	3.3V	I2C Management Bus Data
RTM_CLK0+/-	A2R	LVDS	Differential Reference Clock 0 From AMC Clock Crosspoint Switch to µRTM.
RTM_CLK1+/-	A2R	LVDS	Differential Reference Clock 1 From AMC Clock Crosspoint Switch to µRTM.
DP[45:00] (DP[45:00]_P & DP[45:00]_N)	I/O	LVDS or 2.5V (3.3V input option)	Single-Ended or Differential I/O Connected to Spartan-6 FPGA I/O Banks 0 & 2
GTP0_CLK_R2A+/-	R2A	LVDS	RTM GTP0 Reference Clock (differential)
GTP0_DAT_R2A+/-	R2A	LVDS	RTM GTP0 Receive Data (differential)
GTP0_DAT_A2R+/-	A2R	LVDS	RTM GTP0 Transmit Data (differential)
GTP1_CLK_R2A+/-	R2A	LVDS	RTM GTP1 Reference Clock (differential)
GTP1_DAT_R2A+/-	R2A	LVDS	RTM GTP1 Receive Data (differential)
GTP1_DAT_A2R+/-	A2R	LVDS	RTM GTP1 Transmit Data (differential)

Table 9-14: Zone 3 Interface Signal Description

9.8.5 Quiescence Actions

Notes regarding Quiescence Actions for Zone 3 interface signals.

Spartan-6 GTP transceiver signals

There is no quiescence action for the GTP transceiver signals on the AMC. The transmit signals may always be driven by the FPGA.

The AMC provides AC coupling capacitors for the transmit, receive and reference clock differential pair signals of the GTP transceivers.

Spartan-6 I/O signals

The MMC drives a Zone 3 Interface Enable signal to one of the FPGA I/O pins. The FPGA application may use this signal to Tri-State I/O signals mapped to the Zone 3 interface.

There is no further quiescence action for the Spartan-6 I/O signals connected to the Zone 3 interface.

Clock Crosspoint-Switch signals

There is no quiescence action for the two clock signals driven by the AMCs clock crosspoint-switch to the µRTM. These clock signals are always driven by the AMC (while the AMC payload power is enabled), even when the µRTM payload power is not enabled.

There are no AC coupling capacitors for these lines on the AMC.

JTAG signals

JTAG signals are driven by the AMC while the µRTM is present and µRTM payload power is enabled.

There is no quiescence action for the JTAG signals.

9.8.6 AC Coupling

The AMC provides AC coupling for the GTP transceiver transmit, receive and reference clock signals.

There is no AC coupling on the AMC for the other Zone 3 interface signals.

10 Requirements for Compatible µRTM Designs

This chapter is intended for designers of TAMC651 compatible µRTM's.

10.1 Management Functions

10.1.1 General Notes

The TAMC651 provides the following µRTM related management signals at the Zone 3 (µRTM) interface:

Signal	Description
GND	**Ground**
RTM_PS#	**µRTM present status (input for AMC)**
RTM_MP	**µRTM Management Power (gated AMC MP)**
RTM_SCL, RTM_SDA	**µRTM I2C Management Bus**
RTM_PWR	**µRTM Payload Power (gated AMC PWR)**
RTM _TCK, RTM _TMS, RTM_TDI, RTM _TDO	**µRTM JTAG Chain Signals 3.3V Level (supplied by Payload Power)**

Table 10-1: µRTM Management Signals at the Zone 3 Interface

Other µRTM management functions are handled via the Zone 3 interface I2C management bus (i.e. via an I2C I/O Extender device on the µRTM).

The TAMC651 MMC firmware supports the following additional µRTM management signals handled via the µRTM I2C management bus:

Signal/Description
Hot Swap Handle Status
Blue Hot Swap LED Enable/Disable Control
LED1 (red) Enable/Disable Control
LED2 (green) Enable/Disable Control
EEPROM Write Protect Control (not recommended)
µRTM Payload Power Good Status
µRTM Payload Reset Control
µRTM Payload Enable/Disable Control

Table 10-2: Supported µRTM Management Signals via I2C

10.1.2 Present Detection

The µRTM must connect the RTM_PS# signal to the ground signal.

The TAMC651 provides a pullup resistor (to the AMC-MP power supply rail) on the RTM_PS# signal.

Note: The TAMC651 monitors the RTM_PS# signal for µRTM module present detection. The TAMC651 will gate the AMC Management Power to the µRTM upon µRTM present detection.

10.1.3 Power Good Detection

The µRTM must provide a kind of overall Payload Power Good signal.

See I2C I/O Extender section for additional information.

10.1.4 JTAG Signals

The TAMC651 provides 3.3V level JTAG signals at the Zone 3 Interface.

The µRTM module must not break the JTAG chain. If the µRTM module does not use JTAG, RTM_TDI must be connected to RTM_TDO on the µRTM module.

The JTAG signals at the Zone 3 Interface are not powered by the management power supply, but by the AMC 3.3V payload power supply.

The JTAG signals (except TDO) will be driven by the TAMC651 when all of the following is true:

- The µRTM is present
- The AMC has enabled payload power to the µRTM (µRTM is compatible)
- The AMC has set the ZONE3_EN signal (local signal on AMC)

The µRTM must provide means for safe JTAG signal levels during the time the µRTM JTAG devices are not powered properly. A pulldown resistor on TCK and a pullup resistor on TMS are recommended.

10.1.5 I2C Management Bus

(Only) The following I2C devices / addresses must be present on the µRTM I2C management bus.

Device	Supported Devices	I2C Address	
EEPROM	AT24C32 or compatible	50h	1010000b
Temperature Sensor	LM75 or compatible	48h	1001000b
8-bit I2C I/O Port	PCA9534 or compatible	20h	0100000b

Table 10-3: Supported µRTM I2C Devices

Other I2C devices or addresses are not supported and are also not allowed.

The TAMC651 reserves the following I2C addresses for the AMC board: 70h (1110000), 71h (1110001).

All devices on the µRTM modules I2C management bus must be powered by the RTM_MP power supply.

MTCA.4 limits the total current for the RTM_MP power supply to 30mA. This must be taken into account for the µRTM hardware design (LEDs etc.).

The µRTM must provide pullup resistors to RTM_MP on the I2C 2-wire signals.

10.1.5.1 EEPROM

The µRTM must provide a serial EEPROM on the I2C management bus (AT24C32 or compatible).

The EEPROM I2C address must be 50h (1010000b).

The EEPROM must contain FRU information for the µRTM module.

The EEPROM must be powered by the RTM_MP power supply.

10.1.5.2 Temperature Sensor

The µRTM must provide a temperature sensor on the I2C management bus, as defined below.

The Temperature Sensor must be powered by the RTM_MP power supply.

A LM75 or compatible device with I2C address 48h (1001000b) must be used.

10.1.5.3 I2C I/O Extender

The µRTM must provide an 8-bit I2C I/O Extender device on the I2C management bus used for controlling certain management signals on the µRTM.

The I2C I/O device must be powered by the RTM_MP power supply.

A PCA9534 or compatible device with I2C address 20h (0100000b) must be used.

The TAMC651 supports the following pin/signal assignment for the µRTM I2C I/O Extender device:

I/O Port	I/O Direction	Description
7	I	Payload Power Supply Status 0 = Payload Power Supply status is not Good 1 = Payload Power Supply status is Good
6	O	Payload (Zone 3) Enable Control 0 = Payload Enable signal not active 1 = Payload Enable signal active Intended for Zone 3 interface and other I/O driver enable/disable control.
5	O	Payload Reset Control 0 = Payload Reset signal not active 1 = Payload Reset signal active
4	O	EEPROM Write Protect Control 0 = EEPROM write protection not active 1 = EEPROM write protection active Using this pin is not recommended. See note below.
3	O	LED2 (Green) Control 0 = LED off

		1 = LED on
2	O	LED1 (Red) Control 0 = LED off 1 = LED on
1	O	Hot Swap LED (Blue) Control 0 = LED off 1 = LED on
0	I	Handle Status 0 = Handle/Switch closed 1 = Handle/Switch open

Table 10-4: µRTM I2C I/O Extender Port Assignment

Notes:

(1) Per default (after power-up) all the I2C I/O ports are inputs. External circuitry on the µRTM must ensure the proper function according to the µRTM I2C I/O Extender Port Assignment. E.g. the µRTM board logic must ensure that the Blue Hot Swap LED defaults to the ON state and that LED1 and LED2 default to the OFF state. Therefore the Blue Hot Swap LED should not be connected directly to the I2C I/O port. In general it is recommended to use external LED drivers (controlled by the I2C I/O ports). It is also recommended that the reset signal defaults to the active state and the enable signal defaults to the not-active state. Please see the following example adding a single 74LVC06-type device (6x Inverter with open drain output).

(2) Usually the EEPROM on the µRTM I2C Management Bus provides an input pin for Write Control/Protection. It is recommended to provide some mechanism on the µRTM to control this pin independently from the front AMC/MMC, e.g. a jumper that provides EEPROM write protection when open and supports EEPROM writes when closed. This would make it more convenient to program an empty µRTM EEPROM (thus an incompatible µRTM) per IPMI commands.

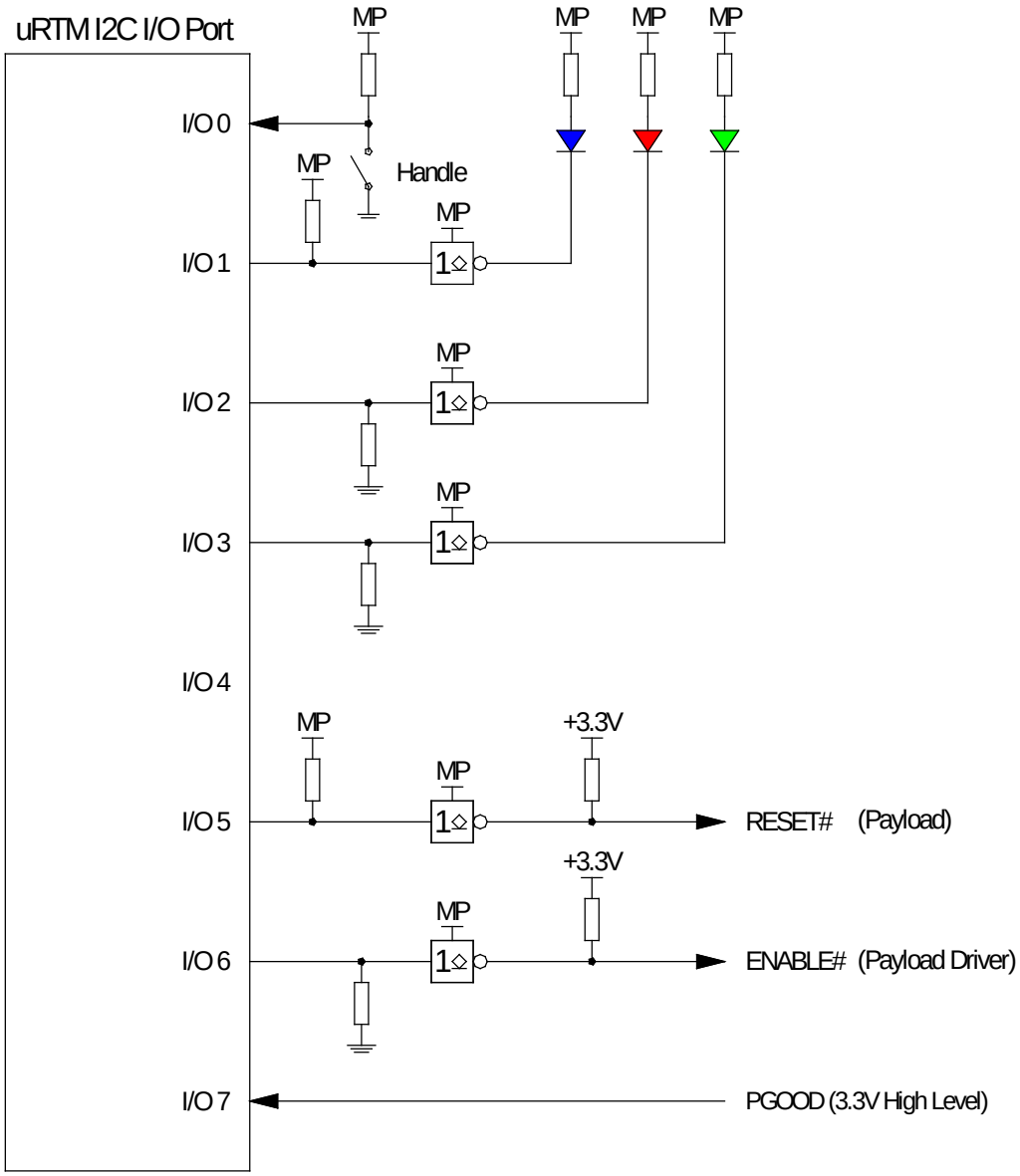


Figure 10-1: Example I2C I/O Extender Interface on µRTM

10.1.6 µRTM FRU Information Requirements

The EEPROM on the µRTM I2C bus must contain FRU information data for the µRTM.

The µRTM FRU information must include:

- Common Header
- Zone 3 Interface Compatibility Record (Multi-Record Area)

The µRTM FRU information may optionally include:

- Board Info Area
- Product Info Area

10.1.6.1 Common Header

The µRTM FRU information (Common Header) must start at EEPROM address 0h.

Offset	Length	Description
0	1	Common Header Format Version [7:4] Reserved. Write as 0h. [3:0] Format Version Number (Value 1h)
1	1	Internal Use Area Starting Offset (in multiples of 8 bytes) 00h indicates that this area is not present.
2	1	Chassis Info Area Starting Offset (in multiples of 8 bytes) 00h indicates that this area is not present.
3	1	Board Info Area Starting Offset (in multiples of 8 bytes) 00h indicates that this area is not present.
4	1	Product Info Area Starting Offset (in multiples of 8 bytes) 00h indicates that this area is not present.
5	1	Multi-Record Area Starting Offset (in multiples of 8 bytes) 00h indicates that this area is not present.
6	1	Value 00h
7	1	Common Header Checksum (zero checksum)

Table 10-5: µRTM FRU Common Header

10.1.6.2 Zone 3 Interface Compatibility Record

In the Multi-Record Area, the µRTM module must only provide the Zone 3 Interface Compatibility Record, defined as follows.

Offset	Length	Description	Value (Hex)
0	1	Record Type ID Value C0h (OEM)	C0
1	1	[7:7] End of list. Set to one for the last record. [6:4] Reserved. Write as 0h. [3:0] Record format version (2h for this definition)	82
2	1	Record Length	0D
3	1	Record Checksum Holds the zero checksum of the record	E0
4	1	Header Checksum Holds the zero checksum of the header	D1
5	3	Manufacturer ID For MTCA.4 the value is 12634 = 0x00315A, LSB first	5A
6			31
7			00
8	1	PICMG Record ID Value 30h	30
9	1	Record Format Version	01

		Value 01h	
10	1	Type of Interface Identifier 03h = OEM interface identifier	03
11	3	Interface Identifier Body Manufacturer ID (IANA) of the OEM that owns the definition of the interface. LS Byte first. 0x0071E3 (TEWS Technologies Private Enterprise Number)	E3
12			71
13			00
14	4	Interface Identifier Body OEM-defined interface designator, 32 bits, LS Byte first 0x828B0000 (0x8 = TAMC, 0x28B = 651)	00
15			00
16			8B
17			82

Table 10-6: Zone 3 Interface Compatibility Record

If the Zone 3 Interface Compatibility record in the µRTM FRU information matches the Zone 3 Interface Compatibility record shown, the TAMC651 considers the µRTM to be compatible. Otherwise the TAMC651 considers the µRTM to be incompatible.

10.1.6.3 Sensor Data Records (SDR)

The TAMC651 MMC provides a SDR for one (mandatory) LM75 temperature sensor located on the µRTM. This pre-configured SDR is kept in the EEPROM of the AMCs MMC.

Parameter	Temperature-Level
Nominal Reading	**25°C**
Normal Maximum	**70°C**
Normal Minimum	**0°C**
Sensor Maximum Reading	**125°C**
Sensor Minimum Reading	**-55°C**
Upper Critical Threshold	**85°C**
Upper Non-Critical Threshold	**75°C**
Lower Critical Threshold	**-40°C**
Lower Non-Critical Threshold	**-30°C**

Table 10-7: Pre-configured µRTM Temperature Sensor

At this time, the TAMC651 MMC firmware does not support any SDR data stored in the µRTM I2C EEPROM.

10.2 User Signals

10.2.1 General I/O Signals

The Zone 3 interface provides 46 differential user signal pairs (RTM_DP[45:00]) directly connected to FPGA bank 0 (RTM_DP[16:00]) and bank 2 (RTM_DP[45:17]). The two wires of a differential pair may also be used as single-ended signals on the FPGA (RTM_DP[x]_P, RTM_DP[x]_N).

FPGA banks 0 and 2 have a bank supply voltage of 2.5V.

For the µRTM design, special care must be taken regarding attaching digital interfaces to the FPGA I/O pins.

For the µRTM design, special care must be taken regarding clock and data signal planning.

Please see the following sub-chapters.

10.2.1.1 Attaching digital interfaces

Differential Signals

The RTM_DP[45:00] differential pair signals on the Zone 3 interface support LVDS as FPGA input and output.

LVDS signals on the µRTM could be directly connected to the RTM_DP[45:00] lines. The RTM_DP[45:00]_P lines are for the “positive signal” and the RTM_DP[45:00]_N lines are for the “negative signal” of a differential pair.

FPGA I/O standard LVDS_25 must be used.

Single-Ended Signals

When used as an FPGA output or in/out pin, FPGA I/O standard LVCMOS25 must be used.

When used as FPGA input only, FPGA I/O standard LVTTL may be used as well.

The following table shows the Spartan-6 DC Characteristics for the LVCMOS25 and LVTTL I/O standard.

FPGA LVCMOS25 Input	
$V_{IL\ max}$	0.7V
$V_{IH\ min}$	1.7V
$V_{IH\ max}$	3.95V
FPGA LVCMOS25 Output	
$V_{OL\ max}$	0.4V (for up to 16mA)
$V_{OH\ min}$	2.1V (for up to 16mA)
$V_{OH\ max}$	approx. 2.5V
FPGA LVTTL Input	
$V_{IL\ max}$	0.8V
$V_{IH\ min}$	2.0V
$V_{IH\ max}$	3.95V

Table 10-8: Spartan-6 LVCMOS25 & LVTTL DC Characteristics

Attached single-ended digital interfaces must support the DC characteristics shown!

Please check the µRTM device DC characteristics accordingly!

Typically the following applies:

µRTM devices with a 1.8V digital interface

Connecting signals of a µRTM device with a 1.8V digital interface may require using a voltage translator device on the µRTM.

Unidirectional signals from an FPGA output to a µRTM device input may work with a direct connection (provided the device tolerates a max high level of 2.5V). **Please check the µRTM device DC characteristics!**

A simple way of cutting the max high level from an FPGA output (with almost zero delay) would be using a 2.5V to 1.8V level translator bus switch (e.g. ADG3241).

For unidirectional signals from the µRTM to the FPGA and bidirectional signals a voltage translator device on the µRTM is recommended.

µRTM devices with a 2.5V digital interface

Typically an FPGA pin operating in the LVCMOS25 I/O standard could be directly connected to µRTM devices with a 2.5V digital interface. **Please check the µRTM device DC characteristics!**

µRTM devices with a 3.3V digital interface

Typically unidirectional signals from a 3.3V µRTM device output could be directly connected to the FPGA input pin. **Please check the µRTM device DC characteristics!**

Unidirectional signals from an FPGA output to a µRTM device input and bidirectional signals may require a voltage translator device on the µRTM. 3.3V digital interfaces with LVTTL compatible input levels may work with a direct FPGA pin connection. **Please check the µRTM device DC characteristics!**

10.2.1.2 Clock and Data Signal Planning

Normally for high-speed I/O implementations the data signals and the associated clock signal must reside in the same FPGA clock region.

The following table shows how the Zone 3 interface user I/O signals are mapped to the FPGA clock regions.

FPGA Bank	FPGA Region	Zone 3 Interface Differential Pair (Data Signals)	Remarks
0	TL	RTM_DP[16, 07:00]	Matched routing length per bank
	TR	RTM_DP[15:08]	
2	BL	RTM_DP[33:17]	Matched routing length per bank
	BR	RTM_DP[45:34]	

Table 10-9: Zone 3 Interface User Signals

The following Zone 3 interface differential signals are connected to FPGA global clock pins:

RTM_DP[15], RTM_DP[16] and RTM_DP[33]

Both the P and N line of these differential pairs are connected to FPGA global clock pins, so these signals could be used as differential or single-ended clock signals but could be used as regular data signals as well.

RTM_DP[33] located in FPGA bank 2 region BL does not need to share regional clock buffers with any GTP resources and is therefore recommended for highest performance requirements (e.g. DDR clock signals from the Zone 3 interface).

RTM_DP[15] and RTM_DP[16] located in FPGA bank 0 share regional clock buffers with FPGA internal GTP resources. The limited number of regional clock buffers in FPGA bank 0 needs to be balanced between required internal GTP resources and the global clock pins. For more details, please see the “User Programmable FPGA” chapter in this manual and the Xilinx “Clocking Resources User Guide” (UG382).

The following table shows a simplified recommendation regarding the use of the Zone 3 interface signals.

	FPGA Bank	FPGA Clock Region	Zone 3 Interface Data Signals (Clock Signal)	Recommended Application
Lowest ← Clock Performance → Highest	2	BL	RTM_DP[32:17] (RTM_DP[33])	High Performance Clock Applications (SDR, DDR data sampling)
	0	TR	RTM_DP[14:08] (RTM_DP[15])	µRTM GTP Transceiver not used: High Performance Clock Applications (SDR, DDR data sampling)
				µRTM GTP Transceiver used: General Purpose I/O Simple Clock Applications

	0	**TL**	**RTM_DP[07:00] (RTM_DP[16)**	**General Purpose I/O Simple Clock Applications**
	2	**BR**	**RTM_DP[45:34] (N/A)**	**General Purpose I/O**

Table 10-10: Simplified µRTM Signal Mapping Recommendation

Detailed clock and data signal/pin assignment planning requires consulting the "User Programmable FPGA" chapter in this manual, as well as consulting the Xilinx "Clocking Resources User Guide (UG382)".

10.2.2 GTP Transceiver Signals

The TAMC651 Zone 3 interface supports up to two GTP transceiver ports (TX/RX pairs).

The TAMC651 provides AC-coupling for all GTP transceiver lines (TX+/-, RX+/-, REFCLK+/-).

For using the GTP lines on the Zone 3 interface, the GTP transceiver reference clock signal(s) must be provided by the µRTM.

Please see the Xilinx Spartan-6 DC and Switching Characteristics (DS162) for details regarding valid GTP transceiver reference clock parameters.

If only one of the two GTP transceiver ports should be used on the µRTM, care should be taken regarding choosing the right one. Please see the "FPGA Bank 0 Clock Region Buffer Resources" table in the "User Programmable FPGA" chapter.

11 Appendix A (Generic User Constraint File)

This appendix provides a generic user constraint file for the TAMC651 Spartan-6 FPGA.

```
## ############################################################################################################ ##
##                                          TEWS TECHNOLOGIES                                                   ##
## ############################################################################################################ ##
##
##   Project Name    : TAMC651 Complete Pinning
##   File Name               : tamc651-xx_fpga.ucf
##   Target Device   : XC6SLXxxT-xFGG484
##   Design Tool     : Xilinx ISE Design Suit Embedded 13.1
##   Simulation Tool : Xilinx ISIM included in Design Tool
##
##   Description     : The file lists all FPGA pins that are connected on the TAMC651
##
##   Owner           : TEWS TECHNOLOGIES GmbH
##                     Am Bahnhof 7
##                     D-25469 Halstenbek
##
##                     Tel.: +49 / (0)4101 / 4058-0
##                     Fax.: +49 / (0)4101 / 4058-19
##                     e-mail: support@tews.com
##
##                     Copyright (c) 2011
##                     TEWS TECHNOLOGIES GmbH
##
##   History         :
##       Version   1 : (SE, 06.06.2011)
##                     Initial Version
##       Version   2 : (SE, 14.06.2011)
##                     Fixed MCB Performance Setting
##                     Added GTP Location Constraints
##       Version   3 : (SE, 01.07.2011)
##                     Fixed Bank Supply Information for RTM Pairs
##       Version   4 : (SE, 08.08.2011)
##                     Changed Default USER_CLK Frequency
##       Version   5 : (SE, 16.12.2011)
##                     The following changes occur in the new version:
##                     - File Rename / Revised Header
##                     - Added driver strength and slew rate on Crosspoint Switch signal nodes for
##                       improved signal integrity
##
##   Comments        : none
##
## ############################################################################################################ ##


## ############################################################################################################ ##
## Section: Miscellaneous
## ############################################################################################################ ##

# Set VCC aux power supply values (necessary for Spartan-6 architecture)
config vccaux = 3.3;


# Prohibit usage of pins that are not allowed for user I/O
config prohibit                          = "C3";           # HSWAPPEN Bank 0
```

```
config prohibit                         = "D3";         # VREF Bank 0
config prohibit                         = "A5";         # VREF Bank 0
config prohibit                         = "G13";        # VREF Bank 0
config prohibit                         = "D19";        # VREF Bank 0

config prohibit                         = "AA21";       # CMPMOSI Bank 2
config prohibit                         = "Y19";        # M1 Bank 2

config prohibit                         = "V15";        # VREF Bank 2
config prohibit                         = "U13";        # VREF Bank 2
config prohibit                         = "AB10";       # VREF Bank 2
config prohibit                         = "Y8";         # VREF Bank 2

config prohibit                         = "U16";        # Special Purpose Backup for DP38_P
config prohibit                         = "U14";        # Special Purpose Backup for DP38_N
config prohibit                         = "AA10";       # Special Purpose Backup for DP22_P
config prohibit                         = "W9";         # Special Purpose Backup for DP22_N

config prohibit                         = "Y4";         # FPGA INIT_B Bank 2

config prohibit                         = "P8";         # VREF Bank 3
config prohibit                         = "M8";         # VREF Bank 3
config prohibit                         = "K8";         # VREF Bank 3
config prohibit                         = "B1";         # VREF Bank 3


## ##################################################################################################### ##
## Section: SPI
## ##################################################################################################### ##

# Define I/O Standards
net "FPGA_DIN"                  iostandard = LVCMOS25;      # Bank 2 Supply 2.5V
net "FPGA_MOSI"                 iostandard = LVCMOS25;      # Bank 2 Supply 2.5V

net "FPGA_CCLK"                 iostandard = LVCMOS25;      # Bank 2 Supply 2.5V
net "FPGA_CSO_B"                iostandard = LVCMOS25;      # Bank 2 Supply 2.5V


# Location Constraints
net "FPGA_DIN"                          loc = "AA20";       # SPI MISO
net "FPGA_MOSI"                         loc = "AB20";

net "FPGA_CCLK"                         loc = "Y20";        # SPI CLK
net "FPGA_CSO_B"                        loc = "AA3";        # SPI S#


## ##################################################################################################### ##
## Section: AMC
## ##################################################################################################### ##

# Location Constraints
net "PCIe_TX_P"                         loc = "B6";         # Bank 101
net "PCIe_TX_N"                         loc = "A6";         # Bank 101
net "PCIe_RX_P"                         loc = "D7";         # Bank 101
net "PCIe_RX_N"                         loc = "C7";         # Bank 101

net "PCIe_REFCLK_P"                     loc = "A10";        # Bank 101
net "PCIe_REFCLK_N"                     loc = "B10";        # Bank 101
```

```
## ############################################################################################################ ##
## Section: RTM
## ############################################################################################################ ##

# Define I/O Standards
net "AMC_ZONE3_EN_3V3"          iostandard = LVCMOS25;       # Bank 0/2 Supply 2.5V

net "RTM_DP_?[*]"               iostandard = LVDS_25;        # Bank 0/2 Supply 2.5V


# Location Constraints
net "AMC_ZONE3_EN_3V3"                loc = "H13";          # Bank 0

net "RTM_DP_P[0]"                     loc = "B3";           # Bank 0
net "RTM_DP_P[1]"                     loc = "B2";           # Bank 0
net "RTM_DP_P[2]"                     loc = "E5";           # Bank 0
net "RTM_DP_P[3]"                     loc = "D4";           # Bank 0
net "RTM_DP_P[4]"                     loc = "C4";           # Bank 0
net "RTM_DP_P[5]"                     loc = "H10";          # Bank 0
net "RTM_DP_P[6]"                     loc = "G8";           # Bank 0
net "RTM_DP_P[7]"                     loc = "F7";           # Bank 0
net "RTM_DP_P[8]"                     loc = "C17";          # Bank 0
net "RTM_DP_P[9]"                     loc = "G16";          # Bank 0
net "RTM_DP_P[10]"                    loc = "H14";          # Bank 0
net "RTM_DP_P[11]"                    loc = "C19";          # Bank 0
net "RTM_DP_P[12]"                    loc = "D17";          # Bank 0
net "RTM_DP_P[13]"                    loc = "B18";          # Bank 0
net "RTM_DP_P[14]"                    loc = "B20";          # Bank 0
net "RTM_DP_P[15]"                    loc = "E16";          # Bank 0
net "RTM_DP_P[16]"                    loc = "G9";           # Bank 0

net "RTM_DP_P[17]"                    loc = "T10";          # Bank 2
net "RTM_DP_P[18]"                    loc = "V11";          # Bank 2
net "RTM_DP_P[19]"                    loc = "W12";          # Bank 2
net "RTM_DP_P[20]"                    loc = "U9";           # Bank 2
net "RTM_DP_P[21]"                    loc = "R9";           # Bank 2
net "RTM_DP_P[22]"                    loc = "W10";          # Bank 2
net "RTM_DP_P[23]"                    loc = "V7";           # Bank 2
net "RTM_DP_P[24]"                    loc = "T8";           # Bank 2
net "RTM_DP_P[25]"                    loc = "Y9";           # Bank 2
net "RTM_DP_P[26]"                    loc = "Y7";           # Bank 2
net "RTM_DP_P[27]"                    loc = "T7";           # Bank 2
net "RTM_DP_P[28]"                    loc = "AA8";          # Bank 2
net "RTM_DP_P[29]"                    loc = "Y5";           # Bank 2
net "RTM_DP_P[30]"                    loc = "AA6";          # Bank 2
net "RTM_DP_P[31]"                    loc = "W6";           # Bank 2
net "RTM_DP_P[32]"                    loc = "AA4";          # Bank 2
net "RTM_DP_P[33]"                    loc = "AA12";         # Bank 2
net "RTM_DP_P[34]"                    loc = "V17";          # Bank 2
net "RTM_DP_P[35]"                    loc = "Y17";          # Bank 2
net "RTM_DP_P[36]"                    loc = "AA18";         # Bank 2
net "RTM_DP_P[37]"                    loc = "W17";          # Bank 2
net "RTM_DP_P[38]"                    loc = "T15";          # Bank 2
net "RTM_DP_P[39]"                    loc = "AA16";         # Bank 2
net "RTM_DP_P[40]"                    loc = "Y16";          # Bank 2
net "RTM_DP_P[41]"                    loc = "W14";          # Bank 2
net "RTM_DP_P[42]"                    loc = "R13";          # Bank 2
net "RTM_DP_P[43]"                    loc = "Y15";          # Bank 2
net "RTM_DP_P[44]"                    loc = "V13";          # Bank 2
net "RTM_DP_P[45]"                    loc = "AA14";         # Bank 2
```

```
net "RTM_DP_N[0]"                   loc = "A3";          # Bank 0
net "RTM_DP_N[1]"                   loc = "A2";          # Bank 0
net "RTM_DP_N[2]"                   loc = "E6";          # Bank 0
net "RTM_DP_N[3]"                   loc = "D5";          # Bank 0
net "RTM_DP_N[4]"                   loc = "A4";          # Bank 0
net "RTM_DP_N[5]"                   loc = "H11";         # Bank 0
net "RTM_DP_N[6]"                   loc = "F9";          # Bank 0
net "RTM_DP_N[7]"                   loc = "F8";          # Bank 0
net "RTM_DP_N[8]"                   loc = "A17";         # Bank 0
net "RTM_DP_N[9]"                   loc = "F17";         # Bank 0
net "RTM_DP_N[10]"                  loc = "G15";         # Bank 0
net "RTM_DP_N[11]"                  loc = "A19";         # Bank 0
net "RTM_DP_N[12]"                  loc = "C18";         # Bank 0
net "RTM_DP_N[13]"                  loc = "A18";         # Bank 0
net "RTM_DP_N[14]"                  loc = "A20";         # Bank 0
net "RTM_DP_N[15]"                  loc = "F16";         # Bank 0
net "RTM_DP_N[16]"                  loc = "F10";         # Bank 0

net "RTM_DP_N[17]"                  loc = "U10";         # Bank 2
net "RTM_DP_N[18]"                  loc = "W11";         # Bank 2
net "RTM_DP_N[19]"                  loc = "Y12";         # Bank 2
net "RTM_DP_N[20]"                  loc = "V9";          # Bank 2
net "RTM_DP_N[21]"                  loc = "R8";          # Bank 2
net "RTM_DP_N[22]"                  loc = "Y10";         # Bank 2
net "RTM_DP_N[23]"                  loc = "W8";          # Bank 2
net "RTM_DP_N[24]"                  loc = "U8";          # Bank 2
net "RTM_DP_N[25]"                  loc = "AB9";         # Bank 2
net "RTM_DP_N[26]"                  loc = "AB7";         # Bank 2
net "RTM_DP_N[27]"                  loc = "U6";          # Bank 2
net "RTM_DP_N[28]"                  loc = "AB8";         # Bank 2
net "RTM_DP_N[29]"                  loc = "AB5";         # Bank 2
net "RTM_DP_N[30]"                  loc = "AB6";         # Bank 2
net "RTM_DP_N[31]"                  loc = "Y6";          # Bank 2
net "RTM_DP_N[32]"                  loc = "AB4";         # Bank 2
net "RTM_DP_N[33]"                  loc = "AB12";        # Bank 2
net "RTM_DP_N[34]"                  loc = "W18";         # Bank 2
net "RTM_DP_N[35]"                  loc = "AB17";        # Bank 2
net "RTM_DP_N[36]"                  loc = "AB18";        # Bank 2
net "RTM_DP_N[37]"                  loc = "Y18";         # Bank 2
net "RTM_DP_N[38]"                  loc = "U15";         # Bank 2
net "RTM_DP_N[39]"                  loc = "AB16";        # Bank 2
net "RTM_DP_N[40]"                  loc = "W15";         # Bank 2
net "RTM_DP_N[41]"                  loc = "Y14";         # Bank 2
net "RTM_DP_N[42]"                  loc = "T14";         # Bank 2
net "RTM_DP_N[43]"                  loc = "AB15";        # Bank 2
net "RTM_DP_N[44]"                  loc = "W13";         # Bank 2
net "RTM_DP_N[45]"                  loc = "AB14";        # Bank 2


net "GBT_DAT_A2R_P[0]"              loc = "B14";         # Bank 123
net "GBT_DAT_A2R_N[0]"              loc = "A14";         # Bank 123
net "GBT_DAT_R2A_P[0]"              loc = "D13";         # Bank 123
net "GBT_DAT_R2A_N[0]"              loc = "C13";         # Bank 123
net "GBT_DAT_A2R_P[1]"              loc = "B16";         # Bank 123
net "GBT_DAT_A2R_N[1]"              loc = "A16";         # Bank 123
net "GBT_DAT_R2A_P[1]"              loc = "D15";         # Bank 123
net "GBT_DAT_R2A_N[1]"              loc = "C15";         # Bank 123

net "GBT_CLK_R2A_P[0]"              loc = "A12";         # Bank 123
```

```
net "GBT_CLK_R2A_N[0]"                loc = "B12";          # Bank 123
net "GBT_CLK_R2A_P[1]"                loc = "E12";          # Bank 123
net "GBT_CLK_R2A_N[1]"                loc = "F12";          # Bank 123


## ############################################################################################## ##
## Section: MLVDS
##
##  Note: Port 16 is unconnected. Thus groups 12-15 and 17-20 exist
##
## ############################################################################################## ##

# Define I/O Standards
net "MLVDS_*_MDE"             iostandard = LVCMOS15;       # Bank 3 Supply 1.5V

net "MLVDS_TX_RE_n[*]"        iostandard = LVCMOS25;       # Bank 1 Supply 2.5V
net "MLVDS_TX_DE[*]"          iostandard = LVCMOS25;       # Bank 1 Supply 2.5V
net "MLVDS_TX_DI[*]"          iostandard = LVCMOS25;       # Bank 1 Supply 2.5V
net "MLVDS_TX_RO[*]"          iostandard = LVCMOS25;       # Bank 1 Supply 2.5V


net "MLVDS_RT[*]"             iostandard = LVCMOS15;       # Bank 3 Supply 1.5V

net "MLVDS_RX_RE_n[*]"        iostandard = LVCMOS25;       # Bank 1 Supply 2.5V
net "MLVDS_RX_DE[*]"          iostandard = LVCMOS25;       # Bank 1 Supply 2.5V
net "MLVDS_RX_DI[*]"          iostandard = LVCMOS25;       # Bank 1 Supply 2.5V
net "MLVDS_RX_RO[*]"          iostandard = LVCMOS25;       # Bank 1 Supply 2.5V


# Location Constraints
net "MLVDS_12_13_MDE"                 loc = "J7";          # Bank 3
net "MLVDS_14_15_MDE"                 loc = "H8";          # Bank 3
net "MLVDS_17_18_MDE"                 loc = "F5";          # Bank 3
net "MLVDS_19_20_MDE"                 loc = "G6";          # Bank 3

net "MLVDS_TX_RE_n[12]"               loc = "N15";         # Bank 1
net "MLVDS_TX_RE_n[13]"               loc = "N20";         # Bank 1
net "MLVDS_TX_RE_n[14]"               loc = "K17";         # Bank 1
net "MLVDS_TX_RE_n[15]"               loc = "K19";         # Bank 1
net "MLVDS_TX_RE_n[17]"               loc = "H16";         # Bank 1
net "MLVDS_TX_RE_n[18]"               loc = "H18";         # Bank 1
net "MLVDS_TX_RE_n[19]"               loc = "F18";         # Bank 1
net "MLVDS_TX_RE_n[20]"               loc = "F20";         # Bank 1

net "MLVDS_TX_DE[12]"                 loc = "N16";         # Bank 1
net "MLVDS_TX_DE[13]"                 loc = "M16";         # Bank 1
net "MLVDS_TX_DE[14]"                 loc = "K18";         # Bank 1
net "MLVDS_TX_DE[15]"                 loc = "K20";         # Bank 1
net "MLVDS_TX_DE[17]"                 loc = "H17";         # Bank 1
net "MLVDS_TX_DE[18]"                 loc = "H19";         # Bank 1
net "MLVDS_TX_DE[19]"                 loc = "F19";         # Bank 1
net "MLVDS_TX_DE[20]"                 loc = "F21";         # Bank 1

net "MLVDS_TX_DI[12]"                 loc = "W22";         # Bank 1
net "MLVDS_TX_DI[13]"                 loc = "Y22";         # Bank 1
net "MLVDS_TX_DI[14]"                 loc = "R22";         # Bank 1
net "MLVDS_TX_DI[15]"                 loc = "T22";         # Bank 1
net "MLVDS_TX_DI[17]"                 loc = "H22";         # Bank 1
net "MLVDS_TX_DI[18]"                 loc = "J22";         # Bank 1
net "MLVDS_TX_DI[19]"                 loc = "D22";         # Bank 1
```

```
net "MLVDS_TX_DI[20]"               loc = "E22";          # Bank 1

net "MLVDS_TX_RO[12]"               loc = "P18";          # Bank 1
net "MLVDS_TX_RO[13]"               loc = "P17";          # Bank 1
net "MLVDS_TX_RO[14]"               loc = "L17";          # Bank 1
net "MLVDS_TX_RO[15]"               loc = "L15";          # Bank 1
net "MLVDS_TX_RO[17]"               loc = "M20";          # Bank 1
net "MLVDS_TX_RO[18]"               loc = "M19";          # Bank 1
net "MLVDS_TX_RO[19]"               loc = "N19";          # Bank 1
net "MLVDS_TX_RO[20]"               loc = "P20";          # Bank 1


net "MLVDS_RT[12]"                  loc = "H4";           # Bank 3
net "MLVDS_RT[13]"                  loc = "G4";           # Bank 3
net "MLVDS_RT[14]"                  loc = "D2";           # Bank 3
net "MLVDS_RT[15]"                  loc = "D1";           # Bank 3
net "MLVDS_RT[17]"                  loc = "F3";           # Bank 3
net "MLVDS_RT[18]"                  loc = "E4";           # Bank 3
net "MLVDS_RT[19]"                  loc = "H6";           # Bank 3
net "MLVDS_RT[20]"                  loc = "G7";           # Bank 3

net "MLVDS_RX_RE_n[12]"             loc = "M21";          # Bank 1
net "MLVDS_RX_RE_n[13]"             loc = "M17";          # Bank 1
net "MLVDS_RX_RE_n[14]"             loc = "J19";          # Bank 1
net "MLVDS_RX_RE_n[15]"             loc = "J16";          # Bank 1
net "MLVDS_RX_RE_n[17]"             loc = "G19";          # Bank 1
net "MLVDS_RX_RE_n[18]"             loc = "H20";          # Bank 1
net "MLVDS_RX_RE_n[19]"             loc = "C20";          # Bank 1
net "MLVDS_RX_RE_n[20]"             loc = "E20";          # Bank 1

net "MLVDS_RX_DE[12]"               loc = "M22";          # Bank 1
net "MLVDS_RX_DE[13]"               loc = "M18";          # Bank 1
net "MLVDS_RX_DE[14]"               loc = "J20";          # Bank 1
net "MLVDS_RX_DE[15]"               loc = "J17";          # Bank 1
net "MLVDS_RX_DE[17]"               loc = "G20";          # Bank 1
net "MLVDS_RX_DE[18]"               loc = "H21";          # Bank 1
net "MLVDS_RX_DE[19]"               loc = "B21";          # Bank 1
net "MLVDS_RX_DE[20]"               loc = "D21";          # Bank 1

net "MLVDS_RX_DI[12]"               loc = "U22";          # Bank 1
net "MLVDS_RX_DI[13]"               loc = "V22";          # Bank 1
net "MLVDS_RX_DI[14]"               loc = "N22";          # Bank 1
net "MLVDS_RX_DI[15]"               loc = "P22";          # Bank 1
net "MLVDS_RX_DI[17]"               loc = "F22";          # Bank 1
net "MLVDS_RX_DI[18]"               loc = "G22";          # Bank 1
net "MLVDS_RX_DI[19]"               loc = "B22";          # Bank 1
net "MLVDS_RX_DI[20]"               loc = "C22";          # Bank 1

net "MLVDS_RX_RO[12]"               loc = "P21";          # Bank 1
net "MLVDS_RX_RO[13]"               loc = "P19";          # Bank 1
net "MLVDS_RX_RO[14]"               loc = "K16";          # Bank 1
net "MLVDS_RX_RO[15]"               loc = "L19";          # Bank 1
net "MLVDS_RX_RO[17]"               loc = "K22";          # Bank 1
net "MLVDS_RX_RO[18]"               loc = "K21";          # Bank 1
net "MLVDS_RX_RO[19]"               loc = "L22";          # Bank 1
net "MLVDS_RX_RO[20]"               loc = "L20";          # Bank 1


## ############################################################################################## ##
## Section: DDR3 Memory
```

```
## ############################################################################################################ ##

# MCB 3, I/O Termination
net "DDR_DQ[*]"                   in_term = none;
net "DDR_?DQS_?"                  in_term = none;

# MCB 3, I/O Standards
net "DDR_DQ[*]"                iostandard = SSTL15_II;      # 1,5V
net "DDR_A[*]"                 iostandard = SSTL15_II;      # 1,5V
net "DDR_BA[*]"                iostandard = SSTL15_II;      # 1,5V
net "DDR_?DQS_?"               iostandard = DIFF_SSTL15_II; # 1,5V
net "DDR_CK_?"                 iostandard = DIFF_SSTL15_II; # 1,5V
net "DDR_CKe"                  iostandard = SSTL15_II;      # 1,5V
net "DDR_RAS_n"                iostandard = SSTL15_II;      # 1,5V
net "DDR_CAS_n"                iostandard = SSTL15_II;      # 1,5V
net "DDR_WE_n"                 iostandard = SSTL15_II;      # 1,5V
net "DDR_ODT"                  iostandard = SSTL15_II;      # 1,5V
net "DDR_RESET_n"              iostandard = LVCMOS15;       # 1,5V
net "DDR_?DM"                  iostandard = SSTL15_II;      # 1,5V
net "DDR_RZQ"                  iostandard = SSTL15_II;      # 1,5V
net "DDR_ZIO"                  iostandard = SSTL15_II;      # 1,5V


# MCB 3, Pin Location Constraints for Clock, Masks, Address, and Controls
net "DDR_A[0]"                           loc = "K2";          # Bank 3
net "DDR_A[1]"                           loc = "K1";          # Bank 3
net "DDR_A[2]"                           loc = "K5";          # Bank 3
net "DDR_A[3]"                           loc = "M6";          # Bank 3
net "DDR_A[4]"                           loc = "H3";          # Bank 3
net "DDR_A[5]"                           loc = "M3";          # Bank 3
net "DDR_A[6]"                           loc = "L4";          # Bank 3
net "DDR_A[7]"                           loc = "K6";          # Bank 3
net "DDR_A[8]"                           loc = "G3";          # Bank 3
net "DDR_A[9]"                           loc = "G1";          # Bank 3
net "DDR_A[10]"                          loc = "J4";          # Bank 3
net "DDR_A[11]"                          loc = "E1";          # Bank 3
net "DDR_A[12]"                          loc = "F1";          # Bank 3
net "DDR_A[13]"                          loc = "J6";          # Bank 3
net "DDR_A[14]"                          loc = "H5";          # Bank 3

net "DDR_BA[0]"                          loc = "J3";          # Bank 3
net "DDR_BA[1]"                          loc = "J1";          # Bank 3
net "DDR_BA[2]"                          loc = "H1";          # Bank 3

net "DDR_CK_P"                           loc = "K4";          # Bank 3
net "DDR_CK_N"                           loc = "K3";          # Bank 3

net "DDR_DQ[0]"                          loc = "R3";          # Bank 3
net "DDR_DQ[1]"                          loc = "R1";          # Bank 3
net "DDR_DQ[2]"                          loc = "P2";          # Bank 3
net "DDR_DQ[3]"                          loc = "P1";          # Bank 3
net "DDR_DQ[4]"                          loc = "L3";          # Bank 3
net "DDR_DQ[5]"                          loc = "L1";          # Bank 3
net "DDR_DQ[6]"                          loc = "M2";          # Bank 3
net "DDR_DQ[7]"                          loc = "M1";          # Bank 3
net "DDR_DQ[8]"                          loc = "T2";          # Bank 3
net "DDR_DQ[9]"                          loc = "T1";          # Bank 3
net "DDR_DQ[10]"                         loc = "U3";          # Bank 3
net "DDR_DQ[11]"                         loc = "U1";          # Bank 3
net "DDR_DQ[12]"                         loc = "W3";          # Bank 3
```

```
net "DDR_DQ[13]"                    loc = "W1";          # Bank 3
net "DDR_DQ[14]"                    loc = "Y2";          # Bank 3
net "DDR_DQ[15]"                    loc = "Y1";          # Bank 3

net "DDR_CKE"                       loc = "F2";          # Bank 3
net "DDR_ODT"                       loc = "L6";          # Bank 3

net "DDR_LDQS_P"                    loc = "N3";          # Bank 3
net "DDR_LDQS_N"                    loc = "N1";          # Bank 3
net "DDR_UDQS_P"                    loc = "V2";          # Bank 3
net "DDR_UDQS_N"                    loc = "V1";          # Bank 3

net "DDR_CAS_n"                     loc = "M4";          # Bank 3
net "DDR_RAS_n"                     loc = "M5";          # Bank 3
net "DDR_WE_n"                      loc = "H2";          # Bank 3

net "DDR_LDM"                       loc = "N4";          # Bank 3
net "DDR_UDM"                       loc = "P3";          # Bank 3

net "DDR_RESET_n"                   loc = "E3";          # Bank 3

net "DDR_RZQ"                       loc = "R7";          # Bank 3
net "DDR_ZIO"                       loc = "W4";          # Bank 3


# Additional Constratints
config mcb_performance                  = standard;      # General MCB constraints


## ##############################################################################################
## Section: Clocking
## ##############################################################################################

# Define I/O Standards
net "PRG_CLK_?[*]"            iostandard = LVDS_25;      # Bank 0/2 Supply 2.5V

net "FPGA_CLK_?[*]"           iostandard = LVDS_25;      # Bank 0/2 Supply 2.5V

net "USER_CLK"                iostandard = LVCMOS25;     # Bank 0 Supply 2.5V

net "CLKGEN_???"              iostandard = LVCMOS25;     # Bank 1 Supply 2.5V

net "CLKSW_SOUT[?]"           iostandard = LVCMOS25;     # Bank 1 Supply 2.5V
net "CLKSW_SIN[?]"            iostandard = LVCMOS25;     # Bank 1 Supply 2.5V
net "CLKSW_CONF"              iostandard = LVCMOS25;     # Bank 1 Supply 2.5V
net "CLKSW_LOAD"              iostandard = LVCMOS25;     # Bank 1 Supply 2.5V

net "FPGA_CLKOUT_?"           iostandard = LVDS_25;      # Bank 1 Supply 2.5V


# I/O Standard Enhancement
net "CLKSW_SOUT[?]"           slow | drive = 8;          # Settings for Signal Integrity
net "CLKSW_SIN[?]"            slow | drive = 8;          # Settings for Signal Integrity
net "CLKSW_CONF"              slow | drive = 8;          # Settings for Signal Integrity
net "CLKSW_LOAD"              slow | drive = 8;          # Settings for Signal Integrity


# Location Constraints
net "PRG_CLK_P[0]"                  loc = "F14";         # Bank 0
net "PRG_CLK_N[0]"                  loc = "F15";         # Bank 0
```

```
net "PRG_CLK_P[1]"                  loc = "T12";          # Bank 2
net "PRG_CLK_N[1]"                  loc = "U12";          # Bank 2

net "FPGA_CLK_P[0]"                 loc = "H12";          # Bank 0
net "FPGA_CLK_N[0]"                 loc = "G11";          # Bank 0
net "FPGA_CLK_P[1]"                 loc = "Y11";          # Bank 2
net "FPGA_CLK_N[1]"                 loc = "AB11";         # Bank 2

net "USER_CLK"                      loc = "AB13";         # Bank 0

net "CLKGEN_SCL"                    loc = "R20";          # Bank 1
net "CLKGEN_SDA"                    loc = "R19";          # Bank 1
net "CLKGEN_INT"                    loc = "P16";          # Bank 1

net "CLKSW_SOUT[0]"                 loc = "R15";          # Bank 1
net "CLKSW_SOUT[1]"                 loc = "T21";          # Bank 1
net "CLKSW_SIN[0]"                  loc = "R17";          # Bank 1
net "CLKSW_SIN[1]"                  loc = "R16";          # Bank 1
net "CLKSW_CONF"                    loc = "T20";          # Bank 1
net "CLKSW_LOAD"                    loc = "T17";          # Bank 1

net "FPGA_CLKOUT_P"                 loc = "R11";          # Bank 2
net "FPGA_CLKOUT_N"                 loc = "T11";          # Bank 2


# Additional Constraints
net "PRG_CLK_P[0]"              tnm_net = "PRG_CLK_P_0";
timespec "TS_PRG_CLK_P_0"               = period "PRG_CLK_P_0" 20 MHz high 50 %;
net "PRG_CLK_P[1]"              tnm_net = "PRG_CLK_P_1";
timespec "TS_PRG_CLK_P_1"               = period "PRG_CLK_P_1" 20 MHz high 50 %;

net "USER_CLK"                  tnm_net = "USER_CLK";
timespec "TS_USER_CLK"                  = period "USER_CLK" 62.5 MHz high 50 %;

net "FPGA_CLK_P[0]"             tnm_net = "FPGA_CLK_P_0";
timespec "TS_FPGA_CLK_P_0"              = period "FPGA_CLK_P_0" 20 MHz high 50 %;
net "FPGA_CLK_P[1]"             tnm_net = "FPGA_CLK_P_1";
timespec "TS_FPGA_CLK_P_1"              = period "FPGA_CLK_P_1" 20 MHz high 50 %;


## ##############################################################################################
## Section: SFP
## ##############################################################################################

# Define I/O Standards
net "SFP_S??"               iostandard = LVCMOS25;      # Bank 1 Supply 2.5V

net "SFP_PS_n"              iostandard = LVCMOS15;      # Bank 3 Supply 1.5V

net "SFP_TX_DIS"            iostandard = LVCMOS15;      # Bank 3 Supply 1.5V
net "SFP_TX_FLT"            iostandard = LVCMOS15;      # Bank 3 Supply 1.5V

net "SFP_RX_BW"             iostandard = LVCMOS15;      # Bank 3 Supply 1.5V
net "SFP_RX_LOS"            iostandard = LVCMOS15;      # Bank 3 Supply 1.5V


# Location Constraints
net "SFP_SCL"                       loc = "T19";          # Bank 1
net "SFP_SDA"                       loc = "T18";          # Bank 1
```

```
net "SFP_PS_n"                          loc = "N6";          # Bank 3

net "SFP_TX_DIS"                        loc = "U4";          # Bank 3
net "SFP_TX_FLT"                        loc = "T4";          # Bank 3

net "SFP_RX_BW"                         loc = "P6";          # Bank 3
net "SFP_RX_LOS"                        loc = "P7";          # Bank 3


net "SFP_TX_P"                          loc = "B8";          # Bank 101
net "SFP_TX_N"                          loc = "A8";          # Bank 101
net "SFP_RX_P"                          loc = "D9";          # Bank 101
net "SFP_RX_N"                          loc = "C9";          # Bank 101

net "SFP_REFCLK_P"                      loc = "C11";         # Bank 101
net "SFP_REFCLK_N"                      loc = "D11";         # Bank 101


## ############################################################################################## ##
## Section: Debug Connector
## ############################################################################################## ##

# Define I/O Standards
net "UART_?X"                  iostandard = LVCMOS25;       # Bank 1 Supply 2.5V


# Location Constraints
net "UART_TX"                           loc = "W20";         # Bank 1
net "UART_RX"                           loc = "Y21";         # Bank 1


## ############################################################################################## ##
## Section: MMC
## ############################################################################################## ##

# Define I/O Standards
net "MMC_S??"                  iostandard = LVCMOS25;       # Bank 1 Supply 2.5V

net "PAYLOAD_RST_3V3_n"        iostandard = LVCMOS25;       # Bank 1 Supply 2.5V

net "LED2_CTRL"                iostandard = LVCMOS15;       # Bank 3 Supply 1.5V
net "LED2_CTRL_MODE"           iostandard = LVCMOS15;       # Bank 3 Supply 1.5V


# Location Constraints
net "MMC_SCL"                           loc = "U19";         # Bank 1
net "MMC_SDA"                           loc = "V21";         # Bank 1

net "PAYLOAD_RST_3V3_n"                 loc = "U20";         # Bank 1

net "LED2_CTRL"                         loc = "T3";          # Bank 3
net "LED2_CTRL_MODE"                    loc = "R4";          # Bank 3


## ############################################################################################## ##
## Section: General Purpose I/O
## ############################################################################################## ##

# Define I/O Standards
net "GPIO_SW[?]"               iostandard = LVCMOS15;       # Bank 3 Supply 1.5V
```

```
net "GPIO_LED[?]"             iostandard = LVCMOS15;       # Bank 3 Supply 1.5V

net "GPIO_BUT_n"              iostandard = LVCMOS15;       # Bank 3 Supply 1.5V


# Location Constraints
net "GPIO_SW[1]"                     loc = "Y3";           # Bank 3
net "GPIO_SW[2]"                     loc = "T6";           # Bank 3
net "GPIO_SW[3]"                     loc = "T5";           # Bank 3
net "GPIO_SW[4]"                     loc = "V5";           # Bank 3

net "GPIO_LED[1]"                    loc = "V3";           # Bank 3
net "GPIO_LED[2]"                    loc = "P5";           # Bank 3
net "GPIO_LED[3]"                    loc = "P4";           # Bank 3
net "GPIO_LED[4]"                    loc = "AA2";          # Bank 3

net "GPIO_BUT_n"                     loc = "AA1";          # Bank 3
```