TAMC900 AMC with 8 high Speed ADCs 105 MSps, 14 Bit

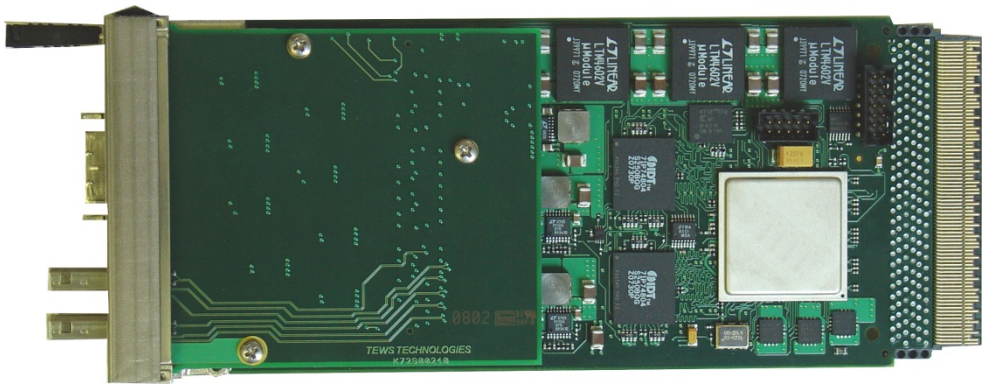

Figure 1: TAMC900 with TAMC900-A1 mounted

Application Information

The TAMC900 is a high speed, high performance analog to digital converter AdvancedMC. In addition to the eight high speed ADCs, it provides excessive preprocessing power by a Virtex-5 FPGA and high speed on board memory for e.g. full bandwidth snapshots.

A Virtex-5 LX30T is assembled on the TAMC900-10R. The TAMC900-25R is assembled with a Virtex-5 SX35T.

AMC Port 4-11 on the TAMC900-10R or Port 0, 1 and 4-9 on the TAMC900-25R can be used to transmit the ADC data to the CPU.

To adapt the TAMC900 to different customer requirements, the TAMC900 is equipped with a Signal Conditioning Adapter (SiCA) that contains the front panel with the connectors for the analog inputs, clock and trigger inputs and the analog signal conditioning.

The TAMC900 provides three clock inputs and three trigger inputs. The three external clock inputs and the PCIe reference clock are routed to a flexible clocking scheme that allows independent clocking of the ADCs in two groups. The trigger inputs are routed to the FPGA.

Eight LTC2254 ADCs provide up to 105 MSps and 14 bit resolution each. The minimum sample rate is 1 Msps.

4 MByte high speed on board QDR-II SRAM enables snapshots of all ADCs at full speed and full resolution for 2ms.

According to AMC.0, the TAMC900 provides an IPMI compliant Module Management Controller (MMC) with temperature monitoring and hot-swap support.

The TAMC900 is delivered with a basic firmware, which allows gathering ADC data from all channels, triggering, clock configuration, and uses a PCIe x4 Link (AMC Port 4-7) to transmit ADC data to the CPU. Driver and Example Application for the basic firmware are available for different operating systems.

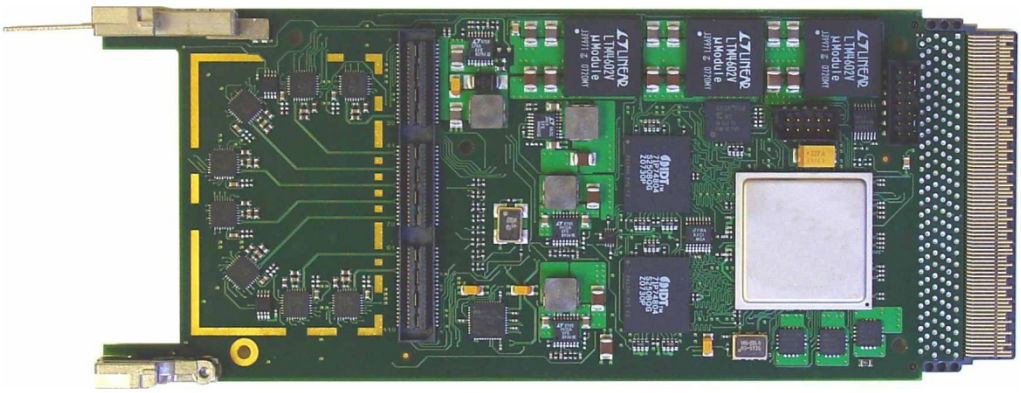

Figure 2: TAMC900

Issue 2.0.1
2017-09-14

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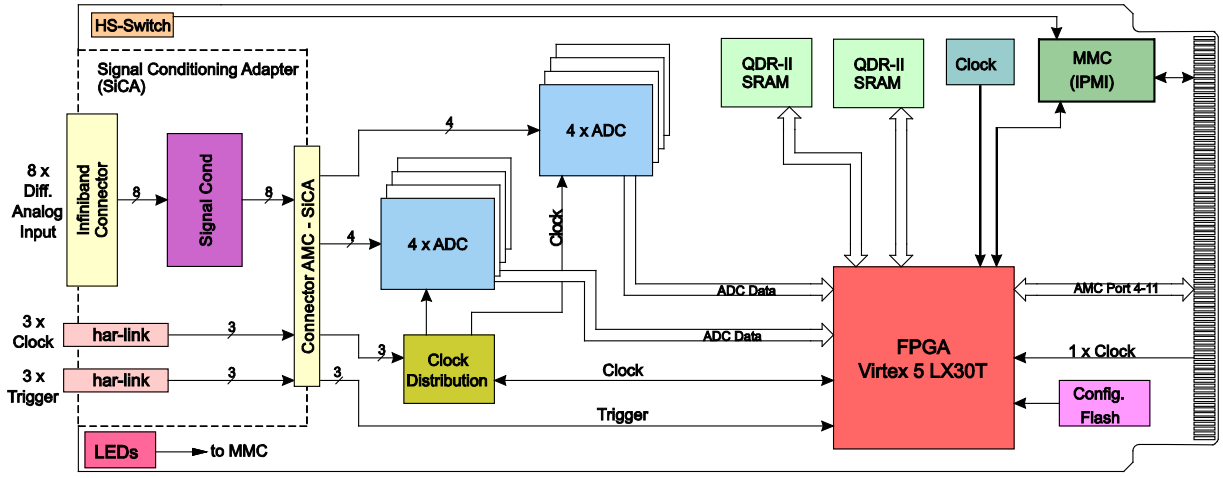

Figure 3: Block Diagram TAMC900-10R

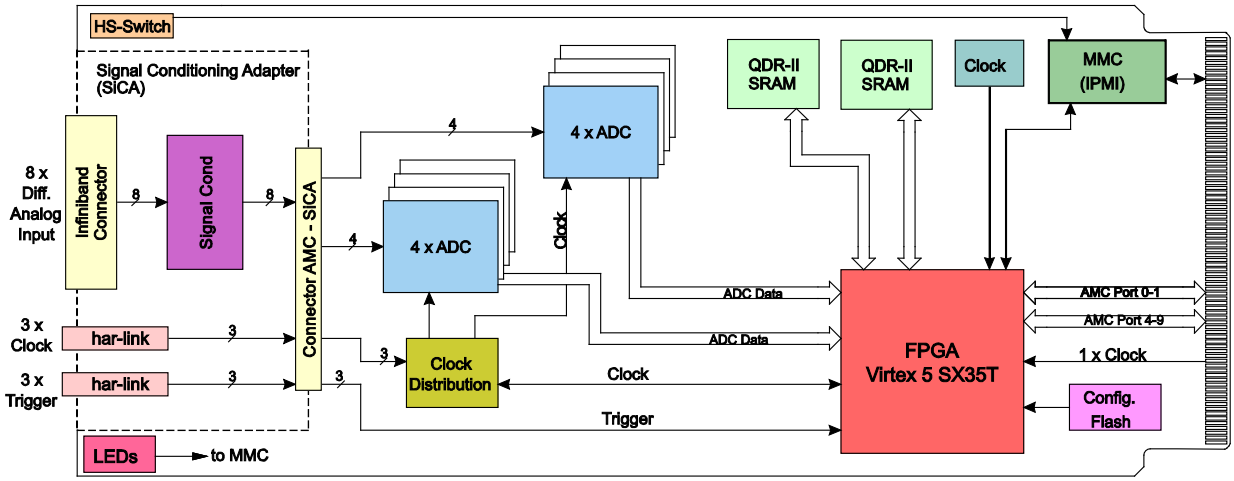

Figure 4: Block Diagram TAMC900-25R

Technical Information

- Form Factor: PCIMG AMC.0
  - Board size: 180.6 mm x 73.5 mm
  - Single width / Mid-Size
- Fabric Interface:
  - TAMC900-10R: Port 4-11
  - TAMC900-25R: Port 0-1 & 4-9
- Virtex-5 FPGA
  - TAMC900-10R: LX30T
  - TAMC900-25R: SX35T
- 4 MByte QDR-II SRAM
- IPMI Support
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red FAIL LED (LED1)
  - Green User LED (LED 2)
- Analog-to-Digital Converter:
  - 8 x LTC2254 ADCs
  - 105 MSps
  - 14 bit
- 3 external clock inputs
- 3 external trigger inputs
- Signal Conditioning Adapter for flexible adoption to customer analog input requirements
- Operating temperature: 0°C to +55°C

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Order Information

RoHS Compliant

TAMC900-10R	8 Ch. 14 Bit 105 MSps ADCs, Virtex-5 XC5VLX30T, 2 x 2 MB QDR-II, AMC port 4-11, requires TAMC900-A1
TAMC900-25R	8 Ch. 14 Bit 105 MSps ADCs, Virtex-5 XC5VLX35T, 2 x 2 MB QDR-II, AMC port 0,1 and 4-9, requires TAMC900-A1
TAMC900-A1-10R	Signal Conditioning Adapter for TAMC900, Gain = 1, Single Mid-Size
TAMC900-A1-11R	Signal Conditioning Adapter for TAMC900, Gain = 1, Single Full-Size

Optional available on request:

- Other FPGA (LX50T, SX50T, FX30T or FX70T)
- 8 MB QDR-II memory
- ADCs with different sample rate and resolution

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

TAMC900-DOC	User Manual for TAMC900
TAMC900-A1-DOC	User Manual for TAMC900-A1

Software

TAMC900-SW-25	Integrity Software Support (for basic firmware)
TAMC900-SW-42	VxWorks Software Support (for basic firmware)
TAMC900-SW-65	Windows Software Support (for basic firmware)
TAMC900-SW-82	Linux Software Support (for basic firmware)
TAMC900-SW-95	QNX Software Support (for basic firmware)

For other operating systems please contact TEWS.

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