The Embedded I/O Company

TEWS TECHNOLOGIES

TCP260

Dual PMC Carrier for 6U CompactPCI (J3/J5 I/O)

Version 1.0

User Manual

Issue 1.0.8

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TCP260-10R

Dual PMC Carrier for 6U CompactPCI

with J3 and J5 I/O and 5V PMC V/IO voltage

TCP260-11R

Dual PMC Carrier for 6U CompactPCI

with J3 and J5 I/O and 3.3V PMC V/IO voltage

TCP260-10R-ET

Dual PMC Carrier for 6U CompactPCI

with J3 and J5 I/O and 5V PMC V/IO voltage,

extended temperature range

TCP260-11R-ET

Dual PMC Carrier for 6U CompactPCI

with J3 and J5 I/O and 3.3V PMC V/IO voltage,

extended temperature range

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
0.0	Preliminary Issue	April 2003
1.0	Initial Issue	July 2003
1.1	Hot Swap Hardware Modification	January 2004
1.2	TCP260-11 board option added	June 2005
1.3	New address TEWS LLC	September 2006
1.4	Extended temperature range versions added	September 2008
1.0.5	New notation of User Manual Issue	April 2009
1.0.6	New hardware version with new PCI-to-PCI bridge	January 2011
1.0.7	Only available in RoHS-compliant version	June 2011
1.0.8	General Revision	August 2014

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1 Product Description

The TCP260 is a standard 6U CompactPCI carrier that provides front I/O and rear I/O for up to two single width PMC modules.

The transparent PCI to PIC Bridge is used as the PCI bridging device between the primary CompactPCI bus and the on board secondary PCI bus where the two PMC slots reside.

Supported PCI bus data widths are 32 bit and 64 bit. Supported PCI bus frequencies are 33 MHz and 66 MHz.

The TCP260 supports standard PMC front I/O and CompactPCI rear I/O. The PMC slot 1 I/O lines are connected directly to the CompactPCI connector J3. The PMC slot 2 I/O lines are connected directly to the CompactPCI connector J5.

The TCP260 also provides hot swapping capability. The TCP260 on board hot swap controller controls the installation and reinstallation process of the TCP260 without powering down the CompactPCI system.

The TCP260 carrier complies with the PICMG 2.0 Revision 3.0 CompactPCI specification.

The TCP260 is available in extended temperature range as TCP260-10R-ET and TCP260-11R-ET.

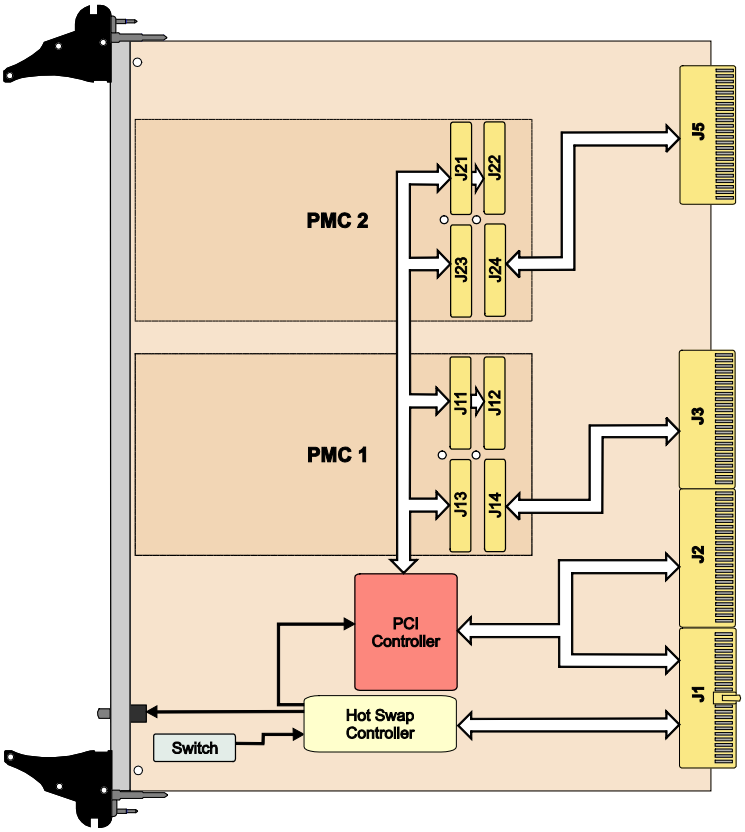

Figure 1-1 : Block Diagram

2 Technical Specification

PCI Interface		
CompactPCI Interface	CompactPCI 6U, conforming to PICMG 2.0 R3.0	
PCI Interface	PCI 2.2 compliant interface, 33 MHz / 66 MHz, 32 bit / 64 bit	
PCI I/O Signaling Voltage	3.3V and 5V tolerant	
PCI to PCI Bridge	TCP260-xx : Pericom PI7C8154A/B	
PMC Interface		
Number of PMC Slots	2	
Supported PMC PCI Data Width	32 bit / 64 bit	
Supported PMC PCI Frequency	33 MHz / 66 MHz	
PCI I/O Signaling Voltage	TCP260-10R / -10R-ET: 5V V/IO voltage TCP260-11R / -11R-ET: 3.3V V/IO voltage	
PMC I/O Access	Front panel I/O P14/P24 Back I/O via CompactPCI J3/J5 connector	
Physical Data		
Power Requirements without PMC Modules plugged	10 mA typical @ VI/O DC 80 mA typical @ +5V DC 100 mA typical @ +3.3V DC 10 mA typical @ + 12V DC <1 mA typical @ -12V DC Additional power is required by plugged PMC modules.	
Maximum Total Power for both PMC Modules	5 A typical @ +5V DC 5 A typical @ +3.3V DC 1 A typical @ +12V DC 1 A typical @ -12V DC	
Overcurrent Protection	All four power supplies are disconnected from PMC modules during an over current situation.	
Temperature Range	TCP260-10R / -11R TCP260-10R-ET / -11R-ET	Operating: 0°C to + 70°C Storage: -40°C to + 100°C Operating: -40°C to + 85°C Storage: -55°C to + 125°C
MTBF	TCP260-xx: 234000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Weight	306 g	
Size	160 mm x 233.35 mm	
Humidity	5 – 95 % non- condensing	

Table 2-1 : Technical Specification

3 PCI to PCI Bridge

3.1 PCI Configuration Registers

3.1.1 PCI to PCI Bridge Header

PCI CFG Register Address	PCI Configuration Register				PCI writeable
	31 24	23 16	15 8	7 0	
0x00	Device ID		Vendor ID		N
0x04	Status		Command		Y
0x08	Class Code			Revision ID	N
0x0C	Reserved	Header Type	Primary Latency Timer	Cache Line Size	Y[15:0]
0x10	Reserved				N
0x14	Reserved				N
0x18	Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	Y
0x1C	Secondary Status		I/O Limit Address	I/O Base Address	Y
0x20	Memory Limit Address		Memory Base Address		Y
0x24	Prefetchable Memory Limit Address		Prefetchable Memory Base Address		Y
0x28	Prefetchable Memory Base Address Upper 32 Bits				Y
0x2C	Prefetchable Memory Limit Address Upper 32 Bits				Y
0x30	I/O Limit Address Upper 16 Bits		I/O Base Address Upper 16 Bits		Y
0x34	Reserved			ECP Pointer	Y
0x38	Reserved				N
0x3C	Bridge Control		Interrupt Pin	Reserved	Y
0x40	Arbiter Control		Diagnostic Control	Chip Control	Y
0x44 – 0x60	Reserved				N
0x64	GPIO Input Data	GPIO Output Enable Control	GPIO Output Data	P_SERR# Event Disable	Y
0x68	Reserved	P_SERR# Status	Secondary Clock Control		Y
0x6C – 0xDB	Reserved				N
0xDC	Power Management Capabilities		Next Item Ptr.	Capability ID	Y
0xE0	Data	PPB Support Extensions	Power Management CSR		Y
0xE4 – 0xFF	Reserved				N

Table 3-1 : PCI to PCI Bridge Header

For further information please refer to the Pericom PCI to PCI Bridge manual.

3.2 Secondary Bus Device Number Mapping

The secondary bus device number of PMC slot 1 and PMC slot 2 is defined by configuration type translation of the PCI to PCI Bridge.

By default PMC slot 1 is mapped to secondary bus device number 0x04, and PMC slot 2 is mapped to secondary bus device number 0x05.

Secondary Bus Device Number (HEX)	Secondary Bus AD(31:16) (Binary)	PCI AD Line used as PMC IDSEL	Purpose
0 1	0000 0000 0000 0001 0000 0000 0000 0010	16 17	Implemented by PCI to PCI bridge but not used on TCP260
2	0000 0000 0000 0100	18	Optional IDSEL for PMC1
3	0000 0000 0000 1000	19	Optional IDSEL for PMC2
4	0000 0000 0001 0000	20	Default IDSEL for PMC1
5	0000 0000 0010 0000	21	Default IDSEL for PMC2
6 -F	0000 0000 0100 0000 1000 0000 0000 0000	22 – 31	Implemented by PCI to PCI bridge but not used on TCP260
10 – 1E	0000 0000 0000 0000	None	Not implemented by PCI to PCI bridge
1F	Special Cycle Data	-	Special Cycles for PMC

Table 3-2 : Secondary Bus Device Number Mapping

3.3 Local Register / Hot Swap Register

The PCI to PCI Bridge does not provide an internal Hot Swap control and status register for the direct control of Hot Swap installation and reinstallation process. Following the PICMG 2.1 R1.0 CompactPCI Hot Swap Specification, the TCP260 uses the alternate register implementation for the on board Hot Swap Register. Additional on board logic provides the required control and status information to handle the Hot Swap process.

The additional on board logic maps the four bits of the Hot Swap Register to the general purpose I/O lines of the PCI to PIC Bridge.

The TCP260 Hot Swap Registers is accessed using the PCI to PIC Bridge GPIO registers in PCI configuration register space.

To read the Hot Swap Register, the PCI to PIC Bridge GPIO lines must first be configured as input only lines. This is done by setting up the GPIO Output Enable Control Register accordingly. Then the PCI to PIC Bridge GPIO Input Data Register can be used to read the Hot Swap Register (after reset the PCI to PIC Bridge GPIO lines are configured as inputs).

To write to the Hot Swap Register, the PCI to PIC Bridge GPIO lines must first be configured as bi-directional I/O lines. This is done by setting up the GPIO Output Enable Control Register accordingly.
Then the GPIO Output Data Register could be used to set or clear the bits in the Hot Swap Register.

Bit / GPIO	Symbol	Description	Access	Reset Value
0	EIM	Mask ENUM# ‘1’ – Enable ENUM# pin ‘0’ – Disable ENUM# pin	R/W	0
1	LOO	Enable / Disable blue Hot Swap LED ‘1’ – Switch blue Hot Swap LED on ‘0’ – Switch blue Hot Swap LED off	R/W	0
2	EXT	Pending Extraction of the TCP260 ‘1’ – Indicates that the board is ready for extraction ‘0’ – Board is still installed The extraction bit can be cleared by writing ‘1’ to the according bit. Setting the bit by software is not possible.	R/W	0
3	INS	Freshly Inserted TCP260 ‘1’ – Indicates that the TCP260 has been inserted ‘0’ – No board changing The insertion bit can be cleared by writing ‘1’ to the according bit. Setting the bit by software is not possible.	R/W	1

Table 3-3 : Hot Swap Control and Status Register

3.3.1 GPIO Output Data Register – Offset 0x65

Bit	Symbol	Description	Access	Reset Value
0	GPIO 0	These four bits clear (setting to logical low level) the GPIO line by writing a '1' to the corresponding bit. Writing a '1' – clears the GPIO line Writing a '0' – no effect Reading reflects the last value written.	R/W	"0000"
1	GPIO 1			
2	GPIO 2			
3	GPIO 3			
4	GPIO 0	These four bits set (setting to logical high level) the GPIO line by writing a '1' to the corresponding bit. Writing a '1' – sets the GPIO line Writing a '0' – no effect Reading reflects the last value written.	R/W	"0000"
5	GPIO 1			
6	GPIO 2			
7	GPIO 3			

Table 3-4 : GPIO Output Data Register

3.3.2 GPIO Output Enable Control Register – Offset 0x66

Bit	Symbol	Description	Access	Reset Value
0	GPIO 0	Writing a '1' – sets the GPIO line mode to input only Writing a '0' – no effect Reading reflects the last value written.	R/W	"0000"
1	GPIO 1			
2	GPIO 2			
3	GPIO 3			
4	GPIO 0	Writing a '1' – sets the GPIO line mode to bidirectional Writing a '0' – no effect Reading reflects the last value written.	R/W	"0000"
5	GPIO 1			
6	GPIO 2			
7	GPIO 3			

Table 3-5 : GPIO Output Enable Control Register

3.3.3 GPIO Input Data Register – Offset 0x67

Bit	Symbol	Description	Access	Reset Value
3 : 0	Reserved	Returns '0' on reads	R	0
4	GPIO 0	Reflects the Hot Swap Register bit 0 :	R	Depends on GPIO lines
5	GPIO 1	Reflects the Hot Swap Register bit 1 :		
6	GPIO 2	Reflects the Hot Swap Register bit 2 :		
7	GPIO 3	Reflects the Hot Swap Register bit 3 :		

Table 3-6 : GPIO Input Data Register

3.4 Secondary PCI Clock

3.4.1 Secondary PCI Clock Combinations

For using 66 MHz PCI bus clock mode with the TCP260, the CompactPCI bus must support 66 MHz operation.

The secondary PCI bus on the TCP260 is configured by the plugged PMC modules. If any plugged PMC module does only support 33 MHz operation, the complete secondary PCI bus will always operate with 33 MHz only.

If the primary PCI bus does only support 33 MHz operation, the secondary PCI bus will also operate with 33 MHz only.

Primary PCI Bus Frequency (CompactPCI Frequency)	PMC1 Frequency Capability	PMC2 Frequency Capability	Secondary PCI Bus Operating Frequency (PMC1 and PMC2 Frequency)
33 MHz	33 MHz or 66 MHz	33 MHz or 66 MHz	33 MHz
66 MHz	33 MHz only	no PMC	33 MHz
66 MHz	no PMC	33 MHz only	33 MHz
66 MHz	33 MHz or 66 MHz	33 MHz only	33 MHz
66 MHz	33 MHz only	33 MHz or 66 MHz	33 MHz
66 MHz	33 MHz or 66 MHz	no PMC	66 MHz
66 MHz	no PMC	33 MHz or 66 MHz	66 MHz
66 MHz	33 MHz or 66 MHz	33 MHz or 66 MHz	66 MHz

Table 3-7 : Secondary PCI Clock Combinations

3.4.2 Disabling Secondary PCI Clocks

The TCP260 always enables both PMC slot PCI clocks even if there is no PMC module plugged.

To disable the PCI clock for PMC slot 1 close Jumper J8.

To disable the PCI clock for PMC slot 2 close Jumper J7.

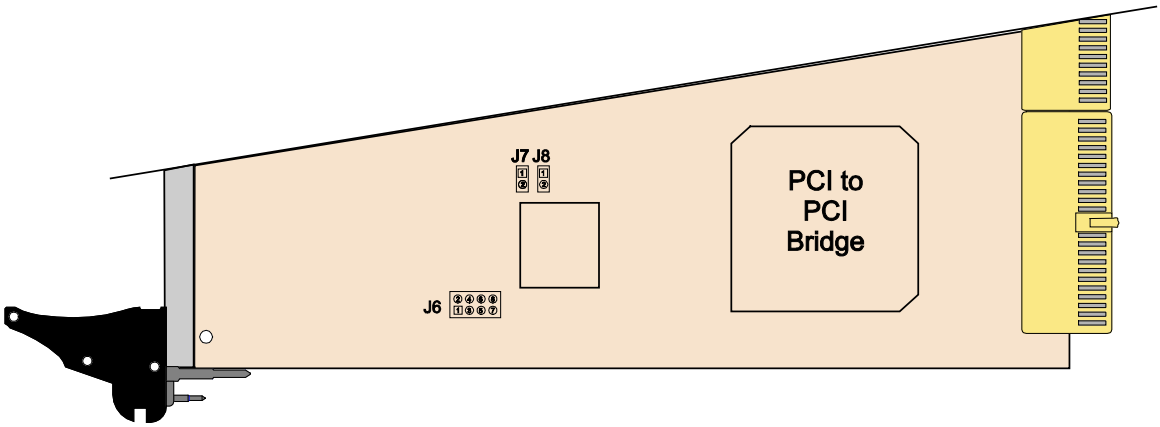

Figure 3-1 : Secondary PCI Clock Disable Jumper Location

Closing the jumper disables the clock for the PMC slot even if there is a PMC module plugged.

4 PMC to PCI Interface

The TCP260 is a standard 6U CompactPCI carrier that provides front I/O and rear I/O for up to two single width PMC modules. The transparent PCI to PCI Bridge provides the bridging between the primary CompactPCI bus and the secondary PCI bus where the two PMC slots reside.

4.1 PMC BUSMODE[4:1] Signals

The BUSMODE[4:1]# signals are unique to IEEE1386 (PMC) and are not found in the PCI or CompactPCI specification. They allow a host to identify the used mezzanine card type as a PMC card or as another existing mezzanine card type. The TCP260 does only support PMC cards. This “PMC only” configuration is indicated by pulling up BUSMODE2#, and pulling down BUSMODE3# and BUSMODE4#. The PMC card should decode the BUSMODE[4:2]# signals and drive out a logic “0” on BUSMODE1#.

4.2 Interrupt Routing

Interrupt	TCP260 –CompactPCI Pin Assignment	PMC 1 Device 4	PMC 2 Device 5
Interrupt A	INT A	INT A	INT B
Interrupt B	INT B	INT B	INT C
Interrupt C	INTC	INTC	INT D
Interrupt D	INT D	INT D	INT A

Table 4-1 : Interrupt Routing

4.3 PCI Signaling Voltage

4.3.1 Secondary PCI Bus PCI Signal Voltage Level

The secondary PCI bus signals connect to the PCI to PCI Bridge secondary PCI bus and to the PMC1 and PMC2 slots.

PMC modules are specified for 3.3V only, 5V only or universal (3.3V or 5V) PCI signal voltage operation.

The TCP260 on board S_V/IO signal voltage level defines the PCI signal voltage level for the TCP260 secondary PCI bus.

The TCP260-10R S_V/IO voltage level is configured as 5V PCI signal voltage.

The TCP260-11R S_V/IO voltage level is configured as 3.3V PCI signal voltage.

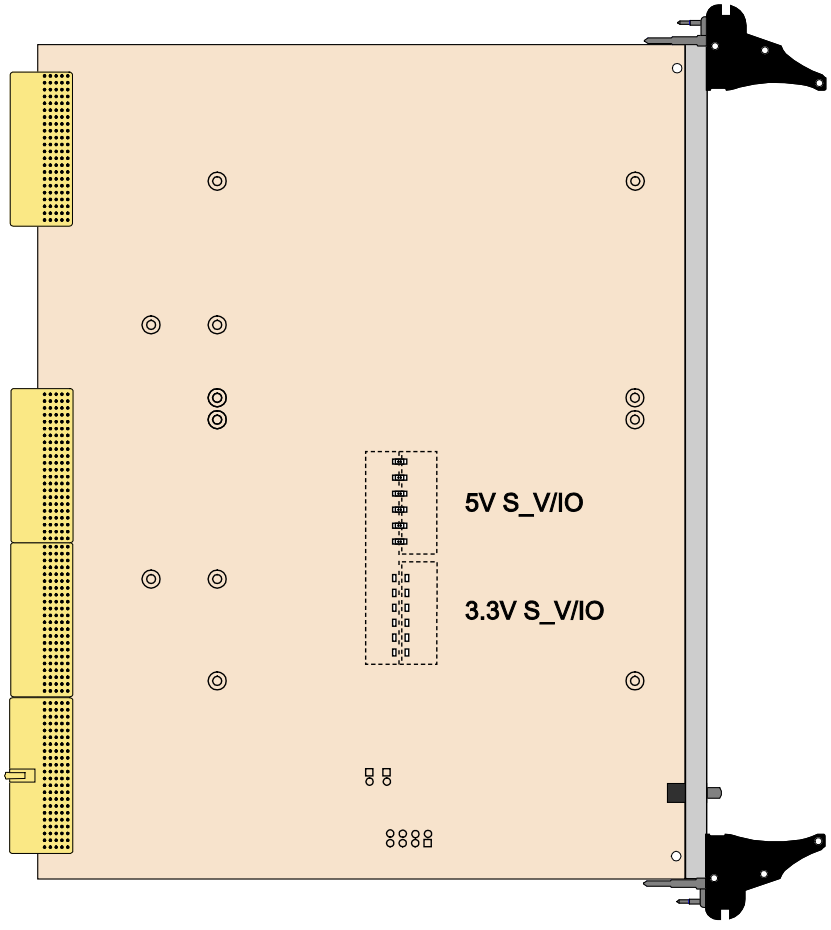

Figure 4-1 : PCI Signal Voltage Configuration Resistors

The S_V/IO signal voltage level is configured on board by resistor placement.

To switch the S_V/IO voltage level between 3.3V PCI signal voltage and 5V PCI signal voltage, six SMD resistors on the bottom side of the TCP260 board must be swapped one location to the other location.

4.3.2 PCI Signaling Levels and Voltage Keying

CompactPCI and PMC boards specify 5 Volt and 3.3 Volt PCI signaling voltage.

To prevent a PMC from being plugged into a PMC system with a different PCI signaling voltage, the PMC specification defines voltage keying by keying pins (on the PMC carrier board) and keying holes (on the PMC module).

PMC cards that only support 5 Volt PCI signaling voltage provides a single keying hole for the 5 Volt keying pin. A 3.3 Volt only PMC provides only the keying hole for the 3.3 Volt keying pin. Universal PMC cards, which can handle 3.3 Volt and 5 Volt PCI signaling voltage, have keying holes for both voltage keying pins.

As factory default, the TCP260-10R is assembled with the 5 Volt keying pin on both PMC slots.

As factory default, the TCP260-11R is assembled with the 3.3 Volt keying pin on both PMC slots.

In certain system configurations it may be necessary to remove the keying pin from one location and assemble it at the other keying pin location.

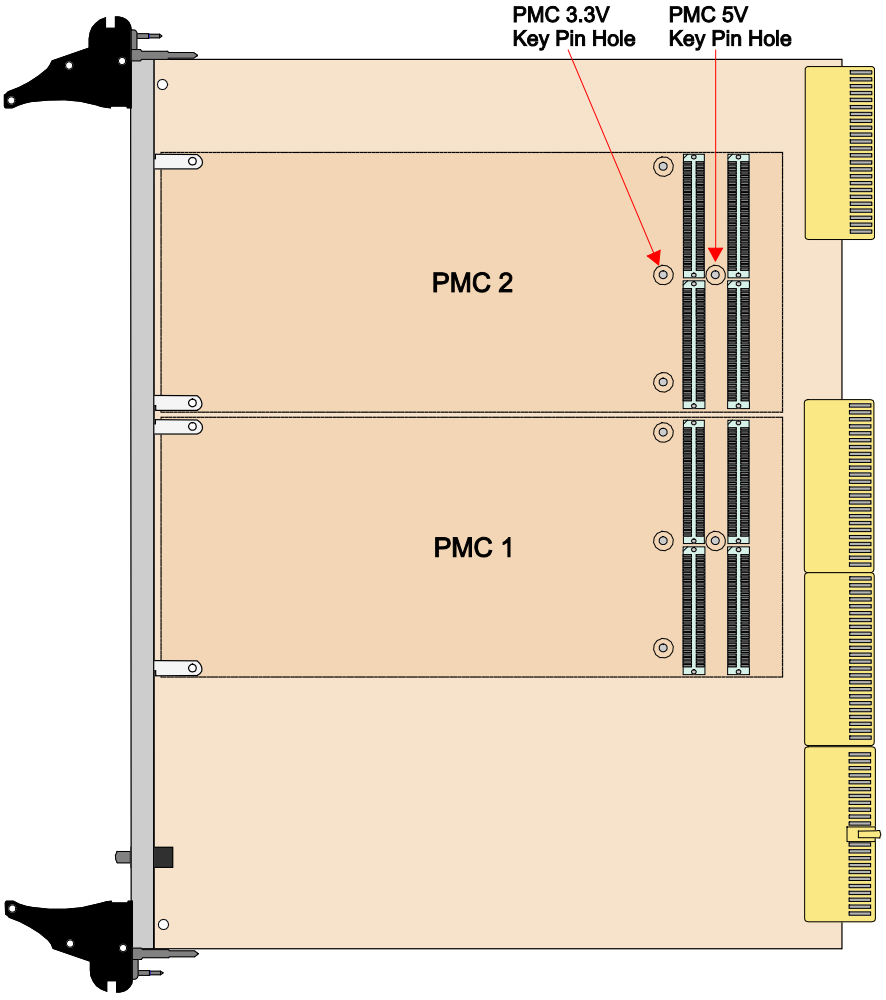

Figure 4-2 : PMC Voltage Keying

Use the following table to identify the required TCP260 Secondary PCI bus configuration for the actual PMC modules that are to be used.

PMC1 PCI Signal Voltage Capability	PMC2 PCI Signal Voltage Capability	TCP260 S_V/IO Configuration	TCP260 5V Keying Pin Configuration	TCP260 3.3V Keying Pin Configuration
-	-	-	-	-
-	3.3V Only	3.3V	Not Installed	Installed
-	3.3V or 5V	3.3V	Not Installed	Installed
		5V	Installed	Not Installed
-	5V Only	5V	Installed	Not Installed
3.3V Only	-	3.3V	Not Installed	Installed
3.3V Only	3.3V Only	3.3V	Not Installed	Installed
3.3V Only	3.3V or 5V	3.3V	Not Installed	Installed
3.3V Only	5V Only	-	-	-
3.3V or 5V	-	3.3V	Not Installed	Installed
		5V	Installed	Not Installed
3.3V or 5V	3.3V Only	3.3V	Not Installed	Installed
3.3V or 5V	3.3V or 5V	3.3V	Not Installed	Installed
		5V	Installed	Not Installed
3.3V or 5V	5V Only	5V	Installed	Not Installed
5V Only	-	5V	Installed	Not Installed
5V Only	3.3V Only	-	-	-
5V Only	3.3V or 5V	5V	Installed	Not Installed
5V Only	5V Only	5V	Installed	Not Installed

Table 4-2 : PCI Signal Voltage Configuration Matrix

Factory default configuration is:

	TCP260-10R	TCP260-11R
S_V/IO Configuration:	5V	3.3V
5V Keying Pin:	Installed	Not Installed
3.3V Keying Pin:	Not Installed	Installed

WARNING !!!

Be sure that the TCP260 Secondary PCI bus Signal Voltage (S_V/IO) configuration matches the TCP260 PMC slots keying pin configuration.

Be sure that the used PMC modules match to the TCP260 Secondary PCI bus Signal Voltage and PMC slot keying pin configuration.

If PMC modules are plugged into a PCI environment where the PCI signaling voltage does not match, damage to the equipment could occur, voiding product warranties.

5 Installation of a PMC Module

Before installing a PMC module, be sure that the power supply for the TCP260 is turned off or the TCP260 is not installed into a CompactPCI system.

The components are Electrostatic Sensitive Devices (ESD). Use an anti-static mat connected to a wristband when handling or installing the components.

The PMC modules are mounted to the TCP260 prior to installation into the CompactPCI system.

If the PMC has a front panel, first remove the cover from the PMC front panel cut-out of the TCP260. Install the PMC at an angle so that the PMC front panel penetrates the PMC front panel cut-out. Then rotate down to mate with the PMC connectors on the TCP260. If the PMC has no front panel, simply plug in the PMC, and leave the cover in the PMC front panel cut-out of the TCP260.

After the PMC module has been installed, it can be mounted on the TCP260 using the mounting screws that come with the PMC module. There are four screw mounting locations, two at the PMC front panel and two at the standoffs near the PMC bus connectors.

WARNING !!!

Be sure that the TCP260 Secondary PCI bus Signal Voltage (S_V/IO) configuration matches the TCP260 PMC slots keying pin configuration.

Be sure that the used PMC modules match to the TCP260 Secondary PCI bus Signal Voltage and PMC slot keying pin configuration.

If PMC modules are plugged into a PCI environment where the PCI signaling voltage does not match, damage to the equipment could occur, voiding product warranties.

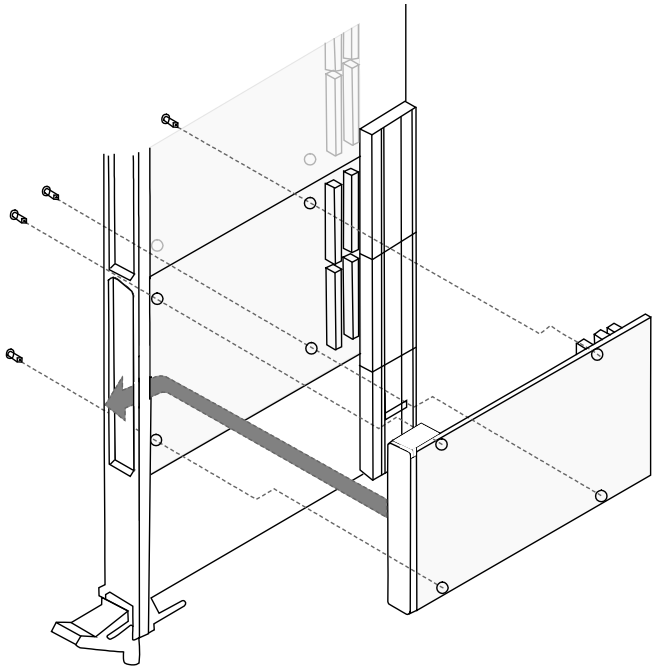

Figure 5-1 : Installation of a PMC Module

6 Hot Swap

6.1 Insertion Process

- Before inserting the TCP260 into a Hot Swap system the used PMC modules must be configured and mounted to the TCP260 PMC slots.
- During insertion process the TCP260 front panel and board ground is de-charged by the ESD stripes and 10Mohm resistors to eliminate different voltage potentials between the TCP260 and the host system.
- The first CompactPCI connector pins that connect during the insertion process are the long power pins. These pins apply power to the PCI to PCI Bridge, the Hot Swap controller and the additional on board logic. The Hot Swap controller resets the PCI to PCI Bridge and precharges the on board PCI signal lines to 1V.
- The blue Hot Swap LED is switched on by hardware.
- The next pins which are connected are the medium length pins. The complete CompactPCI bus belongs to these pins.
- The last pin which is connected to the CompactPCI back plane is the BD_SEL# pin. This line indicates to the Hot Swap controller that all pins are connected and the power supplies for the secondary PCI bus could be switched on.
- When the board is completely inserted and the insertion switch has locked, the INS bit in the Hot Swap Register is set, the ENUM# signal is asserted on the primary CompactPCI bus and the blue Hot Swap LED is switched off to signal not to extract the TCP260.
- The PCI to PCI Bridge can now be accessed (identified) on the primary CompactPCI bus.
- Upon detecting the asserted ENUM# signal, the CompactPCI host can now read the INS bit in the Hot Swap Register to determine if this is an insertion process. By clearing the INS bit, the CompactPCI host indicates to the TCP260 Hot Swap control logic that the host software has been configured.

6.2 Extraction Process

- When the micro-switch on the TCP260 handle is opened, the ENUM# signal is asserted on the CompactPCI bus and the EXT bit is set in the TCP260 Hot Swap Register.
- Upon detecting the asserted ENUM# signal, the host software can now read the EXT bit in the Hot Swap Register to determine if this is an extraction process.
- The host clears the EXT bit in the TCP260 Hot Swap Register to indicate that the host software has logged off the TCP260 from the CompactPCI bus.
- By switching on the blue Hot Swap LED via the TCP260 Hot Swap Register, the host system signals the user to go on with extraction process.
- Now the user is allowed to fully extract the TCP260.

For further information of Hot Swap please refer to the CompactPCI Hot Swap Specification PICMG 2.1 R2.0.

6.3 Non Hot Swap System

If the TCP260 is used in a non Hot Swap System the normal Hot Swap insertion process is dropped out. All PCI bus signals are already connected and be powered up by system control.

The TCP260 detects this normal start process and steps into a well known power on state. The blue Hot Swap LED is switched off by hardware to signal that the user is not allowed to extract the TCP260 from system.

The internal TCP260 Hot Swap state machine is set to state “insertion process completed” which means that the Hot Swap Register is set to the following value:

Bit / GPIO	Symbol	Description	Power On value
0	EIM	‘1’ – Enable ENUM# pin ‘0’ – Disable ENUM# pin	0
1	LOO	‘1’ – Switch blue Hot Swap LED on ‘0’ – Switch blue Hot Swap LED off	0
2	EXT	‘1’ – Indicates that the board is ready for extraction ‘0’ – Board is still installed	0
3	INS	‘1’ – Indicates that the TCP260 has been inserted ‘0’ – No board changing	1

Table 6-1 : Hot Swap Control and Status Register

In this state the PCI to PCI Bridge will work transparent without any Hot Swap device driver. All PCI configuration or data cycles are possible.

The same procedure is running if the TCP260 is still plugged in a Hot Swap system which is powered on or during a PCI bus reset.

7 Pin Assignment

7.1 CompactPCI J1

Position	Row					
	F	E	D	C	B	A
25	GND	5V	3.3V	ENUM#	REQ64#	5V
24	GND	ACK64#	AD[0]	V(I/O) (L)	5V	AD[1]
23	GND	AD[2]	5V (L)	AD[3]	AD[4]	3.3V
22	GND	AD[5]	AD[6]	3.3V (L)	GND	AD[7]
21	GND	C/BE[0]#	M66EN	AD[8]	AD[9]	3.3V
20	GND	AD[10]	AD[11]	V(I/O)	GND	AD[12]
19	GND	AD[13]	GND(L)	AD[14]	AD[15]	3.3V
18	GND	C/BE[1]#	PAR	3.3V	GND	SERR#
17	GND	PERR#	GND (L)	IPMB_SDA	IPMB_SCL	3.3V
16	GND	LOCK#	STOP#	V(I/O)	GND	DEVSEL#
15	GND	TRDY#	BD_SEL#	IRDY#	FRAME#	3.3V
14	GND	key	key	key	key	key
13	GND	key	key	key	key	key
12	GND	key	key	key	key	key
11	GND	C/BE[2]#	GND (L)	AD[16]	AD[17]	AD[18]
10	GND	AD[19]	AD[20]	3.3V	GND	AD[21]
9	GND	AD[22]	GND (L)	AD[23]	IDSEL	C/BE[3]#
8	GND	AD[24]	AD[25]	V(I/O)	GND	AD[26]
7	GND	AD[27]	GND (L)	AD[28]	AD[29]	AD[30]
6	GND	AD[31]	CLK	3.3V (L)	GND	REQ#
5	GND	GNT#	GND (L)	RST#	BRSVP1B5	BRSVP1A5
4	GND	INTS	INTP	V(I/O) (L)	HEALTHY#	IPMB_PWR
3	GND	INTD#	5V (L)	INTC#	INTB#	INTA#
2	GND	TDI	TDO	TMS	5V	TCK
1	GND	5V	+12V	TRST#	-12V	5V

Table 7-1 : CompactPCI J1 Pin Assignment

7.2 CompactPCI J2

Position	Row					
	F	E	D	C	B	A
22	GND	NC	NC	NC	NC	NC
21	GND	NC	NC	NC	NC	NC
20	GND	NC	NC	NC	NC	NC
19	GND	NC	NC	NC	NC	NC
18	GND	NC	NC	NC	NC	NC
17	GND	NC	NC	NC	NC	NC
16	GND	NC	NC	NC	NC	NC
15	GND	NC	NC	NC	NC	NC
14	GND	AD[32]	GND	AD[33]	AD[34]	AD[35]
13	GND	AD[36]	AD[37]	V(I/O)	GND	AD[38]
12	GND	AD[39]	GND	AD[40]	AD[41]	AD[42]
11	GND	AD[43]	AD[44]	V(I/O)	GND	AD[45]
10	GND	AD[46]	GND	AD[47]	AD[48]	AD[49]
9	GND	AD[50]	AD[51]	V(I/O)	GND	AD[52]
8	GND	AD[53]	GND	AD[54]	AD[55]	AD[56]
7	GND	AD[57]	AD[58]	V(I/O)	GND	AD[59]
6	GND	AD[60]	GND	AD[61]	AD[62]	AD[63]
5	GND	PAR64	C/BE[4]#	V(I/O)	EN64#	C/BE[5]#
4	GND	C/BE[6]#	GND	C/BE[7]#	BRSVP2B4	V(I/O)
3	GND	NC	NC	NC	GND	NC
2	GND	NC	NC	NC	NC	NC
1	GND	NC	NC	NC	GND	NC

Table 7-2 : CompactPCI J2 Pin Assignment

7.3 CompactPCI J3

Position	Row					
	F	E	D	C	B	A
19	GND	NC	NC	NC	NC	NC
18	GND	NC	NC	NC	NC	NC
17	GND	NC	NC	NC	NC	NC
16	GND	NC	NC	NC	NC	NC
15	GND	NC	NC	NC	NC	NC
14	GND	5V	5V	3.3V	3.3V	3.3V
13	GND	PMC1 I/O 1	PMC1 I/O 2	PMC1 I/O 3	PMC1 I/O 4	PMC1 I/O 5
12	GND	PMC1 I/O 6	PMC1 I/O 7	PMC1 I/O 8	PMC1 I/O 9	PMC1 I/O 10
11	GND	PMC1 I/O 11	PMC1 I/O 12	PMC1 I/O 13	PMC1 I/O 14	PMC1 I/O 15
10	GND	PMC1 I/O 16	PMC1 I/O 17	PMC1 I/O 18	PMC1 I/O 19	PMC1 I/O 20
9	GND	PMC1 I/O 21	PMC1 I/O 22	PMC1 I/O 23	PMC1 I/O 24	PMC1 I/O 25
8	GND	PMC1 I/O 26	PMC1 I/O 27	PMC1 I/O 28	PMC1 I/O 29	PMC1 I/O 30
7	GND	PMC1 I/O 31	PMC1 I/O 32	PMC1 I/O 33	PMC1 I/O 34	PMC1 I/O 35
6	GND	PMC1 I/O 36	PMC1 I/O 37	PMC1 I/O 38	PMC1 I/O 39	PMC1 I/O 40
5	GND	PMC1 I/O 41	PMC1 I/O 42	PMC1 I/O 43	PMC1 I/O 44	PMC1 I/O 45
4	GND	PMC1 I/O 46	PMC1 I/O 47	PMC1 I/O 48	PMC1 I/O 49	PMC1 I/O 50
3	GND	PMC1 I/O 51	PMC1 I/O 52	PMC1 I/O 53	PMC1 I/O 54	PMC1 I/O 55
2	GND	PMC1 I/O 56	PMC1 I/O 57	PMC1 I/O 58	PMC1 I/O 59	PMC1 I/O 60
1	GND	PMC1 I/O 61	PMC1 I/O 62	PMC1 I/O 63	PMC1 I/O 64	V I/O

Table 7-3 : CompactPCI J3 Pin Assignment

7.4 CompactPCI J5

Position	Row					
	F	E	D	C	B	A
22	GND	NC	NC	NC	NC	NC
21	GND	NC	NC	NC	NC	NC
20	GND	NC	NC	NC	NC	NC
19	GND	NC	NC	NC	NC	NC
18	GND	NC	NC	NC	NC	NC
17	GND	NC	NC	NC	NC	NC
16	GND	NC	NC	NC	NC	NC
15	GND	NC	NC	NC	NC	NC
14	GND	NC	NC	NC	NC	NC
13	GND	PMC2 I/O 1	PMC2 I/O 2	PMC2 I/O 3	PMC2 I/O 4	PMC2 I/O 5
12	GND	PMC2 I/O 6	PMC2 I/O 7	PMC2 I/O 8	PMC2 I/O 9	PMC2 I/O 10
11	GND	PMC2 I/O 11	PMC2 I/O 12	PMC2 I/O 13	PMC2 I/O 14	PMC2 I/O 15
10	GND	PMC2 I/O 16	PMC2 I/O 17	PMC2 I/O 18	PMC2 I/O 19	PMC2 I/O 20
9	GND	PMC2 I/O 21	PMC2 I/O 22	PMC2 I/O 23	PMC2 I/O 24	PMC2 I/O 25
8	GND	PMC2 I/O 26	PMC2 I/O 27	PMC2 I/O 28	PMC2 I/O 29	PMC2 I/O 30
7	GND	PMC2 I/O 31	PMC2 I/O 32	PMC2 I/O 33	PMC2 I/O 34	PMC2 I/O 35
6	GND	PMC2 I/O 36	PMC2 I/O 37	PMC2 I/O 38	PMC2 I/O 39	PMC2 I/O 40
5	GND	PMC2 I/O 41	PMC2 I/O 42	PMC2 I/O 43	PMC2 I/O 44	PMC2 I/O 45
4	GND	PMC2 I/O 46	PMC2 I/O 47	PMC2 I/O 48	PMC2 I/O 49	PMC2 I/O 50
3	GND	PMC2 I/O 51	PMC2 I/O 52	PMC2 I/O 53	PMC2 I/O 54	PMC2 I/O 55
2	GND	PMC2 I/O 56	PMC2 I/O 57	PMC2 I/O 58	PMC2 I/O 59	PMC2 I/O 60
1	GND	PMC2 I/O 61	PMC2 I/O 62	PMC2 I/O 63	PMC2 I/O 64	V I/O

Table 7-4 : CompactPCI J5 Pin Assignment

7.5 PMC J11 / P11 and J21 / P21

Pin	Signal		Signal	Pin
1	TCK		-12V	2
3	GND		INTA#	4
5	INTB#		INTC#	6
7	BUSMODE1#		+5V	8
9	INTD#		PCI-RSVD	10
11	GND		3.3Vaux	12
13	CLK		GND	14
15	GND		GNT#	16
17	REG#		+5V	18
19	V (I/O)		AD[31]	20
21	AD[28]		AD[27]	22
23	AD[25]		GND	24
25	GND		C/BE[3]#	26
27	AD[22]		AD[21]	28
29	AD[19]		+5V	30
31	V (I/O)		AD[17]	32
33	FRAME#		GND	34
35	GND		IRDY#	36
37	DEVSEL#		+5V	38
39	GND		LOCK#	40
41	PCI-RSVD		PCI-RSVD	42
43	PAR		GND	44
45	V (I/O)		AD[15]	46
47	AD[12]		AD[11]	48
49	AD[09]		+5V	50
51	GND		C/BE[0]#	52
53	AD[06]		AD[05]	54
55	AD[04]		GND	56
57	V (I/O)		AD[03]	58
59	AD[02]		AD[01]	60
61	AD[00]		+5V	62
63	GND		REQ64#	64

Table 7-5 : PMC J11/P11 and J21/P21 Pin Assignment

7.6 PMC J12 / P12 and J22 / P22

Pin	Signal		Signal	Pin
1	+12V		TRST#	2
3	TMS		TDO	4
5	TDI		GND	6
7	GND		PCI-RSVD	8
9	PCI-RSVD		PCI-RSVD	10
11	BUSMODE2#		+3.3V	12
13	RST#		BUSMODE3#	14
15	+3.3V		BUSMODE4#	16
17	PME#		GND	18
19	AD[30]		AD[29]	20
21	GND		AD[26]	22
23	AD[24]		+3.3V	24
25	IDSEL		AD[23]	26
27	+3.3V		AD[20]	28
29	AD[18]		GND	30
31	AD[16]		C/BE[2]#	32
33	GND		PMC-RSVD	34
35	TRDY#		+3.3V	36
37	GND		STOP#	38
39	PERR#		GND	40
41	+3.3V		SERR#	42
43	C/BE[1]#		GND	44
45	AD[14]		AD[13]	46
47	M66EN		AD[10]	48
49	AD[08]		+3.3V	50
51	AD[07]		PMC-RSVD	52
53	+3.3V		PMC-RSVD	54
55	PMC-RSVD		GND	56
57	PMC-RSVD		PMC-RSVD	58
59	GND		PMC-RSVD	60
61	ACK64#		+3.3V	62
63	GND		PMC-RSVD	64

Table 7-6 : PMC J12/P12 and J22/P22 Pin Assignment

7.7 PMC J13 / P13 and J23 / P23

Pin	Signal		Signal	Pin
1	PCI-RSVD		GND	2
3	GND		C/BE[7]#	4
5	C/BE[6]#		C/BE[5]#	6
7	C/BE[5]#		GND	8
9	V(I/O)		PAR64	10
11	AD[63]		AD[62]	12
13	AD[61]		GND	14
15	GND		AD[60]	16
17	AD[59]		AD[58]	18
19	AD[57]		GND	20
21	V(I/O)		AD[56]	22
23	AD[55]		AD[54]	24
25	AD[53]		GND	26
27	GND		AD[52]	28
29	AD[51]		AD[50]	30
31	AD[49]		GND	32
33	GND		AD[48]	34
35	AD[47]		AD[46]	36
37	AD[45]		GND	38
39	V(I/O)		AD[44]	40
41	AD[43]		AD[42]	42
43	AD[41]		GND	44
45	GND		AD[40]	46
47	AD[39]		AD[38]	48
49	AD[37]		GND	50
51	GND		AD[36]	52
53	AD[35]		AD[34]	54
55	AD[33]		GND	56
57	V(I/O)		AD[32]	58
59	PCI-RSVD		PCI_RSVD	60
61	PCI-RSVD		GND	62
63	GND		PCI-RSVD	64

Table 7-7 : PMC J13/P13 and J23/P23 Pin Assignment

7.8 PMC J14 / P14 and J24 / P24

Pin	Signal		Signal	Pin
1	I/O 1		I/O 2	2
3	I/O 3		I/O 4	4
5	I/O 5		I/O 6	6
7	I/O 7		I/O 8	8
9	I/O 9		I/O 10	10
11	I/O 11		I/O 12	12
13	I/O 13		I/O 14	14
15	I/O 15		I/O 16	16
17	I/O 17		I/O 18	18
19	I/O 19		I/O 20	20
21	I/O 21		I/O 22	22
23	I/O 23		I/O 24	24
25	I/O 25		I/O 26	26
27	I/O 27		I/O 28	28
29	I/O 29		I/O 30	30
31	I/O 31		I/O 32	32
33	I/O 33		I/O 34	34
35	I/O 35		I/O 36	36
37	I/O 37		I/O 38	38
39	I/O 39		I/O 40	40
41	I/O 41		I/O 42	42
43	I/O 43		I/O 44	44
45	I/O 45		I/O 46	46
47	I/O 47		I/O 48	48
49	I/O 49		I/O 50	50
51	I/O 51		I/O 52	52
53	I/O 53		I/O 54	54
55	I/O 55		I/O 56	56
57	I/O 57		I/O 58	58
59	I/O 59		I/O 60	60
61	I/O 61		I/O 62	62
63	I/O 63		I/O 64	64

Table 7-8 : PMC J14/P14 and J24/P24 Pin Assignment