TCP630 Reconfigurable FPGA with TTL/Differential I/O to PIM Module Slot

Application Information

The TCP630 is a standard 3U 32 bit CompactPCI module providing a user configurable FPGA with 300,000 or 600,000 system gates. All local signals from the PCI controller are routed to the FPGA.

The TCP630 provides 64 ESD-protected TTL lines, 32 differential I/O lines using EIA-422 / EIA-485 compatible, ESD-protected line transceivers or 32 TTL and 16 differential I/Os. All lines are individually programmable as input, output or tri-state. The receivers are always enabled, which allows determining the state of each I/O line at any time. This can be used as read back function for lines configured as outputs. Each TTL I/O line has a pull-up resistor. The pull-up voltage is selectable to be either +3.3V or +5V. The differential I/O lines are terminated by 120Ω resistors.

For flexible front I/O solutions the TCP630 provides a PIM Module slot, allowing active and passive signal conditioning. With the TPIM003 all I/O signals are provided on a HD68 connector. An option also offers in parallel rear I/O via the J2 connector.

TCP630-10R

The FPGA is configured by a serial flash. The flash device is in-system programmable via driver software over the PCI bus. An in-circuit debugging option is available via an optionally mountable JTAG header for readback and real-time debugging of the FPGA design (using Xilinx “ChipScope”).

A programmable clock generator supplies up to six different clock frequencies between 200 kHz and 166 MHz. All outputs are available at the FPGA, one clock source is in addition used as the local clock signal for the PCI controller. The clock generator settings are stored in an EEPROM and can be changed by the driver software through PCI9030 GPIO pins.

The configuration EEPROM of the PCI controller can also be modified by the driver software, to adapt address spaces etc.

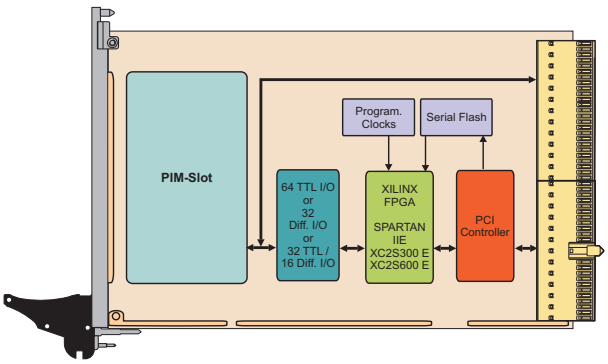
User applications can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com.

For First Time Users the Engineering Documentation TCP630-ED is recommended. The Engineering Documentation includes TCP630-DOC, schematics, data sheets / application notes of the components and well documented sample VHDL source code.

Software Support (TDRV004-SW-xx) for different operating systems is available.

Technical Information

- Standard 3U 32 bit CompactPCI module conforming to PICMG 2.0 R3.0
- PCI 2.2 compliant interface
- 3.3V and 5V PCI Signaling Voltage
- Board size: 160 mm x 100 mm
- Xilinx XC2S300E-6 Spartan-IIE FPGA configured by serial Flash XCF02S or Xilinx XC2S600E-6 Spartan-IIE FPGA configured by serial Flash XCF04S
- Flash device in-system programmable
- 32 bit PCI target interface by PLX PCI9030
- FPGA clock options:
  - Local clock oscillator
  - PLL programmable clock generator (200 KHz – 166 MHz), 6 clock outputs connected to FPGA
- I/O lines
  - 64 TTL I/O, 32 differential I/O or 32 TTL I/O and 16 differential I/O
  - TTL signaling voltage (maximum current: +/-24 mA) or EIA-422/-485 signaling level
  - direction individually programmable
- I/O access:
  64 I/O lines via a PIM Module slot, parallel to 64 I/O lines on rear connector J2
- Operating temperature: -40°C to +85°C



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Order Information

RoHS Compliant

TCP630-10R	Reconfigurable FPGA, 300k Gates, 64 TTL Inputs/Outputs
TCP630-11R	Reconfigurable FPGA, 300k Gates, 32 Differential Inputs/Outputs
TCP630-12R	Reconfigurable FPGA, 300k Gates, 32 TTL Inputs/Outputs and 16 Differential Inputs/Outputs
TCP630-20R	Reconfigurable FPGA, 300k Gates, 64 TTL Inputs/Outputs, J2 I/O
TCP630-21R	Reconfigurable FPGA, 300k Gates, 32 Differential Inputs/Outputs, J2 I/O
TCP630-22R	Reconfigurable FPGA, 300k Gates, 32 TTL Inputs/Outputs and 16 Differential Inputs/Outputs, J2 I/O
TCP630-30R	Reconfigurable FPGA, 600k Gates, 64 TTL Inputs/Outputs
TCP630-31R	Reconfigurable FPGA, 600k Gates, 32 Differential Inputs/Outputs
TCP630-32R	Reconfigurable FPGA, 600k Gates, 32 TTL Inputs/Outputs and 16 Differential Inputs/Outputs
TCP630-40R	Reconfigurable FPGA, 600k Gates, 64 TTL Inputs/Outputs, J2 I/O
TCP630-41R	Reconfigurable FPGA, 600k Gates, 32 Differential Inputs/Outputs, J2 I/O
TCP630-42R	Reconfigurable FPGA, 600k Gates, 32 TTL Inputs/Outputs and 16 Differential Inputs/Outputs, J2 I/O

None RoHS Compliant

TCP630-10	None RoHS compliant version of TCP630-10R
TCP630-11	None RoHS compliant version of TCP630-11R
TCP630-12	None RoHS compliant version of TCP630-12R
TCP630-20	None RoHS compliant version of TCP630-20R
TCP630-21	None RoHS compliant version of TCP630-21R
TCP630-22	None RoHS compliant version of TCP630-22R
TCP630-30	None RoHS compliant version of TCP630-10R
TCP630-31	None RoHS compliant version of TCP630-11R
TCP630-32	None RoHS compliant version of TCP630-12R
TCP630-40	None RoHS compliant version of TCP630-20R
TCP630-41	None RoHS compliant version of TCP630-21R
TCP630-42	None RoHS compliant version of TCP630-22R

Documentation

TCP630-DOC	User Manual
TCP630-ED	Engineering Documentation, includes TCP630-DOC

Software

TDRV004-SW-25	Integrity Software Support
TDRV004-SW-42	VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
TDRV004-SW-65	Windows XP/XPE/2000 Software Support
TDRV004-SW-72	LynxOS Software Support
TDRV004-SW-82	LiNUX Software Support
TDRV004-SW-95	QNX 6 Software Support

For other operating systems please contact TEWS.

Related Products

TPIM003	PIM I/O Module with HD68 SCSI-3 type connector and special pin assignment
TCP001-FP	6U front panel extension for 3U cPCI boards

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