The Embedded I/O Company

TCP885

Four Channel 10/100/1000 Mbit/s Ethernet Adapter

Version 1.0

User Manual

Issue 1.0.1

August 2014

TCP885-10R

Four channel 10/100/1000 Mbit/s Ethernet interface RJ45 front panel I/O, 32bit (cPCI Connector J1 only), extended temperature range (RoHS compliant)

TCP885-20R

Four channel 10/100/1000 Mbit/s Ethernet interface RJ45 front panel I/O, 64bit (cPCI Connector J1 and J2), extended temperature range
(RoHS compliant)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial issue	August 2013
1.0.1	General revision	August 2014

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1 Product Description

The TCP885 is a 3U 32bit/64bit CompactPCI module providing a four channel Ethernet 10BASE-T / 100BASE-TX / 1000BASE-T interface.

The TCP885 is equipped with a transparent PCI/PCI-X to PCIe Bridge which is capable of performing data transfer with a bus width of up to 64 bit at bus frequencies of up to 133 MHz depending on the product order option and the system backplane configuration.

The Bridge and a PCIe Switch provide access to the Intel 82574IT Gigabit Ethernet controllers. Each Ethernet interface supports 10, 100 and 1000 Mbit/s transmission rates for full duplex operation, 10 and 100 Mbit/s transmissions for half duplex operation, and is equipped with a 32 Kbit Serial EEPROM.

The four front panel RJ45 connector Ethernet interfaces of the TCP885 are capable of performing an auto negotiation algorithm which allows both link-partners to find out the best link-parameters by themselves.

The TCP885 is widely user configurable via configuration and status register access over the CompactPCI bus. All ports are galvanically isolated from the Ethernet controllers and LEDs indicate network activities.

On the TCP885-10R only CompactPCI connector J1 is fitted which means that the module is limited to 32bit PCI bus width.

The TCP885-20R is additionally equipped with CompactPCI connector J2 which allows 64bit data transfer in a corresponding backplane system configuration.

The module meets the requirements to operate in extended temperature range from -40° to +85°C.
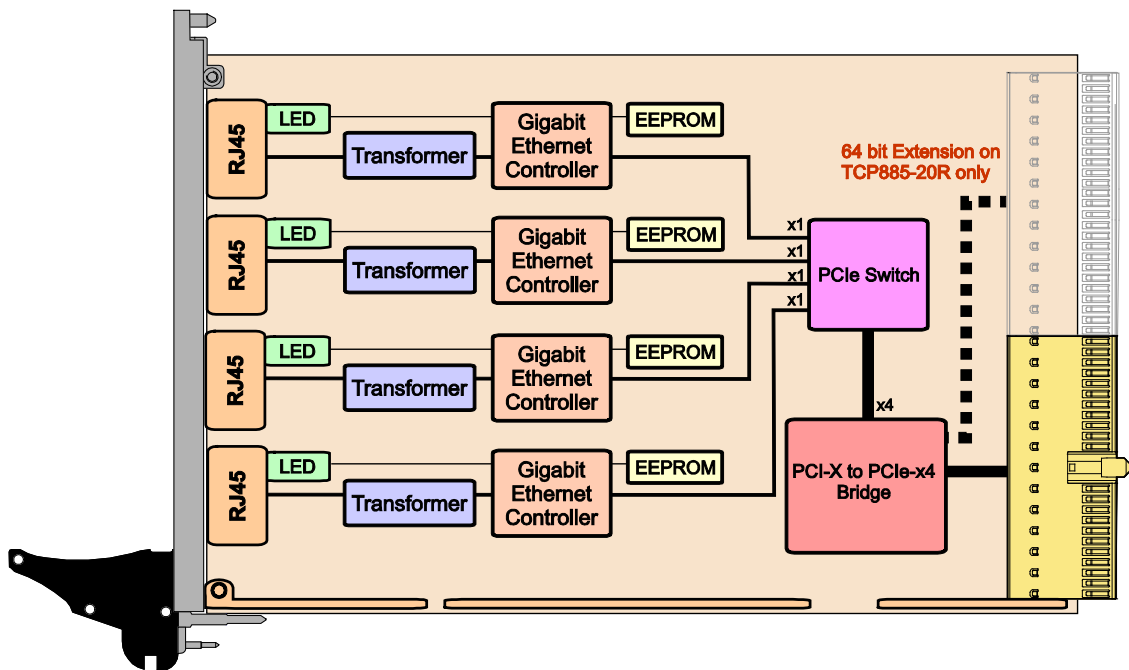

Figure 1-1 : Block Diagram

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2 Technical Specification

cPCI Interface	
Mechanical Interface	CompactPCI (cPCI) Interface conforming to PICMG 2.0 Revision 3.0 3U, 4HP
Electrical Interface	PCI Rev. 3.0 compliant and PCI-X Rev. 2.0a compliant 66 MHz / 32(64) bit PCI and 133 MHz / 32(64) bit PCI-X 3.3V PCI signaling with 5V I/O tolerance
On Board Devices	
PCI/PCI-X to PCIe Bridge	PI7C9X130 (Pericom)
PCIe Switch	89HPES8T5A (IDT)
Gigabit Ethernet Controller	For each interface: 82574IT (Intel)
Ethernet Interface	
Number of Interfaces	4
FIFO	For each interface: Configurable receive and transmit data FIFO, programmable in 1 KB increments
Interrupts	Using PCI INTA, INTB, INTC and INTD
I/O Connector	4x RJ45 (Würth 615 032 137 821 or compatible)
Physical Data	
Power Requirements	1500mA typical @ +3.3V DC (no link) app. additional 70mA per 100Mbit/s link app. additional 300mA per 1Gbit/s link
Temperature Range	Operating: -40°C to +85°C Storage: -40°C to +85°C
MTBF	TCP886-10R: 366000 h TCP886-20R: 345000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	TCP886-10R: 152 g TCP886-20R: 167 g

Table 2-1 : Technical Specification

3 PCI Device Topology on TCP885

The TCP885 uses four Gigabit Ethernet Controllers (Intel 82574IT) each communicating via a PCIe Rev. 1.1 compliant x1 Interface. To be able to access the Ethernet controllers they are connected to the x1 Downstream Ports of a PCIe Switch (IDT 89HPES8T5A). The x4 Upstream Port of the Switch is connected to a PCI/PCI-X to PCIe Bridge (Pericom PI7C9X130) which communicates with the host system.
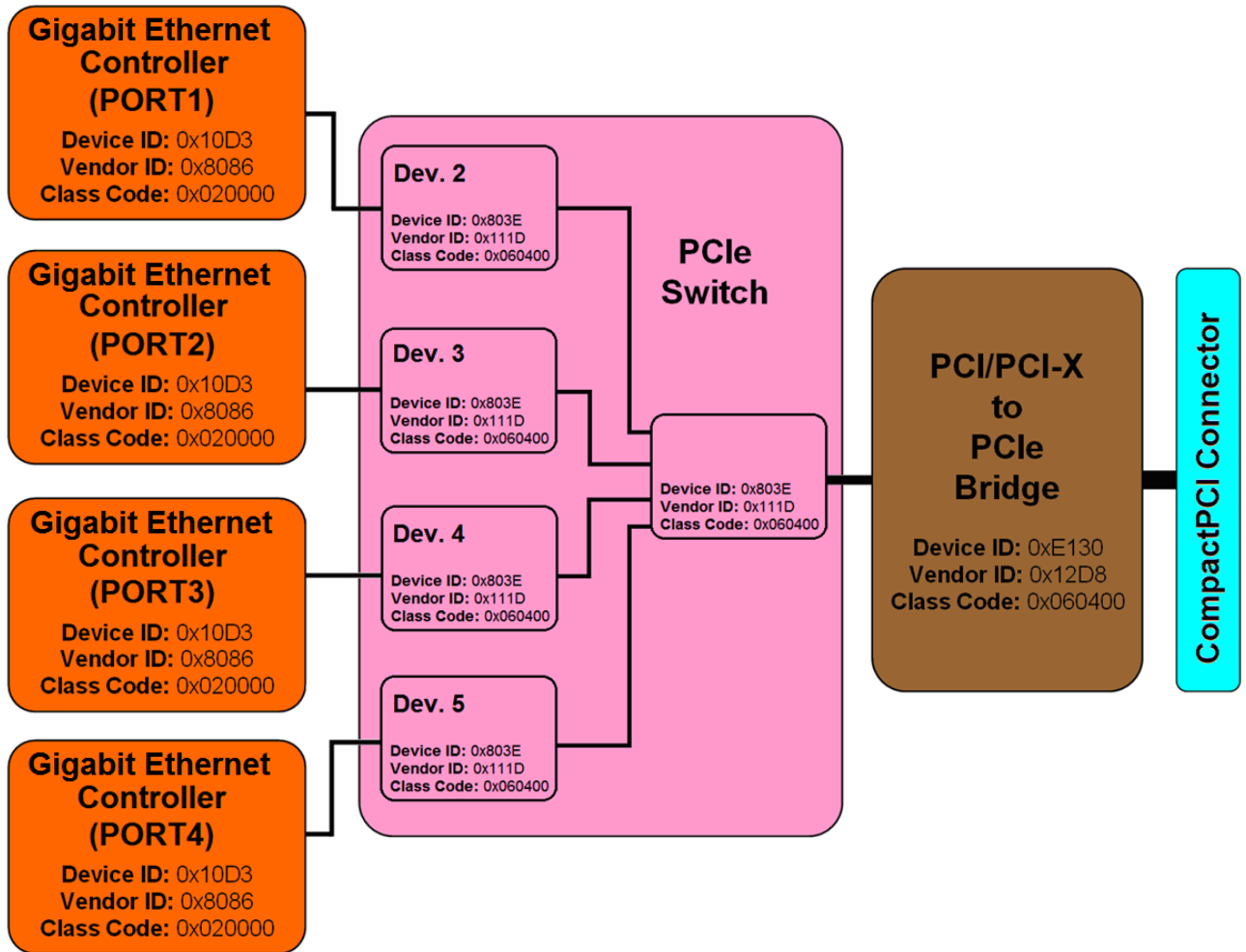

Figure 3-1 : PCI Device Topology

4 Gigabit Ethernet Controller

4.1 Intel 82574IT PCI Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								Initial Values (Hex Values)
	31	24	23	16	15	8	7	0	
0x00	Device ID				Vendor ID				10D3 8086
0x04	Status Register				Command Register				0010 0000
0x08	Class Code						Revision ID		020000 00
0x0C	BIST		Header Type		Latency Timer		Cache Line Size		00 00 00 10
0x10	Base Address 0 (Memory BAR)								FFFE0000 (128 KByte)
0x14	Base Address 1 (Flash BAR)								00000000
0x18	Base Address 2 (IO BAR)								FFFFFFE1 (32 Byte)
0x1C	Base Address 3 (MSI-X BAR)								FFFFC000 (16 KByte)
0x20	Base Address 4								00000000
0x24	Base Address 5								00000000
0x28	CardBus CIS Pointer								00000000
0x2C	Subsystem ID				Subsystem Vendor ID				0000 8086
0x30	Expansion ROM Base Address								00000000
0x34	Reserved						Cap_Ptr		000000 C8
0x38	Reserved								00000000
0x3C	Max_Latency		Min_Grant		Interrupt Pin		Interrupt Line		00 00 01 00

Table 4-1 : Intel 82574IT PCI Header

5 LEDs

The TCP885 provides four Status LEDs in the front panel for quick visual inspection and debugging. A marking is placed close to each LED, to indicate the Ethernet Port the LED corresponds to.

Each Ethernet Port has one LED indicator. See figures below for more details:

LED Status	Description
OFF	No cable is connected or no link is established
ON	A link is established at the corresponding Ethernet Port
BLINKING	Indicates activity: The Ethernet Port transmits or receives data

Table 5-1 : LED Status

6 Pin Assignment – I/O Connectors

On the TCP885 the Ethernet signals are accessible by four RJ45 Connectors. The connectors are located in the CompactPCI front panel.

For pin assignment, see the figures below.

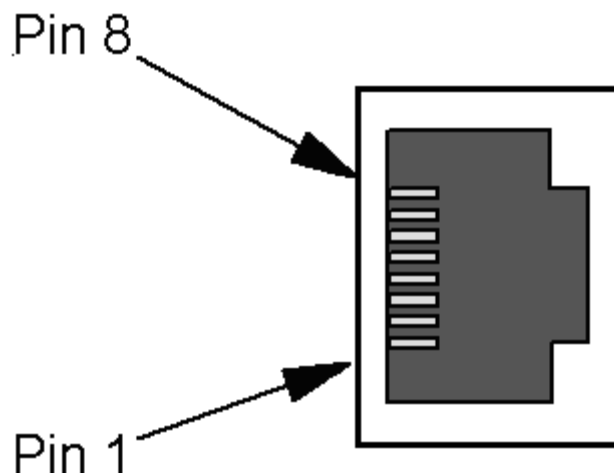| Pin	Signal (1000)	Signal (100, 10)
1	TX0/RX0+	TX+
2	TX0/RX0-	TX-
3	TX1/RX1+	RX+
4	TX2/RX2+	reserved
5	TX2/RX2-	reserved
6	TX1/RX1-	RX-
7	TX3/RX3+	reserved
8	TX3/RX3-	reserved

Table 6-1 : Front I/O pin assignment

Figure 6-1 : RJ45 Connector front view