The Embedded I/O Company

TEWS TECHNOLOGIES

TCPS010-TM

Rear I/O Module for CPCI-S.0 Carrier with 3 QMC Sites

Version 1.0

User Manual

Issue 1.0.0

June 2026

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TCPS010-TM-10R

Rear I/O Module for CPCI-S.0 Carrier with 3 QMC Sites

Document History

Issue	Description	Date
1.0.0	Initial Issue	June 2026

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1 Product Description

The TCPS010-TM is a PICMG CPCI-S.0 R3.0 compatible 3U rear I/O module.

The TCPS010-TM distributes the QMC IOPIPE signals of TEWS' QMC Carriers with rear I/O to three 50 pin ribbon cable box headers, compatible with TEWS standard cable kits. This makes the TCPS010-TM an ideal solution for prototyping CPCI-S.0 systems with QMC rear I/O, or it can be used as a base for custom rear-I/O solutions.

The operating temperature is -40°C to +85°C.

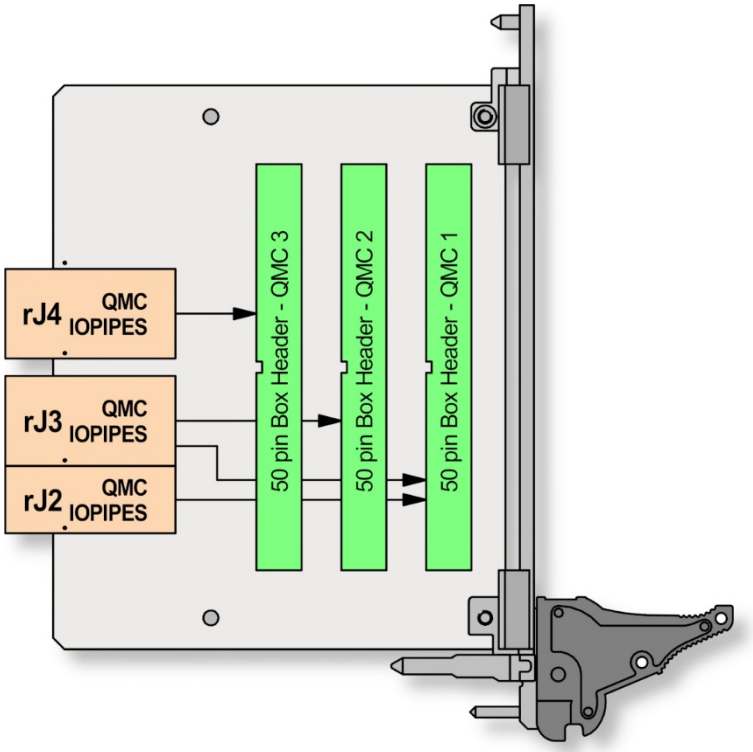

Figure 1-1 : Block Diagram

2 Technical Specification

General	
Mechanical Interface	Compact Serial 3U Rear Board conforming to PICMG CPCI-S.0 R2.0
Electrical Interface	Rear-I/O via rJ2, rJ3 and rJ4

I/O Interface	
IOPIPE Isolation	The TCPS010-TM provides IOPIPE Isolation: 30 V per IPC-2221 between IOPIPEs and 30 V per IPC-2221 against system ground
I/O Connectors	Box headers, 50 pin, 0.100" (2,54 mm)

Physical Data	
Power Requirements	none
Temperature Range	Operating -40 °C to +85 °C Storage -40 °C to +85 °C
MTBF	910 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	110 g

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This CPCI-S.0 module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care!

4 I/O Interface Description

4.1 Overview

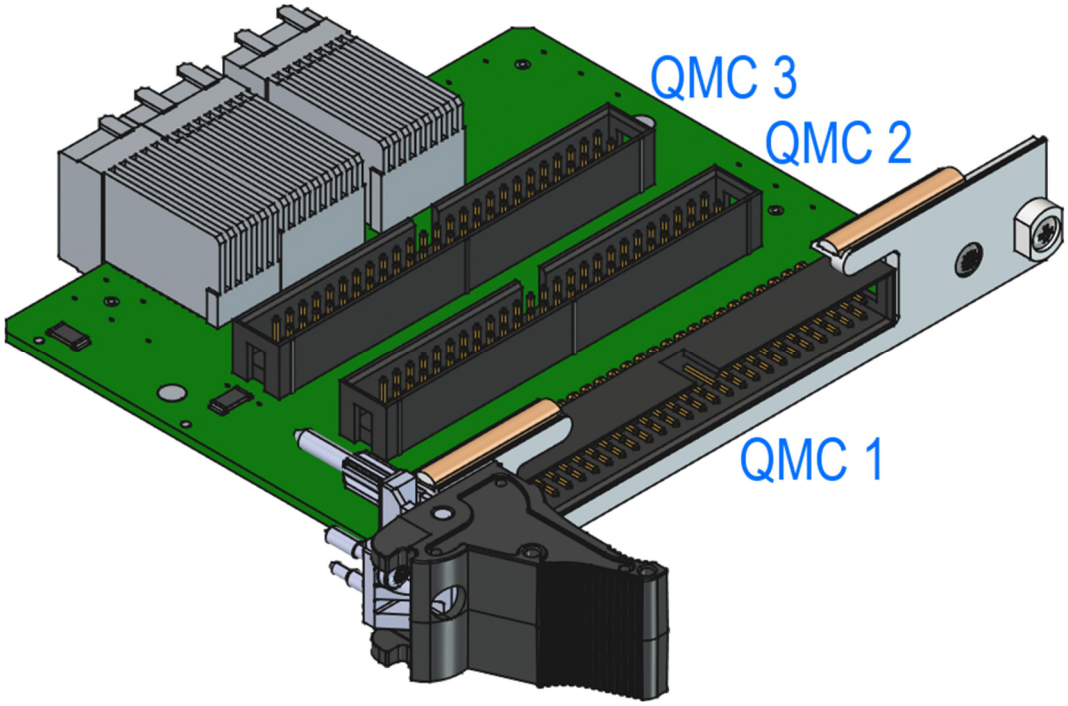

Figure 4-1 : Connector Overview

4.2 QMC IOPIPEs

The TCPS010-TM provides full access to all IOPIPEs of 3 QMCs and maintains the IOPIPE isolation if the carrier provides it.

4.3 CPCI-S.0 rJ2 Connector

4.3.1 Connector Type

Pin-Count	72
Connector Type	AirMax
Source & Order Info	FCI 10114633-101LF

4.3.2 rJ2 Pin Assignment

Pin	2 - 03	2 - 04	2 - 05	2 - 06	2 - 07	2 - 08
L	n.c.	IO1C-	n.c.	IO3A-	n.c.	IO4D-
K	-	IO1C+	IO2B-	IO3A+	GND4	IO4D+
J	-	n.c.	IO2B+	n.c.	GND4	n.c.
I	n.c.	IO1B-	n.c.	GND3	n.c.	IO4C-
H	-	IO1B+	IO2A-	GND3	IO3D-	IO4C+
G	-	n.c.	IO2A+	n.c.	IO3D+	n.c.
F	n.c.	IO1A-	n.c.	IO2D-	n.c.	IO4B-
E	-	IO1A+	GND2	IO2D+	IO3C-	IO4B+
D	-	n.c.	GND2	n.c.	IO3C+	n.c.
C	n.c.	GND1	n.c.	IO2C-	n.c.	IO4A-
B	-	GND1	IO1D-	IO2C+	IO3B-	IO4A+
A	-	n.c.	IO1D+	n.c.	IO3B+	n.c.
	n.c.	QMC 1				

Table 4-1: Peripheral Slot rJ2 Pin Assignment

4.4 CPCI-S.0 rJ3 & rJ4 Connector

4.4.1 Connector Type

Pin-Count	96
Connector Type	AirMax
Source & Order Info	FCI 10060905-101LF

4.4.2 rJ3 Pin Assignment

Pin	3 - 01	3 - 02	3 - 03	3 - 04	3 - 05	3 - 06	3 - 07	3 - 08
L	n.c.	GND1	n.c.	IO2C-	n.c.	IO4A-	n.c.	IO5D-
K	GND5	GND1	IO1D-	IO2C+	IO3B-	IO4A+	GND5	IO5D+
J	GND5	n.c.	IO1D+	n.c.	IO3B+	n.c.	GND5	n.c.
I	n.c.	-	n.c.	IO2B-	n.c.	GND4	n.c.	IO5C-
H	IO5D-	-	IO1C-	IO2B+	IO3A-	GND4	IO4D-	IO5C+
G	IO5D+	n.c.	IO1C+	n.c.	IO3A+	n.c.	IO4D+	n.c.
F	n.c.	-	n.c.	IO2A-	n.c.	IO3D-	n.c.	IO5B-
E	IO5C-	-	IO1B-	IO2A+	GND3	IO3D+	IO4C-	IO5B+
D	IO5C+	n.c.	IO1B+	n.c.	GND3	n.c.	IO4C+	n.c.
C	n.c.	IO5A-	n.c.	GND2	n.c.	IO3C-	n.c.	IO5A-
B	IO5B-	IO5A+	IO1A-	GND2	IO2D-	IO3C+	IO4B-	IO5A+
A	IO5B+	n.c.	IO1A+	n.c.	IO2D+	n.c.	IO4B+	n.c.
	QMC 1	QMC 2						

Table 4-2: Peripheral Slot rJ3 Pin Assignment

4.4.3 rJ4 Pin Assignment

Pin	4 - 01	4 - 02	4 - 03	4 - 04	4 - 05	4 - 06	4 - 07	4 - 08
L	n.c.	GND1	n.c.	IO2C-	n.c.	IO4A-	n.c.	IO5D-
K	-	GND1	IO1D-	IO2C+	IO3B-	IO4A+	GND5	IO5D+
J	-	n.c.	IO1D+	n.c.	IO3B+	n.c.	GND5	n.c.
I	n.c.	-	n.c.	IO2B-	n.c.	GND4	n.c.	IO5C-
H	-	-	IO1C-	IO2B+	IO3A-	GND4	IO4D-	IO5C+
G	-	n.c.	IO1C+	n.c.	IO3A+	n.c.	IO4D+	n.c.
F	n.c.	-	n.c.	IO2A-	n.c.	IO3D-	n.c.	IO5B-
E	-	-	IO1B-	IO2A+	GND3	IO3D+	IO4C-	IO5B+
D	-	n.c.	IO1B+	n.c.	GND3	n.c.	IO4C+	n.c.
C	n.c.	-	n.c.	GND2	n.c.	IO3C-	n.c.	IO5A-
B	-	-	IO1A-	GND2	IO2D-	IO3C+	IO4B-	IO5A+
A	-	n.c.	IO1A+	n.c.	IO2D+	n.c.	IO4B+	n.c.
		QMC 3						

Table 4-3: Peripheral Slot rJ4 Pin Assignment

4.5 QMC I/O Connector

Pin-Count	50
Connector Type	Male Box Header, 50 pin, 0.100" (2,54 mm)
Source & Order Info	Generic parts

The header for QMC 1 is a 90° header, the connectors for QMC 2 and QMC3 are normal box headers. The pin assignment is the same for all three connectors.

4.5.1 Pin Assignment

Pin	QMC I/O	QMC I/O	Pin
1	IO5D+	IO5D-	**2**
3	IO5C+	IO5C-	**4**
5	GND5	GND5	**6**
7	IO5B+	IO5B-	**8**
9	IO5A+	IO5A-	**10**
11	IO4D+	IO4D-	**12**
13	IO4C+	IO4C-	**14**
15	GND4	GND4	**16**
17	IO4B+	IO4B-	**18**
19	IO4A+	IO4A-	**20**
21	IO3D+	IO3D-	**22**
23	IO3C+	IO3C-	**24**
25	GND3	GND3	**26**
27	IO3B+	IO3B-	**28**
29	IO3A+	IO3A-	**30**
31	IO2D+	IO2D-	**32**
33	IO2C+	IO2C-	**34**
35	GND2	GND2	**36**
37	IO2B+	IO2B-	**38**
39	IO2A+	IO2A-	**40**
41	IO1D+	IO1D-	**42**
43	IO1C+	IO1C-	**44**
45	GND1	GND1	**46**
47	IO1B+	IO1B-	**48**
49	IO1A+	IO1A-	**50**

Table 4-4: QMC I/O Connector Pin Assignment