The Embedded I/O Company

TEWS TECHNOLOGIES

TCPS118

8 Channel SSI or Incremental Encoder and Counter Interface, RS-422/TTL I/O, 8x 24 V Input, 8x 24 V Output

Version 1.0

User Manual

Issue 1.0.0

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TCPS118-10R

8 Channel SSI or Incremental Encoder and Counter Interface, RS-422/TTL I/O, 8x 24 V Input, 8x 24 V Output

TCPS118-20R

8 Channel Incremental Encoder and Counter Interface, 24 V I/O, 8x 24 V Input, 8x 24 V Output

Document History

Issue	Description	Date
1.0.0	Initial Issue	May 2025

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1 Product Description

The TCPS118 is a PICMG CPCI-S.0 R2.0 compatible 3U module with eight isolated multifunction counter channels. Each channel can act as a general purpose or quadrature counter for incremental encoders, or as a SSI master. The capabilities of each channel are similar to a TPMC117 channel. All counter and SSI inputs are TTL/RS-422 compatible. Alternatively a 24 V input option is available, in this case only the counter functions are supported. The input signals pass a digital filter for noise suppression before they are further used.

In addition each channel provides an isolated 24 V digital input, and an isolated 24 V digital output, acting as a high-side switch that switches a externally provided 24 V supply voltage.

All I/O is available through a MDR-68 connector.

Software Support (TCPS118-SW-xx) for different operating systems is available.

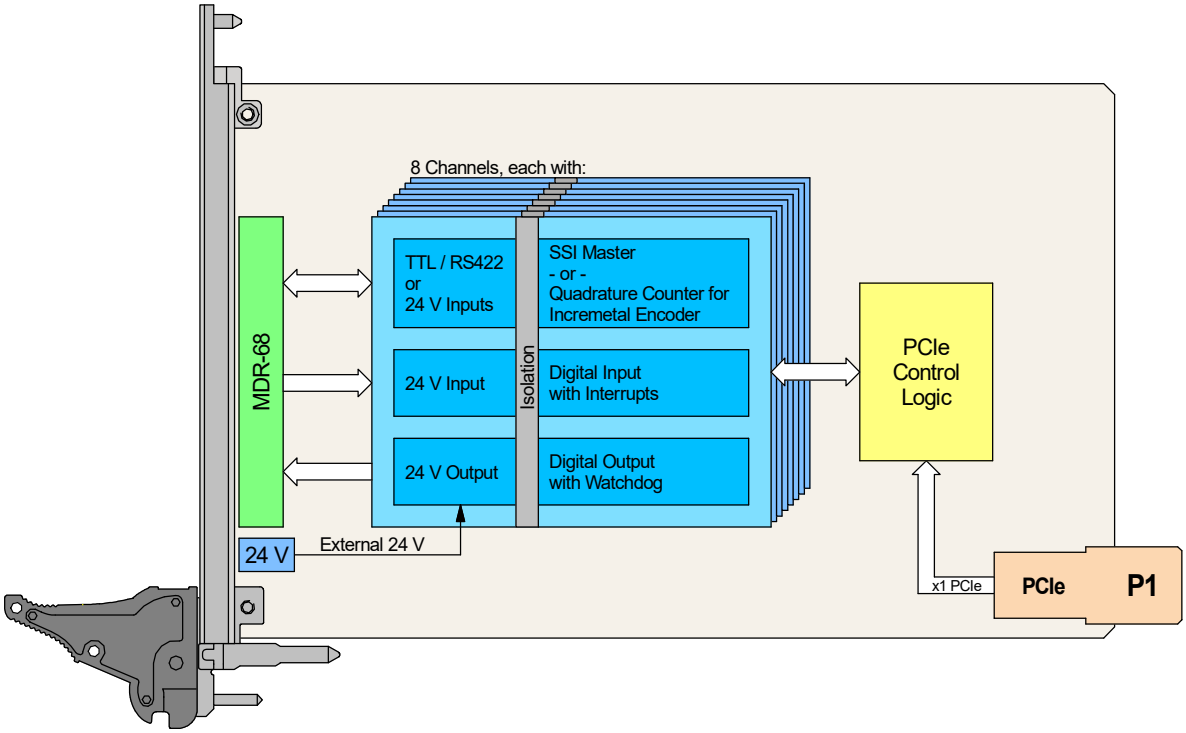

Figure 1-1 : Block Diagram

2 Technical Specification

General	
Mechanical Interface	Compact Serial 3U Front Board conforming to PICMG CPCI-S.0 R2.0
Electrical Interface	PCI Express (Base Specification 2.0) x1 compliant interface

Main On Board Devices	
I/O Transceiver	THVD2450
24 V Digital Inputs	ISO1212
24 V Digital Outputs	Si83404BAA

I/O Interface	
Number of Channels	8x Isolated Encoder / Counter Channels, with 1 input/output and 2 input lines: -10R: RS-485 or TTL single-ended -20R: 24 V 8x 24 V Digital Inputs 8x 24 V Digital Outputs
RS-485 Termination	Jumper-selectable 120 Ω
RS-485 / TTL Protection	±16 kV - Human Body Model Bus voltage: Up to ±25 V DC
24 V Digital Input Voltage	24 V DC typical
24 V Digital Input Current	2.5 mA @ 24 V input voltage
24 V Digital Input Switching Level	10.5 V typical, 8.5 V minimum, 11.5 V maximum (conforms to IEC 61131-2 Type 3)
24 V Digital Input Protection	±2 kV - Human Body Model
24 V Digital Output Current	Up to 600 mA per Output
24 V Digital Output Protection	±3 kV - Human Body Model Current limit and over temperature protection
I/O Connectors	Front I/O: Mini D Ribbon (MDR) Receptacle Connector, 68 pos. Micro-Fit 3.0 Dual-Row Header, 4 pos (External 24 V Supply)

Physical Data	
Power Requirements	200 mA typical @ +12 V DC (idle, or all channels are inputs) 280 mA typical @ +12 V DC (all channels SSI with 4 MHz clock, TTL) 400 mA typical @ +12 V DC (all channels SSI with 4 MHz clock, RS-485)
Temperature Range	Operating 0 °C to +70 °C Storage -40 °C to +125 °C
MTBF	-10R: 133000 h -20R: 420000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	154 g

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This CPCI-S.0 module is sensitive to static electricity. Packing, unpacking and all other module handling has to be done with the appropriate care!

3.2 Forced Air Cooling

This CPCI-S.0 module requires adequate forced air cooling!

3.3 Isolated I/O Ground

Isolated ground signals on the I/O connector must be connected to the corresponding external ground!

4 Terms and Definitions

4.1 Register Bit Access Types

Register Bit Access Type		Description
R	Read	The bit is readable by software (not writeable)
W	Write	The bit is writeable by software (not readable)
R/W	Read/Write	The bit is readable and writeable by software
R/C	Read/Clear	The bit is readable by software The bit is set by firmware Software may clear the bit by writing a '1'
R/S	Read/Set	The bit is readable by software Software may set this bit to '1' The bit is cleared by firmware

Table 4-1 : Register Bit Access Types

When reading reserved register bits, the read value is undefined.

For future software compatibility: For register write access, reserved bits shall be written '0'.

4.2 Signal Direction Types

Signal Direction Types as stated in Pin Assignment tables.

Signal Direction (Dir)	Description
I	TEWS card input Externally driven signal into the TEWS card
O	TEWS card output Signal driven out by TEWS card
I/O	Bi-Directional Signal
OD	TEWS card Open Drain output Signal driven low or tri-stated by TEWS card

Table 4-2 : Signal Direction Types

4.3 Style Conventions

Hexadecimal values are shown with prefix 0x (i.e. 0x029E).

Binary values are shown with prefix 0b (i.e. 0b0110).

"Active Low" signals are shown with a # suffix (i.e. RESET#).

5 Addressing

5.1 PCI Configuration Space

5.1.1 PCI Device Identification

	Offset	
Vendor ID	0x00	0x1498 (TEWS Technologies)
Device ID	0x02	0xB076 (TCPS118)
Revision ID	0x08	0x00
Class Code	0x09	0x118000 (Other Data Acquisition/Signal Processing Controllers)
Subsystem Vendor ID	0x2C	0x1498 (TEWS Technologies)
Subsystem ID	0x2E	0xB00A (TCPS118-10R) 0xB014 (TCPS118-20R)

Table 5-1 : PCI Device Identification

5.1.2 PCI Base Address Registers

BAR	Offset in PCI Config Space	Space Mapping	Size (Byte)	Prefetch	Port Width (Bit)	Endian Mode	Description
0	0x10	MEM	512	No	32	Little	Register Space

Table 5-2 : PCI Base Address Registers

5.2 Register Space

Offset to PCI BAR 0	Register Name	Size (Bit)
Global Control		
0x000	Global Control Register	32
0x004	Global Command Register	32
0x008	Global Status Register	32
0x00C	Watchdog Time Register	32
SSI / Encoder Channel 0		
0x010	SSI Mode Control Register 0	32
0x014	SSI Mode Status Register 0	32
0x018	Counter Mode Control Register 0	32
0x01C	Counter Mode Status Register 0	32
0x020	Counter Mode Preload Register 0	32
0x024	Counter Mode Compare Register 0	32
0x028	Counter Mode Command Register 0	32
0x02C	Debouncing Register 0	32
0x030	Data Register 0	32
0x034	Reserved	32

Offset to PCI BAR 0	Register Name	Size (Bit)
SSI / Encoder Channel 1		
0x038-05C	Same as “SSI / Encoder Channel 0”	32
SSI / Encoder Channel 2		
0x060-084	Same as “SSI / Encoder Channel 0”	32
SSI / Encoder Channel 3		
0x088-0AC	Same as “SSI / Encoder Channel 0”	32
SSI / Encoder Channel 4		
0x0B0-0D4	Same as “SSI / Encoder Channel 0”	32
SSI / Encoder Channel 5		
0x0D8-0FC	Same as “SSI / Encoder Channel 0”	32
SSI / Encoder Channel 6		
0x100-124	Same as “SSI / Encoder Channel 0”	32
SSI / Encoder Channel 7		
0x128-14C	Same as “SSI / Encoder Channel 0”	32
24 V Input and Output		
0x150	24 V Digital Input Register	32
0x154	24 V Digital Input Debounce Register	32
0x158	Reserved	32
0x15C	Reserved	32
0x160	24 V Digital Output Control Register	32
0x164	24 V Digital Output Register	32
0x168	24 V Digital Output Status Register	32
0x16C	Reserved	32
Interval Timer		
0x170	Interval Timer Control Register	32
0x174	Interval Timer Preload Register	32
0x178	Interval Timer Data Register	32
0x17C	Reserved	32
Interrupts		
0x180	Interrupt Enable Register	32
0x184	24 V Input Interrupt Enable Register	32
0x188	Interrupt Status Register	32
0x18C	24 V Input Interrupt Status Register	32
Multiple Channel Read		
0x190	Multiple Channel Read Data Register 0	32
0x194	Multiple Channel Read Data Register 1	32
0x198	Multiple Channel Read Data Register 2	32
0x19C	Multiple Channel Read Data Register 3	32
0x1A0	Multiple Channel Read Data Register 4	32
0x1A4	Multiple Channel Read Data Register 5	32
0x1A8	Multiple Channel Read Data Register 6	32
0x1AC	Multiple Channel Read Data Register 7	32

Offset to PCI BAR 0	Register Name	Size (Bit)
Board Level		
0x1B0-0x1EC	Reserved	32
0x1F0	Test Register	32
0x1F4	Board Health Register	32
0x1F8	Scratchpad Register	32
0x1FC	Firmware Version Register	32

Table 5-3 : Register Space Map

Most registers described here are individual for each channel. These are readily identifiable by a tailing “[x]”.

Addresses and register bits marked as “reserved” should be written as ‘0’. Read values can be arbitrary and should not be relied upon.

5.2.1 Global Control

5.2.1.1 Global Control Register

Bit	Symbol	Description	Access	Reset Value
31:27	-	Reserved, always reads as ‘0’	-	0
26	WD EN	Enable Watchdog 1 = Watchdog enabled 0 = Watchdog disabled	R/W	0
25	TST EN	Enable Test Register Outputs This enables the output driver of the RS-485 transceivers. The output values is controlled with the x_IO0 OUT bits in the Test Register. 1 = Test Register Outputs enabled 0 = Test Register Outputs disabled	R/W	0
24	MCR ITRIG	Interval Timer as trigger for Multiple Channel Read 1: Enable Interval Timer as trigger for Multiple Channel Read 0: Disable Interval Timer as trigger for Multiple Channel Read	R/W	0
23	MCR7	Enable Multiple Channel Read for the corresponding channel 1 = enables Multiple Channel Read 0 = disables Multiple Channel Read See chapter ’6.3 Multiple Channel Read’ for details.	R/W	0
22	MCR6			
21	MCR5			
20	MCR4			
19	MCR3			
18	MCR2			
17	MCR1			
16	MCR0			
15:14	MODE7	Interface Control MODE 11: Channel disabled 10: Counter Mode 01: SSI Mode 00: Channel disabled (the selection between normal SSI mode and SSI Listen-Only mode is done the SSI Mode Control Register)	R/W	00
13:12	MODE6			
11:10	MODE5			
9:8	MODE4			
7:6	MODE3			
5:4	MODE2			
3:2	MODE1			
1:0	MODE0			

Table 5-4 : Global Control Register

5.2.1.2 Global Command Register

Bit	Symbol	Description	Access	Reset Value
31:10	-	Reserved, always reads as ‘0’	-	0
9	MCR CLR	To reset a Multiple Channel Read sequence, write ‘1’ to this bit This also resets the “Multiple Channel Read Data Registers”	R/S	0
8	MCR TRIG	Multiple Channel Read Trigger By writing ‘1’ to this bit, a Multiple Channel Read is triggered. This is only valid for channels which are already enabled for a Multiple Channel Read.	R/S	0
7	LCNT7	Manual Counter Preload This is a copy of the LNCT bit in the Counter Mode Command Register that allows to preload multiple counter simultaneously. Writing a ‘1’ issues a preload of the corresponding counter with the value of the Counter Mode Preload Register. This preload method is only possible for channels in a ‘None Reference Mode’. Before using this preload method, the corresponding Counter Mode Preload Registers must be loaded with valid data	R/S	0
6	LCNT6			
5	LCNT5			
4	LCNT4			
3	LCNT3			
2	LCNT2			
1	LCNT1			
0	LCNT0			

Table 5-5 : Global Command Register

5.2.1.3 Global Status Register

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved, always reads as ‘0’	-	0
15	CCD7	Channel Config Detect RS-422/TTL I/O channels will be marked as ‘0’, 24 V Input channels will be marked as ‘1’	R	0
14	CCD6			
13	CCD5			
12	CCD4			
11	CCD3			
10	CCD2			
9	CCD1			
8	CCD0			
7:4	-	Reserved, always reads as ‘0’	-	0
3	WD LOCK	Watchdog Lock Flag 1 = indicates that the 24 V Digital Output channels have been disabled because the watchdog has expired. Also the 24 V Digital Output Register is locked. Writing ‘1’ to this bit unlocks the Output Register. As long as WD STD is ‘1’ this bit will also stay ‘1’. Reset the watchdog by disabling and enabling it before clearing this bit. 0 = signals normal operation	R/C	0
2	WD STD	Watchdog Status Flag 1 = indicates that the watchdog has expired and has disabled all 24 V Digital Output channels (WD LOCK is set). 0 = signals normal operation	R	0

Bit	Symbol	Description	Access	Reset Value
1:0	MCR STA	Multiple Channel Read Status 11 = A new Multiple Channel Read was triggered while data was still collected, or was not read out. Do a MCR CLR to clear this status. (= MCR OVERFLOW) 10 = Multiple Channel Read Data is valid (for all enabled channels) (= MCR READ PENDING) 01 = Multiple Channel Read was triggered, but data is still collected (= MCR BUSY) 00 = No pending Multiple Channel Read (= MCR IDLE)	R	0

Table 5-6 : Global Status Register

5.2.1.4 Watchdog Time Register

Enable the watchdog with WD EN in the Global Control Register. When enabled, the watchdog timer is loaded with WD TIME each time the Watchdog Time Register is written to (when freshly enabled, the timer needs one write to WD TIME to actually start). When the watchdog timer reaches zero, it is expired, and WD STD is set with the watchdog lock getting active, indicated with WD LOCK.

The watchdog timer can be reset by disabling and enabling it. The watchdog lock must be unlocked by clearing WD LOCK.

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved, always reads as ‘0’	-	0
15:0	WD TIME	Sets the time (in micro-seconds) that has to expire until the watchdog disables all outputs Retrigger the Watchdog by writing a new value.	R/W	0xFF

Table 5-7 : Watchdog Time Register

5.2.2 Channel Register

Each channel can be configured to be an SSI interface, or to work as an encoder counter. Each channel provides separate configuration registers for the SSI and encoder modes. Only the registers of the active mode are used, if a channel is set to SSI mode, the counter mode registers are ignored. The Debouncing Register and the Data Register are shared and active in both modes.

5.2.2.1 SSI Mode Control Register [x]

The control bits in this register are only valid when the channel works in SSI mode.

Bit	Symbol	Description	Access	Reset Value
31:27	SSI DELAY	When doing back-to-back transfers a delay can be configured. This can be used to satisfy the encoder timeout requirements. The delay is configurable in 10 µs steps: “11111” = 310 µs “01111” = 150 µs “00001” = 10 µs “00000” = 0 µs	R/W	0
26:25	SSI START	Method to start a SSI transmission 11 = Do back-to-back transmissions, with a delay configured in SSI DELAY. The delay is timed from the end of a transmission. 10 = Do back-to-back transmissions, with a delay configured in SSI DELAY. The delay is timed from the start of a transmission (thus resulting in an equidistant timing). The sensors timeout (or recovery) requirements must be taken into account. 01 = Use the Interval Timer as trigger for a SSI transmission 00 = A write to the Data Register or a Multiple Channel Read triggers a SSI transmission	R/W	0
24	SSI MODE	1 = SSI Listen-Only Mode 0 = Standard SSI Interface Controller	R/W	0
23	CODE	SSI Data word coding 1 = Gray Code The transferred data word is converted from gray into binary code. The gray code conversion only applies to the data bits 0 = Binary Code	R/W	0
22	EO	Controls the parity detection 1 = odd parity 0 = even parity This bit is ignored if PAR is set to ‘0’.	R/W	0
21:20	PAR	When the encoder provides a parity bit an additional bit is transferred and evaluated as parity bit. 11 = detect parity errors for data & zero bits 10 = detect parity errors for zero bits 01 = detect parity errors for data bits 00 = do not detect parity errors / no parity bit	R/W	0
19:17	ZB	Number of additional bits that are transferred besides the in DB configured data bits. These are encoder dependent and can be e.g. warning or alarm bits, general status or zero bits. ZB = “111” = 7 bits ZB = “001” = 1 bits ZB = “000” = 0 bits	R/W	0

Bit	Symbol	Description	Access	Reset Value
16:12	DB	Number of Data Bits Used to configure the number of data bits in a SSI transmission. Number of bits it DB + 1. DB = 0x1F = 32 bit DB = 0x00 = 1 bit The Parity and Zero bits are not included in this count.	R/W	0
11:0	CR	SSI Clock Rate The SSI Clock Rate will be this value in kHz. Observe the minimal clock rate for you encoder. A value of 0 will result in no clock output.	R/W	0

Table 5-8 : SSI Mode Control Register

5.2.2.2 SSI Mode Status Register [x]

The status bits in this register are only valid when the channel works in SSI mode.

Bit	Symbol	Description	Access	Reset Value
31:17	-	Reserved, always reads as ‘0’	-	0
16	WHILE BUSY	A transmission request was issued while SENSOR STATUS was still ‘1’. The transmission request was ignored, no new data is provided. After the next valid transmission request this bit is reset to ‘0’	R	0
15	SENSOR STATUS	1 = Sensor communication is active. This includes the recovery time. 0 = Sensor communication is idle	R	0
14:12	LISTEN STATUS	Provides status bits for the SSI Listen-Only mode: 100 = the last received transmission had more clock pulses than anticipated 010 = Transmission received OK 001 = the last received transmission had less clock pulses than anticipated	R	0
11:4	ZB STATUS	When enabled the additional ZB are shown here	R	0
3	FAULT	This bit indicates data line faults and loss of communication which can indicate a defective sensor. It is updated after each data transmission. 1 = Data line fault detected 0 = No data line fault detected	R	0
2	PARITY STATUS	If enabled the additional parity bit is shown here. This is the raw bit value without interpretation.	R	0
1	PRY	Parity Error 1 = Parity Error at the last data transmission 0 = No Parity Error at the last data transmission During a transmission the parity error bit is not valid. The parity error status is updated only if the parity enable bit of the corresponding channel is set to ‘1’. Otherwise the parity status is read as ‘0’.	R	0

Bit	Symbol	Description	Access	Reset Value
0	BSY	Busy Bit 0 = Data Ready (set after every completed transmission, even if a parity or a read error was issued) In Standard SSI Interface Controller mode Busy Bit = ‘1’ indicates a transmission in progress. In SSI Listen-Only Mode the Busy Bit is set to ‘1’ when the SSI Listen-Only mode is armed. It is set to '0' when a transmission was received and stays '0' until the data word was read.	R	0

Table 5-9 : SSI Mode Status Register

5.2.2.3 Counter Mode Control Register [x]

The control bits in this register are only valid when the channel works in counter mode.

Bit	Symbol	Description	Access	Reset Value
31:15	-	Reserved, always reads as ‘0’	-	0
14	SLE	Status Latch Enable When set to ‘1’, a “Data Register” read latches the “Counter Mode Status Register”. This way a status that is accompanying a data value can be read. After the “Counter Mode Status Register” is read once, the “Counter Mode Status Register” shows an unlatched status. New “Data Register” reads latch a new status. When set to ‘0’, the “Counter Mode Status Register” is not latched and always shows the actual status.	R/W	0
13	POL I	A,B,I Polarity The Input Polarity Control can be used to adapt the input to the input source polarity. 1 = low active 0 = high active	R/W	0
12	POL B		R/W	0
11	POL A		R/W	0
10:8	ICM	Index Control Mode The Index Control Mode determines how the counter interprets events on the I-input. Reference modes are only valid when Input Mode = Quadrature Count Reference Modes: 111 = Index Mode 110 = Auto Reference Mode 101 = Reference mode Non-Reference Modes: 100 = Reset on I 011 = Gate on I 010 = Latch on I 001 = Load on I 000 = Ignore I-input See chapter ’6.2.3 Index Control Modes’ for details.	R/W	0
7:6	SCM	Special Count Mode 10 = Single Cycle 01 = Divide-by-N 00 / 11 = No special mode active / cycling counter See chapter ’6.2.2 Special Count Modes’ for details.	R/W	0

Bit	Symbol	Description	Access	Reset Value
5:3	CLKDIV	Internal Base Clock 111 = 100 MHz 110 = 50 MHz 101 = 20 MHz 100 = 10 MHz 011 = 5 MHz 010 = 4 MHz 001 = 2 MHz 000 = 1 MHz	R/W	0
2:0	INPUT	Counter Input Mode The Input Mode determines the input source and how the counter interprets these input signals. The Quadrature mode can be used with a 1x, 2x or 4x resolution multiplier. 111 = Quadrature Count 4x with Input A & Input B 110 = Quadrature Count 2x with Input A & Input B 101 = Quadrature Count 1x with Input A & Input B 100 = Up/Down Count with Input A & Input B 011 = Direction Count with Input A & Input B 010 = Timer Mode Down with Internal Clock (CLKDIV) 001 = Timer Mode Up with Internal Clock (CLKDIV) 000 = Counter disabled - See chapter ’6.2.1 Input Modes’ for details.	R/W	0

Table 5-10 : Counter Mode Control Register

5.2.2.4 Counter Mode Status Register [x]

The status bits in this register are only valid when the channel works in counter mode.

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved, always reads as ‘0’	-	0
7	SGL	Single Cycle active In Single Cycle counting mode this bit is set to ‘1’ when the counter is active. It is reset to ‘0’, when the counter has counted down to zero.	R	0
6	OVFL	Data Register Latch Overflow When a Latch Mode event occurs while the Data Register Lock is still active, the data in the Data Register will be retained and this bit will be set to indicate that data was lost. This bit must be reset by writing a ‘1’ to this bit.	R/C	0
5	DRL	Data Register Latch This bit is set to '1', when the Data Register is locked due to a 'Latch on I' or a Multiple Channel Read. This bit is cleared after a read access to the Data Register or by writing a '1' to this bit.	R/C	0
4	DIR	Count Direction This bit indicates the counting direction of the counter. '1' indicates up, '0' indicates down. In the 'Up/Down Count' mode this bit indicates the direction at the last count. In the 'Direction Count' mode this bit corresponds to the B-input.	R	0
3	SGN	Sign The Sign bit is set to '1' when the counter overflows, and is set to '0' when the counter underflows. After reset or power-up this bit should be considered as "don't care" until the first Carry or Borrow occurred.	R	0

Bit	Symbol	Description	Access	Reset Value
2	MAT	Match This bit is set to '1' when the counter value matches the value of the Counter Mode Compare Register. This bit must be reset by writing a ‘1’ to this bit.	R/C	0
1	CRY	Carry This bit is set to '1' when the counter changes from 0xFFFFFFFF to 0x00000000. This bit must be reset by writing a ‘1’ to this bit.	R/C	0
0	BOR	Borrow This bit is set to '1' when the counter changes from 0x00000000 to 0xFFFFFFFF. This bit must be reset by writing a ‘1’ to this bit.	R/C	0

Table 5-11 : Counter Mode Status Register

5.2.2.5 Counter Mode Preload Register [x]

Bit	Symbol	Description	Access	Reset Value
31:0	-	Counter Mode Preload Register The value of this register can be loaded into the counter by: - Setting the LCNT bit in the Counter Mode Command Register - An impulse on the I-input when the 'Load on I'-mode is active - Automatically in the 'Divide-by-N'-mode every time the counter creates a borrow or a carry - Reference modes	R/W	0

Table 5-12 : Counter Mode Preload Register

5.2.2.6 Counter Mode Compare Register [x]

Bit	Symbol	Description	Access	Reset Value
31:0	-	Counter Mode Compare Register Every time the counter matches the Counter Mode Compare Register value, the MAT bit in the Counter Mode Status Register is set to ‘1' and, if enabled, an interrupt is generated.	R/W	0

Table 5-13 : Counter Mode Compare Register

5.2.2.7 Counter Mode Command Register [x]

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved, always reads as ‘0’	-	0
1	LCNT	Load Counter Write ‘1’ to load the counter with the value of the Counter Mode Preload Register.	R/S	0
0	RCNT	Reset Counter Write ‘1’ to reset the counter	R/S	0

Table 5-14 : Counter Mode Command Register

5.2.2.8 Debouncing Register [x]

To avoid false signals caused by noisy input signals, the inputs are digitally filtered. This filter is a typical 3-stage debounce circuit. To address input sources such as mechanical switches with longer bouncing times, the debouncing can be configured here. By default, when DEB TIME is 0, it runs with a 100 MHz sampling clock, resulting in input signals shorter ~30 ns being suppressed. When DEB TIME is not 0, it runs with the selected time base.

This settings is valid for both SSI and counter modes.

Bit	Symbol	Description	Access	Reset Value
31:18	-	Reserved, always reads as '0'	-	0
17:16	DEB BASE	Time base used for the input filter 11 = use 1 ms time base 10 = use 1 µs time base 01 = use 100 ns time base 00 = use 30 ns time base	R/W	0
15:0	DEB TIME	These bits set the filter time together with the time base set by DEB BASE. Filter time is ~DEB TIME * DEB BASE * 3-stages A value of zero effectively turns the debouncer off, only the 3-stage input circuit remains.	R/W	1

Table 5-15 : Debouncing Register

5.2.2.9 Data Register [x]

When the channel is disabled, the Data Register returns 0x00000000 on read accesses.

Depending on the MODEx setting, this register contains the SSI or the counter readings.

SSI Mode

In Standard SSI Interface mode a write access to the Data Register initiates a data transfer from the absolute encoder independently of the other channels.

In SSI Listen-Only Interface mode a read access to the Data Register sets the Busy bit to '1' and the channel is listening again.

The data register may not contain valid data, if the SSI transmission is in progress (the corresponding Busy bit is read as '1').

Counter Mode

The Data Register contains the actual counter value.

While a Multiple Channel Read is in progress, this register may contain latched data. In 'Latch on I' control mode this register contains latched data after a control mode event. See chapter '6.2.4 Data Register Lock' for details.

Bit	Symbol	Description	Access	Reset Value
31:0		Data Register	R	0

Table 5-16 : Data Register

5.2.3 24 V Digital Input & Output

5.2.3.1 24 V Digital Input Register

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved, always reads as ‘0’	-	0
7	DI7	These bits reflect the actual state of the digital 24 V inputs. In “Reference Mode” and “Auto Reference Mode” the digital 24 V inputs are used as reference inputs. In all other modes the digital 24 V inputs can be used as general purpose inputs.	R	0
6	DI6			
5	DI5			
4	DI4			
3	DI3			
2	DI2			
1	DI1			
0	DI0			

Table 5-17 : 24 V Digital Input Register

5.2.3.2 24 V Digital Input Debouncing Register

To avoid false signals caused by noisy input signals, the inputs are digitally filtered. This filter is a typical 3-stage debounce circuit. To address input sources such as mechanical switches with longer bouncing times, the debouncing can be configured here. By default, when DEB TIME is 0, it runs with a 100 MHz sampling clock, resulting in input signals shorter ~30 ns being suppressed. When DEB TIME is not 0, it runs with the selected time base.

Bit	Symbol	Description	Access	Reset Value
31	DI7 ADE	Debouncing Enable Allows to enable the debouncing on a per channel basis 1 = Enable Debouncing 0 = Use default Debouncing (3-stage debouncing, ~30 ns)	R/W	0
30	DI6 ADE			
29	DI5 ADE			
28	DI4 ADE			
27	DI3 ADE			
26	DI2 ADE			
25	DI1 ADE			
24	DI0 ADE			
23:18	-	Reserved, always reads as ‘0’	-	0
17:16	DEB BASE	Time base used for the input filter 11 = use 1 ms time base 10 = use 1 µs time base 01 = use 100 ns time base 00 = use 30 ns time base	R/W	0
15:0	DEB TIME	These bits set the filter time together with the time base set by DEB BASE. Filter time is ~DEB TIME * DEB BASE * 3-stages A value of zero effectively turns the debouncer off, only the 3-stage input circuit remains.	R/W	1

Table 5-18 : 24 V Digital Input Debouncing Register

5.2.3.3 24 V Digital Output Control Register

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved, always reads as ‘0’	-	0
1	DOEN47	Enable output for channels 4-7 1 = outputs enabled 0 = outputs disabled	R/W	0
0	DOEN03	Enable output for channels 0-3 1 = outputs enabled 0 = outputs disabled	R/W	0

Table 5-19 : 24 V Digital Output Control Register

5.2.3.4 24 V Digital Output Register

The 24 V digital output act as high-side switches that switch a externally provided 24 V supply voltage to the output pins.

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved, always reads as ‘0’	-	0
7	DO7	These bits set the 24 V digital outputs: 1 = 24 V digital output enabled (switch is ON) 0 = 24 V digital output disabled (switch is OFF)	R/W	0
6	DO6			
5	DO5			
4	DO4			
3	DO3			
2	DO2			
1	DO1			
0	DO0			

Table 5-20 : 24 V Digital Output Register

5.2.3.5 24 V Digital Output Status Register

In this register FLTxx and WRNxx are hardware status bits set by the output switch. The following table shows an overview over the signaled status. Regard FLTxx as an OR of the various fault conditions.[1]

Descripton	Condition	WRNxx	FLTxx	Output Switch
External Supply is within limits	18 V < EXT_24V < 32 V	0	0	Normal
Low-Voltage Warning	9 V < EXT_24V < 18 V	1	0	Normal
Undervoltage Shutdown	EXT_24V < 9 V	1	1	Turns Off
Overvoltage Constraint	32 V < EXT_24V	0	1	Normal, but Clamps are active
Over-Temperature	Device Temperature > 150 °C	0	1	Turns Off
Over-Current	Switch current > 1 A	0	1	Turns Off

Table 5-21 : 24 V Digital Output Switch Status Bits

Bit	Symbol	Description	Access	Reset Value
31:12	-	Reserved, always reads as ‘0’	-	0
11	FLT47	Fault indicator for channels 4-7 This is a hardware status bit that is set as long the output switch indicates a fault (supply error, over-temperature or over-current)	R	0
10	WRN47	“EXT_24V Low-Voltage Warning” for channels 4-7. This is a hardware status bit that is set as long as the 24 V supply is not within normal parameters	R	0
9	FLT03	Fault indicator for channels 0-3 This is a hardware status bit that is set as long the output switch indicates a fault (supply error, over-temperature or over-current)	R	0
8	WRN03	“EXT_24V Low-Voltage Warning” for channels 0-3. This is a hardware status bit that is set as long as the 24 V supply is not within normal parameters	R	0
7	DOS7	Output status indicators. Shows the true ON or OFF state of an output	R	0
6	DOS6			
5	DOS5			
4	DOS4			
3	DOS3			
2	DOS2			
1	DOS1			
0	DOS0			

Table 5-22 : 24 V Digital Output Status Register

[1] Due to a hardware limitation the flag description is only valid when the EXT_24V is powered, or was at least powered once. If the TCPS118 is powered on while EXT_24V is off, WRN will be 1 and the FLT flag will change between 0 and 1 with a frequency of 10 Hz. Once EXT_24V is powered on, the above description is valid.

5.2.4 Interval Timer

5.2.4.1 Interval Timer Control Register

Bit	Symbol	Description	Access	Reset Value
31:4	-	Reserved, always reads as ‘0’	-	0
2:1	ITTB	Interval Timer Time Base 11 = 1 s 10 = 1 ms 01 = 1 µs 00 = 100 ns	R/W	0
0	ITEN	Interval Timer Enable '1' enables the Interval Timer '0' disables the Interval Timer	R/W	0

Table 5-23 : Interval Timer Control Register

5.2.4.2 Interval Timer Preload Register

Bit	Symbol	Description	Access	Reset Value
31:0	ITPRE	Interval Timer Preload Register Interval time is ITPRE x ITTB	R/W	0

Table 5-24 : Interval Timer Preload Register

5.2.4.3 Interval Timer Data Register

Bit	Symbol	Description	Access	Reset Value
31:0	ITDR	Interval Timer Data Register This register contains the actual Interval Timer Value.	R	0

Table 5-25 : Interval Timer Data Register

5.2.5 Interrupts

5.2.5.1 Interrupt Enable Register

For pending interrupts and interrupt acknowledge see the Interrupt Status Register. Configure the Interrupt Acknowledge Configuration with IRQ ACK CONFIG.

Bit	Symbol	Description	Access	Reset Value
31	IRQ ACK CONFIG	Interrupt Acknowledge Configuration 1 = Interrupts are cleared when the Interrupt Status Register is read 0 = Interrupts are cleared by writing '1' to the appropriate bit in the Interrupt Status Register	R/W	0
30:21	-	Reserved, always reads as '0'	-	0
20	TIEN	Interval Timer Interrupt 1 = Interval Timer Interrupt enabled 0 = Interval Timer Interrupt disabled A Timer Interrupt is generated when the Interval Timer reaches zero	R/W	0
19	FLT47 EN	24 V Digital Output Fault Interrupt for channels 4-7 1 = 24 V Digital Output Fault Interrupt enabled 0 = 24 V Digital Output Fault Interrupt disabled A Fault Interrupt is generated when the FLT47 bit in the 24 V Digital Output Status Register is set	R/W	0
18	FLT03 EN	24 V Digital Output Fault Interrupt for channels 3-0 1 = 24 V Digital Output Fault Interrupt enabled 0 = 24 V Digital Output Fault Interrupt disabled A Fault Interrupt is generated when the FLT03 bit in the 24 V Digital Output Status Register is set	R/W	0
17	WRN47 EN	24 V Digital Output EXT_24V Low-Voltage Warning Interrupt for channels 4-7 1 = EXT_24V Low-Voltage Warning Interrupt enabled 0 = EXT_24V Low-Voltage Warning Interrupt disabled A Fault Interrupt is generated when the WRN47 bit in the 24 V Digital Output Status Register is set	R/W	0
16	WRN03 EN	24 V Digital Output EXT_24V Low-Voltage Warning Interrupt for channels 3-0 1 = EXT_24V Low-Voltage Warning Interrupt enabled 0 = EXT_24V Low-Voltage Warning Interrupt disabled A Fault Interrupt is generated when the WRN03 bit in the 24 V Digital Output Status Register is set	R/W	0

Bit	Symbol	Description	Access	Reset Value
15	FCM EN7	This bit is MODE dependent. SSI: This bit enables the SSI Fault Interrupt. An interrupt will be generated when a data line fault is detected and the FAULT bit in the SSI Mode Status Register is set to '1'. Counter: This bit enables Control Mode Interrupt. An interrupt will be generated on a control mode event. 1 = SSI Fault / Control Mode Interrupt enabled 0 = SSI Fault / Control Mode Interrupt disabled	R/W	0
14	FCM EN6			
13	FCM EN5			
12	FCM EN4			
11	FCM EN3			
10	FCM EN2			
9	FCM EN1			
8	FCM EN0			
7	VCM EN7	This bit is MODE dependent. SSI: This bit enables the SSI Data Valid Interrupt. An interrupt will be generated when a SSI transmission completes and the BSY bit in the SSI Mode Status Register is set to '0'. Counter: This bit enables Counter Match Interrupt. An interrupt will be generated when the counter value reaches the value of the Counter Mode Compare Register. 1 = SSI Data Valid / Counter Match Interrupt enabled 0 = SSI Data Valid / Counter Match Interrupt disabled	R/W	0
6	VCM EN6			
5	VCM EN5			
4	VCM EN4			
3	VCM EN3			
2	VCM EN2			
1	VCM EN1			
0	VCM EN0			

Table 5-26 : Interrupt Enable Register

5.2.5.2 24 V Inputs Interrupt Enable Register

For pending interrupts and interrupt acknowledge see the Interrupt Status Register. Configure the Interrupt Acknowledge Configuration in the Global Control Register.

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved, always reads as '0'	-	0
15	DI7 FIRQ	Digital Input Interrupt Control Enables interrupt on falling edge for the corresponding 24 V digital input. 1 = selects interrupt for falling edge 0 = deselects interrupt for falling edge	R/W	0
14	DI6 FIRQ			
13	DI5 FIRQ			
12	DI4 FIRQ			
11	DI3 FIRQ			
10	DI2 FIRQ			
9	DI1 FIRQ			
8	DI0 FIRQ			
7	DI7 RIRQ	Digital Input Interrupt Control Enables interrupt on rising edge for the corresponding 24 V digital input. 1 = selects interrupt for rising edge 0 = deselects interrupt for rising edge	R/W	0
6	DI6 RIRQ			
5	DI5 RIRQ			
4	DI4 RIRQ			
3	DI3 RIRQ			
2	DI2 RIRQ			
1	DI1 RIRQ			
0	DI0 RIRQ			

Table 5-27 : 24 V Input Interrupt Enable Register

5.2.5.3 Interrupt Status Register

The interrupt status is updated only if the interrupt enable bit of the corresponding channel is set to ‘1’. Otherwise the interrupt status is read as ‘0’.

Bit	Symbol	Description	Access	Reset Value
31:22	-	Reserved, always reads as ‘0’	-	0
21	EDGE STA	Pending 24 V Input Edge Interrupt This is a OR for all bits in the 24 V Input Interrupt Status Register. Acknowledge pending interrupts there.	R	0
20	TISTA	Pending Interval Timer Interrupt (Read), Interrupt acknowledge (Write) On a read-access this bit indicates a pending Interval Timer interrupt. A '1' indicates a pending interrupt. The interrupt is acknowledged by writing a '1' to this bit.	R/C	0
19	FLT47 STA	Pending 24 V Digital Output Fault Interrupt for channels 4-7 (Read), Interrupt acknowledge (Write) On a read-access this bit indicates a pending 24 V Digital Output Fault Interrupt for channels 4-7. A '1' indicates a pending interrupt. The interrupt is acknowledged by writing a '1' to this bit.	R/C	0
18	FLT03 STA	Pending 24 V Digital Output Fault Interrupt for channels 3-0 (Read), Interrupt acknowledge (Write) On a read-access this bit indicates a pending 24 V Digital Output Fault Interrupt for channels 3-0. A '1' indicates a pending interrupt. The interrupt is acknowledged by writing a '1' to this bit.	R/C	0
17	WRN47 STA	Pending 24 V Digital Output EXT_24V Low-Voltage Warning Interrupt for channels 4-7 (Read), Interrupt acknowledge (Write) On a read-access this bit indicates a pending 24 V Digital Output EXT_24V Low-Voltage Warning Interrupt for channels 4-7. A '1' indicates a pending interrupt. The interrupt is acknowledged by writing a '1' to this bit.	R/C	0
16	WRN03 STA	Pending 24 V Digital Output EXT_24V Low-Voltage Warning Interrupt for channels 0-3 (Read), Interrupt acknowledge (Write) On a read-access this bit indicates a pending 24 V Digital Output EXT_24V Low-Voltage Warning Interrupt for channels 0-3. A '1' indicates a pending interrupt. The interrupt is acknowledged by writing a '1' to this bit.	R/C	0

Bit	Symbol	Description	Access	Reset Value
15	FCM STA7	This bit is MODE dependent. SSI: Pending SSI Fault Interrupt (Read). On a read-access this bit indicates a pending SSI Fault Interrupt. A '1' indicates a pending interrupt. Counter: Pending Control Mode Interrupt. On a read-access this bit indicates a pending Control Mode Interrupt. A '1' indicates a pending interrupt. Interrupt acknowledge (Write) The interrupt is acknowledged by writing a '1' to this bit.	R/C	0
14	FCM STA6			
13	FCM STA5			
12	FCM STA4			
11	FCM STA3			
10	FCM STA2			
9	FCM STA1			
8	FCM STA0			
7	VCM STA7	This bit is MODE dependent. SSI: Pending SSI Data Valid Interrupt (Read). On a read-access this bit indicates a pending SSI Data Valid Interrupt. A '1' indicates a pending interrupt. Counter: Pending Counter Match Interrupt. On a read-access this bit indicates a pending Counter Match Interrupt. A '1' indicates a pending interrupt. Interrupt acknowledge (Write) The interrupt is acknowledged by writing a '1' to this bit.	R/C	0
6	VCM STA6			
5	VCM STA5			
4	VCM STA4			
3	VCM STA3			
2	VCM STA2			
1	VCM STA1			
0	VCM STA0			

Table 5-28 : Interrupt Status Register

5.2.5.4 24 V Input Interrupt Status Register

The interrupt status is updated only if the interrupt enable bit of the corresponding channel is set to ‘1’. Otherwise the interrupt status is read as ‘0’.

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved, always reads as ‘0’	-	0
15	FI STA7	Pending 24 V Input Falling Edge Interrupt (Read), Interrupt acknowledge (Write) On a read-access these bits indicate the channels with pending 24 V Input Falling Edge interrupts. A '1' indicates a pending interrupt. The interrupts are acknowledged by writing a '1' to the according bit.	R/C	0
14	FI STA6			
13	FI STA5			
12	FI STA4			
11	FI STA3			
10	FI STA2			
9	FI STA1			
8	FI STA0			
7	RI STA7	Pending 24 V Input Rising Edge Interrupt (Read), Interrupt acknowledge (Write) On a read-access these bits indicate the channels with pending 24 V Input Rising Edge interrupts. A '1' indicates a pending interrupt. The interrupts are acknowledged by writing a '1' to the according bit.	R/C	0
6	RI STA6			
5	RI STA5			
4	RI STA4			
3	RI STA3			
2	RI STA2			
1	RI STA1			
0	RI STA0			

Table 5-29 : 24 V Input Interrupt Status Register

5.2.6 Multiple Channel Read

For Multiple Channel Reads the latched data can be read here. In this way the channel's data register is not blocked by a Multiple Channel Read, also the data can be read in a consecutive way. Each channel has its own Multiple Channel Read Data Register. Only enabled channels are latched here. The data is latched until all enabled channel are read, or the Multiple Channel Read is reset with MCRCLR.

Enable and monitor a Multiple Channel Read in the Global Control and Command Registers.

5.2.6.1 Multiple Channel Read Data Register [x]

Bit	Symbol	Description	Access	Reset Value
31:0	-	MCR Data Register	R/W	0

Table 5-30 : Multiple Channel Read Data Register

5.2.7 Board Level

5.2.7.1 Test Register

This register allows quick testing of the RS-422/TTL in- and outputs. To check the 24 V digital input levels read the 24 V Digital Input Register. To check the 24 V digital outputs, use the 24 V Digital Output registers.

Bit	Symbol	Description	Access	Reset Value
31	7_IO0 OUT	RS-485 transceiver outputs. When TST EN in the Global Control Register is '1', the output drivers of the RS-485 transceivers are enabled and these bits will control the output level of the x_IO0 signals. When TST EN in the Global Control Register is '0', the output drivers of the RS-485 transceivers are controlled by the MODE setting and these bits have no effect.	R/W	0
30	6_IO0 OUT			
29	5_IO0 OUT			
28	4_IO0 OUT			
27	3_IO0 OUT			
26	2_IO0 OUT			
25	1_IO0 OUT			
24	0_IO0 OUT			
23	7_IN2	Channel 7 Inputs	R	0
22	7_IN1			
21	7_IO0			
20	6_IN2	Channel 6 Inputs	R	0
19	6_IN1			
18	6_IO0			
17	5_IN2	Channel 5 Inputs	R	0
16	5_IN1			
15	5_IO0			
14	4_IN2	Channel 4 Inputs	R	0
13	4_IN1			
12	4_IO0			
11	3_IN2	Channel 3 Inputs	R	0
10	3_IN1			
9	3_IO0			
8	2_IN2	Channel 2 Inputs	R	0
7	2_IN1			
6	2_IO0			
5	1_IN2	Channel 1 Inputs	R	0
4	1_IN1			
3	1_IO0			
2	0_IN2	Channel 0 Inputs	R	0
1	0_IN1			
0	0_IO0			

Table 5-31 : Test Register

5.2.7.2 Board Health Register

Bit	Symbol	Description	Access	Reset Value
31:26	-	Reserved, always reads as '0'	-	0
25	PGOOD	Power Good signal from the on-board power supplies. This bit does not cover the isolated +5 V and EXT_24V +24 V supplies	R	1
24:16	-	Reserved	-	0
15:0	FPGA TEMP	Result of the FPGA on-chip temperature sensor measurement in degrees centigrade in steps of 1/256 °C. This is a signed value. A new readout is available every ~100 µs	R	0

Table 5-32 : Board Health Register

5.2.7.3 Scratchpad Register

Bit	Symbol	Description	Access	Reset Value
31:0	SCRTCH	Scratchpad Register Can be used to test read and write operations	R/W	0

Table 5-33 : Scratchpad Register

5.2.7.4 Firmware Version Register

Bit	Symbol	Description	Access	Reset Value
31:24	FW_MAJ	Firmware Major Version	R	0x01
23:16	FW_MIN	Firmware Minor Version	R	0x00
15:8	FW_REV	Firmware Reserved	R	x
7:0	FW_BLD	Firmware Build Count	R	x

Table 5-34 : Firmware Version Register

6 Functional Decription

Each channel can either work as a SSI interface or as an encoder / general purpose counter. The choice between both modes is made in the Global Control Register on a per channel base. In addition to this main functionality the TCPS118 offers isolated 24 V digital inputs and outputs plus an interval timer.

6.1 SSI Mode

6.1.1 SSI Short Description

The Synchronous Serial Interface (SSI) is based on two differential signal lines, CLOCK and DATA. The CLOCK line is an input, the DATA line is an output of the absolute encoder.

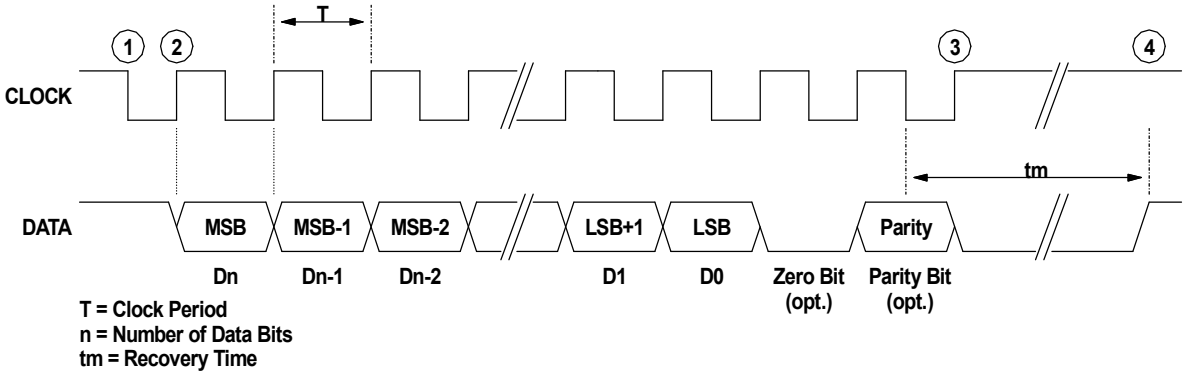

Figure 6-1 : SSI Timing Example

When not transmitting, the clock and data lines are high. To read out the positional data of an absolute encoder, the controller transmits a pulse train on the CLOCK line. The first falling edge of CLOCK ① latches the positional data of the absolute encoder. At the first rising edge of CLOCK ② the absolute encoder presents the most significant bit on the DATA line. On each subsequent rising edge in the CLOCK pulse train the next bit in order is transmitted to the controller.

In addition to the data bits the absolute encoder can transmit a parity bit for error detection. As an option additional bits can be placed between the data and the parity bit. These are encoder dependent and can be e.g. warning or alarm bits, general status or zero bits.

After all bits are transmitted ③, the absolute encoder holds the data line low for tm (= recovery time, typical 10-30 µs). After that the absolute encoder is ready for a new transmission ④. A new transmission must not started before ④.

The maximum achievable baud rate depends on the cable length. Cables are assumed to be twisted pair and screened. Refer to your sensor manufacturer for recommended cable lengths.

6.1.2 Standard SSI Interface Controller Mode

In this mode a TCPS118 channel operates as a standard SSI interface controller. The SSI clock is an output and SSI data signal is an input to the TCPS118.

Signal	Signal Voltage	Function
x_IO0+/-	RS-422	SSI Clock Output
x_IN1+/-	RS-422	SSI Data Input
x_IN2+/-	RS-422	Not used
x_24V_IN	24 V	General Purpose Input
x_24V_OUT	24 V	General Purpose Output

Table 6-1 : Signal Usage in SSI Mode

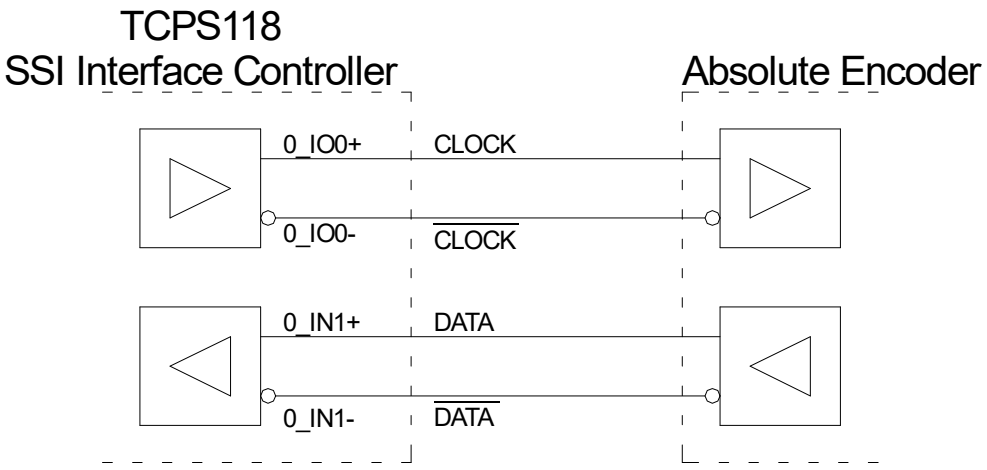

Figure 6-2 : Wiring Example: Channel 0, SSI Interface Controller Mode

This mode is enabled when the Interface Control Mode in the Global Control Register is set to “01” and the SSI MODE bit in the SSI Mode Control Register is set to ‘0’:

Register	Symbol	Setting
Global Control Register	MODEx	“01”
SSI Mode Control Register [x]	SSI MODE	‘0’

Table 6-2 : SSI Standard Mode Selection

In the SSI Mode Control Register the SSI interface must be set up, conforming to the settings required for the connected absolute encoder:

Register	Symbol	Setting
SSI Mode Control Register [x]	CR	SSI Clock Rate
	DB	Data Bits
	ZB	Additional Bits
	PAR	Parity Detection
	EO	Even/Odd Parity
	CODE	Binary/Gray Code

Table 6-3 : SSI Standard Mode Setup

A data transmission is initiated depending on the SSI Start setting in the SSI Mode Control Register. The default is by a write to the Data Register. The SSI interface controller then generates a clock burst, on which the absolute encoder returns its positional data. The SSI Controller receives this data, processes it (parity check, gray- to binary code conversion) and indicates the end of the data transmission with the deassertion of the Busy bit. If enabled, an interrupt is asserted and the positional data can be read in the Data Register.

6.1.3 SSI Listen-Only Mode

The TCPS118 also supports a SSI Listen-Only mode. In this mode a TCPS118 channel listens to an existing SSI interface to observe the data transmissions. Both the SSI clock and data signals are inputs to the TCPS118.

Signal	Signal Voltage	Function
x_IO0+/-	RS-422	Not used
x_IN1+/-	RS-422	SSI Data Input
x_IN2+/-	RS-422	SSI Clock Input
x_24V_IN	24 V	General Purpose Input
x_24V_OUT	24 V	General Purpose Output

Table 6-4 : Signal Usage in SSI Listen-Only Mode

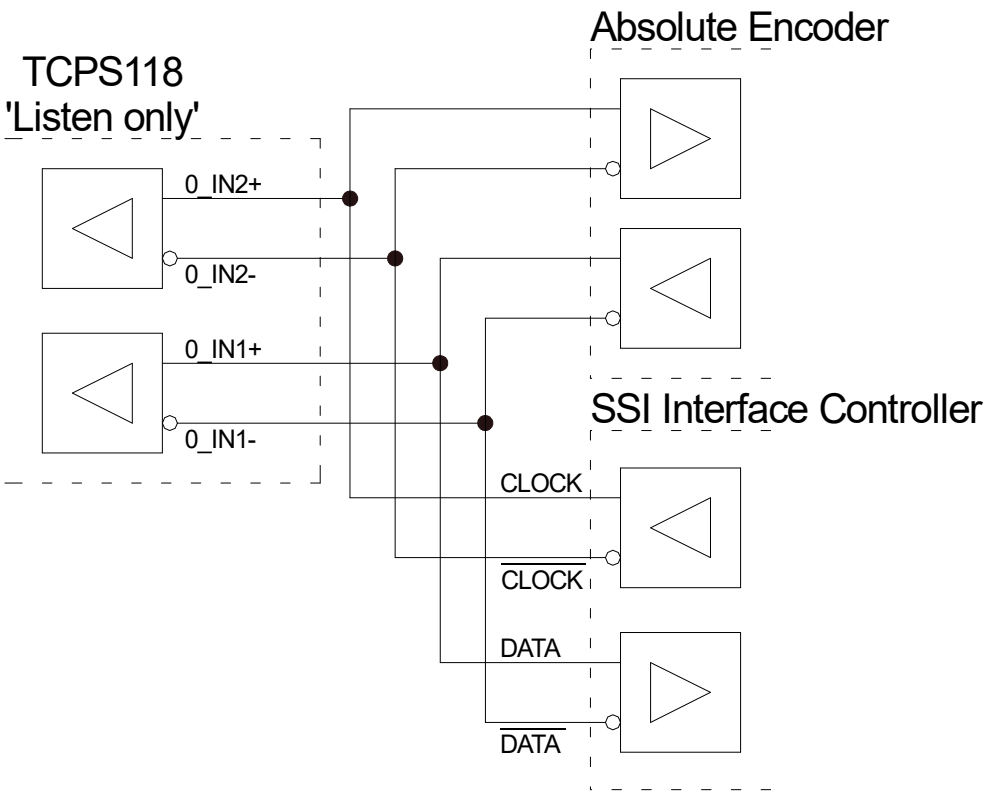

Figure 6-3 : Wiring Example: Channel 0, SSI Listen-Only Mode

This mode is enabled when the Interface Control Mode in the Global Control Register is set to “01” and the SSI MODE bit in the SSI Mode Control Register is set to ‘1’:

Register	Symbol	Setting
Global Control Register	MODEx	“01”
SSI Mode Control Register [x]	SSI MODE	‘1’

Table 6-5 : SSI Listen-Only Mode Selection

In the SSI Mode Control Register the SSI interface must be set up, conforming to the settings required for the observed SSI interface:

Register	Symbol	Setting
SSI Mode Control Register [x]	CR	-
	DB	Data Bits
	ZB	Additional Bits
	PAR	Parity Detection
	EO	Even/Odd Parity
	CODE	Binary/Gray Code

Table 6-6 : SSI Listen-Only Mode Setup

The clock rate setting in the SSI Mode Control Register is ‘don’t care’; the clock rate of the observed SSI interface will be detected automatically.

After the SSI Mode Control Register is set up, the channel listens (indicated by BSY = ‘1’).

A data transfer is initiated by the observed SSI interface. The positional data will be received and processed (parity check, gray- to binary code conversion) and the end of the data transmission is indicated with the deassertion of the Busy bit. The positional data can be read in the Data Register and, if enabled, an interrupt is asserted.

Reading the Data Register will set the Busy bit to ‘1’ and the channel is listening again.

Note that in this mode the clock rate setting in the SSI Mode Control Register is ignored; the Clock Rate will be detected automatically. Writes to the Data Register are also ignored for channels in this mode.

The LISTEN STATUS bits in the SSI Mode Status Register provide an indication if the last transmission was successfully received. To detect read errors, the width of the first SSI clock pulse is measured to detect the clock rate. This clock rate is multiplied by 4 and used as the initial value for a timeout timer. Every new received bit resets the timeout timer, and is counted. When the transmission ends, a timeout will eventually occur, and the number of received bits is compared to the number of anticipated bits. LISTEN STATUS then shows if less, more, or the exact number of bits are received.

6.1.4 SSI Mode Behavior Differences

	Standard SSI Interface Mode	SSI Listen-Only Mode
Control Register	Control Register SSI bits fully used Bit 24 (SSI MODE) is set to '0'	Clock rate setting in Control Register is 'don't care' Bit 24 (SSI MODE) is set to '1'
Status Register	Busy bit = '1' during transmission	Busy bit = '1' during transmission or after the data word was read (channel is listening again)
Listen Status	LISTEN STATUS is always "000"	LISTEN STATUS shows status of the last transmission
Connections	Connect external SSI data outputs to TCPS118 'x_IN1+/-' inputs. Connect external SSI Clock inputs to TCPS118 'x_IO0+/-' outputs.	Connect external SSI data to TCPS118 'x_IN1+/-' inputs. Connect external SSI clock to TCPS118 'x_IN2+/-' inputs.
Data Transfer Start	Data transfer is initiated based on SSI START setting or a Multiple Channel Read	Data transfer is initiated by external SSI interface controller

Table 6-7 : SSI Mode Behavior Differences

6.2 Counter Mode

The TCPS118 counter offers a number of counter modes, which can be set up in the Counter Mode Control Register.

The Input Mode selects which inputs are used and how they are interpreted by the counter. The Special Count Modes alter the general behavior of the counter. The Index Control Modes set additional control modes using a control signal, either the x_IN2 input or the x_24V_IN input.

6.2.1 Input Modes

The Input Mode determines the input source and how the counter interprets these input signals. The following descriptions mostly use the "descriptive labels" of the input signals.

Input Mode	**Signal**				
	x_IO0	**x_IN1**	**x_IN2**	**x_24V_IN**	**x_24V_OUT**
	Input	Input	Input	Input	Output
	-10R: RS-422 / TTL | -20R: 24 V			24 V	24 V
Timer	Not used	Not used	Control Mode (optional): Load, Latch, Gate, Reset	General Purpose Input	General Purpose Output
Direction Count	Count	Count Direction (up/down)			
Up/Down Count	Count UP	Count DOWN			
Quadrature Counter	Quadrature **A**	Quadrature **B**	Index **I** Control Mode (optional): Load, Latch, Gate, Reset	Reference Modes (optional) or General Purpose Input	
Descriptive Label	A-input	B-input	I-Input	Ref-Input	-

Table 6-8 : Counter Input Modes

6.2.1.1 Timer Mode

In Timer mode the counter uses an internal clock as input. Depending on the CLKDIV setting in Counter Mode Control Register, the internal clock is prescaled as follows:

CLKDIV	Clock Frequency
100	100 MHz
110	50 MHz
101	20 MHz
100	10 MHz
011	5 MHz
010	4 MHz
001	2 MHz
000	1 MHz

Table 6-9 : Timer Mode Clock Prescaler

6.2.1.2 Direction Count

The counter acts as up/down counter. Counting pulses are generated when a transition from low to high of the A-input is detected. The B-input determines the count direction.

B-Input	Count Direction
0	Down
1	Up

Table 6-10 : Count Directions

6.2.1.3 Up/Down Count

The counter acts as up-/down counter. Counting pulses are generated when a transition from low to high of either the A- or the B-input is detected. The A-input counts up, the B-input counts down. Simultaneous transitions on the A- and B-input do not generate a counting pulse.

6.2.1.4 Quadrature Count

The counter acts as quadrature counter. A-input is quadrature input A, B-input is quadrature input B. The quadrature inputs can be interpreted as 1x, 2x or 4x counting. 1x lets the counter count once for each full cycle of the quadrature inputs, 2x lets the counter count once for each half cycle of the quadrature inputs and 4x lets the counter count once for each quarter cycle of the quadrature inputs. The count direction (increase or decrease) is determined by the relative phase of the A- and B-signals.

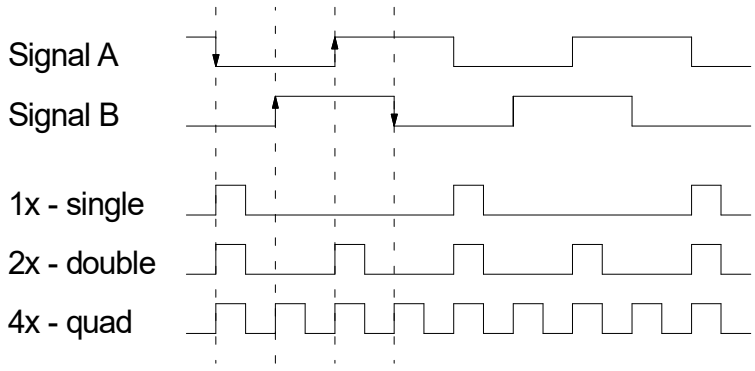

Figure 6-4 : Quadrature Signals

6.2.2 Special Count Modes

In normal operation, the counter is a cycling counter. Two additional special count modes are available. The Count Modes are available for every Input Mode.

6.2.2.1 Divide-by-N

The counter is enabled in the Counter Mode Control Register and will run until it is disabled. The counter is loaded with the content of the Counter Mode Preload register every time the counter creates a borrow or a carry.

6.2.2.2 Single Cycle

The counter is enabled in the Counter Mode Control Register and will start on following events:

- A manual preload or reset in the Counter Mode Command Register
- A manual counter preload in the Global Control Register
- A control mode event in ‘Load on I’ or ‘Reset on I’ mode.

The counter will stop when it would create a borrow or a carry.

6.2.3 Index Control Modes

The Index Control Mode determines how events on the I-input are interpreted. With the exception of the ‘Gate on I’ mode, all modes react on a level change on the I-input. Due to the digital input filtering, a change in the input level is only detected, when the input line is stable for at least 30 ns (depending on the setting in the Debouncing Register). The following table gives an overview of the index control mode events.

Index Control Mode	Polarity	
	High-Active (POL = 0)	Low-Active (POL = 1)
No I-Control	-	-
Load on I	Rising Edge	Falling Edge
Latch on I	Rising Edge	Falling Edge
Gate on I	High Level	Low Level
Reset on I	Rising Edge	Falling Edge
Reference Mode	Rising Edge	Falling Edge
Auto Reference Mode	Rising Edge	Falling Edge
Index Mode	Rising Edge	Falling Edge

Table 6-11 : Index Control Mode Events

The control modes ‘Reference Mode’, ‘Auto Reference Mode’ and ‘Index Mode’ are only valid when the input mode is quadrature count. They control the counter with the encoder index input in cooperation with a reference switch connected to the isolated 24 V digital input.

An interrupt can be generated on a control mode event. This is only available for the Load-, Latch-, Gate- and Reset on I modes.

Index Control Mode	Interrupt Generation
No Control Mode	No Interrupt
Load Mode Latch Mode Reset Mode	Control Mode Event
Gate Mode	Gate Closed

Table 6-12 : Index Control Mode Interrupt Generation

6.2.3.1 No I-Control

In this mode the I-input is ignored.

6.2.3.2 Load On I

An event on the I-input loads the counter with the content of the Counter Mode Preload Register. If the 'Single Cycle' mode is active, the event on the I-input will start the counter. The counter can also be preloaded by writing '1' to the 'Load Counter' (LCNT) bit in the Counter Mode Command Register.

This control mode can be used to establish a known reference position in a mechanical system.

6.2.3.3 Latch On I

An event on the I-input loads and locks the Data Register with the actual counter value (see chapter ’6.2.4 Data Register Lock’ for details). It will remain latched until the Data Register is read or the latch is released with the DRL bit in the Counter Mode Status Register.

When a ‘Latch on I’ event occurs while the Data Register Lock is still active, the data in the Data Register will be retained and the Data Register Lock Overflow (OVFL) will be set to indicate that data was lost.

This control mode can be used to capture a position in a mechanical system.

6.2.3.4 Gate On I

The signal level on the I-input enables or disables counting. Remember that in this mode the I-input is level sensitive.

I-Input	Counter
0	Disabled
1	Enabled

Table 6-13 : Gate Mode

In this mode an interrupt is generated (if enabled) when the gate is being closed (I-Input transition from ‘1’ to ‘0’).

When a signal with constant frequency is connected to the A- and B-inputs, this control mode can be used for impulse width measurements.

6.2.3.5 Reset On I

An event on the I-input resets (clears) the counter. If the 'Single Cycle' mode is active, the event on the I-input starts the counter.

The counter can also be reset by writing '1' to the 'Reset Counter' (RCNT) bit in the Counter Mode Command Register.

This control mode can be used to establish a known home or reference position in a mechanical system.

6.2.3.6 Reference Mode

Similar to the “Load on I” mode this control mode can be used to establish a known reference position in a mechanical system. It uses the combination of the isolated 24 V digital Ref-Input (i.e. from a limit switch) and the I-Input. A specific Ref-Input signal and a following I-Input impulse produces a counter preload.

The following figure shows the two normal preload accesses. An encoder motion area with eight index pulses and the corresponding Ref-Input is described as an example. Two different ‘start positions’ (1a and 1b) are shown:

Position 1a

Direction is forward and the Ref-Input is active. After moving to an area where the Ref-Input is inactive the direction is changed. The next index pulse after entering the area with Ref-Input active triggers the preload function for the counter.

Position 1b

Direction is backwards and the Ref-Input is inactive. After entering the area with Ref-Input active the next index pulse triggers the preload function for the counter.

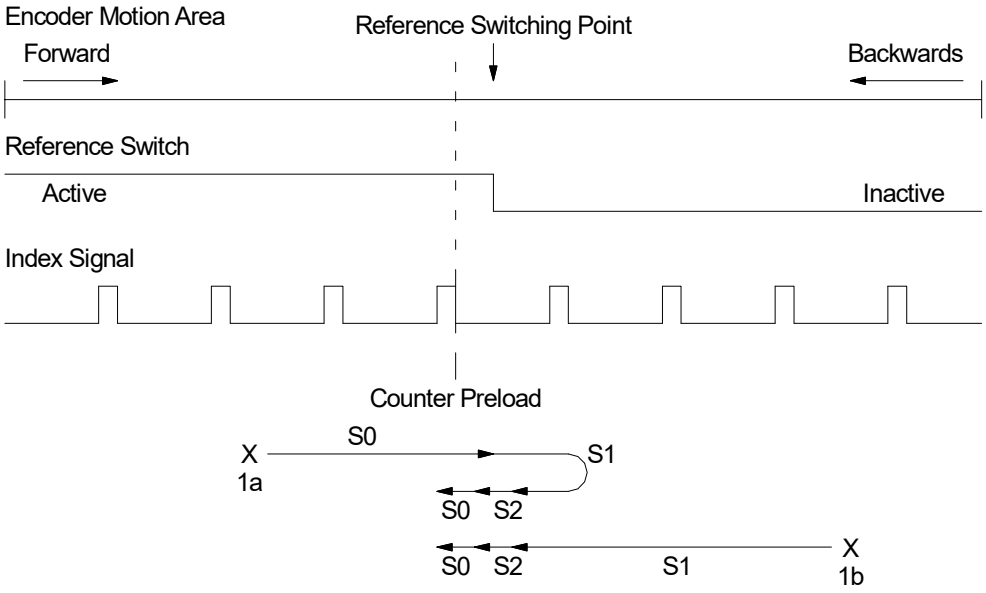

Figure 6-5 : Reference Mode Preload Example

A correct execution of the reference function can be monitored in the Counter Mode Control Register. After successful execution the Index Control Mode (ICM) is reset from Reference Mode to No I-Control Mode.

6.2.3.7 Auto Reference Mode

This mode is the automation of the Reference Mode. Every time the reference switching point and a following index pulse are crossed during backward direction, a new preload is generated. In “Auto Reference Mode” there is no change of the Index Control Mode (ICM) in the Counter Mode Control Register!

6.2.3.8 Index Mode

In this mode the Ref-Input is not used. Only the index impulse produces a counter preload. After setting this mode the next occurrence of the index signal independent from direction will preload the counter. A correct execution of this preload function can be monitored in the Counter Mode Control Register. After successful execution the Index Control Mode (ICM) is reset from Index Mode to No I-Control Mode.

6.2.4 Data Register Lock

The Data Register is loaded and locked with the actual counter value on following conditions:

- Latch in I Mode
- Multiple Channel Read

The Data Register is locked until following conditions are met:

- A read-access to the Data Register
- A write '1' to the Reset Counter (RCNT) bit in the Counter Mode Command Register

Until the lock is released, the Data Register will not load again. The status of the Data Register lock can be monitored in the Counter Mode Status Register (DRL). When the lock is released, the Data Register retains its value until it is loaded again.

When a Multiple Channel Read is issued or a Latch Mode event occurs while a Data Register is locked, the Data Register content will be retained and the Data Register Latch Overflow (OVFL) will be set in the Counter Mode Status Register to indicate that data was lost.

6.3 Multiple Channel Read

The TCPS118 provides a Multiple Channel Read (MCR) feature. A Multiple Channel Read allows to take a snapshot of the enabled channels. It can be enabled on a per channel basis in the Global Control Register. A MCR can be manually triggered with the MCR TRIG bit in the Global Command Register or automatically by the interval timer.

The Multiple Channel Read feature is not indented to be used with SSI channels that are set to Listen-Only, due to the unpredictable timing, or SSI channels using back-to-back transfers.

An MCR latches the current data of enabled channels into the Multiple Channel Read Data Registers. The data of channels in Counter Mode is instantly available. For channels in SSI Mode the MCR starts a transmission, which takes time to complete. For SSI channels the SSI START setting must be “00”.

To monitor the progress of the data collection, the MCR STA bits in the Global Command Register provide a MCR BUSY and MCR READ PENDING indication. MCR STA will hold MCR READ PENDING until the Data Registers of all enabled channels were read. To reset a Multiple Channel Read sequence beforehand, write ‘1’ to the MCR CLR bit in the Global Command Register.

When a new Multiple Channel Read is triggered while the MCR status is MCR BUSY or MCR READ PENDING, new data will be latched, and new SSI transmission will be started for channels that have their transmissions already finished. The MCR OVERFLOW will be set, to indicate that data was overwritten. While MCR OVERFLOW is set, the Multiple Channel Read continues to work and latches new data when triggered, but the MCR OVERFLOW is active until it is cleared.

	SSI	Counter	SSI & Counter
Data availability	When all channel transmissions are complete	Instantly	SSI: When all channel transmissions are completed Counter: Instantly
Data availability indication	MCR STA = “10”	MCR STA = “10”	MCR STA = “10” Counter data may already be read before MCR STA = “10”

Table 6-14 : Multiple Channel Read Data Availability

MCR STA	Shortform	Description
00	MCR IDLE	No pending Multiple Channel Read. All previous latched data has been read, or MCR is not active
01	MCR BUSY	MCR was triggered, but data is still being collected (SSI transmissions are still in progress)
10	MCR READ PENDING	MCR data is valid. This status is hold until all data has been read
11	MCR OVERFLOW	A new Multiple Channel Read was triggered while data was still collected, or was not read out. Do a MCR CLR to clear this status

Table 6-15 : Multiple Channel Read Status

Example:

Channels 0-3 are configured for SSI mode, channels 4-7 are configured for counter mode. Channels 1, 4 and 6 are enabled for Multiple Channel Read. A write to the MCR TRIG bit starts the Multiple Channel Read. Channel 1 starts a transmission and the data of channels 4 and 6 is latched. The data of the enabled counter channels is instantly available and can be read at once. The SSI data is not available until MCR STA is set to “10”. When all enabled channels were read, MCR STA is reset to “00”.

There is no designated interrupt to indicate the completion of a Multiple Channel Read. Alternatively an interrupt can be set up for the SSI channel that takes the longest time to complete a transmission. If only counter channels are read, an interrupt is not necessary because the counter data is instantly available.

6.4 24 V Digital Inputs

The TCPS118 offers one isolated 24 V digital input per channel. The inputs can be electronically debounced. Each 24 V digital input can generate an interrupt, triggered on rising or falling edge. Depending on the selected counter reference mode the input can be used as a general purpose input or as a reference input.

6.5 24 V Digital Outputs

The TCPS118 offers one isolated 24 V digital output per channel. This output is a general purpose output.

The TCPS118 provides a watchdog timer. When enabled, the watchdog timer must be refreshed in regular intervals. If the watchdog timer expires, it disables all 24 V digital outputs. The watchdog is disabled after power-on or reset.

6.6 Interval Timer

In addition to the timer modes provided by the counter channels, a separate interval timer is available. The interval timer can be used as a reference timer in closed loop applications or as a trigger for a Multiple Channel Read.

The interval timer is a 32 bit preloadable counter with a programmable clock rate. On activation the counter loads from the Interval Timer Preload Register und starts counting down. When the counter reaches zero, it generates an interrupt (if enabled), is automatically preloaded again and continues counting. The ITTB setting in the Interval Timer Control Register determines the time base the Interval Timer uses.

Calculate the interval times using the time base with the following formula:

Interval Time = Value of Interval Timer Preload Register * Time Base

ITTB	Clock Period
00	100 ns
01	1 µs
10	1 ms
11	1 s

Table 6-16 : Interval Timer Time Bases

7 I/O Interface Description

7.1 I/O Electrical Interface

7.1.1 RS-422 I/O

The following schematic shows the principle input wiring for one RS-422 input signal. A 120 Ω termination resistor is provided and can be disabled by removing a jumper.

When a RS-422 I/O shall be used for single-ended/TTL signaling, the termination jumper should be removed, and the "-" terminal should be left open. When configured as output (only x_IO0), it will provide a 5 V TTL compatible signal on the "+" terminal. As input it can receive a 3-5 V TTL compatible signal on the "+" terminal. A biasing network on the "-" terminal will set the switching level to about 1.5 V.

The TCPS118 uses Fault-Protected RS-485 compatible transceivers and receivers for the RS-422 signals.

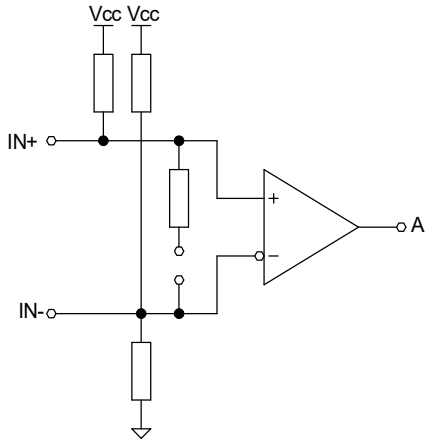

Figure 7-1 : RS-422 Input Circuit

Parameter	Min	Typical	Max
Input voltage	-	5 V	±25 V
Switching level (TTL-mode)	-	1.5 V	-
Hysteresis (TTL-mode)	-	0.2 V	-
Termination	-	120 Ω	-
Switching Frequency	-	-	10 MHz

Table 7-1 : RS-422 Input Characteristics

The TCPS118-10R provides two rows of termination jumpers. These are marked on the PCB with the channel number 0-7 and the signal A / B / C.

Generic Signal Name	Jumper Marking
x_IO0	A
x_IN1	B
x_IN2	C

Table 7-2 : Jumper Markings

In the following example picture the channels 0 to 3 have jumper inserted, so they are configured as RS-422 channels. The channels 4 to 7 have their jumper removed and can be used as single-ended TTL inputs.

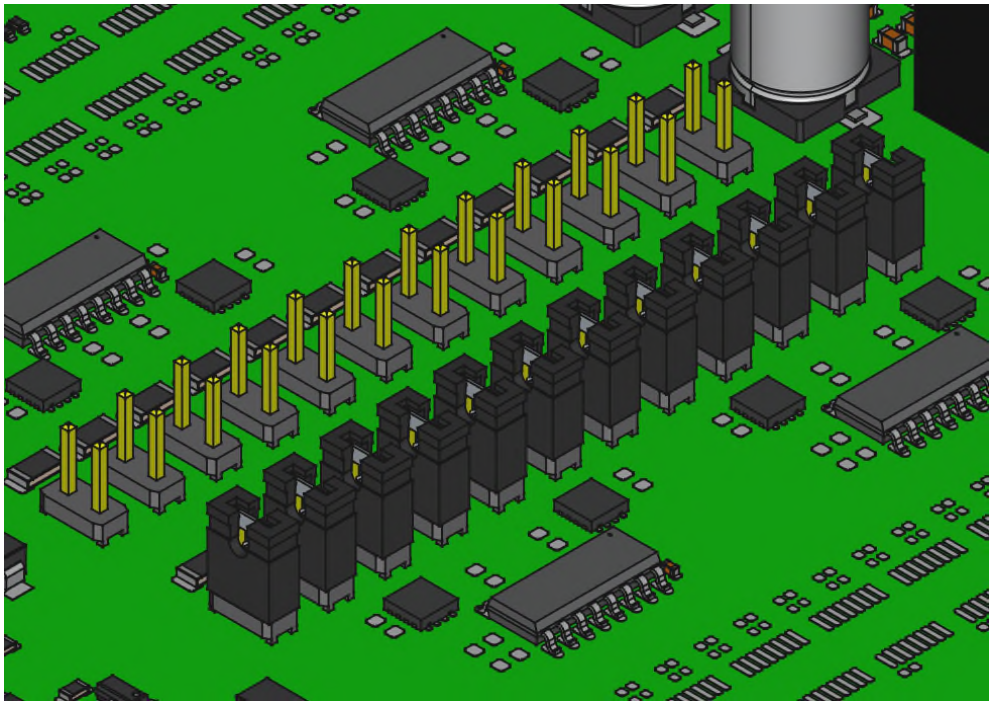

Figure 7-2 : Example Jumper Placement

7.1.2 Digital 24 V Inputs

The TCPS118 offers one galvanically isolated digital 24 V input per channel. A high performance input circuit ensures a defined switching point with an input characteristics compliant to IEC 61131-2 Type 3.

The inputs operate in a sinking configuration for high-side switching. The external circuit must connect a externally supplied voltage to the x_24V_IN pin.

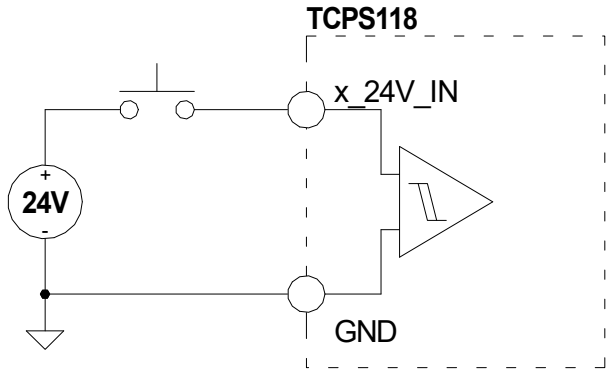

Figure 7-3 : 24 V Input Circuit

Parameter	Min	Typical	Max
Input voltage	9 V	24 V	36 V
Input Current	-	2.5 mA	-
Switching Level	8.5 V	10.5 V	11.5 V
Hysteresis	-	1.2 V	-
Input Frequency	-	-	1 kHz

Table 7-3 : Digital 24 V Input Characteristics

7.1.3 24 V Digital Outputs

The TCPS118 offers one galvanically isolated 24 V digital output per channel. The outputs operate in a sourcing configuration for high-side switching. It connects the externally supplied 24 V EXT_24V to the x_24V_OUT pin.

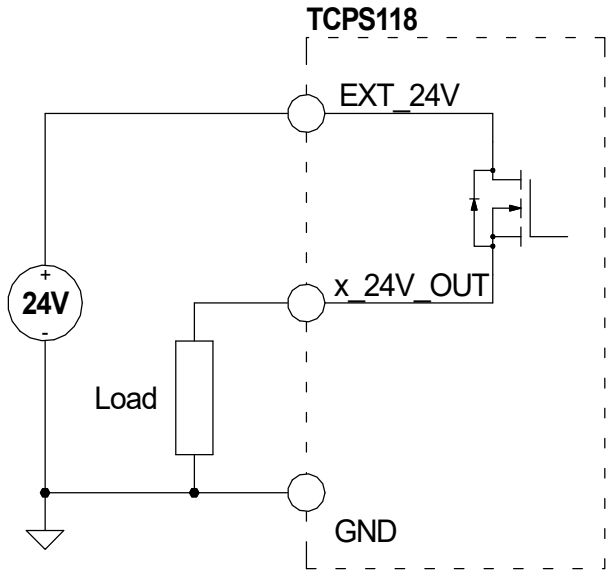

Figure 7-4 : 24 V Digital Output Circuit

Parameter	Min	Typical	Max
Output voltage	9 V	24 V	27 V
Output current	-	600 mA	700 mA
Switching Frequency	-	-	1 kHz

Table 7-4 : 24 V Digital Output Characteristics

7.2 Front Panel LED Indicator

A front panel LED near the front handle marked with “HS” provides board status information.

LED	Color	State	Description
HS	Red	On	Power Fail
		Off	Power Good, or Power is off
	Green	On	Board status is ok, PCIe link is up
		Blinking	Board status is ok, PCIe link is not up
		Off	Board status is not ok, or Power is off

Table 7-5 : Front Panel LED Description

7.3 CPCI-S.0 P1 Connector

7.3.1 Connector Type

Pin-Count	72
Connector Type	AirMax
Source & Order Info	FCI 10052825-101LF

Table 7-6 : CPCI-S.0 P1 Connector Type

7.3.2 Pin Assignment

Pin	1 - 01	1 - 02	1 - 03	1 - 04	1 - 05	1 - 06
A	+12V	GND	1_USB3_Tx+	GND	1_PE_Tx00+	GND
B	STANDBY	I²C_SCL	1_USB3_Tx-	1_USB2+	1_PE_Tx00-	1_PE_Tx02+
C	GND	I²C_SDA	GA0	1_USB2-	GND	1_PE_Tx02-
D	+12V	GND	1_USB3_Rx+	GND	1_PE_Rx00+	GND
E	+12V	reserved	1_USB3_Rx-	PE_CLKIN+	1_PE_Rx00-	1_PE_Rx02+
F	GND	reserved	GA1	PE_CLKIN-	GND	1_PE_Rx02-
G	+12V	GND	SATA_SDI	GND	1_PE_Tx01+	GND
H	+12V	RST#	SATA_SDO	1_SATA_Tx+	1_PE_Tx01-	1_PE_Tx03+
I	GND	WAKE_OUT#	GA2	1_SATA_Tx-	GND	1_PE_Tx03-
J	+12V	GND	SATA_SCL	GND	1_PE_Rx01+	GND
K	+12V	PCIE_EN#	SATA_SL	1_SATA_Rx+	1_PE_Rx01-	1_PE_Rx03+
L	GND	SYSEN#	GA3	1_SATA_Rx-	GND	1_PE_Rx03-

Table 7-7 : CPCI-S.0 P1 Connector Pin Assignment

7.4 Front I/O Connectors

The TCPS118 provides a 68 pos. MDR connector (“X1”) and a connector for the external 24 V supply (“24 V”).

7.4.1 Connector Type

Pin-Count	4
Connector Type	Molex Micro-Fit 3.0 Dual-Row Header, 4 pos
Source & Order Info	430450400
Mating Part	e.g. 0430250400 (Receptable), or e.g. 2451320410 (Overmolded Cable Assembly, 1 m)

Table 7-8 : External 24 V Supply Connector Type

Pin-Count	68
Connector Type	Mini D Ribbon (MDR) receptacle, 68 pos
Source & Order Info	3M N10268-52E3PC (or compatible)
Mating Part	e.g. 3M 10150-6000EC or TA113

Table 7-9 : X1 MDR Front I/O Connector Type

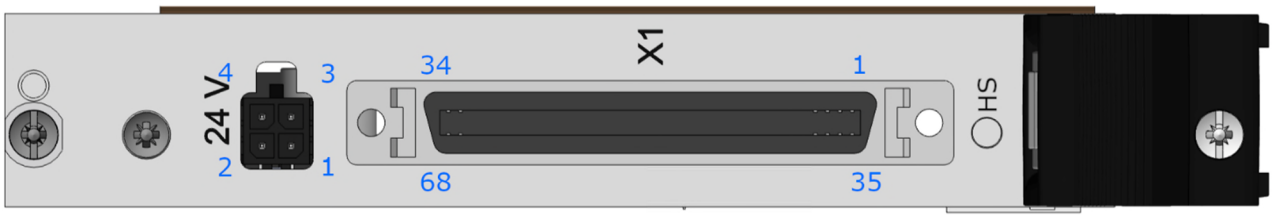

Figure 7-5 : Front I/O Connector Pin Location

7.4.2 External 24 V Supply Connector Pin Assignment

Pin	Signal	Dir	Level
4	EXT_24V	I	24 V
2	EXT_24V	I	24 V

Pin	Signal	Dir	Level
3	GND	I	GND
1	GND	I	GND

Table 7-10 : External 24 V Supply Connector Pin Assignment

7.4.3 Front I/O Connector Pin Assignment TCPS118-10R (Generic)

Pin	Signal	Dir	Level
1	GND	-	GND
2	0_IO0+	I/O	RS-422 / TTL
3	0_IN1+	I	RS-422 / TTL
4	0_IN2+	I	RS-422 / TTL
5	0_24V_IN	I	24 V
6	1_IO0+	I/O	RS-422 / TTL
7	1_IN1+	I	RS-422 / TTL
8	1_IN2+	I	RS-422 / TTL
9	1_24V_IN	I	24 V
10	2_IO0+	I/O	RS-422 / TTL
11	2_IN1+	I	RS-422 / TTL
12	2_IN2+	I	RS-422 / TTL
13	2_24V_IN	I	24 V
14	3_IO0+	I/O	RS-422 / TTL
15	3_IN1+	I	RS-422 / TTL
16	3_IN2+	I	RS-422 / TTL
17	3_24V_IN	I	24 V
18	4_IO0+	I/O	RS-422 / TTL
19	4_IN1+	I	RS-422 / TTL
20	4_IN2+	I	RS-422 / TTL
21	4_24V_IN	I	24 V
22	5_IO0+	I/O	RS-422 / TTL
23	5_IN1+	I	RS-422 / TTL
24	5_IN2+	I	RS-422 / TTL
25	5_24V_IN	I	24 V
26	6_IO0+	I/O	RS-422 / TTL
27	6_IN1+	I	RS-422 / TTL
28	6_IN2+	I	RS-422 / TTL
29	6_24V_IN	I	24 V
30	7_IO0+	I/O	RS-422 / TTL
31	7_IN1+	I	RS-422 / TTL
32	7_IN2+	I	RS-422 / TTL
33	7_24V_IN	I	24 V
34	GND	-	GND

Pin	Signal	Dir	Level
35	GND	-	GND
36	0_IO0-	I/O	RS-422 / TTL
37	0_IN1-	I	RS-422 / TTL
38	0_IN2-	I	RS-422 / TTL
39	0_24V_OUT	O	24 V
40	1_IO0-	I/O	RS-422 / TTL
41	1_IN1-	I	RS-422 / TTL
42	1_IN2-	I	RS-422 / TTL
43	1_24V_OUT	O	24 V
44	2_IO0-	I/O	RS-422 / TTL
45	2_IN1-	I	RS-422 / TTL
46	2_IN2-	I	RS-422 / TTL
47	2_24V_OUT	O	24 V
48	3_IO0-	I/O	RS-422 / TTL
49	3_IN1-	I	RS-422 / TTL
50	3_IN2-	I	RS-422 / TTL
51	3_24V_OUT	O	24 V
52	4_IO0-	I/O	RS-422 / TTL
53	4_IN1-	I	RS-422 / TTL
54	4_IN2-	I	RS-422 / TTL
55	4_24V_OUT	O	24 V
56	5_IO0-	I/O	RS-422 / TTL
57	5_IN1-	I	RS-422 / TTL
58	5_IN2-	I	RS-422 / TTL
59	5_24V_OUT	O	24 V
60	6_IO0-	I/O	RS-422 / TTL
61	6_IN1-	I	RS-422 / TTL
62	6_IN2-	I	RS-422 / TTL
63	6_24V_OUT	O	24 V
64	7_IO0-	I/O	RS-422 / TTL
65	7_IN1-	I	RS-422 / TTL
66	7_IN2-	I	RS-422 / TTL
67	7_24V_OUT	O	24 V
68	GND	-	GND

Table 7-11 : Front I/O Connector Pin Assignment TCPS118-10R (Generic)

7.4.4 Front I/O Connector Pin Assignment TCPS118-10R (by Function)

Pin	Generic Name	SSI Mode	Dir	Counter Mode	Dir	Level
1	GND	GND	-	GND	-	GND
2	0_IO0+	0_CLK_OUT+	O	0_A+	I	RS-422 / TTL
3	0_IN1+	0_DATA_IN+	I	0_B+	I	
4	0_IN2+	0_CLK_IN+	I	0_I+	I	
5	0_24V_IN	0_24V_IN	I	0_24V_IN	I	24 V
6	1_IO0+	1_CLK_OUT+	O	1_A+	I	RS-422 / TTL
7	1_IN1+	1_DATA_IN+	I	1_B+	I	
8	1_IN2+	1_CLK_IN+	I	1_I+	I	
9	1_24V_IN	1_24V_IN	I	1_24V_IN	I	24 V
10	2_IO0+	2_CLK_OUT+	O	2_A+	I	RS-422 / TTL
11	2_IN1+	2_DATA_IN+	I	2_B+	I	
12	2_IN2+	2_CLK_IN+	I	2_I+	I	
13	2_24V_IN	2_24V_IN	I	2_24V_IN	I	24 V
14	3_IO0+	3_CLK_OUT+	O	3_A+	I	RS-422 / TTL
15	3_IN1+	3_DATA_IN+	I	3_B+	I	
16	3_IN2+	3_CLK_IN+	I	3_I+	I	
17	3_24V_IN	3_24V_IN	I	3_24V_IN	I	24 V
18	4_IO0+	4_CLK_OUT+	O	4_A+	I	RS-422 / TTL
19	4_IN1+	4_DATA_IN+	I	4_B+	I	
20	4_IN2+	4_CLK_IN+	I	4_I+	I	
21	4_24V_IN	4_24V_IN	I	4_24V_IN	I	24 V
22	5_IO0+	5_CLK_OUT+	O	5_A+	I	RS-422 / TTL
23	5_IN1+	5_DATA_IN+	I	5_B+	I	
24	5_IN2+	5_CLK_IN+	I	5_I+	I	
25	5_24V_IN	5_24V_IN	I	5_24V_IN	I	24 V
26	6_IO0+	6_CLK_OUT+	O	6_A+	I	RS-422 / TTL
27	6_IN1+	6_DATA_IN+	I	6_B+	I	
28	6_IN2+	6_CLK_IN+	I	6_I+	I	
29	6_24V_IN	6_24V_IN	I	6_24V_IN	I	24 V
30	7_IO0+	7_CLK_OUT+	O	7_A+	I	RS-422 / TTL
31	7_IN1+	7_DATA_IN+	I	7_B+	I	
32	7_IN2+	7_CLK_IN+	I	7_I+	I	
33	7_24V_IN	7_24V_IN	I	7_24V_IN	I	24 V
34	GND	GND	-	GND	-	GND

Pin	Generic Name	SSI Mode	Dir	Counter Mode	Dir	Level
35	GND	GND	-	GND	-	GND
36	0_IO0-	0_CLK_OUT-	O	0_A-	I	RS-422 / TTL
37	0_IN1-	0_DATA_IN-	I	0_B-	I	
38	0_IN2-	0_CLK_IN-	I	0_I-	I	
39	0_24V_OUT	0_24V_OUT	O	0_24V_OUT	O	24 V
40	1_IO0-	1_CLK_OUT-	O	1_A-	I	RS-422 / TTL
41	1_IN1-	1_DATA_IN-	I	1_B-	I	
42	1_IN2-	1_CLK_IN-	I	1_I-	I	
43	1_24V_OUT	1_24V_OUT	O	1_24V_OUT	O	24 V
44	2_IO0-	2_CLK_OUT-	O	2_A-	I	RS-422 / TTL
45	2_IN1-	2_DATA_IN-	I	2_B-	I	
46	2_IN2-	2_CLK_IN-	I	2_I-	I	
47	2_24V_OUT	2_24V_OUT	O	2_24V_OUT	O	24 V
48	3_IO0-	3_CLK_OUT-	O	3_A-	I	RS-422 / TTL
49	3_IN1-	3_DATA_IN-	I	3_B-	I	
50	3_IN2-	3_CLK_IN-	I	3_I-	I	
51	3_24V_OUT	3_24V_OUT	O	3_24V_OUT	O	24 V
52	4_IO0-	4_CLK_OUT-	O	4_A-	I	RS-422 / TTL
53	4_IN1-	4_DATA_IN-	I	4_B-	I	
54	4_IN2-	4_CLK_IN-	I	4_I-	I	
55	4_24V_OUT	4_24V_OUT	O	4_24V_OUT	O	24 V
56	5_IO0-	5_CLK_OUT-	O	5_A-	I	RS-422 / TTL
57	5_IN1-	5_DATA_IN-	I	5_B-	I	
58	5_IN2-	5_CLK_IN-	I	5_I-	I	
59	5_24V_OUT	5_24V_OUT	O	5_24V_OUT	O	24 V
60	6_IO0-	6_CLK_OUT-	O	6_A-	I	RS-422 / TTL
61	6_IN1-	6_DATA_IN-	I	6_B-	I	
62	6_IN2-	6_CLK_IN-	I	6_I-	I	
63	6_24V_OUT	6_24V_OUT	O	6_24V_OUT	O	24 V
64	7_IO0-	7_CLK_OUT-	O	7_A-	I	RS-422 / TTL
65	7_IN1-	7_DATA_IN-	I	7_B-	I	
66	7_IN2-	7_CLK_IN-	I	7_I-	I	
67	7_24V_OUT	7_24V_OUT	O	7_24V_OUT	O	24 V
68	GND	GND	-	GND	-	GND

Table 7-12 : Front I/O Connector Pin Assignment TCPS118-10R (by Function)

7.4.5 Front I/O Connector Pin Assignment TCPS118-20R (Generic)

Please note that since 24 V input channels are all inputs, the SSI configuration is not available.

Pin	Signal	Dir	Level
1	GND	-	GND
2	0_IO0+	I	24 V
3	0_IN1+	I	24 V
4	0_IN2+	I	24 V
5	0_24V_IN	I	24 V
6	1_IO0+	I	24 V
7	1_IN1+	I	24 V
8	1_IN2+	I	24 V
9	1_24V_IN	I	24 V
10	2_IO0+	I	24 V
11	2_IN1+	I	24 V
12	2_IN2+	I	24 V
13	2_24V_IN	I	24 V
14	3_IO0+	I	24 V
15	3_IN1+	I	24 V
16	3_IN2+	I	24 V
17	3_24V_IN	I	24 V
18	4_IO0+	I	24 V
19	4_IN1+	I	24 V
20	4_IN2+	I	24 V
21	4_24V_IN	I	24 V
22	5_IO0+	I	24 V
23	5_IN1+	I	24 V
24	5_IN2+	I	24 V
25	5_24V_IN	I	24 V
26	6_IO0+	I	24 V
27	6_IN1+	I	24 V
28	6_IN2+	I	24 V
29	6_24V_IN	I	24 V
30	7_IO0+	I	24 V
31	7_IN1+	I	24 V
32	7_IN2+	I	24 V
33	7_24V_IN	I	24 V
34	GND	-	GND

Pin	Signal	Dir	Level
35	GND	-	GND
36	-	-	-
37	-	-	-
38	-	-	-
39	0_24V_OUT	O	24 V
40	-	-	-
41	-	-	-
42	-	-	-
43	1_24V_OUT	O	24 V
44	-	-	-
45	-	-	-
46	-	-	-
47	2_24V_OUT	O	24 V
48	-	-	-
49	-	-	-
50	-	-	-
51	3_24V_OUT	O	24 V
52	-	-	-
53	-	-	-
54	-	-	-
55	4_24V_OUT	O	24 V
56	-	-	-
57	-	-	-
58	-	-	-
59	5_24V_OUT	O	24 V
60	-	-	-
61	-	-	-
62	-	-	-
63	6_24V_OUT	O	24 V
64	-	-	-
65	-	-	-
66	-	-	-
67	7_24V_OUT	O	24 V
68	GND	-	GND

Table 7-13 : Front I/O Connector Pin Assignment TCPS118-20R (Generic)

7.4.6 Front I/O Connector Pin Assignment TCPS118-20R (by Function)

Please note that since 24 V input channels are all inputs, the SSI configuration is not available.

Pin	Generic Name	SSI Mode	Dir	Counter Mode	Dir	Level
1	GND	GND	-	GND	-	GND
2	0_IO0+	-	-	0_A+	I	24 V
3	0_IN1+	-	-	0_B+	I	
4	0_IN2+	-	-	0_I+	I	
5	0_24V_IN	0_24V_IN	I	0_24V_IN	I	24 V
6	1_IO0+	-	-	1_A+	I	24 V
7	1_IN1+	-	-	1_B+	I	
8	1_IN2+	-	-	1_I+	I	
9	1_24V_IN	1_24V_IN	I	1_24V_IN	I	24 V
10	2_IO0+	-	-	2_A+	I	24 V
11	2_IN1+	-	-	2_B+	I	
12	2_IN2+	-	-	2_I+	I	
13	2_24V_IN	2_24V_IN	I	2_24V_IN	I	24 V
14	3_IO0+	-	-	3_A+	I	24 V
15	3_IN1+	-	-	3_B+	I	
16	3_IN2+	-	-	3_I+	I	
17	3_24V_IN	3_24V_IN	I	3_24V_IN	I	24 V
18	4_IO0+	-	-	4_A+	I	24 V
19	4_IN1+	-	-	4_B+	I	
20	4_IN2+	-	-	4_I+	I	
21	4_24V_IN	4_24V_IN	I	4_24V_IN	I	24 V
22	5_IO0+	-	-	5_A+	I	24 V
23	5_IN1+	-	-	5_B+	I	
24	5_IN2+	-	-	5_I+	I	
25	5_24V_IN	5_24V_IN	I	5_24V_IN	I	24 V
26	6_IO0+	-	-	6_A+	I	24 V
27	6_IN1+	-	-	6_B+	I	
28	6_IN2+	-	-	6_I+	I	
29	6_24V_IN	6_24V_IN	I	6_24V_IN	I	24 V
30	7_IO0+	-	-	7_A+	I	24 V
31	7_IN1+	-	-	7_B+	I	
32	7_IN2+	-	-	7_I+	I	
33	7_24V_IN	7_24V_IN	I	7_24V_IN	I	24 V
34	GND	GND	-	GND	-	GND

Pin	Generic Name	SSI Mode	Dir	Counter Mode	Dir	Level
35	GND	GND	-	GND	-	GND
36	-	-	-	-	-	-
37	-	-	-	-	-	
38	-	-	-	-	-	
39	0_24V_OUT	0_24V_OUT	O	0_24V_OUT	O	24 V
40	-	-	-	-	-	-
41	-	-	-	-	-	
42	-	-	-	-	-	
43	1_24V_OUT	1_24V_OUT	O	1_24V_OUT	O	24 V
44	-	-	-	-	-	-
45	-	-	-	-	-	
46	-	-	-	-	-	
47	2_24V_OUT	2_24V_OUT	O	2_24V_OUT	O	24 V
48	-	-	-	-	-	-
49	-	-	-	-	-	
50	-	-	-	-	-	
51	3_24V_OUT	3_24V_OUT	O	3_24V_OUT	O	24 V
52	-	-	-	-	-	-
53	-	-	-	-	-	
54	-	-	-	-	-	
55	4_24V_OUT	4_24V_OUT	O	4_24V_OUT	O	24 V
56	-	-	-	-	-	-
57	-	-	-	-	-	
58	-	-	-	-	-	
59	5_24V_OUT	5_24V_OUT	O	5_24V_OUT	O	24 V
60	-	-	-	-	-	-
61	-	-	-	-	-	
62	-	-	-	-	-	
63	6_24V_OUT	6_24V_OUT	O	6_24V_OUT	O	24 V
64	-	-	-	-	-	-
65	-	-	-	-	-	
66	-	-	-	-	-	
67	7_24V_OUT	7_24V_OUT	O	7_24V_OUT	O	24 V
68	GND	GND	-	GND	-	GND

Table 7-14 : Front I/O Connector Pin Assignment TCPS118-20R (by Function)