

TCPS210

**CompactPCI-Serial Carrier with 3 QMC Sites,
PCIe Gen3 x4, Rear-I/O**

Version 1.0

User Manual

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TCPS210-10R

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PCIe Gen3 x4, Rear-I/O

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Table of Contents

TCPS210	1
Document History	3
Table of Contents	4
List of Figures	5
List of Tables	6
1 PRODUCT DESCRIPTION	7
2 TECHNICAL SPECIFICATION	8
3 HANDLING AND OPERATION INSTRUCTIONS	9
3.1 ESD Protection	9
3.2 Forced Air Cooling	9
3.3 Isolated I/O Ground	9
3.4 Installation	9
3.4.1 QMC Installation	10
3.4.2 QMC Removal	10
4 QMC INTERFACE	11
4.1 QMC Sites	11
4.2 PCI Express Device Topology	12
4.3 Power	12
4.3.1 Power Limits for QMC Modules	12
5 I/O INTERFACE DESCRIPTION	13
5.1 QMC IOPIEs	13
5.2 Front Panel LED Indicator	13
5.3 CPCI-S.0 P1 Connector	14
5.3.1 Connector Type	14
5.3.2 Pin Assignment	14
5.4 CPCI-S.0 P2 & P3 & P4 Connector (Isolated IOPIPE)	15
5.4.1 Connector Type	15
5.4.2 P4 Pin Assignment	15
5.4.3 P3 Pin Assignment	15
5.4.4 P2 Pin Assignment	16
5.5 QMC Carrier Connector	16
5.5.1 Connector Type	16
5.5.2 Pin Assignments	16

List of Figures

FIGURE 1-1 : BLOCK DIAGRAM.....	7
FIGURE 3-1 : QMC REMOVAL.....	10
FIGURE 4-1 : QMC SITE OVERVIEW.....	11
FIGURE 4-2 : PCI EXPRESS DEVICE TOPOLOGY	12
FIGURE 5-1 : TCPS210 FRONT PANEL.....	13

List of Tables

TABLE 2-1 : TECHNICAL SPECIFICATION.....	8
TABLE 4-1 : POWER LIMITS FOR EACH QMC SITE	12
TABLE 5-1 : LINK STATUS LED.....	13
TABLE 5-2 : BOARD STATUS LED.....	13
TABLE 5-3 : CPCI-S.0 P1 CONNECTOR TYPE.....	14
TABLE 5-4 : PERIPHERAL SLOT P1 PIN ASSIGNMENT	14
TABLE 5-5 : CPCI-S.0 P2, P3 & P4 CONNECTOR TYPE	15
TABLE 5-6 : PERIPHERAL SLOT P4 PIN ASSIGNMENT	15
TABLE 5-7 : PERIPHERAL SLOT P3 PIN ASSIGNMENT	15
TABLE 5-8 : PERIPHERAL SLOT P2 PIN ASSIGNMENT	16

1 Product Description

The TCPS210 is a PICMG CPCI-S.0 R3.0 compatible 3U module providing 3 single-width QMC sites, used to build modular, flexible and cost effective I/O solutions for all kinds of applications like process control, medical systems, telecommunication and traffic control.

It can be populated with up to 3 single-width QMC modules, a double-width QMC module and a single-width QMC module, or a triple-width QMC module.

The PCI Express x4 link from the host board (CompactPCI-Serial CPU) is distributed to the 3 QMC sites as x4 links by a non-blocking PCI-Express switch.

QMC I/O is accessible via the CompactPCI-Serial Rear-I/O connectors P2, P3 and P4.

For enhanced system monitoring an IPMC controller is mounted on the TCPS210, enabling real-time QMC health status tracking and seamless communication. For integration in your specific system configuration please contact TEWS.

The TCPS210 QMC Carrier is designed to support integration into conduction cooled systems. Please contact TEWS to discuss your specific system requirements.

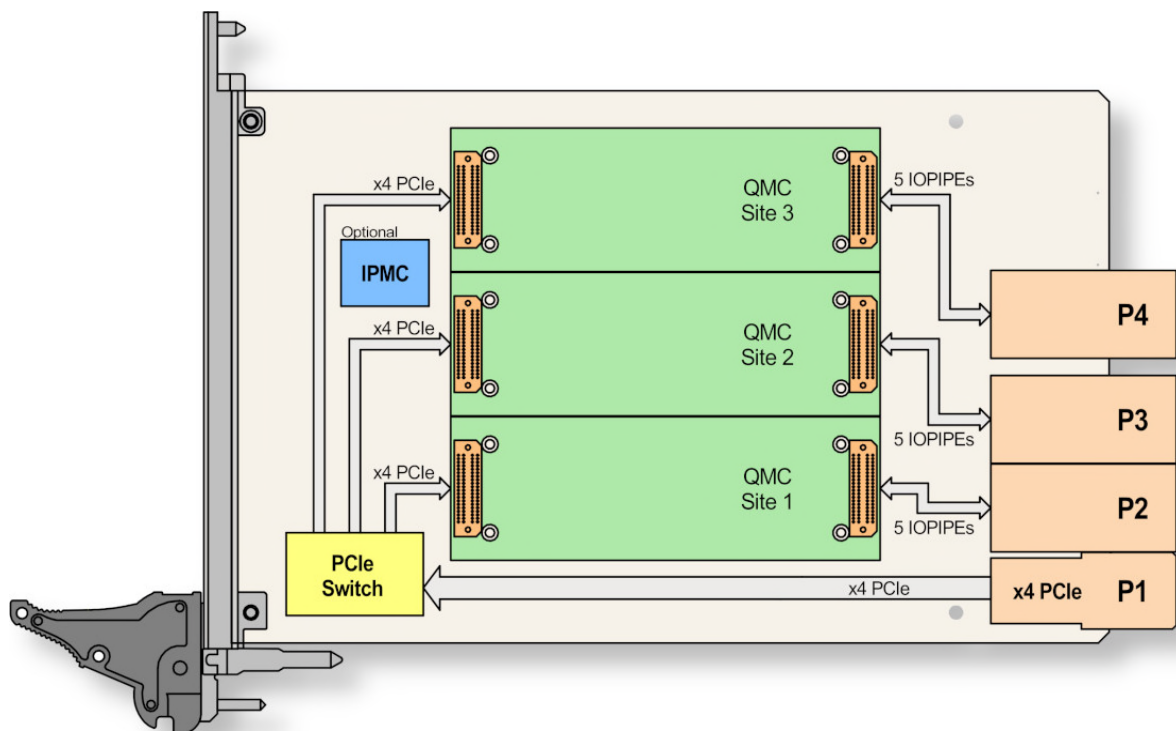


Figure 1-1 : Block Diagram

2 Technical Specification

General	
Mechanical Interface	Compact Serial 3U Front Board conforming to PICMG CPCI-S.0 R3.0
Electrical Interface	PCI Express (Base Specification 3.1) x4 compliant interface

Main On Board Devices	
PCIe Switch	PI7C9X3G816GP (Pericom)

QMC Interface	
Mechanical Interface	ANSI/VITA 93.0-2025 (QMC – Small Form Factor Mezzanine Card)
Number of QMC Sites	3x single-width QMC Sites Can be used for double- or triple-width QMCs
QMC Interface	PCIe Gen3 x4
IOPIPE Isolation	The TCPS210 provides IOPIPE isolation: 30 V per IPC-2221 between IOPIPEs and 30 V per IPC-2221 against system ground
IOPIPE Connection	All QMC IOPIPEs are connected to the CPCI-S.0 Rear I/O
I/O Connectors	Rear I/O: P2, P3 & P4

Physical Data	
Power Requirements	150 mA typical @ +12 V DC 5 mA typical @ +5 V DC (STANDBY) (without QMCs)
Temperature Range	Operating -40 °C to +85 °C Storage -40 °C to +85 °C
MTBF	321 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G _B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	175 g

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection



This CPCI-S.0 module is sensitive to static electricity. Packing, unpacking and all other module handling has to be done with appropriate care!

3.2 Forced Air Cooling



This CPCI-S.0 module generates noticeable heat and requires adequate forced air cooling!
Temperature Control is required!
Forced air cooling is mandatory at ambient temperatures exceeding 25°C!

3.3 Isolated I/O Ground



Isolated ground signals on the I/O connector must be connected to the corresponding external ground!

3.4 Installation

The QMC modules have to be mounted on the TCPS210 prior to installation into the system.

Before installing a QMC module, be sure that the power supply for the TCPS210 is turned off.

The TCPS210 and QMCs are both Electrostatic Sensitive Devices (ESD). Use an anti-static mat connected to a wristband when handling or installing the components.

Make sure that the QMC has the correct orientation before mounting it on the TCPS210. The QMC host connector faces the TCPS210's front panel.

After the QMC module has been installed, it can be secured on the TCPS210 using the mounting screws that come with the TCPS210. There are four screw mounting locations per single QMC module, two at the QMC I/O connector and two at the QMC system connector.

3.4.1 QMC Installation

QMCs are protected against wrong insertion by a polarization feature incorporated in the connector.

QMCs are easily installed by placing them aligned with the Carrier's connectors and gently pressing them onto the Carrier.

The QMC can now be screwed to the Carrier as needed.

3.4.2 QMC Removal

When removing the QMC from the Carrier, care must also be taken to ensure that both plugs are disconnected simultaneously and in parallel. To do this, grasp both short sides of the PCB with both hands at the tabs and carefully lift the QMC.

- Remove the screws that secure the QMC on the carrier, if needed.
- Gently and simultaneously un-plug both connectors of the QMC.

Be aware that there is the potential for damaging the QMC Module or Carrier during QMC Module extraction. Applying an unequal force to the two connectors while unplugging can cause a misalignment, which then can potentially result in damaging the connectors or boards.

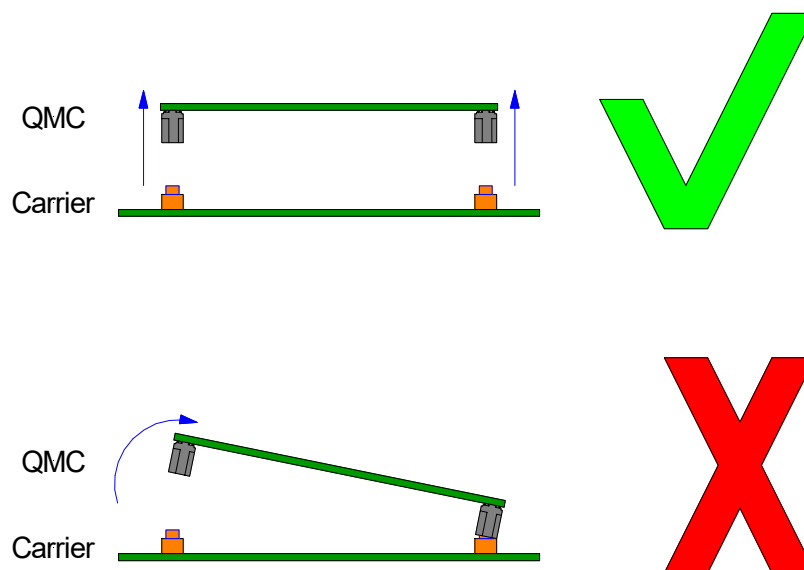


Figure 3-1 : QMC Removal

4 QMC Interface

4.1 QMC Sites

The TCPS210 has three QMC sites. They can be used independently for three single-width QMC modules, for combinations of one single-width and one double-width QMC module, or together for one triple-width QMC module. They are arranged in the following way:

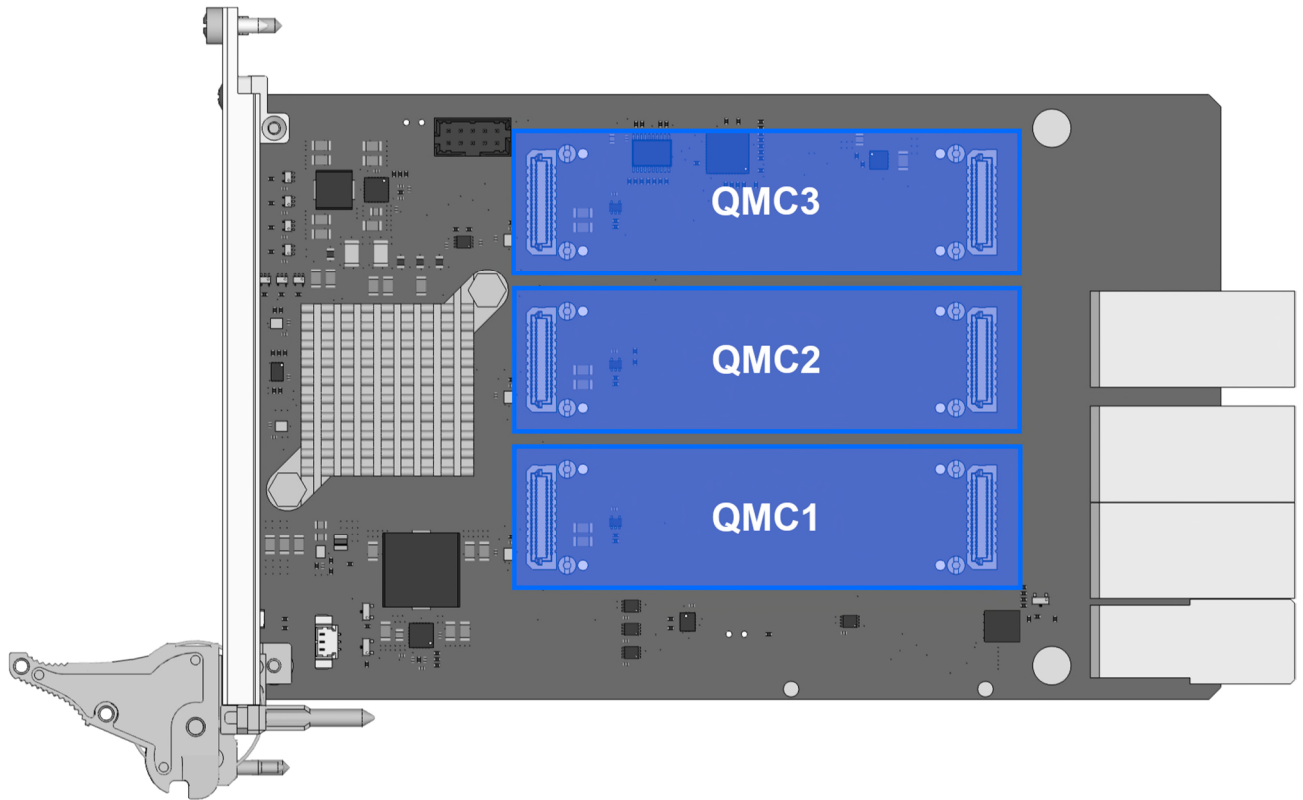


Figure 4-1 : QMC Site Overview

4.2 PCI Express Device Topology

The TCPS210 connects the PCIe x4 Link from the backplane via a PCIe Switch to the QMC sites, each also as x4 link. The x4 Upstream Port of the PCIe Switch is connected to the backplane over the CPCI-S.0 P1 connector. The x4 Downstream Ports of the PCIe Switch are connected to the QMC sites.

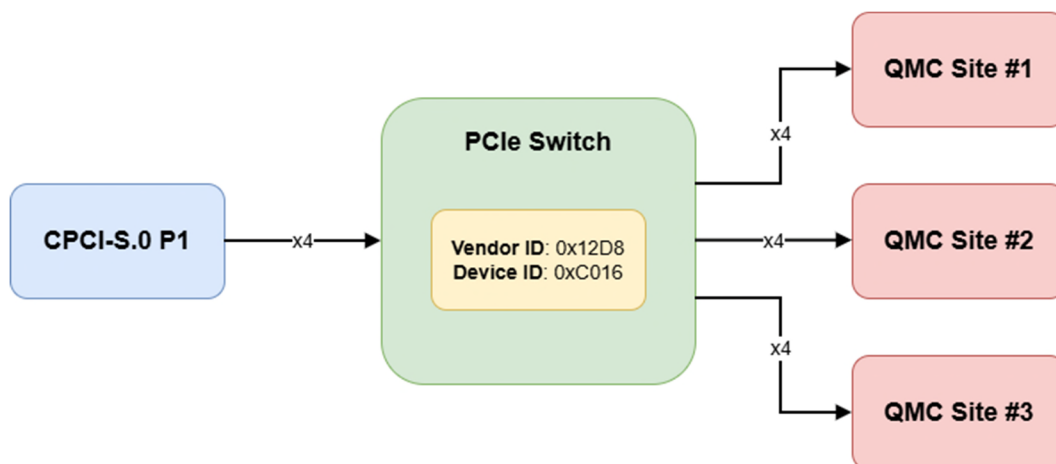


Figure 4-2 : PCI Express Device Topology

4.3 Power

The TCPS210 provides the following power supplies to each QMC Site:

- +12 V
- +3.3 V
- +3.3 V Aux

4.3.1 Power Limits for QMC Modules

In principle, a Single-width QMC can draw up to 30 W of power. With three QMC sites, the potential power draw would exceed the available power permitted for a CPCI-S.0 module. For this reason, the QMC power draw has to be limited.

The cumulative power draw of a single QMC should be limited to 15 W.

The following power limits apply to the QMC sites:

Variant	Voltage	Tolerance %	Current Limit
TCPS210-10R	V12	±10%	1.25 A
	V3.3	±5%	2.1 A
	V3.3AUX	±10%	150 mA (must be shared by all QMCs and the carrier)

Table 4-1 : Power Limits for each QMC Site

Even with the limit to 15 W, users should keep in mind that appropriate system cooling solutions are required when it is utilized by three QMCs.

5 I/O Interface Description

5.1 QMC IOPIPEs

The TCPS210 does support IOPIPE isolation.

All QMC IOPIPEs are routed to CPCI-S.0 Rear I/O.

5.2 Front Panel LED Indicator

The TCPS210 front panel provides four PCIe link status LEDs for quick visual inspection and debugging. A marking is placed close to each LED, to indicate the PCIe link the LED corresponds to.

Each port has one LED indicator. See table below for more details:

LED	Color	State	Description
"QMC 3" "QMC 2" "QMC 1" "Host"	Green	On	Link Up at 8.0 GT/s
		Blinking (2 Hz)	Link Up at 5.0 GT/s
		Blinking (1 Hz)	Link Up at 2.5 GT/s
		Off	Link is down

Table 5-1 : Link Status LED

An additional LED near the front handle provided board status information:

LED	Color	State	Description
"HS"	Red	On	Power Fail
		Off	Power Good, or Power is off
	Green	On	Power Good
		Off	Power not Good, or Power is off

Table 5-2 : Board Status LED



Figure 5-1 : TCPS210 Front Panel

5.3 CPCI-S.0 P1 Connector

5.3.1 Connector Type

Pin-Count	72
Connector Type	AirMax
Source & Order Info	FCI 10052825-101LF

Table 5-3 : CPCI-S.0 P1 Connector Type

5.3.2 Pin Assignment

Pin	1 - 01	1 - 02	1 - 03	1 - 04	1 - 05	1 - 06
L	GND	SYSEN#	GA3	1_SATA_Rx-	GND	1_PE_Rx03-
K	+12V	PCIE_EN#	SATA_SL	1_SATA_Rx+	1_PE_Rx01-	1_PE_Rx03+
J	+12V	GND	SATA_SCL	GND	1_PE_Rx01+	GND
I	GND	WAKE_OUT#	GA2	1_SATA_Tx-	GND	1_PE_Tx03-
H	+12V	RST#	SATA_SDO	1_SATA_Tx+	1_PE_Tx01-	1_PE_Tx03+
G	+12V	GND	SATA_SDI	GND	1_PE_Tx01+	GND
F	GND	reserved	GA1	PE_CLKIN-	GND	1_PE_Rx02-
E	+12V	reserved	1_USB3_Rx-	PE_CLKIN+	1_PE_Rx00-	1_PE_Rx02+
D	+12V	GND	1_USB3_Rx+	GND	1_PE_Rx00+	GND
C	GND	I ² C_SDA	GA0	1_USB2-	GND	1_PE_Tx02-
B	STANDBY	I ² C_SCL	1_USB3_Tx-	1_USB2+	1_PE_Tx00-	1_PE_Tx02+
A	+12V	GND	1_USB3_Tx+	GND	1_PE_Tx00+	GND

Table 5-4 : Peripheral Slot P1 Pin Assignment

5.4 CPCI-S.0 P2 & P3 & P4 Connector (Isolated IOPIPE)

5.4.1 Connector Type

Pin-Count	96
Connector Type	AirMax
Source & Order Info	FCI 10052837-101LF

Table 5-5 : CPCI-S.0 P2, P3 & P4 Connector Type

5.4.2 P4 Pin Assignment

Pin	4 - 01	4 - 02	4 - 03	4 - 04	4 - 05	4 - 06	4 - 07	4 - 08
L	n.c.	GND1	n.c.	IO2C-	n.c.	IO4A-	n.c.	IO5D-
K	-	GND1	IO1D-	IO2C+	IO3B-	IO4A+	GND5	IO5D+
J	-	n.c.	IO1D+	n.c.	IO3B+	n.c.	GND5	n.c.
I	n.c.	-	n.c.	IO2B-	n.c.	GND4	n.c.	IO5C-
H	-	-	IO1C-	IO2B+	IO3A-	GND4	IO4D-	IO5C+
G	-	n.c.	IO1C+	n.c.	IO3A+	n.c.	IO4D+	n.c.
F	n.c.	-	n.c.	IO2A-	n.c.	IO3D-	n.c.	IO5B-
E	-	-	IO1B-	IO2A+	GND3	IO3D+	IO4C-	IO5B+
D	-	n.c.	IO1B+	n.c.	GND3	n.c.	IO4C+	n.c.
C	n.c.	-	n.c.	GND2	n.c.	IO3C-	n.c.	IO5A-
B	-	-	IO1A-	GND2	IO2D-	IO3C+	IO4B-	IO5A+
A	-	n.c.	IO1A+	n.c.	IO2D+	n.c.	IO4B+	n.c.
		QMC 3						

Table 5-6 : Peripheral Slot P4 Pin Assignment

5.4.3 P3 Pin Assignment

Pin	3 - 01	3 - 02	3 - 03	3 - 04	3 - 05	3 - 06	3 - 07	3 - 08
L	n.c.	GND1	n.c.	IO2C-	n.c.	IO4A-	n.c.	IO5D-
K	GND5	GND1	IO1D-	IO2C+	IO3B-	IO4A+	GND5	IO5D+
J	GND5	n.c.	IO1D+	n.c.	IO3B+	n.c.	GND5	n.c.
I	n.c.	-	n.c.	IO2B-	n.c.	GND4	n.c.	IO5C-
H	IO5D-	-	IO1C-	IO2B+	IO3A-	GND4	IO4D-	IO5C+
G	IO5D+	n.c.	IO1C+	n.c.	IO3A+	n.c.	IO4D+	n.c.
F	n.c.	-	n.c.	IO2A-	n.c.	IO3D-	n.c.	IO5B-
E	IO5C-	-	IO1B-	IO2A+	GND3	IO3D+	IO4C-	IO5B+
D	IO5C+	n.c.	IO1B+	n.c.	GND3	n.c.	IO4C+	n.c.
C	n.c.	IO5A-	n.c.	GND2	n.c.	IO3C-	n.c.	IO5A-
B	IO5B-	IO5A+	IO1A-	GND2	IO2D-	IO3C+	IO4B-	IO5A+
A	IO5B+	n.c.	IO1A+	n.c.	IO2D+	n.c.	IO4B+	n.c.
	QMC 1	QMC 2						

Table 5-7 : Peripheral Slot P3 Pin Assignment

5.4.4 P2 Pin Assignment

Pin	2 - 01	2 - 02	2 - 03	2 - 04	2 - 05	2 - 06	2 - 07	2 - 08
L	GND	-	n.c.	IO1C-	n.c.	IO3A-	n.c.	IO4D-
K	-	-	-	IO1C+	IO2B-	IO3A+	GND4	IO4D+
J	-	GND	-	n.c.	IO2B+	n.c.	GND4	n.c.
I	GND	-	n.c.	IO1B-	n.c.	GND3	n.c.	IO4C-
H	-	-	-	IO1B+	IO2A-	GND3	IO3D-	IO4C+
G	-	GND	-	n.c.	IO2A+	n.c.	IO3D+	n.c.
F	GND	-	n.c.	IO1A-	n.c.	IO2D-	n.c.	IO4B-
E	-	-	-	IO1A+	GND2	IO2D+	IO3C-	IO4B+
D	-	GND	-	n.c.	GND2	n.c.	IO3C+	n.c.
C	GND	-	n.c.	GND1	n.c.	IO2C-	n.c.	IO4A-
B	-	-	-	GND1	IO1D-	IO2C+	IO3B-	IO4A+
A	-	GND	-	n.c.	IO1D+	n.c.	IO3B+	n.c.
	n.c.			QMC 1				

Table 5-8 : Peripheral Slot P2 Pin Assignment

5.5 QMC Carrier Connector

5.5.1 Connector Type

Pin-Count	80
Connector Type	Samtec AccelerateHD, 4x20 pins 11 mm stacking height
Source & Order Info	Samtec ADM6-20-03.5-L-4-0-A

5.5.2 Pin Assignments

See VITA 93.0 (QMC) Specification