The Embedded I/O Company

TEWS TECHNOLOGIES

TCPS892

Four Channel 10/100/1000 Mbit/s Ethernet

Version 1.0

User Manual

Issue 1.0.1

November 2021

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

TCPS892-10R

Four Channel 10/100/1000 Mbit/s Ethernet, Intel I350, P3 Rear I/O

(RoHS compliant)

Issue	Description	Date
0.9.0	Preliminary issue	March 2021
1.0.0	Initial Issue	September 2021
1.0.1	Minor Correction to the Block Diagram	November 2021

Table of Contents

List of Figures

List of Tables

1 Product Description

The TCPS892 is a PICMG CPCI-S.0 R2.0 compatible 3U module providing a four channel Ethernet 10Base-T / 100Base-TX / 1000Base-T interface.

The Intel I350 provides integrated PHYs that support 10, 100 and 1000 Mbit/s transmission rates and is equipped with a 1 Mbit Serial Flash to support PXE and iSCSI boot.

The four Ethernet interfaces of the TCPS892 are capable of performing an auto negotiation algorithm which allows both link-partners to determine the best link-parameters. The TCPS892 supports IEEE 1588/802.1AS Precision Time Protocol (PTP).

The controller is equipped with a 128 Kbit EEPROM storing configuration data. LEDs in the front panel indicate the different network activities.

All ports are galvanically isolated from the Ethernet controllers and are routed to the P3 rear I/O connector.

An accompanying CompactPCI Serial 3U Rear Board TCPS007-TM with reconstruction filters and four RJ45 connectors is available.

Software support:

- Software support for Intel™ I350 at www.intel.com
- For operating systems not supported by Intel™, please contact TEWS.

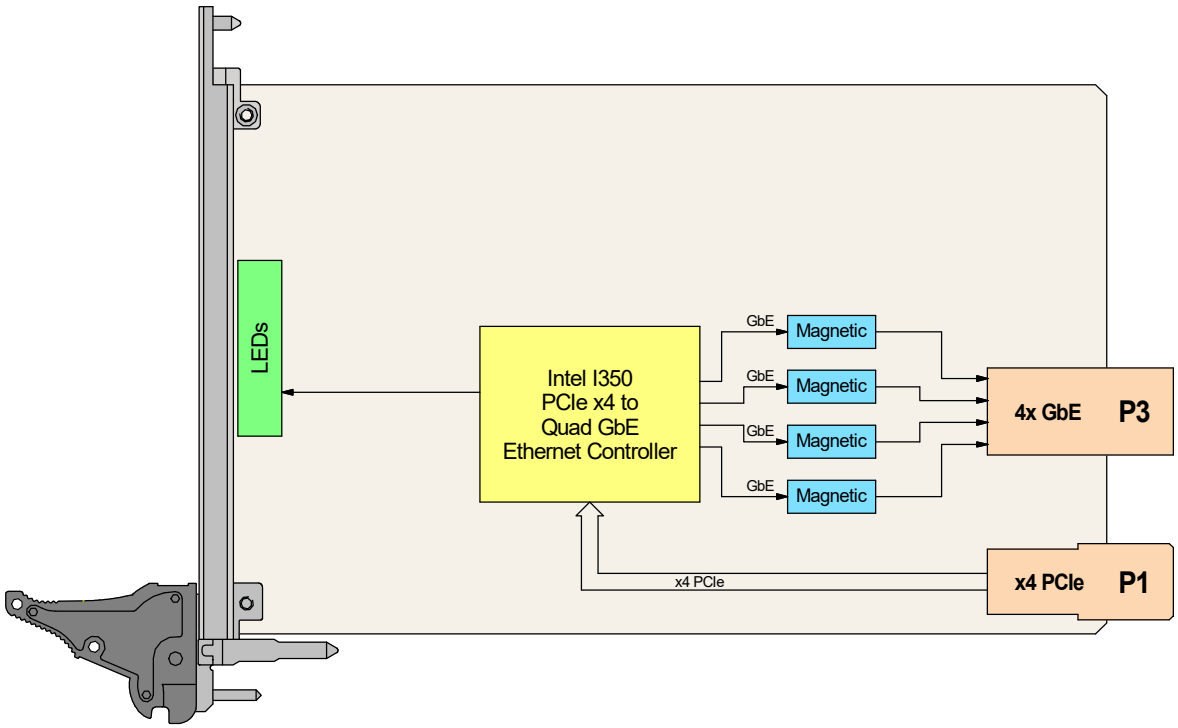

Figure 1-1 : Block Diagram

2 Technical Specification

Interface	
Mechanical Interface	Compact Serial 3U Front Board conforming to PICMG CPCI-S.0 R2.0
Electrical Interface	PCI Express (Base Specification 2.1) x4 compliant interface

On Board Devices	
Gigabit Ethernet Controller	I350-AM4 (Intel)

I/O Interface	
Number of Channels	4
I/O Standards	1000Base-T 100Base-TX 10Base-T
I/O Connector	P3 rear I/O

Physical Data		
Power Requirements	400 mA typical @ +12 V DC	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	539000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	151 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This CPCI-S.0 module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

3.2 Power Dissipation

This CPCI-S.0 module requires adequate forced air cooling!

4 PCI Interface

4.1 Multifunctional Device (Intel Corporation)

The Intel I350-AM4 Gigabit Ethernet Controller is represented by a multifunctional device on the PCI bus. The four different Ethernet Channels can be identified by the corresponding function of the device.

Vendor-ID	0x8086 (Intel Corporation)
Device-ID	0x1521 (I350 Gigabit Copper Network Connection)

Table 4-1 : Bus : Device : Function 0x00

Vendor-ID	0x8086 (Intel Corporation)
Device-ID	0x1521 (I350 Gigabit Copper Network Connection)

Table 4-2 : Bus : Device : Function 0x01

Vendor-ID	0x8086 (Intel Corporation)
Device-ID	0x1521 (I350 Gigabit Copper Network Connection)

Table 4-3 : Bus : Device : Function 0x02

Vendor-ID	0x8086 (Intel Corporation)
Device-ID	0x1521 (I350 Gigabit Copper Network Connection)

Table 4-4 : Bus : Device : Function 0x03

4.2 PCI Identifiers

Vendor-ID	0x8086 (Intel Corporation)
Device-ID	0x1521 (I350 Gigabit Copper Network Connection)
Class Code	0x0200 (Ethernet Controller)
Subsystem Vendor-ID	0xFFFF
Subsystem Device-ID	0x0000

Table 4-5 : PCI Identifiers

4.3 PCI Base Address Register Configuration

PCI Base Address Register (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	256K	32	Little	Internal Registers
1 (0x14)	-	-	-	-	-
2 (0x18)	I/O	32	32	Little	Internal Registers
3 (0x1C)	MEM	16K	32	Little	MSI-X BAR

Table 4-6 : PCI Base Address Registers

5 LEDs

The TCPS892 front panel provides four ethernet status LEDs for quick visual inspection and debugging. A marking is placed close to each LED, to indicate the port the LED corresponds to.

Each port has one LED indicator. See table below for more details:

LED Status	Description
OFF	No cable is connected or no link is established
ON	A link is established at the corresponding Ethernet Port
BLINKING	Indicates activity: The Ethernet Port transmits or receives data

Table 5-1 : Ethernet LED Status

An additional LED near the front handle provided board status information:

LED	Color	State	Description
Front Panel	Red	On	Power Fail
		Off	Power Good, or Power is off
	Green	On	Power Good
		Off	Power is off

Table 5-2 : Board Status LED

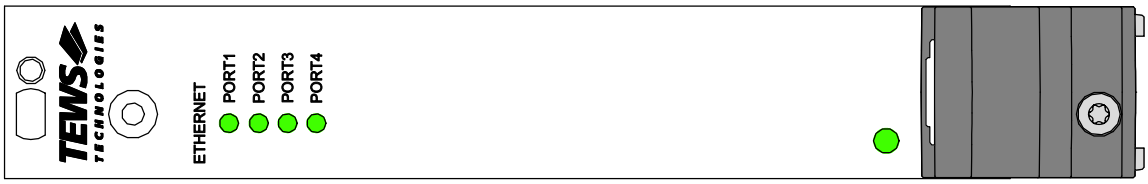

Figure 5-1 : TCPS892 Front Panel

6 Pin Assignment – I/O Connector

6.1 CPCI-S.0 P1 Connector

Pin	1 - 01	1 - 02	1 - 03	1 - 04	1 - 05	1 - 06
A	+12V	GND	1_USB3_Tx+	GND	1_PE_Tx00+	GND
B	STANDBY	I²C_SCL	1_USB3_Tx-	1_USB2+	1_PE_Tx00-	1_PE_Tx02+
C	GND	I²C_SDA	GA0	1_USB2-	GND	1_PE_Tx02-
D	+12V	GND	1_USB3_Rx+	GND	1_PE_Rx00+	GND
E	+12V	reserved	1_USB3_Rx-	PE_CLKIN+	1_PE_Rx00-	1_PE_Rx02+
F	GND	reserved	GA1	PE_CLKIN-	GND	1_PE_Rx02-
G	+12V	GND	SATA_SDI	GND	1_PE_Tx01+	GND
H	+12V	RST#	SATA_SDO	1_SATA_Tx+	1_PE_Tx01-	1_PE_Tx03+
I	GND	WAKE_OUT#	GA2	1_SATA_Tx-	GND	1_PE_Tx03-
J	+12V	GND	SATA_SCL	GND	1_PE_Rx01+	GND
K	+12V	PCIE_EN#	SATA_SL	1_SATA_Rx+	1_PE_Rx01-	1_PE_Rx03+
L	GND	SYSEN#	GA3	1_SATA_Rx-	GND	1_PE_Rx03-

Table 6-1 : Peripheral Slot P1 Pin Assignment

6.2 CPCI-S.0 P3 Connector

Pin	3 - 01	3 - 02	3 - 03	3 - 04	3 - 05	3 - 06	3 - 07	3 - 08
A	ETH_0_0+	GND	ETH_2_0+	GND	-	GND	-	GND
B	ETH_0_0-	ETH_1_0+	ETH_2_0-	ETH_3_0+	-	-	-	-
C	GND	ETH_1_0-	GND	ETH_3_0-	GND	-	GND	-
D	ETH_0_1+	GND	ETH_2_1+	GND	-	GND	-	GND
E	ETH_0_1-	ETH_1_1+	ETH_2_1-	ETH_3_1+	-	-	-	-
F	GND	ETH_1_1-	GND	ETH_3_1-	GND	-	GND	-
G	ETH_0_2+	GND	ETH_2_2+	GND	-	GND	-	GND
H	ETH_0_2-	ETH_1_2+	ETH_2_2-	ETH_3_2+	-	-	-	-
I	GND	ETH_1_2-	GND	ETH_3_2-	GND	-	GND	-
J	ETH_0_3+	GND	ETH_2_3+	GND	(TERM)	GND	(TERM)	GND
K	ETH_0_3-	ETH_1_3+	ETH_2_3-	ETH_3_3+	(TERM)	(TERM)	(TERM)	(TERM)
L	GND	ETH_1_3-	GND	ETH_3_3-	GND	(TERM)	GND	(TERM)

Table 6-2 : Peripheral Slot P3 Pin Assignment

(TERM) is an optional connection to the termination plane

Signal naming is “ETH_*Channel_Diff-Pair*+/-”.