The Embedded I/O Company

TEWS TECHNOLOGIES

TDRV020-SW-42

VxWorks Device Driver

Reconfigurable FPGA

Version 1.0.x

User Manual

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TDRV020-SW-42

VxWorks Device Driver

FPGA Platform Example Application

Supported Modules:
TMPE623
TMPE627
TMPE633

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1 Introduction

The TDRV020-SW-42 VxWorks device driver software allows the operation of the supported hardware modules conforming to the VxWorks I/O system specification.

The driver provides an application programming interface (API) which allows OS independent access to the devices for compatibility between different OS versions and OS.

The TDRV020-SW-42 VxWorks device driver was designed to demonstrate the usage of main functions of the supported FPGA platform example application in a legacy and VxBus VxWorks driver environment. The well documented device driver software can be used as base for customized FPGA platform applications.

The TDRV020-SW-42 device driver supports the following features:

- Read/write access to FPGA registers (8,16,32-bit)
- Resource allocation for supported modules
- Wait for interrupts
- Register Callback functions for interrupt handling
- Driver functions are thread-safe as long as unique handles are used.

The TDRV020-SW-42 supports the modules listed below:

TMPE623	Reconfigurable FPGA with Digital I/O	PCIe Mini Card
TMPE627	Reconfigurable FPGA with AD/DA and Digital I/O	PCIe Mini Card
TMPE633	Reconfigurable FPGA with Digital I/O	PCIe Mini Card

In this document all supported modules and devices will be called TDRV020. Specials for certain devices will be advised.

To get more information about the features and use of supported devices it is recommended to read the manuals for the supported modules listed below.

TEWS TECHNOLOGIES VxWorks Device Drivers – Installation Guide
Hardware User Manual documentation
Related FPGA Design documentation

2 API Documentation

2.1 General Functions

2.1.1 tdrv020Open

NAME

tdrv020Open – open a device.

SYNOPSIS

```
TDRV020_HANDLE tdrv020Open
(
      char          *DeviceName
)
```

DESCRIPTION

Before I/O can be performed to a device, a device handle must be opened by a call to this function. If the legacy TDRV020 driver is used, this function will also install the legacy driver and create devices with the first call. The VxBus TDRV020 driver will be installed automatically by the VxBus system.

The tdrv020Open function can be called multiple times (e.g. in different tasks)

PARAMETERS

DeviceName

This parameter points to a null-terminated string that specifies the name of the device. The first TDRV020 device is named “/tdrv020/0” the second device is named “/tdrv020/1” and so on.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE     hdl;

…
```

…

```
/*
** open the specified device
*/
hdl = tdrv020Open(“/tdrv020/0”);
if (hdl == NULL)
{
     /* handle open error */
}
```

RETURNS

A device handle, or NULL if the function fails. An error code will be stored in *errno*.

ERROR CODES

The error codes are stored in *errno.*

The error code is a standard error code set by the I/O system.

2.1.2 tdrv020Close

NAME

tdrv020Close – close a device.

SYNOPSIS

```
TDRV020_STATUS tdrv020Close
(
     TDRV020_HANDLE       hdl
)
```

DESCRIPTION

This function closes a previously opened device.

PARAMETERS

hdl

This value specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;

/*
** close the device
*/
result = tdrv020Close(hdl);
if (result != TDRV020_OK)
{
     /* handle close error */
}
```

RETURNS

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid

2.1.3 tdrv020GetPciInfo

NAME

tdrv020GetPciInfo – get information of the module PCI header

SYNOPSIS

```
TDRV020_STATUS tdrv020GetPciInfo
(
    TDRV020_HANDLE          hdl,
    TDRV020_PCIINFO_BUF     *pPciInfoBuf
)
```

DESCRIPTION

This function returns information of the module PCI header in the provided data buffer.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pPciInfoBuf

This argument is a pointer to the structure TDRV020_PCIINFO_BUF that receives information of the module PCI header.

```
typedef struct
{
    unsigned short      vendorId;
    unsigned short      deviceId;
    unsigned short      subSystemId;
    unsigned short      subSystemVendorId;
    int                 pciBusNo;
    int                 pciDevNo;
    int                 pciFuncNo;
} TDRV020_PCIINFO_BUF;
```

vendorId

PCI module vendor ID.

deviceId

PCI module device ID

subSystemId

PCI module sub system ID

subSystemVendorId

PCI module sub system vendor ID

pciBusNo

Number of the PCI bus, where the module resides.

pciDevNo

PCI device number

pciFuncNo

PCI function number

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE          hdl;
TDRV020_STATUS          result;
TDRV020_PCIINFO_BUF     pciInfoBuf

/*
** get module PCI information
*/
result = tdrv020GetPciInfo(hdl, &pciInfoBuf);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid

2.1.4 tdrv020RestorePciHeader

NAME

tdrv020RestorePciHeader – Restore the PCI header of the User-FPGA

SYNOPSIS

```
TDRV020_STATUS tdrv020RestorePciHeader
(
    TDRV020_HANDLE      hdl
)
```

DESCRIPTION

This function restores the PCI header of the User-FPGA, using values stored upon driver start. After reconfiguration of a User-FPGA, the PCI header configuration is lost. To allow further accesses to the User-FPGA, the PCI header must be restored using this function.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE    hdl;
TDRV020_STATUS    result;

/*
** Restore the PCI header of the User-FPGA
*/
result = tdrv020RestorePciHeader( hdl );
if (result != TDRV020_OK)
{
    /* handle error */
}
```

RETURNS

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified TDRV020_HANDLE is invalid.
TDRV020_ERR_NOSYS	This function is not supported by the device.

2.2 Register Access Functions

2.2.1 tdrv020Read8

NAME

tdrv020Read8 – read 8-bit values from PCI BAR space

SYNOPSIS

```
TDRV020_STATUS tdrv020Read8
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    int                 offset,
    int                 numItems,
    unsigned char       *pData
)
```

DESCRIPTION

This function reads the specified number of items from the PCI BAR space by using single byte (8-bit) accesses.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

offset

This argument specifies the start offset within the PCI BAR space.

numItems

This argument specifies the number of items (8-bit) to read.

pData

This argument is a pointer to an unsigned char buffer which will be filled with the specified number of items from the PCI BAR space. The allocated space must be large enough to hold the specified amount of data.

EXAMPLE

```
#include “tdrv020api.h”

#define NUM_ITEMS  256

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
int                offset;
unsigned char      dataBuf[NUM_ITEMS];


offset = 0x0000;
/*
** read 256 Bytes from the User FPGA Register Area
*/
result = tdrv020Read8(hdl, TDRV020_RES_MEM_1, offset, NUM_ITEMS, dataBuf);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	The specified access range exceeds PCI BAR limits
TDRV020_ERR_ACCESS	The specified PCI resource is not available

2.2.2 tdrv020ReadBE16

NAME

tdrv020ReadBE16 – read 16-bit values from PCI BAR space in big-endian order

SYNOPSIS

```
TDRV020_STATUS tdrv020ReadBE16
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    int                 offset,
    int                 numItems,
    unsigned short      *pData
)
```

DESCRIPTION

This function reads the specified number of items from the PCI BAR space by using 16-bit accesses. The values are returned as big-endian values that mean on Intel x86 architectures the multi-byte data will be byte-swapped.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

offset

This argument specifies the start offset within the PCI BAR space.

numItems

This argument specifies the number of items (16-bit) to read.

pData

This argument is a pointer to an unsigned short buffer which will be filled with the specified number of items from the PCI BAR space. The allocated space must be large enough to hold the specified amount of data.

EXAMPLE

```
#include “tdrv020api.h”

#define NUM_ITEMS  128

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
int                offset;
unsigned short     dataBuf[NUM_ITEMS];

offset = 0x0000;
/*
** read 256 Bytes from the User FPGA Register Area
*/
result = tdrv020ReadBE16(hdl, TDRV020_RES_MEM_1, offset, NUM_ITEMS,
                                                  dataBuf);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	The specified access range exceeds PCI BAR limits
TDRV020_ERR_ACCESS	The specified PCI resource is not available

2.2.3 tdrv020ReadLE16

NAME

tdrv020ReadLE16 – read 16-bit values from PCI BAR space in little-endian order

SYNOPSIS

```
TDRV020_STATUS tdrv020ReadLE16
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    int                 offset,
    int                 numItems,
    unsigned short      *pData
)
```

DESCRIPTION

This function reads the specified number of items from the PCI BAR space by using 16-bit accesses. The values are returned as little-endian values that means on Intel x86 architectures the multi-byte data will not be byte-swapped.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

offset

This argument specifies the start offset within the PCI BAR space.

numItems

This argument specifies the number of items (16-bit) to read.

pData

This argument is a pointer to an unsigned short buffer which will be filled with the specified number of items from the PCI BAR space. The allocated space must be large enough to hold the specified amount of data.

EXAMPLE

```
#include “tdrv020api.h”

#define NUM_ITEMS  128

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
int                offset;
unsigned short     dataBuf[NUM_ITEMS];

offset = 0x0000;
/*
** read 256 Bytes from the User FPGA Register Area
*/
result = tdrv020ReadLE16(hdl, TDRV020_RES_MEM_1, offset, NUM_ITEMS,
                                                  dataBuf);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	The specified access range exceeds PCI BAR limits
TDRV020_ERR_ACCESS	The specified PCI resource is not available

2.2.4 tdrv020ReadBE32

NAME

tdrv020ReadBE32 – read 32-bit values from PCI BAR space in big-endian order

SYNOPSIS

```
TDRV020_STATUS tdrv020ReadBE32
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    int                 offset,
    int                 numItems,
    unsigned int        *pData
)
```

DESCRIPTION

This function reads the specified number of items from the PCI BAR space by using 32-bit accesses. The values are returned as big-endian values that means on Intel x86 architectures the multi-byte data will be byte-swapped.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

offset

This argument specifies the start offset within the PCI BAR space.

numItems

This argument specifies the number of items (32-bit) to read.

pData

This argument is a pointer to an unsigned int buffer which will be filled with the specified number of items from the PCI BAR space. The allocated space must be large enough to hold the specified amount of data.

EXAMPLE

```
#include “tdrv020api.h”

#define NUM_ITEMS  1

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
int                offset;
unsigned int       dataBuf[NUM_ITEMS];

offset = 0;
/*
** read Digital Input Register of FPGA Example Design
*/
result = tdrv020ReadBE32(hdl, TDRV020_RES_MEM_1, offset, NUM_ITEMS,
                                                  dataBuf);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	The specified access range exceeds PCI BAR limits
TDRV020_ERR_ACCESS	The specified PCI resource is not available

2.2.5 tdrv020ReadLE32

NAME

tdrv020ReadLE32 – read 32-bit values from PCI BAR space in little-endian order

SYNOPSIS

```
TDRV020_STATUS tdrv020ReadLE32
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    int                 offset,
    int                 numItems,
    unsigned int        *pData
)
```

DESCRIPTION

This function reads the specified number of items from the PCI BAR space by using 32-bit accesses. The values are returned as little-endian values that means on Intel x86 architectures the multi-byte data will not be byte-swapped.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

offset

This argument specifies the start offset within the PCI BAR space.

numItems

This argument specifies the number of items (32-bit) to read.

pData

This argument is a pointer to an unsigned int buffer which will be filled with the specified number of items from the PCI BAR space. The allocated space must be large enough to hold the specified amount of data.

EXAMPLE

```
#include “tdrv020api.h”

#define NUM_ITEMS  1

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
int                offset;
unsigned int       dataBuf[NUM_ITEMS];

offset = 0;
/*
** read Digital Input Register of FPGA Example Design
*/
result = tdrv020ReadLE32(hdl, TDRV020_RES_MEM_1, offset, NUM_ITEMS,
                                                  dataBuf);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	The specified access range exceeds PCI BAR limits
TDRV020_ERR_ACCESS	The specified PCI resource is not available

2.2.6 tdrv020Write8

NAME

tdrv020Write8 – write 8-bit values to the PCI BAR space

SYNOPSIS

```
TDRV020_STATUS tdrv020Write8
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    int                 offset,
    int                 numItems,
    unsigned char       *pData
)
```

DESCRIPTION

This function writes the specified number of items to the PCI BAR space by using single byte (8-bit) accesses.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

offset

This argument specifies the start offset within the PCI BAR space.

numItems

This argument specifies the number of items (8-bit) to write.

pData

This argument is a pointer to an unsigned char buffer with the data items to write. The allocated space must be large enough to hold the specified amount of data.

EXAMPLE

```
#include “tdrv020api.h”

#define NUM_ITEMS  4

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
int                offset;
unsigned char      dataBuf[NUM_ITEMS];

dataBuf[0] = 0xAA;
dataBuf[1] = 0x55;
…

offset = 0x00;

/*
** write 4 bytes to a 32bit Scratchpad Register
*/
result = tdrv020Write8(hdl, TDRV020_RES_MEM_1, offset, NUM_ITEMS, dataBuf);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	The specified access range exceeds PCI BAR limits
TDRV020_ERR_ACCESS	The specified PCI resource is not available

2.2.7 tdrv020WriteBE16

NAME

tdrv020WriteBE16 – write 16-bit values to the PCI BAR space big-endian order

SYNOPSIS

```
TDRV020_STATUS tdrv020WriteBE16
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    int                 offset,
    int                 numItems,
    unsigned short      *pData
)
```

DESCRIPTION

This function writes the specified number of items to the PCI BAR space by using 16-bit accesses.

The values are written in big-endian order that means on Intel x86 architectures the multi-byte data will be byte-swapped.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

offset

This argument specifies the start offset within the PCI BAR space.

numItems

This argument specifies the number of items (16-bit) to write.

pData

This argument is a pointer to an unsigned short buffer with the data items to write. The allocated space must be large enough to hold the specified amount of data.

EXAMPLE

```
#include “tdrv020api.h”

#define NUM_ITEMS  2

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
int                offset;
unsigned short     dataBuf[NUM_ITEMS];

dataBuf[0] = 0xAA55;
dataBuf[1] = 0x55AA;
…

offset = 0xF8;
/*
** write 2 datawords to a 32bit Scratchpad Register
*/
result = tdrv020WriteBE16(hdl, TDRV020_RES_MEM_1, offset, NUM_ITEMS,
                                                    dataBuf);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	The specified access range exceeds PCI BAR limits
TDRV020_ERR_ACCESS	The specified PCI resource is not available

2.2.8 tdrv020WriteLE16

NAME

tdrv020WriteLE16 – write 16-bit values to the PCI BAR space in little-endian order

SYNOPSIS

```
TDRV020_STATUS tdrv020WriteLE16
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    int                 offset,
    int                 numItems,
    unsigned short      *pData
)
```

DESCRIPTION

This function writes the specified number of items to the PCI BAR space by using 16-bit accesses.

The values are written in little-endian order that means on Intel x86 architectures the multi-byte data will not be byte-swapped.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

offset

This argument specifies the start offset within the PCI BAR space.

numItems

This argument specifies the number of items (16-bit) to write.

pData

This argument is a pointer to an unsigned short buffer with the data items to write. The allocated space must be large enough to hold the specified amount of data.

EXAMPLE

```
#include “tdrv020api.h”

#define NUM_ITEMS  2

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
int                offset;
unsigned short     dataBuf[NUM_ITEMS];

dataBuf[0] = 0xAA55;
dataBuf[1] = 0x55AA;
…

offset = 0xF8;
/*
** write 2 data words to a 32bit Scratchpad Register
*/
result = tdrv020WriteLE16(hdl, TDRV020_RES_MEM_1, offset, NUM_ITEMS,
                                                    dataBuf);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	The specified access range exceeds PCI BAR limits
TDRV020_ERR_ACCESS	The specified PCI resource is not available

2.2.9 tdrv020WriteBE32

NAME

tdrv020WriteBE32 – write 32-bit values to the PCI BAR space big-endian order

SYNOPSIS

```
TDRV020_STATUS tdrv020WriteBE32
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    int                 offset,
    int                 numItems,
    unsigned int        *pData
)
```

DESCRIPTION

This function writes the specified number of items to the PCI BAR space by using 32-bit accesses.

The values are written in big-endian order that means on Intel x86 architectures the multi-byte data will be byte-swapped.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

offset

This argument specifies the start offset within the PCI BAR space.

numItems

This argument specifies the number of items (32-bit) to write.

pData

This argument is a pointer to an unsigned int buffer with the data items to write. The allocated space must be large enough to hold the specified amount of data.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
int                offset;
unsigned int       data;

data      = 0x12345678;
offset    = 0xF8;
/* Write Test data into a 32bit Scratchpad Register */
result = tdrv020WriteBE32(hdl, TDRV020_RES_MEM_1, offset, 1, &data);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	The specified access range exceeds PCI BAR limits
TDRV020_ERR_ACCESS	The specified PCI resource is not available

2.2.10 tdrv020WriteLE32

NAME

tdrv020WriteLE32 – write 32-bit values to the PCI BAR space in little-endian order

SYNOPSIS

```
TDRV020_STATUS tdrv020WriteLE32
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    int                 offset,
    int                 numItems,
    unsigned int        *pData
)
```

DESCRIPTION

This function writes the specified number of items to the PCI BAR space by using 32-bit accesses.

The values are written in little-endian order that means on Intel x86 architectures the multi-byte data will not be byte-swapped.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

offset

This argument specifies the start offset within the PCI BAR space.

numItems

This argument specifies the number of items (32-bit) to write.

pData

This argument is a pointer to an unsigned int buffer with the data items to write. The allocated space must be large enough to hold the specified amount of data.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
int                offset;
unsigned int       data;

data      = 0x12345678;
offset    = 0xF8;
/* Write Test data into a 32bit Scratchpad Register */
result = tdrv020WriteLE32(hdl, TDRV020_RES_MEM_1, offset, 1, &data);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	The specified access range exceeds PCI BAR limits
TDRV020_ERR_ACCESS	The specified PCI resource is not available

2.3 Resource Mapping Functions

2.3.1 tdrv020PciResourceMap

NAME

tdrv020PciResourceMap – map a PCI resource directly into the process context

SYNOPSIS

```
TDRV020_STATUS tdrv020PciResourceMap
(
    TDRV020_HANDLE      hdl,
    int                 pciResource,
    unsigned char       **pPtr,
    unsigned int        *pSize
)
```

DESCRIPTION

This function maps the specified PCI resource of the hardware module directly into the process context. The retrieved pointer can be used for direct non-cached register access.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pciResource

This parameter specifies the desired PCI Memory resource to be used for this access. In general, a PCI target (PCIe bridge) supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

The Base Address Register usage is programmable and can be changed by modifying the PCIe bridge configuration. Therefore the following table is just an example how the PCI Base Address Registers could be used.

PCI Base Address Register	PCI Address-Type	TDRV020 Resource
0	MEM	TDRV020_RES_MEM_1
1	MEM *(not used)*	TDRV020_RES_MEM_2
2	MEM *(not used)*	TDRV020_RES_MEM_3

pPtr

This argument is a pointer to an unsigned char pointer that receives the start address of the mapped PCI resource.

pSize

This argument returns the size of the mapped PCI resource in bytes.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
unsigned char      *pReg;
unsigned int       size;

/*
** map first memory PCI resource
*/
result = tdrv020PciResourceMap(hdl, TDRV020_RES_MEM_1, &pReg, &size);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_ACCESS	Specified PCI resource not available
TDRV020_ERR_NOMEM	Unable to allocate memory

2.3.2 tdrv020PciResourceUnmap

NAME

tdrv020PciResourceUnmap – unmap a previously mapped PCI resource

SYNOPSIS

```
TDRV020_STATUS tdrv020PciResourceUnmap
(
    TDRV020_HANDLE      hdl,
    unsigned char       *pPtr
)
```

DESCRIPTION

This function unmaps a previously mapped PCI resource, freeing the system resources used for this mapping.

PARAMETERS

hdl

This argument specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

pPtr

This argument is a pointer to an unsigned char pointer that represents the start address of the previously mapped PCI resource. This pointer must have been received from the corresponding mapping function.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE      hdl;
TDRV020_STATUS      result;
unsigned char       *pReg;

…
```

…

```
/*
** unmap a previously mapped PCI resource
*/
result = tdrv020PciResourceUnmap(hdl, pReg);
if (result != TDRV020_OK)
{
     /* handle error */
}
```

RETURN VALUE

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified device handle is invalid
TDRV020_ERR_INVAL	Invalid pointer specified

2.4 Interrupt Functions

2.4.1 tdrv020InterruptConfig

NAME

tdrv020InterruptConfig – Configure the Interrupt handling method for User-FPGA implementations

SYNOPSIS

```
TDRV020_STATUS tdrv020InterruptConfig
(
    TDRV020_HANDLE      hdl,
    int                 ControlType,
    int                 ReadPciResource,
    int                 ReadAccessWidth,
    unsigned int        ReadOffset,
    unsigned int        ReadMask,
    int                 WritePciResource,
    int                 WriteAccessWidth,
    unsigned int        WriteOffset,
    unsigned int        WriteMask,
    unsigned int        WriteValue
)
```

DESCRIPTION

This function configures the interrupt handling method for User-FPGA specific implementations. Interrupt handling must be implemented on driver-level, so the driver must be configured properly to acknowledge an interrupt of the user-specific FPGA implementation.

Make sure to configure the interrupt handling before the User-FPGA implementation raises interrupts.

PARAMETERS

hdl

This value specifies the callback handle retrieved by a call to the corresponding register-function.

IntAckMethod

This value specifies the interrupt acknowledgement method. Following values are possible:

Value	Description
TDRV020_INTACK_READ	Interrupt is cleared upon reading a status register.
TDRV020_INTACK_READCLEAR	Interrupt is cleared by writing the read register bits into the same register, using the same access width as for the read access.
TDRV020_INTACK_READWRITE	Interrupt is cleared upon writing a static value to a specific register.
TDRV020_INTACK_READWRITEMASK	Interrupt is cleared upon writing a static value to a specific register using a bit-mask, leaving specified original register bits unchanged.

ReadPciResource

This parameter specifies the desired PCI Memory resource to be used for reading the interrupt status. In general, a PCI target supports up to six base address registers. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

ReadAccessWidth

This parameter specifies the desired access width for reading the interrupt status. The driver always uses little-endian accesses. Following values are possible:

Value	Description
TDRV020_ACCESSWIDTH_8	A BYTE (8bit) register access is used.
TDRV020_ACCESSWIDTH_16	A WORD (16bit) register access is used.
TDRV020_ACCESSWIDTH_32	A DWORD (32bit) register access is used.

ReadOffset

This argument specifies the register offset within the PCI BAR space used for reading the interrupt status.

ReadMask

This argument specifies the bit-mask used for interrupt detection. This argument can be used to mask-out static register bits for proper support of PCI interrupt sharing.

WritePciResource

This parameter specifies the desired PCI Memory resource to be used for writing a static value. In general, a PCI target supports up to six base address registers. This parameter is not used for IntAckMethod READ and READCLEAR. Following values are possible:

Value	Description
TDRV020_RES_MEM_1	First found PCI Memory area.
TDRV020_RES_MEM_2	Second found PCI Memory area.
TDRV020_RES_MEM_3	Third found PCI Memory area.
TDRV020_RES_MEM_4	Fourth found PCI Memory area.
TDRV020_RES_MEM_5	Fifth found PCI Memory area.
TDRV020_RES_MEM_6	Sixth found PCI Memory area.

WriteAccessWidth

This parameter specifies the desired access width for writing the static value. The driver always uses little-endian accesses. This parameter is not used for IntAckMethod READ and READCLEAR. Following values are possible:

Value	Description
TDRV020_ACCESSWIDTH_8	A BYTE (8bit) register access is used.
TDRV020_ACCESSWIDTH_16	A WORD (16bit) register access is used.
TDRV020_ACCESSWIDTH_32	A DWORD (32bit) register access is used.

WriteOffset

This argument specifies the register offset within the PCI BAR space used for writing the static value. This parameter is not used for IntAckMethod READ and READCLEAR.

WriteMask

This argument specifies the bit-mask used for write access. This argument can be used to mask-out static register bits, changing only the desired ones. Specifying 0x00000000 is not valid. This parameter is not used for IntAckMethod READ and READCLEAR.

WriteValue

This argument specifies the static value to be used for writing. This parameter is not used for IntAckMethod READ and READCLEAR.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE          hdl;
TDRV020_STATUS          result;

/*
**  Example 1:
**  Configure the Interrupt Handler to use READCLEAR method
**  - InterruptStatus Register in first PCI MemRes, at Offset 0x20
**  - Use 32bit accesses
*/
result = tdrv020InterruptConfig( hdl,
              TDRV020_INTACK_READCLEAR,
              TDRV020_RES_MEM_1,          // ReadPciResource
              TDRV020_ACCESSWIDTH_32,     // ReadAccessWidth
              0x20,                       // ReadOffset
              0xFFFFFFFF,                 // check all register-bits
              0, 0, 0, 0, 0               // do not use write-
                                          // parameters
         );
if (result == TDRV020_OK)
{
     / *OK */
} else {
     /* handle error */
}
```

…

```
/*
**  Example 2:
**  Configure the Interrupt Handler to use READWRITE method
**  - InterruptStatus Register at PCI Memory Resource 1, Offset 0x20
**  - Use 32bit accesses, check all register-bits
**  - disable the Interrupt by writing 0x00000000 to PCI Memory Resource 1,
**    Offset 0x24
*/
result = tdrv020InterruptConfig( hdl,
              TDRV020_INTACK_READWRITE,
              TDRV020_RES_MEM_1,          /* ReadPciResource      */
              TDRV020_ACCESSWIDTH_32,     /* ReadAccessWidth      */
              0x20,                       /* ReadOffset
              0xFFFFFFFF,                 /* ReadMask             */
              TDRV020_RES_MEM_1,          /* WritePciResource     */
              TDRV020_ACCESSWIDTH_32,     /* WriteAccessWidth     */
              0x24,                       /* WriteOffset          */
              0xFFFFFFFF,                 /* WriteMask            */
              0x00000000                  /* WriteValue           */
         );
if (result == TDRV020_OK)
{
     / *OK */
} else {
     /* handle error */
}
```

RETURNS

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified handle is invalid.
TDRV020_ERR_INVAL	The specified flags are invalid.
TDRV020_ERR_NOSYS	This function is not supported by the device.

2.4.2 tdrv020InterruptWait

NAME

tdrv020InterruptWait – Wait for incoming Local Interrupt Source

SYNOPSIS

```
TDRV020_STATUS tdrv020InterruptWait
(
    TDRV020_HANDLE      hdl,
    unsigned int        interruptMask,
    unsigned int        *pInterruptOccurred,
    int                 timeout
);
```

DESCRIPTION

This function waits for interrupts on the specified local interrupt sources. Multiple functions may wait for the same interrupt source to occur.

The delay between an incoming interrupt and the return of the described function is system-dependent, and is most likely several microseconds.

PARAMETERS

hdl

This value specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

interruptMask

This parameter specifies specific interrupt bits to wait for. The interrupt bits are compared to the “Interrupt Pending Register” configured by parameter ReadOffset (function tdrv020InterruptConfig). Please refer to the User-FPGA Design for further information on the possible interrupt bits. The function returns if at least one of the specified interrupt sources is detected.

pInterruptOccurred

If at least one of the specified interrupt sources occur, the value is returned through this pointer. Please refer to the User-FPGA Design for further information on the possible interrupt bits.

timeout

This value specifies the timeout in milliseconds the function will wait for the interrupt to arrive. The granularity depends on the operating system. To wait indefinitely, specify -1 as timeout parameter.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
unsigned int       interruptMask;
unsigned int       interruptOccurred;

/*
** Wait at least 5 seconds for incoming interrupts on lower 3 bits
*/
interruptMask = (0x07 << 0);
result = tdrv020InterruptWait(   hdl,
                                 interruptMask,
                                 &interruptOccurred,
                                 5000 );
if (result == TDRV020_OK)
{
     /* Interrupt arrived.                                  */
     /* Now acknowledge interrupt source in FPGA logic   */
     /* to clear the Interrupt Sources.                  */
     /* Use tdrv020Read and tdrv020Write functions for   */
     /* register access.                                    */
} else {
     /* handle error */
}
```

RETURNS

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified TDRV020_HANDLE is invalid.
TDRV020_ERR_NORESOURCE	Failed to allocate resources for the wait job
TDRV020_ERR_TIMEOUT	The specified timeout occurred.

2.4.3 tdrv020InterruptRegisterCallbackThread

NAME

tdrv020InterruptRegisterCallbackThread – Register a User Callback Function for Interrupt Handling

SYNOPSIS

```
TDRV020_STATUS tdrv020InterruptRegisterCallbackThread
(
    TDRV020_HANDLE      hdl,
    int                 threadPriority,
    int                 stackSize,
    unsigned int        interruptMask,
    FUNCINTCALLBACK     callbackFunction,
    void                *funcparam,
    TDRV020_HANDLE      *pCallbackHandle
)
```

DESCRIPTION

This function registers a user callback function which is executed after detection of the specified interrupt source. It is possible to register multiple callback functions to one or a set (bit mask) of interrupt sources.

The callback function is executed in a thread context, so using TDRV020 device driver functions and system functions is allowed. The callback function should be kept as short as possible. The specified callback function is executed with the occurred interrupt bits and the specified function parameter as function arguments. Additionally, a status value is passed to the callback function, which reflects the result of the involved API functions.

The delay between an incoming interrupt and the execution of the callback function is system-dependent, and is most likely several microseconds.

PARAMETERS

hdl

This value specifies the device handle to the hardware module retrieved by a call to the corresponding open-function.

threadPriority

This parameter specifies the priority to be used for the callback thread. Possible values are:

Value	Description
TDRV020_PRIORITY_NORMAL	Highest driver support task priority (51)
TDRV020_PRIORITY_HIGH	Highest possible priority (0)
TDRV020_PRIORITY_LOW	Highest application task priority (100)

Other values (0..255) might be possible (see also VxWorks Kernel Programmer's Guide).

stackSize

This parameter specifies the stack size to be used for the callback tread. The value is specified in bytes.

interruptMask

This parameter specifies specific interrupt bits to wait for. The interrupt bits are compared to the "Interrupt Pending Register" configured by parameter ReadOffset (function tdrv020InterruptConfig). Please refer to the User-FPGA Design for further information on the possible interrupt bits. The callback function is executed if at least one of the specified interrupt sources occurred.

callbackFunction

This parameter is a function pointer to the user callback function. The callback function pointer is defined as follows:

```
typedef void(*FUNCINTCALLBACK)( TDRV020_HANDLE   hdl,
                                unsigned int     interruptOccurred,
                                void             *param,
                                TDRV020_STATUS   status );
```

hdl

This parameter specifies a device handle which can be used for hardware access or other API functions by the callback function.

interruptOccurred

This parameter is a 32bit value reflecting the occurred interrupts. It is useful if the callback function handles multiple interrupt sources. Please refer to the User-FPGA Design for further information on the possible interrupt bits.

param

This parameter is the user-specified *funcparam* value (see below) which has been specified on callback registration. This value can be used to pass a pointer to a specific control structure, to supply the callback function with specific information.

status

This parameter hands over interrupt callback status information. The callback function needs to check this parameter. If the specified interrupt source has occurred properly, and no errors were detected, this parameter is TDRV020_OK. If this parameter differs from TDRV020_OK, an internal error has been detected and the callback handling is stopped. The callback function must implement an appropriate error handling.

funcparam

This value specifies a user parameter, which will be handed over to the callback function on execution. This parameter can be used to pass a pointer to a specific control structure used by the callback function.

pCallbackHandle

This value specifies a pointer to a handle, where the callback handle will be returned. This callback handle must be used to unregister a callback function.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE     hdl;
TDRV020_STATUS     result;
unsigned int       interruptMask;
USER_DATA_AREA     userDataArea;
TDRV020_HANDLE     callbackHandle;

/* forward declaration of callback functions */
void callback_TIMER(    TDRV020_HANDLE     hdl,
                        unsigned int       interruptOccurred,
                        void               *param,
                        TDRV020_STATUS     status);
/*
**  Register callback function for TIMER Interrupt
**  Use a “normal” priority, and 64KB stack.
*/
interruptMask = (1 << 1);
result = tdrv020InterruptRegisterCallbackThread(hdl,
                                                TDRV020_PRIORITY_NORMAL,
                                                0x10000,
                                                interruptMask,
                                                callback_TIMER,
                                                &userDataArea,
                                                &callbackHandle);
...
...
if (result != TDRV020_OK)
{
     /* handle error */
}

…
```

```
…

/*
** Initialize and start the Timer function, using register accesses.
*/

…

/*
** Callback Function, using API Functions for Register Access
*/
void callback_TIMER(    TDRV020_HANDLE     hdl,
                        unsigned int       interruptOccurred,
                        void               *param,
                        TDRV020_STATUS     status)
{
     TDRV020_STATUS     result;
     USER_DATA_AREA     *pUsrData = (USER_DATA_AREA*)param;
     unsigned int       u32values[4];

     if (status != TDRV020_OK)
     {
          /* handle error status */
     }

     printf("[Timer Interrupt]\n");

     /*
     ** Now do something, e.g. read 4x 32bit values from the FPGA design.
     */
     result = tdrv020ReadLE32(    hdl,
                                  TDRV020_RES_MEM_1,
                                  0x00,
                                  4,
                                  u32values );
     /* handle errors */
     return;
}
```

RETURNS

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified TDRV020_HANDLE is invalid.
TDRV020_ERR_INVAL	Function or callback handle pointer is NULL.
TDRV020_ERR_NODEV	Failed to allocate a callback handle
TDRV020_ERR_TASK_CREATE	Creation of the callback thread (task) failed.

2.4.4 tdrv020InterruptUnregisterCallback

NAME

tdrv020InterruptUnregisterCallback – Unregister a User Callback Function

SYNOPSIS

```
TDRV020_STATUS tdrv020InterruptUnregisterCallback
(
    TDRV020_HANDLE      hdl
)
```

DESCRIPTION

This function unregisters a previously registered user callback thread or ISR function.

PARAMETERS

hdl

This value specifies the callback handle retrieved by a call to the corresponding register-function.

EXAMPLE

```
#include “tdrv020api.h”

TDRV020_HANDLE     callbackHdl;
TDRV020_STATUS     result;

/*
** Unregister a callback function
*/
result = tdrv020InterruptUnregisterCallback(callbackHdl);
if (result == TDRV020_OK)
{
    / *OK */
} else {
    /* handle error */
}
```

RETURNS

On success, TDRV020_OK is returned. In the case of an error, the appropriate error code is returned by the function.

ERROR CODES

Error Code	Description
TDRV020_ERR_INVALID_HANDLE	The specified callback handle is invalid.

2.5 Endian Conversion Functions

The following conversion functions can be used to develop endian-neutral software, especially for direct access to mapped PCI resources.

2.5.1 endian_be16

NAME

endian_be16 – big-endian conversion function

SYNOPSIS

unsigned short endian_be16
(
    unsigned short u16value
)

DESCRIPTION

This function converts a short integer value (16-bit) from the native CPU endian order to big-endian order. That means on Intel x86 architectures the value will be byte-swapped, as opposed to PowerPC architectures.

PARAMETERS

u16value

This argument specifies the data to convert

EXAMPLE

```
#include “tdrv020api.h”

unsigned short *pRawData, bigEndianData;

/* setup pRawData pointer to the correct location first */

bigEndianData = endian_be16(*pRawData);
```

RETURN VALUE

This function returns the passed value in the big-endian order.

2.5.2 endian_le16

NAME

endian_le16 – little-endian conversion function

SYNOPSIS

unsigned short endian_le16
(
    unsigned short u16value
)

DESCRIPTION

This function converts a short integer value (16-bit) from the native CPU endian order to little-endian order. That means on PowerPC architectures the value will be byte-swapped, as opposed to Intel x86 architectures.

PARAMETERS

u16value

This argument specifies the data to convert

EXAMPLE

```
#include “tdrv020api.h”

unsigned short *pRawData, littleEndianData;

/* setup pRawData pointer to the correct location first */

littleEndianData = endian_le16(*pRawData);
```

RETURN VALUE

This function returns the passed value in the little-endian order.

2.5.3 endian_be32

NAME

endian_be32 – big-endian conversion function

SYNOPSIS

unsigned int endian_be32
(
    unsigned short   u32value
)

DESCRIPTION

This function converts an integer value (32-bit) from the native CPU endian order to big-endian order. That means on Intel x86 architectures the value will be byte-swapped, as opposed to PowerPC architectures.

PARAMETERS

u32value

This argument specifies the data to convert

EXAMPLE

```
#include “tdrv020api.h”

unsigned short *pRawData, bigEndianData;

/* setup pRawData pointer to the correct location first */

bigEndianData = endian_be32(*pRawData);
```

RETURN VALUE

This function returns the passed value in the big-endian order.

2.5.4 endian_le32

NAME

endian_le32 – little-endian conversion function

SYNOPSIS

unsigned short endian_le32
(
    unsigned short u32value
)

DESCRIPTION

This function converts an integer value (32-bit) from the native CPU endian order to little-endian order. That means on PowerPC architectures the value will be byte-swapped, as opposed to Intel x86 architectures.

PARAMETERS

u32value

This argument specifies the data to convert

EXAMPLE

```
#include “tdrv020api.h”

unsigned short *pRawData, littleEndianData;

/* setup pRawData pointer to the correct location first */

littleEndianData = endian_le32(*pRawData);
```

RETURN VALUE

This function returns the passed value in the little-endian order.

3 Legacy I/O System Functions

This chapter describes functions which are relevant only for the legacy TDRV020 driver.

3.1 tdrv020PciInit

NAME

tdrv020PciInit() – Generic PCI device initialization

SYNOPSIS

void tdrv020PciInit()

DESCRIPTION

This function is required only for Intel x86 VxWorks platforms. The purpose is to setup the MMU mapping for all required TDRV020 PCI spaces (base address register) and to enable the TDRV020 device for access.

The global variable *tdrv020Status* obtains the result of the device initialization and can be polled later by the application before the driver will be installed.

Value	Meaning
> 0	Initialization successful completed. The value of tdrv020Status is equal to the number of mapped PCI spaces
0	No TDRV020 device found
< 0	Initialization failed. The value of (tdrv020Status & 0xFF) is equal to the number of mapped spaces until the error occurs. Possible cause: Too few entries for dynamic mappings in sysPhysMemDesc[]. Remedy: Add dummy entries as necessary (syslib.c).

EXAMPLE

```
extern void tdrv020PciInit();

tdrv020PciInit();
```

4 Debugging and Diagnostic

The TDRV020 device driver provides functions and debug statements to display versatile information of the driver installation and status on the debugging console.

By default the TDRV020 show routine is included in the driver and can be called from the VxWorks shell. If this function is not needed or program space is rare the function can be removed from the code by un-defining the macro INCLUDE_TDRV020_SHOW in tdrv020drv.c

The tdrv020Show function displays detailed information about probed modules, assignment of devices respective device names to probed TRDV020 modules and device statistics.

If TDRV020 modules were probed but no devices were created it may helpful to enable debugging code inside the driver code by defining the macro TDRV020_DEBUG in tdrv020drv.c. Certain debug information can be selected by assigning one or more (logical OR) TDRV_DBD_xxx values to variable tdrv020Debug.

In contrast to VxBus TDRV020 devices, legacy TDRV020 devices must be created "manually". This will be done with the first call to the tdrv020Open API function.

```
-> tdrv020Show
Probed Modules:
    [0] TDRV020: Bus=3, Dev=0, DevId=0xa26f, VenId=0x1498, Init=OK, vxDev=0xffff800000004050

Associated Devices:
    [0] TDRV020: /tdrv020/0

Device Statistics:
    /tdrv020/0:
        open count           = 0
        job count            = 0
        interrupt count      = 0

        Available PCI Resources:
        [0] : address = 0xffff8000200bf000  size=0x1000
value = 0 = 0x0
```