

The Embedded I/O Company



TFMC684

32 Differential Channel FMC Mezzanine Module

Version 1.0

User Manual

Issue 1.0.2

April 2017

TEWS TECHNOLOGIES GmbH

Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

TFMC684-10R

FMC Mezzanine Module for 32bit M-LVDS I/O, VHDCI-68 Front Panel Connector, extended temperature range

(RoHS compliant)

TFMC684-20R

FMC Mezzanine Module for 32bit RS-485/RS-422 I/O, VHDCI-68 Front Panel Connector, extended temperature range

(RoHS compliant)

This document contains information, which is proprietary to TEWS TECHNOLOGIES GmbH. Any reproduction without written permission is forbidden.

TEWS TECHNOLOGIES GmbH has made any effort to ensure that this manual is accurate and complete. However TEWS TECHNOLOGIES GmbH reserves the right to change the product described in this document at any time without notice.

TEWS TECHNOLOGIES GmbH is not liable for any damage arising out of the application or use of the device described herein.

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an 'Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

©2012-2017 by TEWS TECHNOLOGIES GmbH

All trademarks mentioned are property of their respective owners.

Issue	Description	Date
1.0.0	Initial issue	October 2012
1.0.1	RS-485/RS-422 Variant (-20R) added	November 2016
1.0.2	Front I/O Connector view corrected	April 2017

Table of Contents

1	PRODUCT DESCRIPTION	6
2	TECHNICAL SPECIFICATION	7
2.1	IPMI Serial EEPROM	8
3	HANDLING AND OPERATING INSTRUCTIONS	9
3.1	ESD Protection	9
4	DATA DIRECTION CONFIGURATION.....	9
5	JTAG CHAIN.....	9
6	PIN ASSIGNMENT – I/O CONNECTOR	10
6.1	Front I/O Connector	10
6.1.1	Pin Assignment.....	11
6.2	FMC Connector	12
6.2.1	Pin Assignment.....	13
6.2.1.1	User Defined Signals on Bank A	14

List of Figures

FIGURE 1-1 : BLOCK DIAGRAM.....	6
FIGURE 6-1 : FRONT I/O CONNECTOR VIEW.....	10
FIGURE 6-2 : FMC CONNECTOR TOP VIEW.....	12

List of Tables

TABLE 2-1 : TECHNICAL SPECIFICATION.....	7
TABLE 4-1 : DATA DIRECTION CONFIGURATION.....	9
TABLE 6-1 : FRONT I/O CONNECTOR TYPE.....	10
TABLE 6-2 : PIN ASSIGNMENT FRONT I/O CONNECTOR.....	11
TABLE 6-3 : FMC CONNECTOR TYPE.....	12
TABLE 6-4 : PIN ASSIGNMENT FMC CONNECTOR.....	13
TABLE 6-5 : USER DEFINED SIGNALS ON BANK A.....	15

1 Product Description

The TFM684 is an FMC (FPGA Mezzanine Card) Mezzanine Module complying with the ANSI/VITA 57.1 standard that offers the possibility to add a 32bit M-LVDS (Multipoint Low Voltage Differential Signaling) I/O Interface or a 32bit RS-485/RS-422 I/O Interface to FMC Carrier Cards.

The Low Pin Count FMC Connector provides 32 independent control signals which configure the direction of each Differential Transceiver.

The 32 data lines are routed as single-ended traces from the FMC Connector to the Differential Transceivers where they are converted into 32 differential pairs.

The TFM684-10R meets the TIA/EIA-899 standard (Type-2 Receivers) and the TFM684-20R meets the TIA/EIA-485 and the TIA/EIA-422 standard.

The 32 bits of differential I/O are connected to a VHDCI-68 Connector in the front panel.

On every of the 32 bits the TFM684-10R supports signaling rates up to 200Mbit/s which means that a 100MHz clock can be transmitted or in other words that 200M of voltage transitions per second can be performed. The TFM684-20R supports signaling rates up to 16Mbit/s.

All signals connecting the Differential Driver/Receivers with the FMC Carrier are powered by an adjustable voltage generated by the Carrier. Because of voltage translation devices on the TFM684 this voltage can range from 1.2V to 3.6V which allows the FPGA's I/O cells to be configured for various different I/O standards.

The signaling standard reference voltage pin, which is powered by the TFM684, provides half of the adjustable voltage generated by the carrier for I/O standards requiring a reference voltage.

A power good LED indicates whether all voltages on the TFM684, which are provided by the FMC Carrier, are within limits.

The TFM684 is equipped with an I²C EEPROM which acts as an IPMI resource requesting the value of the adjustable voltage, for example.

The module meets the requirements to operate in extended temperature range from -40° to +85°C.

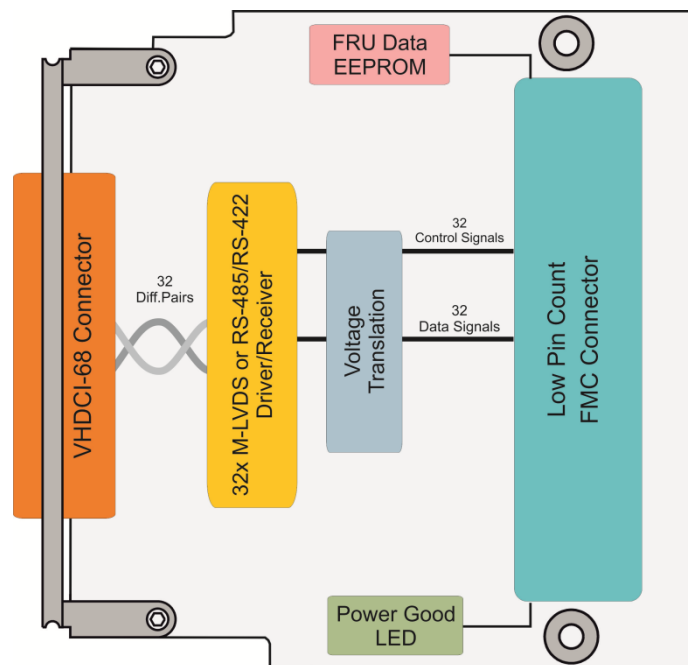


Figure 1-1 : Block Diagram

2 Technical Specification

FMC Interface		
Mechanical Interface	FPGA Mezzanine Card (FMC) Mezzanine Module conforming to ANSI/VITA 57.1 Single Width, 10mm stacking height Air cooled Commercial Grade with Front Panel Regions 1 and 2 populated	
Electrical Interface	Low-Pin Count Connector 64 User defined signals on Bank A 1.2V to 3.6V Signaling Voltage (VADJ) Nominal Voltage: 1.8V (Preferred VADJ Signaling Voltage)	
On Board Devices		
M-LVDS Driver and Receiver	SN65MLVD206 (Texas Instruments) or compatible	
RS-485/RS-422 Transceiver	MAX3078E (Maxim Integrated) or compatible	
EEPROM	M24C02 (STMicroelectronics) or compatible	
I/O Interface		
Number of Channels	32 differential channels	
Maximum Speed	200Mbit/s on each channel (M-LVDS) 16Mbit/s on each channel (RS-485/RS-422)	
I/O Connector	Front I/O VHDCI68 / SCSI-V (Honda HDRA-EC68LFDT-SL+ or compatible)	
Physical Data		
Power Specification in FRU multi-record data	max. 300mA @ VADJ	DC Load
	max. 800mA @ +3.3V (-10R) max. 2000mA @ +3.3V (-20R)	
	max. 1mA @ VREF_A_M2C	DC Output
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	TFMC684-10R: 873000 h TFMC684-20R: 684000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G _B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	43 g	

Table 2-1 : Technical Specification

2.1 IPMI Serial EEPROM

The on-board M24C02 EEPROM contains hardware definition information that may be read by an external controller using IPMI commands and I²C serial bus transactions. The mezzanine module description data on the TFMC684 includes the minimum records defined in the Platform Management FRU Information Storage Definition V1.0.

See the FMC Standard ANSI/VITA 57.1 and Platform Management FRU Information Storage Definition V1.0 for more information.

3 Handling and Operating Instructions

3.1 ESD Protection



The FMC module is sensitive to static electricity. Packing, unpacking and all other module handling has to be done in an ESD/EOS protected Area.

4 Data Direction Configuration

The data direction of every channel on the TFMC684 can be configured independently by driving the OUT/IN# pins on the FMC Connector accordingly.

If the FMC Carrier drives this signal 'high' the corresponding M-LVDS or RS-485/RS-422 device transmits data and if the signal is driven 'low' it receives data.

At power-up or when the FMC Carrier's FPGA is unconfigured all devices are configured to receive data.

Voltage Level on OUT/IN# pin	Transceiver Configuration
Low	Receiver
High	Driver

Table 4-1 : Data Direction Configuration

5 JTAG Chain

The TFMC684 does not use Boundary Scan.

TDO and TDI are connected on the TFMC684 to ensure continuity of the FMC Carrier's JTAG Chain. TMS, TCK and TRST# are left unconnected.

6 Pin Assignment – I/O Connector

6.1 Front I/O Connector

Pin-Count	68
Connector Type	68-pin Very High Density Cable Interconnect (VHDCI) SCSI-V, female
Source & Order Info	Honda HDRA-EC68LFDT-SL+ or compatible

Table 6-1 : Front I/O Connector Type

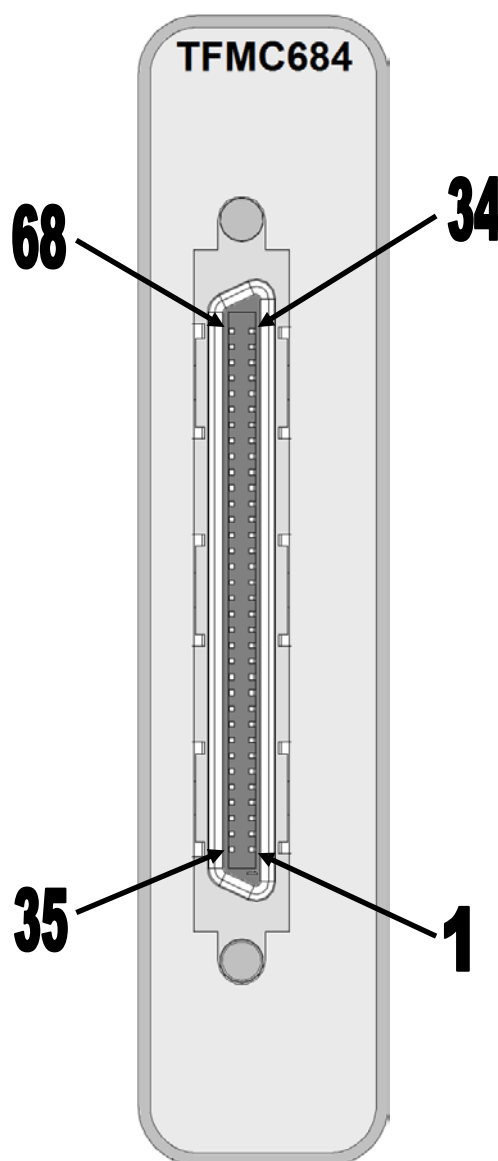


Figure 6-1 : Front I/O Connector view

6.1.1 Pin Assignment

Pin	Signal	Pin	Signal
68	I/O_31-	34	I/O_31+
67	I/O_30-	33	I/O_30+
66	I/O_29-	32	I/O_29+
65	I/O_28-	31	I/O_28+
64	I/O_27-	30	I/O_27+
63	I/O_26-	29	I/O_26+
62	I/O_25-	28	I/O_25+
61	I/O_24-	27	I/O_24+
60	GND	26	GND
59	I/O_23-	25	I/O_23+
58	I/O_22-	24	I/O_22+
57	I/O_21-	23	I/O_21+
56	I/O_20-	22	I/O_20+
55	I/O_19-	21	I/O_19+
54	I/O_18-	20	I/O_18+
53	I/O_17-	19	I/O_17+
52	I/O_16-	18	I/O_16+
51	I/O_15-	17	I/O_15+
50	I/O_14-	16	I/O_14+
49	I/O_13-	15	I/O_13+
48	I/O_12-	14	I/O_12+
47	I/O_11-	13	I/O_11+
46	I/O_10-	12	I/O_10+
45	I/O_9-	11	I/O_9+
44	I/O_8-	10	I/O_8+
43	GND	9	GND
42	I/O_7-	8	I/O_7+
41	I/O_6-	7	I/O_6+
40	I/O_5-	6	I/O_5+
39	I/O_4-	5	I/O_4+
38	I/O_3-	4	I/O_3+
37	I/O_2-	3	I/O_2+
36	I/O_1-	2	I/O_1+
35	I/O_0-	1	I/O_0+

Table 6-2 : Pin Assignment Front I/O Connector

6.2 FMC Connector

Pin-Count	160 (Low Pin Count)
Connector Type	40 x 10 array (Samtec SEARAY Series), SEAM-40-03.5-10-A, terminal / male
Source & Order Info	Samtec ASP-134604-01 (Leadfree) or compatible

Table 6-3 : FMC Connector Type

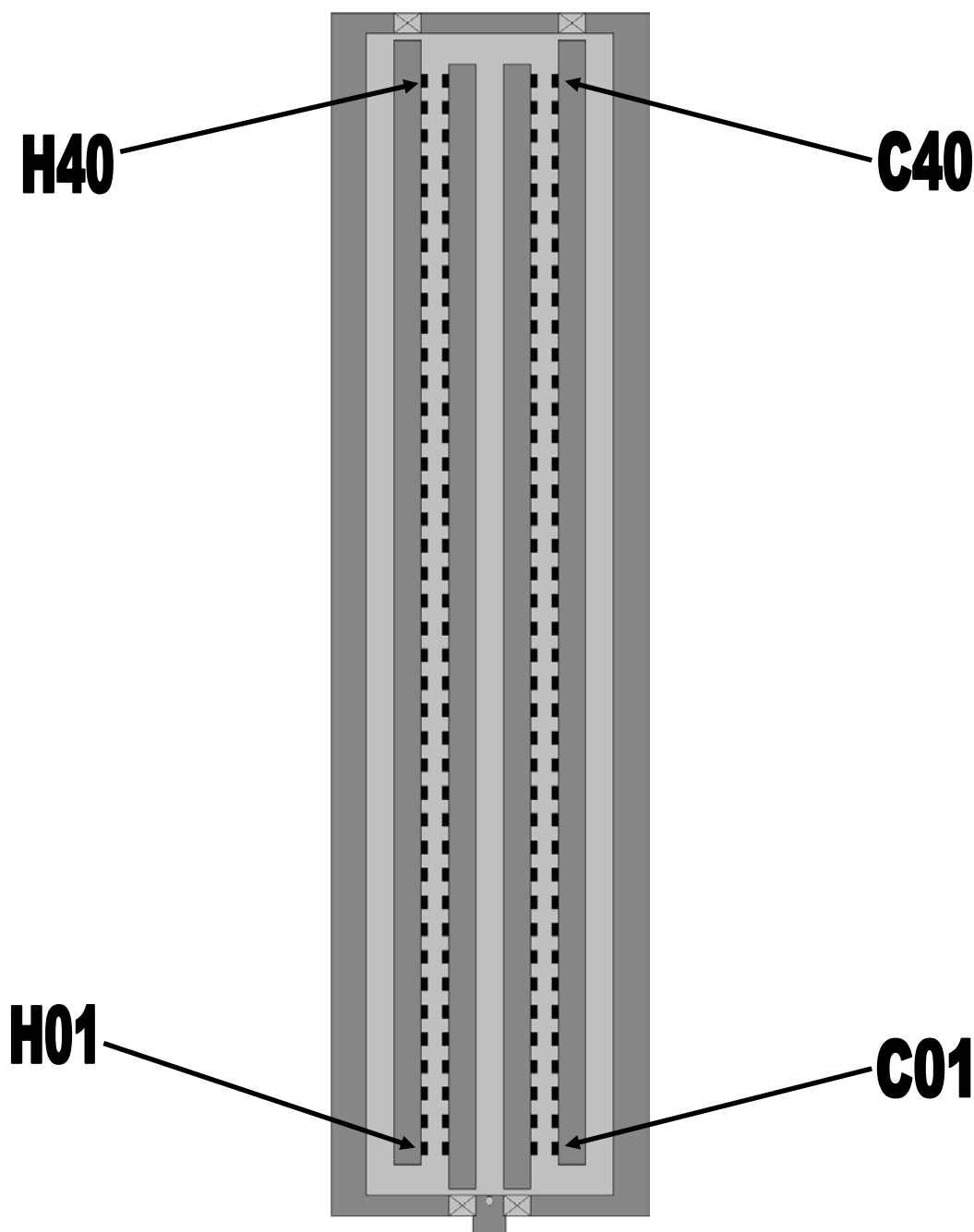


Figure 6-2 : FMC Connector top view

6.2.1 Pin Assignment

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A M2C (VADJ/2)	GND (GND)	NC	NC	PG_C2M (PG_C2M)	GND (GND)	NC	NC
2	NC	NC	PRSNT M2C_L (GND)	CLK1 M2C_P (NC)	NC	NC	GND (GND)	DP0_C2M_P (NC)	NC	NC
3	NC	NC	GND (GND)	CLK1 M2C_N (NC)	NC	NC	GND (GND)	DP0_C2M_N (NC)	NC	NC
4	NC	NC	CLK0 M2C_P (NC)	GND (GND)	NC	NC	GBTCLK0 M2C_P (NC)	GND (GND)	NC	NC
5	NC	NC	CLK0 M2C_N (NC)	GND (GND)	NC	NC	GBTCLK0 M2C_N (NC)	GND (GND)	NC	NC
6	NC	NC	GND (GND)	LA00_P_CC (DATA_0)	NC	NC	GND (GND)	DP0_M2C_P (NC)	NC	NC
7	NC	NC	LA02_P (DATA_2)	LA00_N_CC (OUT/IN#_0)	NC	NC	GND (GND)	DP0_M2C_N (NC)	NC	NC
8	NC	NC	LA02_N (OUT/IN#_2)	GND (GND)	NC	NC	LA01_P_CC (DATA_1)	GND (GND)	NC	NC
9	NC	NC	GND (GND)	LA03_P (DATA_3)	NC	NC	LA01_N_CC (OUT/IN#_1)	GND (GND)	NC	NC
10	NC	NC	LA04_P (DATA_4)	LA03_N (OUT/IN#_3)	NC	NC	GND (GND)	LA06_P (DATA_6)	NC	NC
11	NC	NC	LA04_N (OUT/IN#_4)	GND (GND)	NC	NC	LA05_P (DATA_5)	LA06_N (OUT/IN#_6)	NC	NC
12	NC	NC	GND (GND)	LA08_P (DATA_8)	NC	NC	LA05_N (OUT/IN#_5)	GND (GND)	NC	NC
13	NC	NC	LA07_P (DATA_7)	LA08_N (OUT/IN#_8)	NC	NC	GND (GND)	GND (GND)	NC	NC
14	NC	NC	LA07_N (OUT/IN#_7)	GND (GND)	NC	NC	LA09_P (DATA_9)	LA10_P (DATA_10)	NC	NC
15	NC	NC	GND (GND)	LA12_P (DATA_12)	NC	NC	LA09_N (OUT/IN#_9)	LA10_N (OUT/IN#_10)	NC	NC
16	NC	NC	LA11_P (DATA_11)	LA12_N (OUT/IN#_12)	NC	NC	GND (GND)	GND (GND)	NC	NC
17	NC	NC	LA11_N (OUT/IN#_11)	GND (GND)	NC	NC	LA13_P (DATA_13)	GND (GND)	NC	NC
18	NC	NC	GND (GND)	LA16_P (DATA_16)	NC	NC	LA13_N (OUT/IN#_13)	LA14_P (DATA_14)	NC	NC
19	NC	NC	LA15_P (DATA_15)	LA16_N (OUT/IN#_16)	NC	NC	GND (GND)	LA14_N (OUT/IN#_14)	NC	NC
20	NC	NC	LA15_N (OUT/IN#_15)	GND (GND)	NC	NC	LA17_P_CC (DATA_17)	GND (GND)	NC	NC
21	NC	NC	GND (GND)	LA20_P (DATA_20)	NC	NC	LA17_N_CC (OUT/IN#_17)	GND (GND)	NC	NC
22	NC	NC	LA19_P (DATA_19)	LA20_N (OUT/IN#_20)	NC	NC	GND (GND)	LA18_P_CC (DATA_18)	NC	NC
23	NC	NC	LA19_N (OUT/IN#_19)	GND (GND)	NC	NC	LA23_P (DATA_23)	LA18_N_CC (OUT/IN#_18)	NC	NC
24	NC	NC	GND (GND)	LA22_P (DATA_22)	NC	NC	LA23_N (OUT/IN#_23)	GND (GND)	NC	NC
25	NC	NC	LA21_P (DATA_21)	LA22_N (OUT/IN#_22)	NC	NC	GND (GND)	GND (GND)	NC	NC
26	NC	NC	LA21_N (OUT/IN#_21)	GND (GND)	NC	NC	LA26_P (DATA_26)	LA27_P (DATA_27)	NC	NC
27	NC	NC	GND (GND)	LA25_P (DATA_25)	NC	NC	LA26_N (OUT/IN#_26)	LA27_N (OUT/IN#_27)	NC	NC
28	NC	NC	LA24_P (DATA_24)	LA25_N (OUT/IN#_25)	NC	NC	GND (GND)	GND (GND)	NC	NC
29	NC	NC	LA24_N (OUT/IN#_24)	GND (GND)	NC	NC	TCK (NC)	GND (GND)	NC	NC
30	NC	NC	GND (GND)	LA29_P (DATA_29)	NC	NC	TDI (TDI)	SCL (SCL)	NC	NC
31	NC	NC	LA28_P (DATA_28)	LA29_N (OUT/IN#_29)	NC	NC	TDO (TDI)	SDA (SDA)	NC	NC
32	NC	NC	LA28_N (OUT/IN#_28)	GND (GND)	NC	NC	3P3VAUX (+3.3Vaux)	GND (GND)	NC	NC
33	NC	NC	GND (GND)	LA31_P (DATA_31)	NC	NC	TMS (NC)	GND (GND)	NC	NC
34	NC	NC	LA30_P (DATA_30)	LA31_N (OUT/IN#_31)	NC	NC	TRST_L (NC)	GA0 (GA0)	NC	NC
35	NC	NC	LA30_N (OUT/IN#_30)	GND (GND)	NC	NC	GA1 (GA1)	12P0V (NC)	NC	NC
36	NC	NC	GND (GND)	LA33_P (NC)	NC	NC	3P3V (+3.3V)	GND (GND)	NC	NC
37	NC	NC	LA32_P (NC)	LA33_N (NC)	NC	NC	GND (GND)	12P0V (NC)	NC	NC
38	NC	NC	LA32_N (NC)	GND (GND)	NC	NC	3P3V (+3.3V)	GND (GND)	NC	NC
39	NC	NC	GND (GND)	VADJ (VADJ)	NC	NC	GND (GND)	3P3V (+3.3V)	NC	NC
40	NC	NC	VADJ (VADJ)	GND (GND)	NC	NC	3P3V (+3.3V)	GND (GND)	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Table 6-4 : Pin Assignment FMC Connector

6.2.1.1 User Defined Signals on Bank A

User Defined Signal	Name	FMC Connector Pin
LA00_P_CC	DATA_0	G06
LA00_N_CC	OUT/IN#_0	G07
LA01_P_CC	DATA_1	D08
LA01_N_CC	OUT/IN#_1	D09
LA02_P	DATA_2	H07
LA02_N	OUT/IN#_2	H08
LA03_P	DATA_3	G09
LA03_N	OUT/IN#_3	G10
LA04_P	DATA_4	H10
LA04_N	OUT/IN#_4	H11
LA05_P	DATA_5	D11
LA05_N	OUT/IN#_5	D12
LA06_P	DATA_6	C10
LA06_N	OUT/IN#_6	C11
LA07_P	DATA_7	H13
LA07_N	OUT/IN#_7	H14
LA08_P	DATA_8	G12
LA08_N	OUT/IN#_8	G13
LA09_P	DATA_9	D14
LA09_N	OUT/IN#_9	D15
LA10_P	DATA_10	C14
LA10_N	OUT/IN#_10	C15
LA11_P	DATA_11	H16
LA11_N	OUT/IN#_11	H17
LA12_P	DATA_12	G15
LA12_N	OUT/IN#_12	G16
LA13_P	DATA_13	D17
LA13_N	OUT/IN#_13	D18
LA14_P	DATA_14	C18
LA14_N	OUT/IN#_14	C19
LA15_P	DATA_15	H19
LA15_N	OUT/IN#_15	H20
LA16_P	DATA_16	G18
LA16_N	OUT/IN#_16	G19
LA17_P_CC	DATA_17	D20
LA17_N_CC	OUT/IN#_17	D21
LA18_P_CC	DATA_18	C22
LA18_N_CC	OUT/IN#_18	C23
LA19_P	DATA_19	H22
LA19_N	OUT/IN#_19	H23
LA20_P	DATA_20	G21
LA20_N	OUT/IN#_20	G22
LA21_P	DATA_21	H25
LA21_N	OUT/IN#_21	H26
LA22_P	DATA_22	G24
LA22_N	OUT/IN#_22	G25
LA23_P	DATA_23	D23
LA23_N	OUT/IN#_23	D24
LA24_P	DATA_24	H28
LA24_N	OUT/IN#_24	H29

LA25 P	DATA 25	G27
LA25 N	OUT/IN# 25	G28
LA26 P	DATA 26	D26
LA26 N	OUT/IN# 26	D27
LA27 P	DATA 27	C26
LA27 N	OUT/IN# 27	C27
LA28 P	DATA 28	H31
LA28 N	OUT/IN# 28	H32
LA29 P	DATA 29	G30
LA29 N	OUT/IN# 29	G31
LA30 P	DATA 30	H34
LA30 N	OUT/IN# 30	H35
LA31 P	DATA 31	G33
LA31 N	OUT/IN# 31	G34
LA32 P	not connected	H37
LA32 N	not connected	H38
LA33 P	not connected	G36
LA33 N	not connected	G37

Table 6-5 : User Defined Signals on Bank A