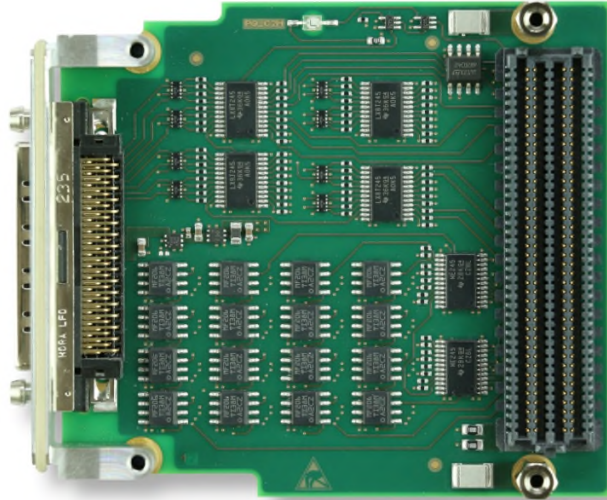## TFMC685 16 Differential I/O and 32 Digital I/O FPGA Mezzanine Card

TFMC685-10R

Application Information

The TFMC685 is an FMC (FPGA Mezzanine Card) Mezzanine Module complying with the ANSI/VITA 57.1 standard that offers the possibility to add a 16bit M-LVDS (Multipoint Low Voltage Differential Signaling) I/O Interface or a 16bit RS-485/RS-422 I/O Interface to FMC Carrier Cards. In addition to one of these two Differential I/O standards, the TFMC685 provides four 8bit wide 5V input tolerant 3.3V Digital I/O Interfaces and a 5V Supply pin (100mA) protected by a fuse.

The Low Pin Count FMC Connector provides 16 independent control signals which configure the direction of each Differential Transceiver and four independent control signals which configure the direction of each 8bit wide Digital I/O Gate.

The 16 data lines for M-LVDS or RS-485/RS-422 are routed as single-ended traces from the FMC Connector to the Differential Transceivers where they are converted into 16 differential pairs. The 32 data lines for Digital I/O are level shifted to be 5V tolerant at the front panel connector.

The TFMC685-10R meets the TIA/EIA-899 standard (Type-2 Receivers) and the TFMC685-20R meets the TIA/EIA-485 and the TIA/EIA-422 standard.

The 16 bits of Differential I/O, the 32 bits of Digital I/O and the 5V Supply are connected to a female VHDCI-68 Connector in the front panel.

All of the 16 M-LVDS Transceivers on the TFMC685-10R support signaling rates up to 200Mbit/s which means that a 100MHz clock can be transmitted or in other words that 200M of voltage transitions per second can be performed. The TFMC685-10R has an on-board 100Ω termination on all 16 M-LVDS Interfaces.

All RS-485/RS-422 Transceivers on the TFMC685-20R support signaling rates up to 50Mbit/s. The TFMC685-20R has an on-board 120Ω termination on all 16 RS-485/RS-422 Interfaces.

All signals connecting the Transceivers with the FMC Carrier are powered by an adjustable voltage generated by the Carrier. Because of voltage translation devices on the TFMC685 this voltage can range from 1.2V to 3.6V which allows the Carrier's FPGA I/O cells to be configured for various different I/O standards.

The signaling standard reference voltage at pin H1 of the FMC Connector, which is powered by the TFMC685, provides half of the adjustable voltage generated by the carrier for I/O standards requiring a reference voltage.

A power good LED indicates whether the FMC Carrier has signaled that all voltages it provides to the TFMC685 are within limits.

The TFMC685 is equipped with an I2C EEPROM which acts as an IPMI resource requesting the value of the adjustable voltage, for example.

The module meets the requirements to operate in extended temperature range from -40° to +85°C.

Technical Information

- Form Factor: Single Width, 10mm stacking height FMC Mezzanine module conforming to ANSI/VITA 57.1-2019
  - Board size: 76.5 mm x 69 mm
  - Air cooled Commercial Grade with Front Panel
  - Regions 1 and 2 populated
- Low-Pin Count (LPC) FMC Connector
  - 68 User defined signals on Bank A
  - 1.2V to 3.6V Signaling Voltage (VADJ)
  - Nominal Voltage: 1.8V (Preferred VADJ Signaling Voltage)
- IPMI resource: FRU hardware definition information stored in on-board EEPROM

- 16x M-LVDS or RS-485/RS-422 Transceiver
  - 100Ω termination for M-LVDS
  - 120Ω termination for RS-485/RS-422
- 4x 8bit Digital I/O
  - 5V input tolerant
- 5V Supply pin
  - 100mA fuse protected
- Female VHDCI-68 Front Connector
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 G_B 20°C)
  TFMC685-10R: 755000 h
  TFMC685-20R: 787000 h
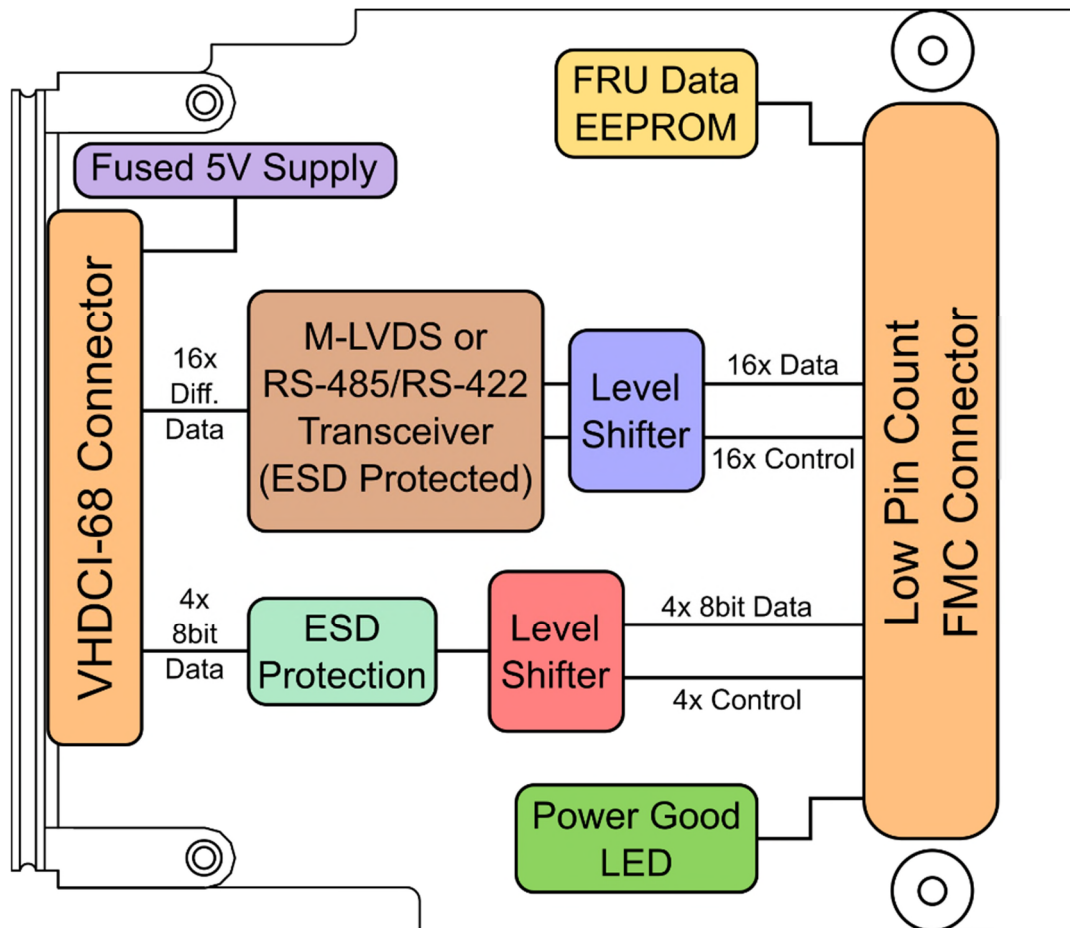
Order Information

RoHS Compliant

TFMC685-10R   FMC for 16 M-LVDS I/O, 32 Digital I/O, VHDCI-68 Front Panel Connector
TFMC685-20R   FMC for 16 RS485/RS422 I/O, 32 Digital I/O, VHDCI-68 Front Panel Connector

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.