The Embedded I/O Company

TEWS TECHNOLOGIES

TFMC685

16 Differential I/O and 32 Digital I/O FPGA Mezzanine Card

Version 1.0

User Manual

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TFMC685-10R

FMC for 16 M-LVDS I/O, 32 Digital I/O, VHDCI-68 Front Panel Connector

TFMC685-20R

FMC for 16 RS485/RS422 I/O, 32 Digital I/O, VHDCI-68 Front Panel Connector

Document History

Issue	Description	Date
1.0.0	Initial Issue	March 2025

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1 Product Description

The TFMC685 is an FMC (FPGA Mezzanine Card) Mezzanine Module complying with the ANSI/VITA 57.1 standard that offers the possibility to add a 16bit M-LVDS (Multipoint Low Voltage Differential Signaling) I/O Interface or a 16bit RS-485/RS-422 I/O Interface to FMC Carrier Cards. In addition to one of these two Differential I/O standards, the TFMC685 provides four 8bit wide 5V input tolerant 3.3V Digital I/O Interfaces and a 5V Supply pin (100mA) protected by a fuse.

The Low Pin Count FMC Connector provides 16 independent control signals which configure the direction of each Differential Transceiver and four independent control signals which configure the direction of each 8bit wide Digital I/O Gate.

The 16 data lines for M-LVDS or RS-485/RS-422 are routed as single-ended traces from the FMC Connector to the Differential Transceivers where they are converted into 16 differential pairs. The 32 data lines for Digital I/O are level shifted to be 5V tolerant at the front panel connector.

The TFMC685-10R meets the TIA/EIA-899 standard (Type-2 Receivers) and the TFMC685-20R meets the TIA/EIA-485 and the TIA/EIA-422 standard.

The 16 bits of Differential I/O, the 32 bits of Digital I/O and the 5V Supply are connected to a female VHDCI-68 Connector in the front panel.

All of the 16 M-LVDS Transceivers on the TFMC685-10R support signaling rates up to 200Mbit/s which means that a 100MHz clock can be transmitted or in other words that 200M of voltage transitions per second can be performed. The TFMC685-10R has an on-board 100Ω termination on all 16 M-LVDS Interfaces.

All RS-485/RS-422 Transceivers on the TFMC685-20R support signaling rates up to 50Mbit/s. The TFMC685-20R has an on-board 120Ω termination on all 16 RS-485/RS-422 Interfaces.

All signals connecting the Transceivers with the FMC Carrier are powered by an adjustable voltage generated by the Carrier. Because of voltage translation devices on the TFMC685 this voltage can range from 1.2V to 3.6V which allows the Carrier's FPGA I/O cells to be configured for various different I/O standards.

The signaling standard reference voltage at pin H1 of the FMC Connector, which is powered by the TFMC685, provides half of the adjustable voltage generated by the carrier for I/O standards requiring a reference voltage.

A power good LED indicates whether the FMC Carrier has signaled that all voltages it provides to the TFMC685 are within limits.

The TFMC685 is equipped with an I2C EEPROM which acts as an IPMI resource requesting the value of the adjustable voltage, for example.

The module meets the requirements to operate in extended temperature range from -40° to +85°C.

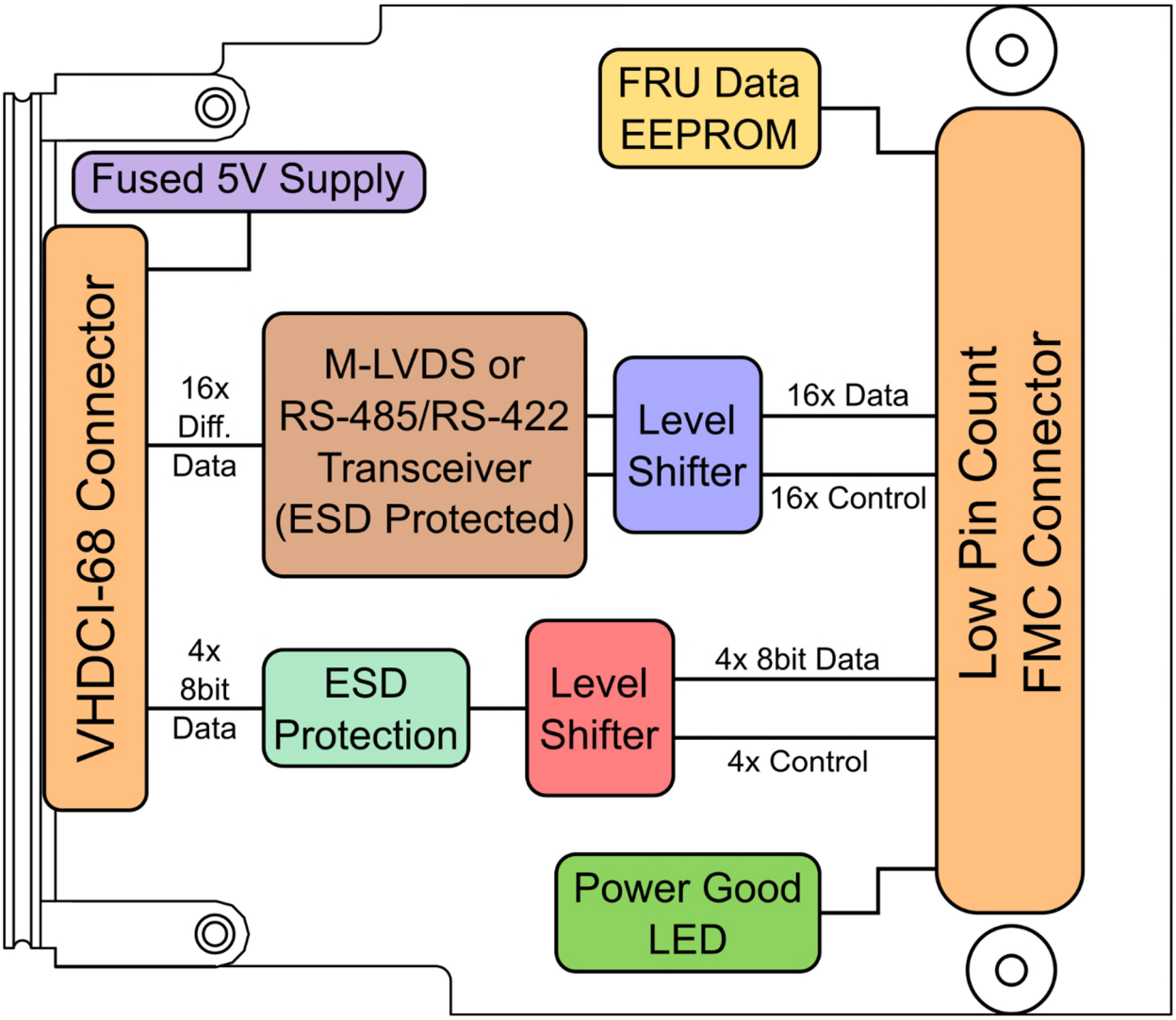


Figure 1-1 : Block Diagram

2 Technical Specification

General	
Mechanical Interface	FMC (FPGA Mezzanine Card) Mezzanine Module conforming to ANSI/VITA 57.1-2019 Single-Width (76.5 mm x 69 mm) 10mm stacking height Air cooled Commercial Grade with Front Panel Regions 1 and 2 populated
Electrical Interface	Low-Pin Count (LPC) FMC Connector 1.2V to 3.6V Signaling Voltage (VADJ) compatible Nominal Voltage: 1.8V (Preferred VADJ Signaling Voltage) 68 User defined signals on Bank A

Main On Board Devices	
M-LVDS Transceiver	SN65MLVD206D (Texas)
RS-485/RS-422 Transceiver	THVD1450D (Texas)
Digital I/O Bus Transceiver	SN74LXC8T245PWR (Texas)
FRU I²C Bus EEPROM	M24C02-RMN6 (STMicroelectronics)

I/O Interface	
M-LVDS	16 Channels 100Ω termination
RS-485/RS-422	16 Channels 120Ω termination
Digital I/O	32 Channels (4 Bidirectional 8bit Transceivers) LVTTL/TTL Level Outputs: max 24 mA per channel Inputs: 5 V tolerant
5V Supply	100 mA fuse protected
I/O Connector	VHDCI-68 Female Connector (Honda HDRA-EC68LFDT-SL+ or compatible)

Physical Data	
Power Requirements	300 mA max @ VADJ DC 800 mA max @ +3.3V DC
Temperature Range	Operating -40°C to +85°C Storage -40°C to +85°C
MTBF	TFMC685-10R: 755000 h TFMC685-20R: 787000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	42 g

Table 2-1 : Technical Specification

2.1 IPMI Serial EEPROM

The on-board M24C02-R EEPROM contains hardware definition information that may be read by an external controller using IPMI commands and I²C serial bus transactions. The mezzanine module description data on the TFMC685 includes the minimum records defined in the Platform Management FRU Information Storage Definition V1.0.

See the FMC Standard ANSI/VITA 57.1 and Platform Management FRU Information Storage Definition V1.0 for more information.

3 Handling and Operation Instructions

3.1 ESD Protection

This FMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care!

4 Data Direction Configuration

The data direction of the 16 differential channels and of the four 8bit wide Digital I/O interfaces on the TFMC685 can be configured independently by driving the OUT/IN#_DIFFxx or OUT/IN#_GATEx pins on the FMC Connector accordingly.

If the FMC Carrier drives a OUT/IN#_DIFFxx signal 'high' the corresponding M-LVDS or RS-485/RS-422 device transmits data and if the signal is driven 'low' it receives data.

If the FMC Carrier drives a OUT/IN#_GATEx signal 'high' the corresponding 8bit wide Digital I/O Gate transmits data and if the signal is driven 'low' it receives data.

At power-up or when the FMC Carrier's FPGA is unconfigured all devices are configured to receive data.

Voltage Level on OUT/IN# pin	Transceiver Configuration
Low	Receiver
High	Driver

Table 4-1 : Data Direction Configuration

5 JTAG Chain

The TFMC685 does not use Boundary Scan.

TDO and TDI are connected on the TFMC685 to ensure continuity of the FMC Carrier's JTAG Chain. TMS, TCK and TRST# are left unconnected.

6 I/O Interface Description

6.1 Overview

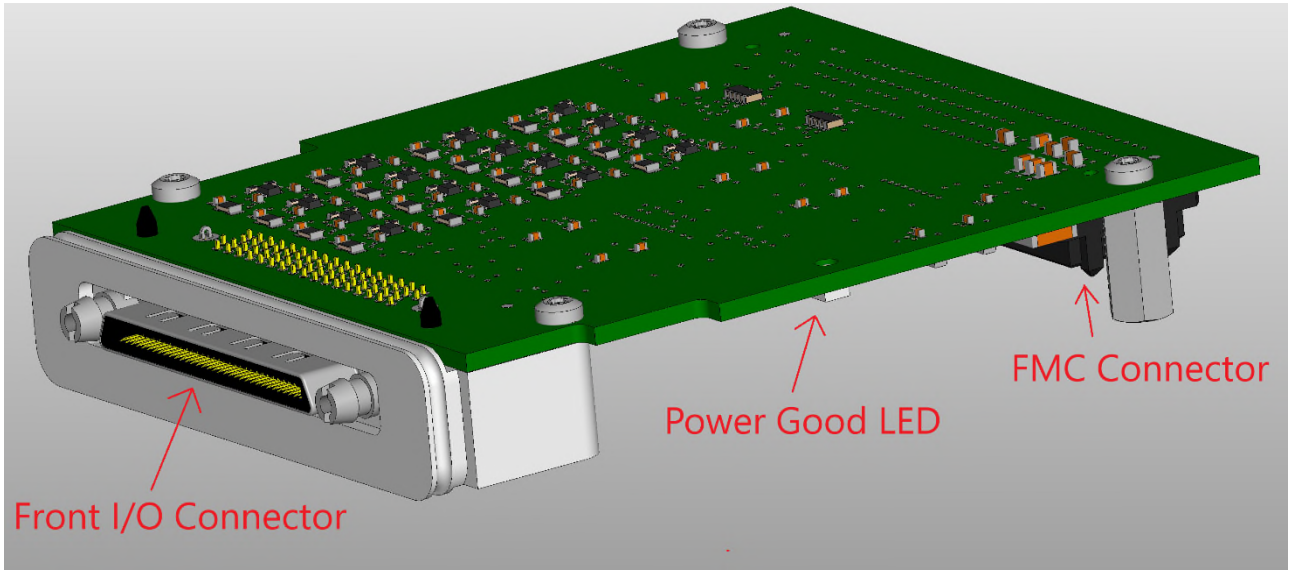


Figure 6-1 : Overview

6.2 LED Description

A power good LED indicates whether the FMC Carrier has signaled that all voltages it provides to the TFMC685 are within tolerance.

LED	Color	State	Description
PG_C2M	Green	On	FMC Carrier's power supplies VADJ, 12P0V and 3P3V are within tolerance
PG_C2M	Green	Off	FMC Carrier's power supplies VADJ, 12P0V and 3P3V have not powered-up properly

Table 6-1 : LED Description

6.3 Front I/O Connector

6.3.1 Connector Type

Pin-Count	68
Connector Type	68-pin Very High Density Cable Interconnect (VHDCI) SCSI-V, female
Source & Order Info	Honda HDRA-EC68LFDT-SL+ or compatible

Table 6-2 : Front I/O Connector Type

6.3.2 Pin Assignment

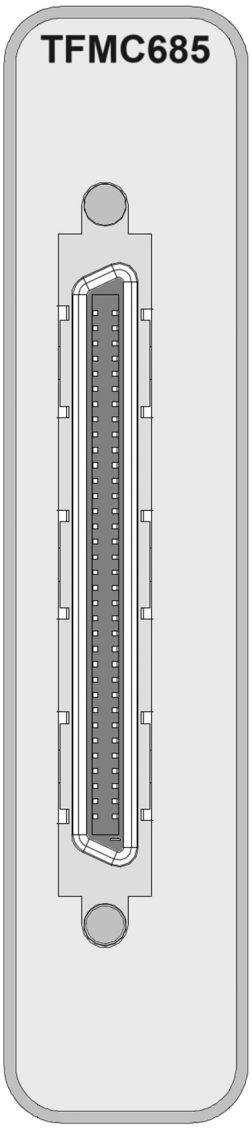
Signal	Pin		Pin	Signal
GATE3_7	68		34	GATE3_6
GATE3_5	67		33	GATE3_4
GATE3_3	66		32	GATE3_2
GATE3_1	65		31	GATE3_0
GND	64		30	GATE2_7
GATE2_6	63		29	GATE2_5
GATE2_4	62		28	GATE2_3
GATE2_2	61		27	GATE2_1
GATE2_0	60		26	GND
GATE1_7	59		25	GATE1_6
GATE1_5	58		24	GATE1_4
GATE1_3	57		23	GATE1_2
GATE1_1	56		22	GATE1_0
GND	55		21	GATE0_7
GATE0_6	54		20	GATE0_5
GATE0_4	53		19	GATE0_3
GATE0_2	52		18	GATE0_1
GATE0_0	51		17	+5V_FUSED
DIFFERENTIAL_15-	50		16	DIFFERENTIAL_15+
DIFFERENTIAL_14-	49		15	DIFFERENTIAL_14+
DIFFERENTIAL_13-	48		14	DIFFERENTIAL_13+
DIFFERENTIAL_12-	47		13	DIFFERENTIAL_12+
DIFFERENTIAL_11-	46		12	DIFFERENTIAL_11+
DIFFERENTIAL_10-	45		11	DIFFERENTIAL_10+
DIFFERENTIAL_09-	44		10	DIFFERENTIAL_09+
DIFFERENTIAL_08-	43		9	DIFFERENTIAL_08+
DIFFERENTIAL_07-	42		8	DIFFERENTIAL_07+
DIFFERENTIAL_06-	41		7	DIFFERENTIAL_06+
DIFFERENTIAL_05-	40		6	DIFFERENTIAL_05+
DIFFERENTIAL_04-	39		5	DIFFERENTIAL_04+
DIFFERENTIAL_03-	38		4	DIFFERENTIAL_03+
DIFFERENTIAL_02-	37		3	DIFFERENTIAL_02+
DIFFERENTIAL_01-	36		2	DIFFERENTIAL_01+
DIFFERENTIAL_00-	35		1	DIFFERENTIAL_00+

Table 6-3 : Front I/O Connector Pin Assignment

6.4 FMC Connector

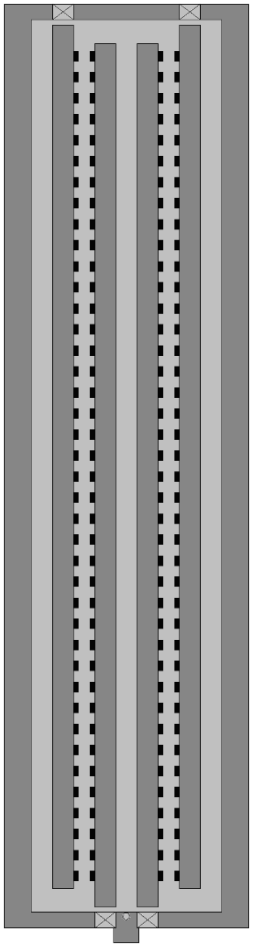
6.4.1 Connector Type

Pin-Count	160 (Low Pin Count)
Connector Type	40 x 10 array (Samtec SEARAY Series) SEAM-40-03.5-10-A, terminal / male
Source & Order Info	Samtec ASP-134604-01 (Leadfree) or compatible

Table 6-4 : FMC Connector Type

6.4.2 Pin Assignment

Signal	Pin	Pin	Signal
VADJ (VADJ)	H40	G40	GND (GND)
GND (GND)	H39	G39	VADJ (VADJ)
LA32_N (DATA_GATE3_6)	H38	G38	GND (GND)
LA32_P (DATA_GATE3_5)	H37	G37	LA33_N (OUT/'IN'_GATE3)
GND (GND)	H36	G36	LA33_P (DATA_GATE3_7)
LA30_N (DATA_GATE3_2)	H35	G35	GND (GND)
LA30_P (DATA_GATE3_1)	H34	G34	LA31_N (DATA_GATE3_4)
GND (GND)	H33	G33	LA31_P (DATA_GATE3_3)
LA28_N (DATA_GATE2_7)	H32	G32	GND (GND)
LA28_P (DATA_GATE2_6)	H31	G31	LA29_N (DATA_GATE3_0)
GND (GND)	H30	G30	LA29_P (OUT/'IN'_GATE2)
LA24_N (OUT/'IN'_GATE1)	H29	G29	GND (GND)
LA24_P (DATA_GATE1_7)	H28	G28	LA25_N (DATA_GATE2_1)
GND (GND)	H27	G27	LA25_P (DATA_GATE2_0)
LA21_N (DATA_GATE1_2)	H26	G26	GND (GND)
LA21_P (DATA_GATE1_1)	H25	G25	LA22_N (DATA_GATE1_4)
GND (GND)	H24	G24	LA22_P (DATA_GATE1_3)
LA19_N (DATA_GATE0_7)	H23	G23	GND (GND)
LA19_P (DATA_GATE0_6)	H22	G22	LA20_N (DATA_GATE1_0)
GND (GND)	H21	G21	LA20_P (OUT/'IN'_GATE0)
LA15_N (OUT/'IN'_DIFF15)	H20	G20	GND (GND)
LA15_P (DATA_DIFF15)	H19	G19	LA16_N (DATA_GATE0_1)
GND (GND)	H18	G18	LA16_P (DATA_GATE0_0)
LA11_N (OUT/'IN'_DIFF11)	H17	G17	GND (GND)
LA11_P (DATA_DIFF11)	H16	G16	LA12_N (OUT/'IN'_DIFF12)
GND (GND)	H15	G15	LA12_P (DATA_DIFF12)
LA07_N (OUT/'IN'_DIFF07)	H14	G14	GND (GND)
LA07_P (DATA_DIFF07)	H13	G13	LA08_N (OUT/'IN'_DIFF08)
GND (GND)	H12	G12	LA08_P (DATA_DIFF08)
LA04_N (OUT/'IN'_DIFF04)	H11	G11	GND (GND)
LA04_P (DATA_DIFF04)	H10	G10	LA03_N (OUT/'IN'_DIFF03)
GND (GND)	H09	G09	LA03_P (DATA_DIFF03)
LA02_N (OUT/'IN'_DIFF02)	H08	G08	GND (GND)
LA02_P (DATA_DIFF02)	H07	G07	LA00_N_CC (OUT/'IN'_DIFF00)
GND (GND)	H06	G06	LA00_P_CC (DATA_DIFF00)
CLK0_M2C_N (NC)	H05	G05	GND (GND)
CLK0_M2C_P (NC)	H04	G04	GND (GND)
GND (GND)	H03	G03	CLK1_M2C_N (NC)
PRSNT_M2C_L (GND)	H02	G02	CLK1_M2C_P (NC)
VREF_A_M2C (VADJ/2)	H01	G01	GND (GND)



Signal	Pin	Pin	Signal
3P3V (+3,3V)	D40	C40	GND (GND)
GND (GND)	D39	C39	3P3V (+3,3V)
3P3V (+3,3V)	D38	C38	GND (GND)
GND (GND)	D37	C37	12P0V (NC)
3P3V (+3,3V)	D36	C36	GND (GND)
GA1 (GA1)	D35	C35	12P0V (NC)
TRST_L (NC)	D34	C34	GA0 (GA0)
TMS (NC)	D33	C33	GND (GND)
3P3VAUX (+3,3Vaux)	D32	C32	GND (GND)
TDO (TDI)	D31	C31	SDA (SDA)
TDI (TDI)	D30	C30	SCL (SCL)
TCK (NC)	D29	C29	GND (GND)
GND (GND)	D28	C28	GND (GND)
LA26_N (DATA_GATE2_3)	D27	C27	LA27_N (DATA_GATE2_5)
LA26_P (DATA_GATE2_2)	D26	C26	LA27_P (DATA_GATE2_4)
GND (GND)	D25	C25	GND (GND)
LA23_N (DATA_GATE1_6)	D24	C24	GND (GND)
LA23_P (DATA_GATE1_5)	D23	C23	LA18_N_CC (DATA_GATE0_5)
GND (GND)	D22	C22	LA18_P_CC (DATA_GATE0_4)
LA17_N_CC (DATA_GATE0_3)	D21	C21	GND (GND)
LA17_P_CC (DATA_GATE0_2)	D20	C20	GND (GND)
GND (GND)	D19	C19	LA14_N (OUT/'IN'_DIFF14)
LA13_N (OUT/'IN'_DIFF13)	D18	C18	LA14_P (DATA_DIFF14)
LA13_P (DATA_DIFF13)	D17	C17	GND (GND)
GND (GND)	D16	C16	GND (GND)
LA09_N (OUT/'IN'_DIFF09)	D15	C15	LA10_N (OUT/'IN'_DIFF10)
LA09_P (DATA_DIFF09)	D14	C14	LA10_P (DATA_DIFF10)
GND (GND)	D13	C13	GND (GND)
LA05_N (OUT/'IN'_DIFF05)	D12	C12	GND (GND)
LA05_P (DATA_DIFF05)	D11	C11	LA06_N (OUT/'IN'_DIFF06)
GND (GND)	D10	C10	LA06_P (DATA_DIFF06)
LA01_N_CC (OUT/'IN'_DIFF01)	D09	C09	GND (GND)
LA01_P_CC (DATA_DIFF01)	D08	C08	GND (GND)
GND (GND)	D07	C07	DP0_M2C_N (NC)
GND (GND)	D06	C06	DP0_M2C_P (NC)
GBTCLK0_M2C_N (NC)	D05	C05	GND (GND)
GBTCLK0_M2C_P (NC)	D04	C04	GND (GND)
GND (GND)	D03	C03	DP0_C2M_N (NC)
GND (GND)	D02	C02	DP0_C2M_P (NC)
PG_C2M (PG_C2M)	D01	C01	GND (GND)

Table 6-5 : FMC Connector Pin Assignment

6.4.2.1 User Defined Signals on Bank A

User Defined Signal	Name	FMC Connector Pin
LA00_P_CC	DATA_DIFF00	G06
LA00_N_CC	OUT/'IN' DIFF00	G07
LA01_P_CC	DATA_DIFF01	D08
LA01_N_CC	OUT/'IN' DIFF01	D09
LA02_P	DATA_DIFF02	H07
LA02_N	OUT/'IN' DIFF02	H08
LA03_P	DATA_DIFF03	G09
LA03_N	OUT/'IN' DIFF03	G10
LA04_P	DATA_DIFF04	H10
LA04_N	OUT/'IN' DIFF04	H11
LA05_P	DATA_DIFF05	D11
LA05_N	OUT/'IN' DIFF05	D12
LA06_P	DATA_DIFF06	C10
LA06_N	OUT/'IN' DIFF06	C11
LA07_P	DATA_DIFF07	H13
LA07_N	OUT/'IN' DIFF07	H14
LA08_P	DATA_DIFF08	G12
LA08_N	OUT/'IN' DIFF08	G13
LA09_P	DATA_DIFF09	D14
LA09_N	OUT/'IN' DIFF09	D15
LA10_P	DATA_DIFF10	C14
LA10_N	OUT/'IN' DIFF10	C15
LA11_P	DATA_DIFF11	H16
LA11_N	OUT/'IN' DIFF11	H17
LA12_P	DATA_DIFF12	G15
LA12_N	OUT/'IN' DIFF12	G16
LA13_P	DATA_DIFF13	D17
LA13_N	OUT/'IN' DIFF13	D18
LA14_P	DATA_DIFF14	C18
LA14_N	OUT/'IN' DIFF14	C19
LA15_P	DATA_DIFF15	H19
LA15_N	OUT/'IN' DIFF15	H20
LA16_P	DATA_GATE0_0	G18
LA16_N	DATA_GATE0_1	G19
LA17_P_CC	DATA_GATE0_2	D20
LA17_N_CC	DATA_GATE0_3	D21
LA18_P_CC	DATA_GATE0_4	C22
LA18_N_CC	DATA_GATE0_5	C23
LA19_P	DATA_GATE0_6	H22
LA19_N	DATA_GATE0_7	H23
LA20_P	OUT/'IN' GATE0	G21
LA20_N	DATA_GATE1_0	G22
LA21_P	DATA_GATE1_1	H25
LA21_N	DATA_GATE1_2	H26
LA22_P	DATA_GATE1_3	G24
LA22_N	DATA_GATE1_4	G25
LA23_P	DATA_GATE1_5	D23
LA23_N	DATA_GATE1_6	D24
LA24_P	DATA_GATE1_7	H28
LA24_N	OUT/'IN' GATE1	H29
LA25_P	DATA_GATE2_0	G27
LA25_N	DATA_GATE2_1	G28
LA26_P	DATA_GATE2_2	D26
LA26_N	DATA_GATE2_3	D27
LA27_P	DATA_GATE2_4	C26
LA27_N	DATA_GATE2_5	C27
LA28_P	DATA_GATE2_6	H31
LA28_N	DATA_GATE2_7	H32
LA29_P	OUT/'IN' GATE2	G30
LA29_N	DATA_GATE3_0	G31
LA30_P	DATA_GATE3_1	H34
LA30_N	DATA_GATE3_2	H35
LA31_P	DATA_GATE3_3	G33
LA31_N	DATA_GATE3_4	G34
LA32_P	DATA_GATE3_5	H37
LA32_N	DATA_GATE3_6	H38
LA33_P	DATA_GATE3_7	G36
LA33_N	OUT/'IN' GATE3	G37

Table 6-6 : User Defined Signals on Bank A