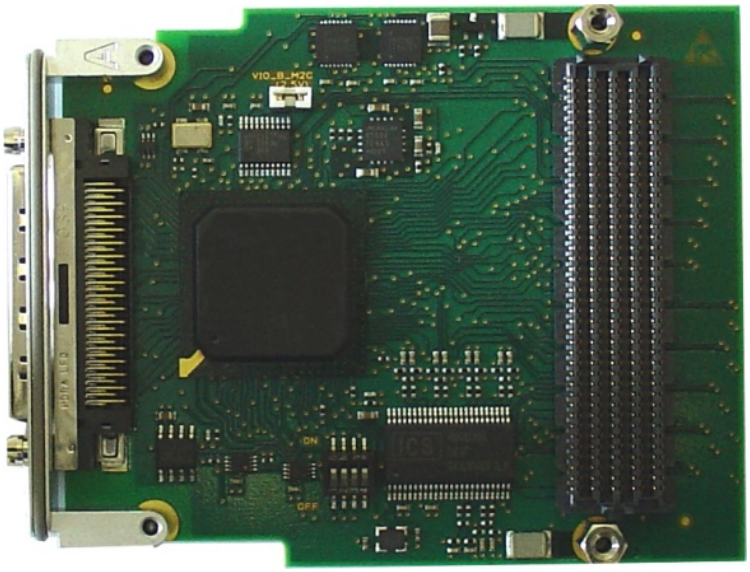
The Embedded I/O Company

TFMC900 Test FMC Mezzanine Module



Application Information

The TFMC900 is an FMC (FPGA Mezzanine Card) Mezzanine Module designed to test ANSI/VITA 57.1 FMC Carriers during development or series production. Additionally, it offers the possibility to realise various I/O solutions for connected FMC Carriers.

Interconnection of the High Pin Count FMC Connector signals can be verified by JTAG and by functional tests. A loop-back of the 10 multi-gigabit transceiver interfaces allows interconnection checks for the high-speed serial interfaces.

All voltages on the TFMC900 generated by the FMC Carrier are measured by Analog-to-Digital Converters which transfer the results via the JTAG interface.

The user configurable on-board Spartan-II FPGA, which is connected to the FMC Connector User Defined Signals and to a 68-pin Front I/O Connector, can be used to implement different I/O interfaces for the connected FMC Carrier.
The FPGA is connected to a Platform Flash to store configuration data which is accessible via the JTAG chain.

The TFMC900 is delivered with a blank configuration device. FPGA applications can be developed using the design software ISE WebPACK which can be downloaded free of charge at http://www.xilinx.com.

The FMC Connector User Defined Signals of Bank A are powered by an adjustable voltage generated by the Carrier which is preset to 3.3V (LVTTL) by IPMI. This voltage can be reduced to 2.5V (LVCMOS2) by changing the IPMI resource data inside the on-board I²C EEPROM for FPGAs not supporting the LVTTL signaling standard.

The voltage pins powering the I/O Bank B are connected to 2.5V generated by the FMC Mezzanine Module.

The TFMC900 generates six LVDS reference clock pairs and distributes them to the FMC Carrier. The frequency (common for all clock pairs) is adjustable by three dip switches on board.
The module meets the requirements to operate in extended temperature range from -40° to +85°C.

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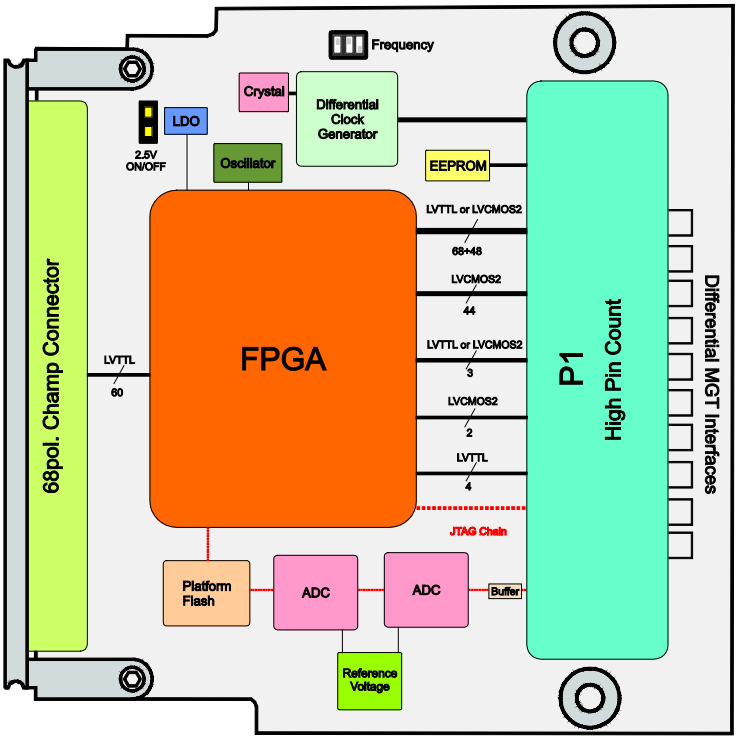
Technical Information

- Form Factor: Single-width 10 mm stacking height FPGA Mezzanine Card (FMC) Mezzanine Module conforming to ANSI/VITA 57.1
  - Board size: 84 mm x 69 mm
  - Air cooled Commercial Grade with Front Panel
  - Regions 1, 2 and 3 populated
- High Pin Count (HPC) FMC Connector
- 10 differential MGT interfaces are looped-back
- ADC with JTAG Interface to measure voltages
- Reconfigurable Spartan-II FPGA with Platform Flash
  - 40 MHz Clock
  - 68+48 FMC Bank A signals powered by VADJ
  - 44 FMC Bank B signals powered by 2.5V
  - VREF_A_M2C, VREF_B_M2C and RES0 powered by VADJ
  - Both VIO_B_M2C pins powered by 2.5V
  - GA0, GA1, PG_M2C and PG_C2M powered by 3.3V
  - 60 Front I/O signals powered by 3.3V
- The 60 Front I/O LVTTL signals at the VHDCI68/SCSI-V Connector are 5V tolerant
- On-board EEPROM contains IPMI hardware definition
- 2.5V I/O voltage for Bank B provided to the Carrier
- Adjustable differential clock generator
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 G_B 20°C) TFMC900-10R: 655000 h



Order Information

RoHS Compliant

TFMC900-10R Test FMC, test ANSI/VITA 57.1 FMC Carriers during development or series production, HPC-FMC, VHD68 connector

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

TFMC900-DOC User Manual

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