The Embedded I/O Company

TEWS TECHNOLOGIES

TFMC900

Test FMC Mezzanine Module

Version 1.0

User Manual

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TFMC900-10R

Test FMC Mezzanine Module, Front Panel I/O, extended temperature range

(RoHS compliant)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial issue	June 2011
1.0.1	General Revision	August 2014

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1 Product Description

The TFMC900 is an FMC (FPGA Mezzanine Card) Mezzanine Module that can be used in two different fields of use:

1.1 Interconnection Test Module

On the one hand it can be used to test ANSI/VITA 57.1 FMC Carriers during development or series production. Interconnection of the FMC Connector signals can be verified by JTAG and functional tests.

The Bank A and Bank B user defined signals of the High Pin Count FMC Connector are connected to a Spartan-II FPGA on the FMC Mezzanine Module which is blank at factory default. This offers the possibility to perform a JTAG interconnection test.

The HPC FMC Connector provides up to 10 multi-gigabit transceiver interfaces. For each of the 10 interfaces the differential pair coming from the FMC Carrier is connected with the corresponding differential pair going to the FMC Carrier. Connecting each TX differential pair with its corresponding RX differential pair on the FMC Mezzanine Module allows an MGT interface interconnection check by the FMC Carrier.

The power supplies provided by the FMC Carrier are measured by Analog-to-Digital Converters on the TFMC900. The results are transferred via JTAG interface to interpret whether the voltages are within defined limits. To guarantee that every power supply pin is connected the ADC measures every power pin of the FMC Connector independently.

One of the two voltage pins powering I/O Bank B is connected to 2.5V generated by the FMC Mezzanine Module. Additionally, both voltage pins are connected to Spartan-II user I/O pins to be able to verify whether the connection between the two pins is given, taking the route over the FMC Carrier. To be able to simulate a Low Pin Count FMC Mezzanine Module a jumper is available on board to disconnect the 2.5V Bank B I/O power from the FMC Connector.

The signaling standard reference voltages for the FMC Carrier I/O Bank A and Bank B which are specified to be generated by the FMC Mezzanine Module are connected to Spartan-II user I/O pins for interconnection test purposes. They do not provide a voltage because they are not needed for the signaling standards of the TFMC900.

The geographical address bits of the I²C bus connected to the on-board EEPROM are additionally connected to Spartan-II user I/O pins so that they are connected to boundary scan cells at least at one end.

The power-good signal generated by the FMC Carrier when 3.3V, 3.3Vaux, 12V and the adjustable voltage are stable, the power-good signal generated by the TFMC900 when 2.5V is stable and the reserved pin of the High Pin Count FMC Connector which is not connected on the FMC Carrier are also connected to user I/O pins of the Spartan-II.

1.2 Spartan-II FMC I/O Interface

On the other hand the user configurable on-board Spartan-II FPGA clocked at 40 MHz which is connected to the FMC Connector user defined signals and to a Front I/O Connector offers the possibility to implement various I/O solutions which allows the TFMC900 to act as an I/O interface for the connected FMC Carrier.

60 user I/O pins of the Spartan-II are connected to the 68pin VHDCI/SCSI-V Connector in the front panel. Voltages up to 5V can be applied to the Front I/O Connector and the FPGA I/O standard for these signals is LVTTL (3.3V).

Having the flexibility of reconfiguring the FPGA with a JTAG-capable Platform Flash Device, several I/O test environments are imaginable. The TFMC900 is delivered with a blank configuration device and FPGA applications can be developed using the design software ISE WebPACK which can be downloaded free of charge at http://www.xilinx.com.

On the FMC Mezzanine Module the user defined signals of the FMC Connector are routed single-ended and not differentially. These signals coming from the FMC Carrier FPGA are divided into Bank A and Bank B.

The FMC Connector user defined signals of Bank A are powered by an adjustable voltage generated by the Carrier which is preset to 3.3V (LVTTL) by IPMI. This voltage can be reduced to 2.5V (LVCMOS2) by changing the IPMI resource data inside the on-board I²C EEPROM for FPGAs not supporting the LVTTL signaling standard. The voltage pin providing the I/O voltage for Bank B is connected to 2.5V generated by the FMC Mezzanine Module which means that the TFMC900 sets the signaling standard of Bank B to LVCMOS2.

The TFMC900 is equipped with an I²C EEPROM which acts as an IPMI resource requesting the value of the adjustable voltage VADJ, for example. The EEPROM interprets the geographical address signals set by the FMC Carrier to determine its I²C address.

The TFMC900 generates six differential LVDS reference clock pairs and distributes them to the FMC Carrier. The frequency (common for all clock pairs) is adjustable by three dip switches on-board. The clock direction pin of the HPC FMC Connector is tied to ground because all differential clock pairs are distributed from the FMC Mezzanine Module to the FMC Carrier.

PG_C2M which indicates whether all voltage generated by the Carrier are ramped up acts as an enable signal for the LDO on the TFMC900 generating 2.5V. The VITA 57.1 Specification states that the FMC Mezzanine Module must output a LVTTL high level as soon as the reference voltages for Bank A and Bank B of the Carrier FPGA and the Bank B I/O voltage are stable. As there are no reference voltages generated by the FMC Mezzanine Module and the Bank B I/O is powered by 2.5V, this signal is pulled high by the LDO Linear Regulator generating the 2.5V on the TFMC900 as soon as the voltage is within reasonable limits.

The active-low module present signal which is pulled-up by the Carrier is tied to ground by the TFMC900 to indicate that a Mezzanine Module is connected to the FMC Carrier.

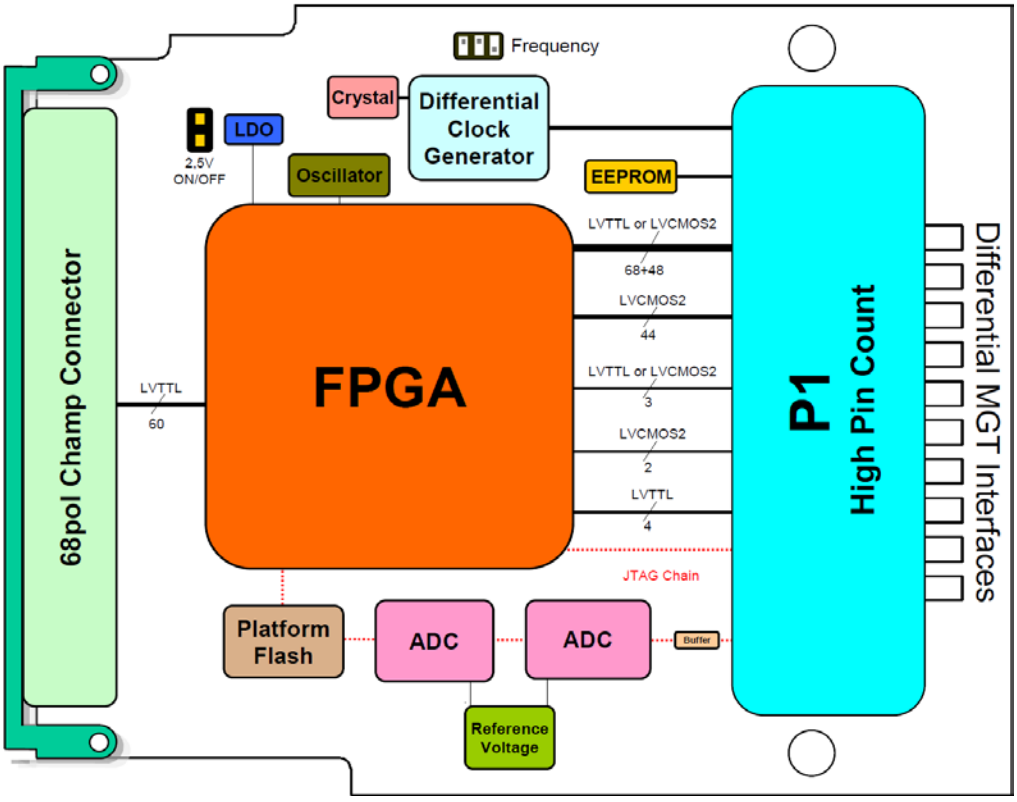

Figure 1-1 : Block Diagram

The module meets the requirements to operate in extended temperature range from -40° to +85°C.

2 Technical Specification

FMC Interface		
Mechanical Interface	FPGA Mezzanine Card (FMC) Mezzanine Module confirming to ANSI/VITA 57.1 Single Width, 10mm stacking height Air cooled Commercial Grade with Front Panel Regions 1, 2 and 3 populated	
Electrical Interface	High-Pin Count Connector **User defined signals on Bank A:** 3.3V or 2.5V Signaling Voltage **User defined signals on Bank B:** 2.5V Signaling Voltage	
On Board Devices		
FPGA	Spartan-II XC2S150-5 FG G 456 I (Xilinx)	
Platform Flash	XCF01S VOG20 C (Xilinx)	
Differential Clock Generator	ICS9FG108D (Integrated Device Technology)	
ADC	SCANSTA476 (National Semiconductor)	
EEPROM	M24C02 (STMicroelectronics)	
I/O Interface		
Number of Channels	60 channels at 3.3V signaling voltage (5V tolerant)	
I/O Connector	Front I/O VHDCI68 / SCSI-V (Honda HDRA-EC68LFDT-SL+ or compatible)	
Physical Data		
Power Specification in FRU multi-record data	max. 1000mA @ VADJ max. 2000mA @ +3.3V max. 10mA @ +12V	DC Load
	max. 1000mA @ VIO_B_M2C max. 0mA @ VREF_A_M2C max. 0mA @ VREF_B_M2C	DC Output
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	655000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	47 g	

Table 2-1 : Technical Specification

2.1 IPMI Serial EEPROM

The on-board M24C02 EEPROM contains hardware definition information that may be read by an external controller using IPMI commands and I²C serial bus transactions. The mezzanine module description data on the TFMC900 includes the minimum records defined in the Platform Management FRU Information Storage Definition V1.0.

See the FMC Standard ANSI/VITA 57.1 and Platform Management FRU Information Storage Definition V1.0 for more information.

3 Differential Clock Generator Configuration

The TFMC900 is equipped with DIP Switches that can be used to set the frequency of the differential clocks supplied to the FMC Carrier FPGA for its multi-gigabit interfaces and user defined differential clock usage. The DIP Switch number 4 is not connected.

Figure 3-1 : DIP Switches

	DIP Switch			
Differential Clock Frequency	**1**	**2**	**3**	**4**
100 MHz	OFF	OFF	OFF	don't care
125 MHz	ON	OFF	OFF	don't care
133.33 MHz	OFF	ON	OFF	don't care
166.67 MHz	ON	ON	OFF	don't care
200 MHz	OFF	OFF	ON	don't care
266.66 MHz	ON	OFF	ON	don't care
333.33 MHz	OFF	ON	ON	don't care
400 MHz	ON	ON	ON	don't care

Table 3-1 : DIP Switch Configuration

4 Interconnection Test

Some signals of the High Pin Count FMC Connector cannot or not completely be covered in a JTAG Boundary Scan routine because they do not have a boundary scan cell at both ends. The following table lists theses signals and explains how interconnection can be verified. Additionally it shows which of these signals are connected to Spartan-II user I/O pins on the TFMC900 and therefore are connected to a boundary scan cell at least at one end.

Signal	Alternative Interconnection Test	Connected to Spartan-II
DP0_C2M_P	The 10 multi-gigabit transceiver interfaces can be tested by performing a loop-back communication because every differential TX pair is connected to its corresponding RX pair on the TFMC900.	NO
DP0_C2M_N		NO
DP0_M2C_P		NO
DP0_M2C_N		NO
DP1_C2M_P		NO
DP1_C2M_N		NO
DP1_M2C_P		NO
DP1_M2C_N		NO
DP2_C2M_P		NO
DP2_C2M_N		NO
DP2_M2C_P		NO
DP2_M2C_N		NO
DP3_C2M_P		NO
DP3_C2M_N		NO
DP3_M2C_P		NO
DP3_M2C_N		NO
DP4_C2M_P		NO
DP4_C2M_N		NO
DP4_M2C_P		NO
DP4_M2C_N		NO
DP5_C2M_P		NO
DP5_C2M_N		NO
DP5_M2C_P		NO
DP5_M2C_N		NO
DP6_C2M_P		NO
DP6_C2M_N		NO
DP6_M2C_P		NO
DP6_M2C_N		NO
DP7_C2M_P		NO
DP7_C2M_N		NO
DP7_M2C_P		NO
DP7_M2C_N		NO
DP8_C2M_P		NO
DP8_C2M_N		NO
DP8_M2C_P		NO
DP8_M2C_N		NO
DP9_C2M_P		NO
DP9_C2M_N		NO
DP9_M2C_P		NO
DP9_M2C_N		NO
GBTCLK0_M2C_P	The differential multi-gigabit reference clocks are implicitly tested by verifying the MGT interface.	NO
GBTCLK0_M2C_N		NO
GBTCLK1_M2C_P		NO
GBTCLK1_M2C_N		NO

CLK0_M2C_P	The additional four differential clock pairs can be verified by the logic of the FMC Carrier FPGA as the frequency is defined by DIP Switch configuration.	NO
CLK0_M2C_N		NO
CLK1_M2C_P		NO
CLK1_M2C_N		NO
CLK2_BIDIR_P		NO
CLK2_ BIDIR _N		NO
CLK3_ BIDIR _P		NO
CLK3_ BIDIR _N		NO
PG_C2M	The Spartan-II senses when the Carrier drives this LVTTL signal high.	YES
VIO_B_M2C	Connected to 2.5V on TFMC900: Carrier FPGA I/O Bank B power is implicitly tested by transferring data on Bank B signals.	YES
VIO_B_M2C	Not Connected to 2.5V on TFMC900: LVCMOS2 high level (2,5V) can be sensed on the pin when interconnection is given.	YES
3P3VAUX	The corresponding JTAG ADC result indicates that the pin is properly connected.	NO
3P3V	The corresponding JTAG ADC result indicates that all four pins are properly connected.	NO
3P3V		NO
3P3V		NO
3P3V		NO
PG_M2C	The Carrier FPGA can measure whether a high LVTTL level is present at that pin.	YES
VADJ	The corresponding JTAG ADC result indicates that all four pins are properly connected.	NO
VADJ		NO
VADJ		NO
VADJ		NO
SCL	The I²C Interface is implicitly tested by communicating with the EEPROM that contains the FRU data.	NO
SDA		NO
GA0		YES
GA1		YES
12P0V	The corresponding JTAG ADC result indicates that the pins are properly connected.	NO
12P0V		NO
RES0	The reserved pin is not connected on the FMC Carrier.	YES
PRSNT_M2C_L	The TFMC900 connects this signal to ground which can be sensed by the Carrier.	NO
CLK_DIR	The TFMC900 connects this signal to ground which can be sensed by the Carrier.	NO

Table 4-1 : Interconnection Test

5 Disconnecting I/O Bank B Power Supply

To be able to simulate a Low Pin Count FMC Mezzanine Module which does not supply VIO_B_M2C the 2.5V power supply can be disconnected from the FMC Connector.

To disconnect 2.5V from the FMC Connector the jumper J1 must not be slipped over the according jumper pins. The possible configurations are illustrated in the following figure.

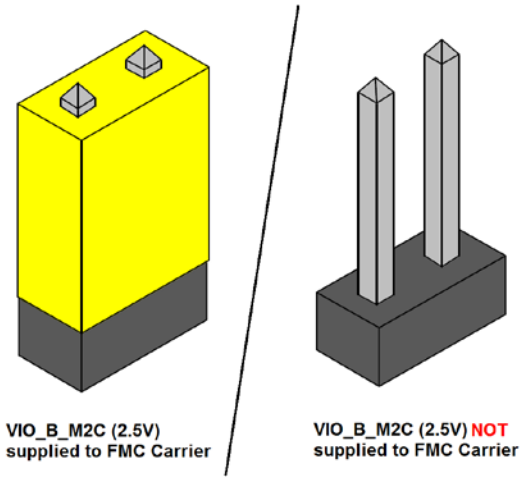

Figure 5-1 : Jumper configuration

6 JTAG Chain

The "JTAG" or "Boundary Scan" Chain is displayed in the following figure:

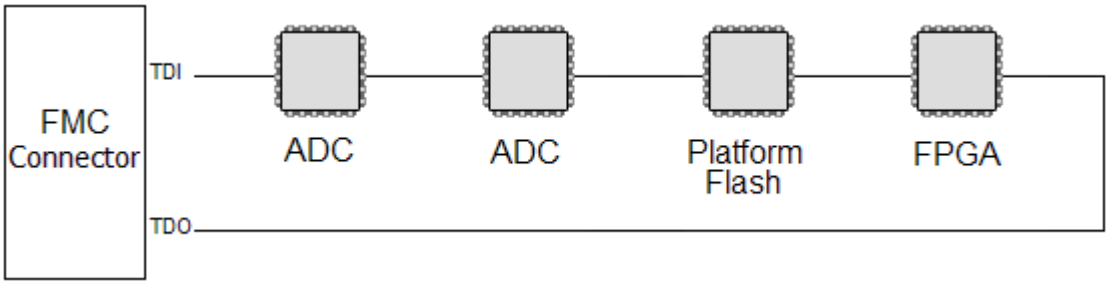

Figure 6-1 : JTAG Chain

7 FPGA Logic

7.1 Top Entity

To support the implementation of an FPGA design a typical VHDL top entity is displayed in the following:

```
entity TFMC900 is
  port
  (

    -- 40 MHz Clock
    CLK : in std_logic;

    -- User defined signals on Bank A (LPC and HPC)
    LA_P : in std_logic_vector(33 downto 0);
    LA_N : in std_logic_vector(33 downto 0);

    -- User defined signals on Bank A (HPC)
    HA_P : in std_logic_vector(23 downto 0);
    HA_N : in std_logic_vector(23 downto 0);

    -- User defined signals on Bank B (HPC)
    HB_P : in std_logic_vector(21 downto 0);
    HB_N : in std_logic_vector(21 downto 0);

    -- Geographical address
    GA : in std_logic_vector(1 downto 0);

    -- Reference voltages for the signaling standards of Bank A and Bank B
    VREF_A_M2C : in std_logic;
    VREF_B_M2C : in std_logic;

    -- Main voltage for I/O pins of Bank B
    VIO_B_M2C : in std_logic_vector(2 downto 1);

    -- FMC Carrier power-good (VADJ, 3.3Vaux, 3.3V, 12V)
    PG_C2M : in std_logic;

    -- TFMC900 power-good (VREF_A_M2C, VREF_B_M2C, VIO_B_M2C)
    PG_M2C : in std_logic;

    -- Reserved pin
    RES0 : in std_logic;

    -- 60 Front I/O champ connector pins
    FRONT : out std_logic_vector(59 downto 0)
  );
end TFMC900;
```

7.2 UCF File

To be able to use the top entity a *.ucf file is needed which is displayed in the following.

When the IPMI data inside the on-board EEPROM is modified to set VADJ generated by the FMC Carrier from 3.3V to 2.5V, which changes the I/O standard of the Bank A user defined signals, the UCF file has to be modified and the IOSTANDARD of all signals marked #(VADJ) has to be set from LVTTL to LVCMOS2.

```
##########################################################################
# Location Constraints and I/O Standard
##########################################################################

# 40 MHz Clock
NET "CLK"                LOC = "A11"      |IOSTANDARD = LVTTL; #(3.3V)

# User defined signals on Bank A (LPC and HPC)
NET "LA_P<0>"            LOC = "F2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<0>"            LOC = "V1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<1>"            LOC = "Y1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<1>"            LOC = "T2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<2>"            LOC = "R1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<2>"            LOC = "P2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<3>"            LOC = "V2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<3>"            LOC = "V3"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<4>"            LOC = "P3"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<4>"            LOC = "F3"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<5>"            LOC = "H3"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<5>"            LOC = "AB4"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<6>"            LOC = "Y2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<6>"            LOC = "J3"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<7>"            LOC = "M4"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<7>"            LOC = "G4"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<8>"            LOC = "V4"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<8>"            LOC = "N4"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<9>"            LOC = "AA5"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<9>"            LOC = "AA4"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<10>"           LOC = "AB5"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<10>"           LOC = "E4"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<11>"           LOC = "G5"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<11>"           LOC = "M6"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<12>"           LOC = "H5"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<12>"           LOC = "N5"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<13>"           LOC = "AA6"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<13>"           LOC = "L6"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<14>"           LOC = "W6"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<14>"           LOC = "V7"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<15>"           LOC = "AB9"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<15>"           LOC = "Y10"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<16>"           LOC = "Y7"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<16>"           LOC = "V8"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<17>"           LOC = "V9"       |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<17>"           LOC = "V10"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<18>"           LOC = "V11"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<18>"           LOC = "U12"      |IOSTANDARD = LVTTL; #(VADJ)
```

```
NET "LA_P<19>"          LOC = "AA12"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<19>"          LOC = "AA13"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<20>"          LOC = "AB11"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<20>"          LOC = "U11"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<21>"          LOC = "W14"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<21>"          LOC = "AA15"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<22>"          LOC = "AA14"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<22>"          LOC = "Y14"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<23>"          LOC = "AB13"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<23>"          LOC = "V13"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<24>"          LOC = "W16"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<24>"          LOC = "V16"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<25>"          LOC = "AB16"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<25>"          LOC = "Y16"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<26>"          LOC = "AB15"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<26>"          LOC = "V15"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<27>"          LOC = "V14"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<27>"          LOC = "Y15"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<28>"          LOC = "Y17"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<28>"          LOC = "AB18"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<29>"          LOC = "AB17"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<29>"          LOC = "AA17"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<30>"          LOC = "V17"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<30>"          LOC = "AB19"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<31>"          LOC = "W17"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<31>"          LOC = "AA18"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<32>"          LOC = "W18"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<32>"          LOC = "AA20"     |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_P<33>"          LOC = "Y18"      |IOSTANDARD = LVTTL; #(VADJ)
NET "LA_N<33>"          LOC = "AA19"     |IOSTANDARD = LVTTL; #(VADJ)

# User defined signals on Bank A (HPC)
NET "HA_P<0>"           LOC = "H1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<0>"           LOC = "D2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<1>"           LOC = "F1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<1>"           LOC = "G1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<2>"           LOC = "L1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<2>"           LOC = "W1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<3>"           LOC = "K1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<3>"           LOC = "J2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<4>"           LOC = "R2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<4>"           LOC = "U1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<5>"           LOC = "H2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<5>"           LOC = "T1"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<6>"           LOC = "M3"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<6>"           LOC = "E3"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<7>"           LOC = "W2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<7>"           LOC = "N3"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<8>"           LOC = "W3"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<8>"           LOC = "G3"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<9>"           LOC = "U2"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<9>"           LOC = "AB3"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<10>"          LOC = "K4"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<10>"          LOC = "F4"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<11>"          LOC = "U4"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<11>"          LOC = "L4"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<12>"          LOC = "P4"       |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<12>"          LOC = "W5"       |IOSTANDARD = LVTTL; #(VADJ)
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NET "HA_P<13>"          LOC = "K5"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<13>"          LOC = "T4"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<14>"          LOC = "J5"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<14>"          LOC = "M5"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<15>"          LOC = "F5"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<15>"          LOC = "AB6"     |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<16>"          LOC = "R5"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<16>"          LOC = "T5"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<17>"          LOC = "L5"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<17>"          LOC = "Y6"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<18>"          LOC = "W7"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<18>"          LOC = "Y9"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<19>"          LOC = "Y8"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<19>"          LOC = "AB10"    |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<20>"          LOC = "AA7"     |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<20>"          LOC = "AA8"     |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<21>"          LOC = "W9"      |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<21>"          LOC = "W10"     |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<22>"          LOC = "W11"     |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<22>"          LOC = "Y12"     |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_P<23>"          LOC = "V12"     |IOSTANDARD = LVTTL; #(VADJ)
NET "HA_N<23>"          LOC = "Y13"     |IOSTANDARD = LVTTL; #(VADJ)

# User defined signals on Bank B (HPC)
NET "HB_P<0>"           LOC = "R18"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<0>"           LOC = "T19"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<1>"           LOC = "N18"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<1>"           LOC = "T18"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<2>"           LOC = "J18"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<2>"           LOC = "M18"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<3>"           LOC = "G18"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<3>"           LOC = "L18"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<4>"           LOC = "G19"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<4>"           LOC = "U19"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<5>"           LOC = "P18"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<5>"           LOC = "M19"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<6>"           LOC = "V20"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<6>"           LOC = "T20"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<7>"           LOC = "N19"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<7>"           LOC = "F19"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<8>"           LOC = "H19"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<8>"           LOC = "U20"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<9>"           LOC = "P19"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<9>"           LOC = "J19"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<10>"          LOC = "T21"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<10>"          LOC = "P21"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<11>"          LOC = "N20"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<11>"          LOC = "V21"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<12>"          LOC = "W21"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<12>"          LOC = "AA22"    |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<13>"          LOC = "P20"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<13>"          LOC = "M20"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<14>"          LOC = "F20"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<14>"          LOC = "E20"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<15>"          LOC = "V22"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<15>"          LOC = "L21"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<16>"          LOC = "U22"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<16>"          LOC = "G20"     |IOSTANDARD = LVCMOS2; #(2.5V)
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NET "HB_P<17>"          LOC = "D21"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<17>"          LOC = "F22"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<18>"          LOC = "G21"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<18>"          LOC = "J22"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<19>"          LOC = "W22"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<19>"          LOC = "J20"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<20>"          LOC = "K22"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<20>"          LOC = "E21"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_P<21>"          LOC = "J21"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "HB_N<21>"          LOC = "L22"     |IOSTANDARD = LVCMOS2; #(2.5V)

# Geographical address
NET "GA<0>"             LOC = "C19"     |IOSTANDARD = LVTTL; #(3.3V)
NET "GA<1>"             LOC = "A20"     |IOSTANDARD = LVTTL; #(3.3V)

# Reference voltages for the signaling standards of Bank A and Bank B
NET "VREF_A_M2C"        LOC = "C1"      |IOSTANDARD = LVTTL; #(VADJ)
NET "VREF_B_M2C"        LOC = "B1"      |IOSTANDARD = LVTTL; #(VADJ)

# Main voltage for I/O pins of Bank B
NET "VIO_B_M2C<1>"      LOC = "D22"     |IOSTANDARD = LVCMOS2; #(2.5V)
NET "VIO_B_M2C<2>"      LOC = "E22"     |IOSTANDARD = LVCMOS2; #(2.5V)

# FMC Carrier power-good (VADJ, 3.3Vaux, 3.3V, 12V)
NET "PG_C2M"            LOC = "B3"      |IOSTANDARD = LVTTL; #(3.3V)

# TFMC900 power-good (VREF_A_M2C, VREF_B_M2C, VIO_B_M2C)
NET "PG_M2C"            LOC = "A3"      |IOSTANDARD = LVTTL; #(3.3V)

# Reserved pin
NET "RES0"              LOC = "AB20"    |IOSTANDARD = LVTTL; #(VADJ)

# 60 Front I/O champ connector pins
NET "FRONT<0>"          LOC = "C18"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<1>"          LOC = "B18"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<2>"          LOC = "B19"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<3>"          LOC = "A19"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<4>"          LOC = "C17"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<5>"          LOC = "B17"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<6>"          LOC = "A18"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<7>"          LOC = "D17"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<8>"          LOC = "D16"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<9>"          LOC = "C16"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<10>"         LOC = "E16"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<11>"         LOC = "A17"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<12>"         LOC = "D15"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<13>"         LOC = "C15"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<14>"         LOC = "A16"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<15>"         LOC = "E15"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<16>"         LOC = "E14"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<17>"         LOC = "D14"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<18>"         LOC = "B15"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<19>"         LOC = "A15"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<20>"         LOC = "B14"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<21>"         LOC = "C13"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<22>"         LOC = "C14"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<23>"         LOC = "D13"     |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<24>"         LOC = "F12"     |IOSTANDARD = LVTTL; #(3.3V)
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NET "FRONT<25>"          LOC = "D12"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<26>"          LOC = "B13"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<27>"          LOC = "E12"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<28>"          LOC = "C12"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<29>"          LOC = "E11"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<30>"          LOC = "B12"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<31>"          LOC = "D11"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<32>"          LOC = "B10"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<33>"          LOC = "D10"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<34>"          LOC = "A10"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<35>"          LOC = "C10"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<36>"          LOC = "A9"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<37>"          LOC = "D9"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<38>"          LOC = "E10"      |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<39>"          LOC = "B9"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<40>"          LOC = "E9"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<41>"          LOC = "B8"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<42>"          LOC = "A8"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<43>"          LOC = "D8"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<44>"          LOC = "E8"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<45>"          LOC = "B7"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<46>"          LOC = "A7"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<47>"          LOC = "C7"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<48>"          LOC = "D7"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<49>"          LOC = "B6"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<50>"          LOC = "E7"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<51>"          LOC = "C6"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<52>"          LOC = "D6"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<53>"          LOC = "B5"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<54>"          LOC = "A5"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<55>"          LOC = "C5"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<56>"          LOC = "E6"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<57>"          LOC = "D5"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<58>"          LOC = "A4"       |IOSTANDARD = LVTTL; #(3.3V)
NET "FRONT<59>"          LOC = "B4"       |IOSTANDARD = LVTTL; #(3.3V)

# Unused FPGA pins
CONFIG PROHIBIT = "L17"; #(2.5V)
CONFIG PROHIBIT = "F18"; #(2.5V)
CONFIG PROHIBIT = "C22"; #(2.5V)
CONFIG PROHIBIT = "D20"; #(2.5V)
CONFIG PROHIBIT = "H22"; #(2.5V)
CONFIG PROHIBIT = "H20"; #(2.5V)
CONFIG PROHIBIT = "K20"; #(2.5V)
CONFIG PROHIBIT = "N22"; #(2.5V)
CONFIG PROHIBIT = "R21"; #(2.5V)
CONFIG PROHIBIT = "T22"; #(2.5V)
CONFIG PROHIBIT = "Y21"; #(2.5V)
CONFIG PROHIBIT = "V19"; #(2.5V)
CONFIG PROHIBIT = "C21"; #(2.5V)
CONFIG PROHIBIT = "L20"; #(2.5V)
CONFIG PROHIBIT = "M22"; #(2.5V)
CONFIG PROHIBIT = "F21"; #(2.5V)
CONFIG PROHIBIT = "H18"; #(2.5V)
CONFIG PROHIBIT = "N21"; #(2.5V)
CONFIG PROHIBIT = "R19"; #(2.5V)
CONFIG PROHIBIT = "U21"; #(2.5V)
CONFIG PROHIBIT = "W12"; #(VADJ)
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CONFIG PROHIBIT = "Y11"; #(VADJ)
CONFIG PROHIBIT = "K21"; #(VADJ)
CONFIG PROHIBIT = "E1"; #(VADJ)
CONFIG PROHIBIT = "L3"; #(VADJ)
CONFIG PROHIBIT = "M1"; #(VADJ)
CONFIG PROHIBIT = "E2"; #(VADJ)
CONFIG PROHIBIT = "H4"; #(VADJ)
CONFIG PROHIBIT = "K3"; #(VADJ)
CONFIG PROHIBIT = "N2"; #(VADJ)
CONFIG PROHIBIT = "R4"; #(VADJ)
CONFIG PROHIBIT = "T3"; #(VADJ)
CONFIG PROHIBIT = "W8"; #(VADJ)
CONFIG PROHIBIT = "C11"; #(3.3V)

##########################################################################
# Timing Constraints
##########################################################################

NET "CLK" TNM_NET = "CLK";
TIMESPEC "TS_CLK" = PERIOD "CLK" 25 ns HIGH 50 %;
```

8 Pin Assignment – I/O Connector

8.1 Front I/O Connector

Pin-Count	68
Connector Type	68-pin Very High Density Cable Interconnect (VHDCI) SCSI-V, female
Source & Order Info	Honda HDRA-EC68LFDT-SL+ or compatible

Table 8-1 : Front I/O Connector Type

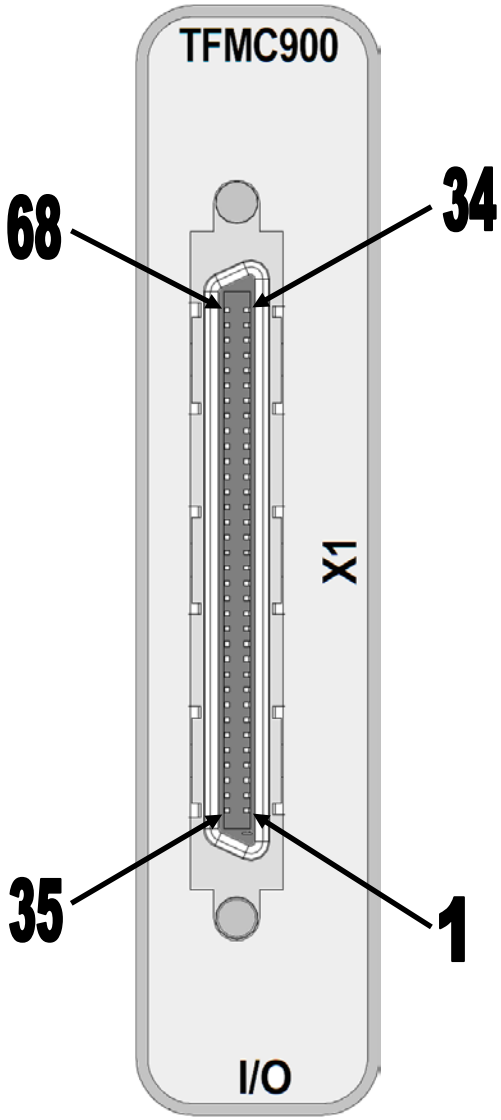

Figure 8-1 : Front I/O Connector view

8.1.1 Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
68	FRONT_00	67	FRONT_01	34	FRONT_02	33	FRONT_03
66	FRONT_04	65	FRONT_05	32	FRONT_06	31	FRONT_07
64	FRONT_08	63	FRONT_09	30	FRONT_10	29	FRONT_11
62	FRONT_12	61	FRONT_13	28	FRONT_14	27	FRONT_15
60	FRONT_16	59	FRONT_17	26	FRONT_18	25	FRONT_19
58	GND	57	GND	24	GND	23	GND
56	FRONT_20	55	FRONT_21	22	FRONT_22	21	FRONT_23
54	FRONT_24	53	FRONT_25	20	FRONT_26	19	FRONT_27
52	FRONT_28	51	FRONT_29	18	FRONT_30	17	FRONT_31
50	FRONT_32	49	FRONT_33	16	FRONT_34	15	FRONT_35
48	FRONT_36	47	FRONT_37	14	FRONT_38	13	FRONT_39
46	GND	45	GND	12	GND	11	GND
44	FRONT_40	43	FRONT_41	10	FRONT_42	9	FRONT_43
42	FRONT_44	41	FRONT_45	8	FRONT_46	7	FRONT_47
40	FRONT_48	39	FRONT_49	6	FRONT_50	5	FRONT_51
38	FRONT_52	37	FRONT_53	4	FRONT_54	3	FRONT_55
36	FRONT_56	35	FRONT_57	2	FRONT_58	1	FRONT_59

Table 8-2 : Pin Assignment Front I/O Connector

8.2 FMC Connector

Pin-Count	400 (High Pin Count)
Connector Type	40 x 10 array (Samtec SEARAY Series), SEAM-40-03.5-10-A, terminal / male
Source & Order Info	Samtec ASP-134488-01 (Leadfree) or compatible

Table 8-3 : FMC Connector Type

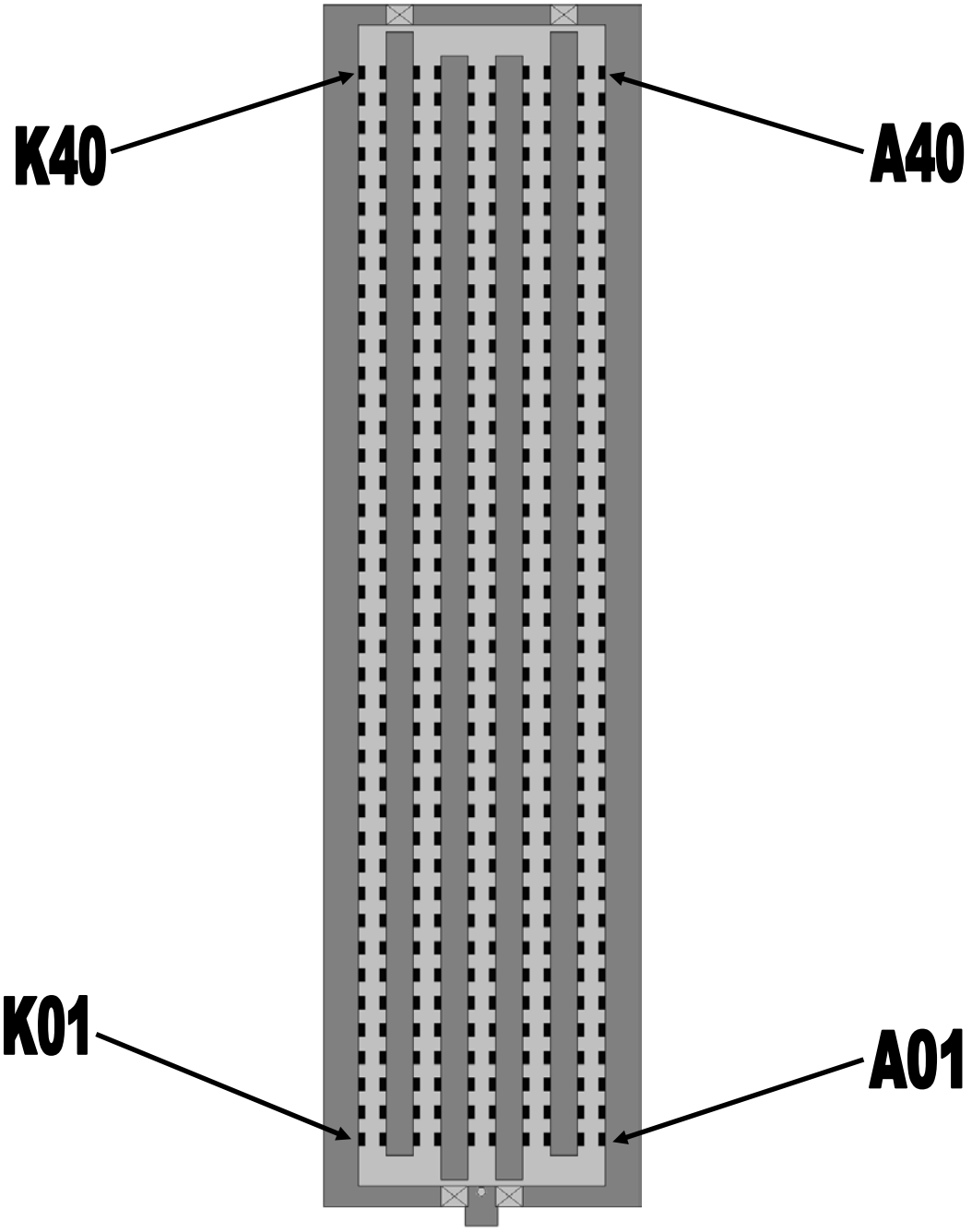

Figure 8-2 : FMC Connector view

8.2.1 Pin Assignment

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Table 8-4 : Pin Assignment FMC Connector

9 Known Issues

The power net VADJ generated by the FMC Carrier is split into four nets on the TFMC900:

- VADJ_A
- VADJ_B
- VADJ_C
- VADJ_D

Due to this fact interconnection of every supply pin on the FMC Connector can be verified independently as every pin is connected to a different ADC input.

In revision V1.0 Rev.A a hardware design error lead to the decision to connect VADJ_A to VADJ_C and to connect VADJ_B to VADJ_D which means that it is not possible to check every voltage pin independently.

This issue will be solved in the next board release.