The Embedded I/O Company

TIP102

Motion Controller with

Incremental Encoder Interface

Version 1.1

User Manual

Issue 1.1.9

November 2008

TIP102-1x

One axis motion controller incremental encoder interface

TIP102-2x

Two axes motion controller incremental encoder interface

TIP102-TM-10

Transition Module for TIP102-1x
Isolated 24V digital I/O

TIP102-TM-11

Transition Module for TIP102-1x
Isolated 24V digital I/O, encoder

TIP102-TM-12

Transition Module for TIP102-1x
Isolated 24V digital I/O, encoder, analog out

TIP102-TM-13

Transition Module for TIP102-1x
Isolated 24V digital I/O, encoder, analog in & out

TIP102-TM-20

Transition Module for TIP102-2x
Isolated 24V digital I/O

TIP102-TM-21

Transition Module for TIP102-2x
Isolated 24V digital I/O, encoder

TIP102-TM-22

Transition Module for TIP102-2x
Isolated 24V digital I/O, encoder, analog out

TIP102-TM-23

Transition Module for TIP102-2x
Isolated 24V digital I/O, encoder, analog in & out

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	April 1994
1.1	Extended	December 1994
1.2	Technical Specification	April 1996
1.3	General Revision	October 2003
1.4	Add ID PROM contents for version 1.1	September 2004
1.5	Additional note for ADC conversion	October 2004
1.6	More detailed description of the various I/O signals	October 2005
1.7	New address TEWS LLC	September 2006
1.8	Signal Polarity Clarification in Pin Assignment Tables	February 2007
1.1.9	Complete revision during redesign process Documentation versioning scheme has changed	November 2008

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1 Product Description

The TIP102 family is IndustryPack® compatible modules with complete one or two axes high precision motion control interfaces, using incremental encoder with RS422 or TTL signal level for position feedback. The transition module TIP102-TM-xx is required for the signal conditioning and optional galvanically isolation of the various input and output signals.

The position feedback is provided by an incremental encoder interface and a 24 bit up/down counter. The level of the encoder signals can be TTL or RS422. Optionally, the encoder signals can be isolated on the transition module by high speed optocouplers. The encoder signals pass a digital filter for noise suppression before they are fed into the counter and the reference logic. The counter is programmable for single, double and quadruples analysis of the encoder two phase signals.

Calibration of the position feedback to an absolute reference point is done by an adjustable reference logic. This logic incorporates several modes of operation and hardware configurations (Reference Switches, Encoder Index Pulse, External Triggers) for the generation of the reference condition. During normal operation, the automatic recalibration of the measurement system is practicable with the "auto reference" mode, whenever the system passes the reference location.

Two isolated 24V DC digital inputs have limit switch functionality. Each of these inputs drives a floating optocoupler output as hardware feedback. These outputs can be used to disable the power on the motor power amplifier, dependent on the actual direction. One additional isolated 24V digital input is for free use by the software, for example as emergency stop input. A floating optical output can be controlled by software, for example as enable signal for the motor power amplifier.

A 16 bit digital to analog converter (DAC) produces a +/-10V controller output signal which can be used as speed or torque source for the power amplifier of the motor drive system. A galvanically isolation of this signal with the help of an isolation amplifier will be supplied as a transition module option.

A 12 bit analog to digital converter (ADC) with a configurable input voltage range is also available.
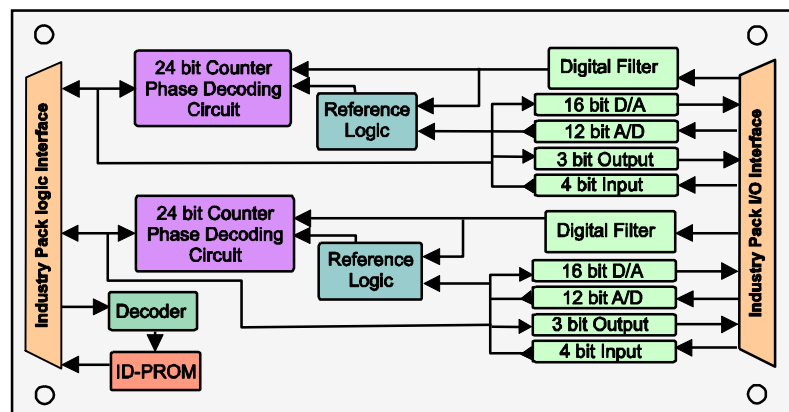
Figure 1-1 : Block Diagram

2 Technical Specification

2.1 TIP102-xx

Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995
ID ROM Data	Format I
I/O Space	Used without wait states
Memory Space	Not used
Interrupts	Interrupt 1 (IP signal INTREQ0#) for axis 1 Interrupt 2 (IP signal INTREQ1#) for axis 2
DMA	Not supported
Clock Rate	8 MHz
Module Type	Type I
Number of Axes	TIP102-1x: 1 axis TIP102-2x: 2 axes
Encoder Interface	Incremental encoder interface with 24 bit up/down counter
Input Count Frequency	Up to 2 MHz
Analog Input	1 ADC per axis, 12 bit, 10µs, input voltage +/-10V
Analog Input Overvoltage	Protection up to 25Vpp
Analog Output	1 DAC per axis, 16 bit, output voltage +/-10V
Analog Output Current	+/-5mA
Digital Inputs	5 inputs per axis TTL level
Digital Outputs	2 outputs per axis TTL level
External Trigger	TTL input and TTL output
Interface Connector	50-conductor flat cable
Power Requirements	25mA @ +5V DC 50mA @ +12V DC 45mA @ -12V DC
Temperature Range	Operating -40° C to +85 °C Storage -45°C to +125°C
MTBF	TIP102-1x : 698000 h TIP102-2x : 561000 h
Humidity	5 – 95 % non-condensing
Weight	28 g
Transition Module	TIP102-TM-xx is required, provides signal conditioning and optional isolation of digital and analog I/O signals

Figure 2-1 : Technical Specification TIP102-xx

2.2 Transition Module TIP102-TM-xx

Board Data	
Size	1 VME slot (6U)
Number of Axes	1 axis for TIP102-1x 2 axes for TIP102-2x
Encoder Interface	Signal level TTL or RS422 optional galvanically isolated
Analog Input	1 input per axis, input voltage +/-10V optional isolated (ADC on TIP102)
Analog Input Overvoltage	Overvoltage protection up to 100Vpp with galvanic isolation up to 12Vpp without galvanic isolation
Analog Output	1 output per axis, overvoltage +/-10V optional isolated (DAC device is located on TIP102)
Analog Output Current	+/-20mA with galvanically isolation +/-50mA without galvanically isolation
Digital Inputs per Axis (isolated)	General purpose input 24V DC Reference switch input 24V DC Limit switch 1 control input 24V DC Limit switch 2 control input 24V DC Encoder error input TTL (low active)
Digital Outputs per Axis (isolated)	Enable output 24V DC (+ "in position" LED indication)
Digital Outputs directly driven from Inputs per Axis (isolated)	Limit_Switch_1 Output 24V DC Limit_Switch_2 Output 24V DC
External Trigger	1 isolated TTL I/O per axis (jumper selectable input or output)
24V Output Load	Max. 1000 ohm
Physical data	
Power Requirements	TIP102-TM-1x : 100mA typical @ +5V DC (without load), <60mA typical @ ±12V DC (without load) TIP102-TM-2x : 180mA typical @ +5V DC (without load), <90mA typical @ ±12V DC (without load)
Temperature Range	Operating: 0° C to +70 °C Storage: -45°C to +125°C
MTBF	TIP102-TM-10: 1271000 h, TIP102-TM-11: 759000 h TIP102-TM-12: 1091000 h, TIP102-TM-13: 644000 h TIP102-TM-20: 867000 h, TIP102-TM-21: 488000 h TIP102-TM-22: 785000 h, TIP102-TM-23: 436000 h
Humidity	5 – 95 % non-condensing
Weight	TIP102-TM-1x: min. 150g TIP102-TM-2x: max. 250g

Figure 2-2 : Technical Specification TIP102-TM-xx

3 ID PROM Contents

Address	Function	Contents
0x01	ASCII 'I'	**0x49**
0x03	ASCII 'P'	**0x50**
0x05	ASCII 'A'	**0x41**
0x07	ASCII 'C'	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	TIP102-1x: **0x0A** TIP102-2x: **0x0B**
0x0D	Revision	**0x11**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x0C**
0x17	CRC	TIP102-1x: **0x9E** TIP102-2x: **0xFF**

Figure 3-1 : TIP102 V1.1 - ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP102 is accessible in the I/O space of the IP Module.

Address	Symbol	Description	Size (Bit)	Access
0x01	INPSR1	Input / Status Register	8	R/C
0x03	OUTCR1	Output Control Register	8	R/W
0x05	CNTDA1	Counter Data Register	8	R/W
0x07	CNTCS1	Counter Control / Status Register	8	R/W
0x08	DACDA1	DAC Data Register	16	W
0x0B	ADCCS1	ADC Control / Status Register	8	R/W
0x0C	ADCDA1	ADC Data Register	16	R
0x0F	CONCR1	Configuration Control Register	8	R/W
0x3F	INTVEC	Interrupt Vector Register	8	R/W

Figure 4-1 : Register Set TIP102-1x

On the TIP102-2x two axes motion controller, the second axis can be accessed through a second set of Control and Status Registers. Only the INTVEC Interrupt Vector Register is shared between both axes.

Address	Symbol	Description	Size (Bit)	Access
0x21	INPSR2	Input / Status Register	8	R/C
0x23	OUTCR2	Output Control Register	8	R/W
0x25	CNTDA2	Counter Data Register	8	R/W
0x27	CNTCS2	Counter Control / Status Register	8	R/W
0x28	DACDA2	DAC Data Register	16	W
0x2B	ADCCS2	ADC Control / Status Register	8	R/W
0x2C	ADCDA2	ADC Data Register	16	R
0x2F	CONCR2	Configuration Control Register	8	R/W

Figure 4-2 : Register Set TIP102-2x

4.2 Input and Status Register (INPSR)

The Input and Status Register INPSR1 (INPSR2) holds the actual status of all digital input lines as well as the status of the internal control logic (including interrupt generation, reference logic and digital filter).

Bit	Symbol	Description	Access	Reset Value
7	Interrupt Status	Interrupt Status 1 = corresponding axis has generated an interrupt request. Interrupts have to be enabled in the corresponding CONCR register first. Bit must be reset under software control by writing '1' to it. Bit is automatically cleared with the IP_RESET signal.	R/C	0
6	Refer. Done	Reference Logic Status 1 = the TIP102 reference function, which was started with a specific command in the corresponding CONCR register, has completed successfully. Bit must be reset under software control by a random write cycle to the corresponding CONCR. Bit is automatically cleared with the IP_RESET signal.	R/C	0
5	Encoder Error	Latched Encoder Error Status 1 = error in the timing of the encoder phase signals has been recognized or the encoder itself has reported an error. The source of this flag is the error detection logic within the digital filter for the encoder phase signals or the input of the encoder signal ENC_ERROR. Bit must be reset under software control by writing '1' to it. Bit is automatically cleared with the IP_RESET signal.	R/C	0
4	General Input	General Purpose Input 1 = input is active 0 = input is not active This status bit corresponds to the General-Purpose input (Pin 5) on the X102/202 connector of the TIP102-TM transition module.	R	
3	Trigger Input	External Trigger Input 1 = trigger input is active 0 = trigger input is not active This bit reflects the state of the external Trigger output switch (Pins 6 & 14) on the X102/202 connector of the TIP102-TM transition module. The bidirectional Trigger I/O signal must be configured as	R	

Bit	Symbol	Description	Access	Reset Value
		input when this bit is going to be used. The transition module TIP102-TM-xx has one set of isolated trigger I/O signals, which are jumper configurable as trigger input or trigger output (see chapter "Trigger I/O Jumper Configuration").		
2	Ref Switch	Reference Input (could also be used as another general purpose input) 1 = input is active 0 = input is not active This status bit corresponds to the Reference input (Pin 12) on the X102/202 connector of the TIP102-TM transition module.	R	
1	High Limit	High Limit Switch Control Input 1 = switch is activated 0 = switch is not activated This status bit corresponds to the Limit_Switch_2_Control input (Pin 4) on the X102/202 connector of the TIP102-TM transition module.	R	
0	Low Limit	Low Limit Switch Control Input 1 = switch is activated 0 = switch is not activated This status bit corresponds to the Limit_Switch_1_Control input (Pin 11) on the X102/202 connector of the TIP102-TM transition module.	R	

Figure 4-3 : Input and Status Register (INPSR)

4.3 Output Control Register (OUTCR)

The Output Control Register OUTCR1 (OUTCR2) controls the status of digital output signals.

Bit	Symbol	Description	Access	Reset Value
7:2		Not used	R	0
1		Status LED Bit controls the status of a LED located on the transition module. It can be read and written by software. This bit is automatically cleared with the IP_RESET signal.	R/W	0
0		Servo Amplifier Enable Bit controls the status of a floating optocoupler output which is normally connected to the enable input of the servo amplifier of the motor drive system. It can be read and written by software. This bit is automatically cleared with the IP_RESET signal.	R/W	0

Figure 4-4 : Output Control Register (OUTCR)

4.4 Counter Data Register (CNTDA)

The Counter Data Register CNTDA1 (CNTDA2) is the data I/O port to the LS7166 counter chip. It is used to the read counter position or to write a preset value. Because the LS7166 is a 24 bit counter, and the Data Register is only 8 bit wide, each data transfer needs three read or write cycles in sequence.

4.4.1 Reading Counter Data

The 24 bit data value of the counter can only be accessed through a 24 bit Output Latch (OL) internal the LS7166. The data is latched into the OL under software control by setting bit 1 in the counter MCR register to '1' (see chapter "Master Control Register") or by an external hardware signal (see chapter "External Trigger Input"). After that the data can be read through the CNTDA1 (CNTDA2) in three cycles in sequence. The transfer is least significant byte first, most significant byte last.

The access to the three data bytes within the Output Latch (OL) is controlled by an internal address pointer, which is automatically incremented with each read cycle. This pointer should be reset directly prior the three read cycles by setting bit 0 in the counter MCR register (see chapter "Master Control Register").

4.4.2 Writing Counter Data

The 24 bit counter can be loaded from a 24 bit Preset Register (PR) internal the LS7166. The preset data has to be written to the PR through the CNTDA1 (CNTDA2) in three cycles in sequence. The transfer is least significant byte first, most significant byte last. The data is then transferred to the counter under software control by setting bit 3 in the counter MCR register to '1' (see chapter "Master Control Register"), by the reference logic (see chapter "Reference Logic") or by an external hardware signal (see chapter "External Trigger Input").

The access to the three data byte within the Preload Register (PR) is controlled by an internal address pointer, which is automatically incremented with each read cycle. This pointer should be reset directly prior the three read cycles by setting bit 0 in the counter MCR register (see chapter "Master Control Register").

4.5 Counter Control and Status Register (CNTCS)

The Counter Control and Status Register of the TIP102 is an interface to the internal Control and Status Registers of the LS7166 Counter. These registers have a special addressing mode. They use the two most significant bits (Bit 7:6) of the data bus to decide which register receives the data.

For a better understanding of these internal registers they are presented in the following section.

4.5.1 Master Control Register (MCR)

A write to the Counter Control and Status Register CNTCS1 (CNTCS2) with bit 6 = '0' and bit 7 = '0' will be a write to the Master Control Register of the LS7166 counter chip.

Bit	Symbol	Description	Access
7		Write '0'	W
6		Write '0'	W
5		Master Reset 1 = perform a master reset on the LS7166 counter chip and put it into initial state	W
4		Reset COMPT 1 = clear the compare toggle flag COMPT	W
3		Transfer PR to CNTR 1 = transfer the previously loaded 24 bit data value into the counter (CNTR)	W
2		Reset of CNTR, BWT, CYT, Set SIGN Register 1 = set the counter (CNTR) data value to zero, clear the borrow- and carry-toggle flag and set the sign bit.	W
1		Transfer CNTR to OL 1 = latch the current 24 bit value of the counter (CNTR) into the OL register of the LS7166 counter chip for subsequent read-out. This bit can be combined with bit 0 to reset the OL address pointer at the same time.	W
0		Reset PR/OL address pointer 1 = reset the internal PR/OL address pointer of the LS7166 counter chip, which is used during reads and writes to the CNTDA1/CNTDA2 register to access the three bytes forming the 24 bit data word.	W

Figure 4-5 : Counter Master Control Register (MCR)

4.5.2 Input Control Register (ICR)

A write to the Counter Control and Status Register CNTCS1 (CNTCS2) with bit 6 = '1' and bit 7 = '0' will be a write to the Input Control Register of the LS7166 counter chip.

Bit	Symbol	Description	Access
7		Write '0'	W
6		Write '1'	W
5		Configuration LCTR/LLTC pin of the LS7166 1 = event will latch the actual counter data value into the OL register. 0 = event (reference or external trigger) will load the counter with the contents of the PR register. On the TIP102 this pin is controlled by the reference and external trigger logic (see chapter "Functional Description").	W
4		Configuration ABGT/RCTR **Bit must always be set to '0' for the operation of the TIP102-xx.**	W
3		A/B Input Enable 1 = enable A and B counter inputs 0 = disable all counting functions **For standard motion controller application of the TIP102 the counter should be always enabled.**	W
2		Decrement Counter once 1 = decrement the counter data value by one	W
1		Increment Counter once 1 = increment the counter data value by one	W
0		A/B Input Mode 1 = define A as count input and B as count direction input with B='0' for up and B='1' for down 0 = define A as up count input and B as down count input **In a standard motion controller application the TIP102 will operate with an incremental encoder and the counter chip LS7166 programmed to quadrature mode by configuring the QR register (see chapter "Quadrature Register"). In this case the A/B input mode bit has no function.**	W

Figure 4-6 : Counter Input Control Register (ICR)

4.5.3 Output Control Register (OCR)

A write to the Counter Control and Status Register CNTCS1 (CNTCS2) with bit 6 = '0' and bit 7 = '1' will be a write to the Output Control Register of the LS7166 counter chip.

> **For the standard motion controller application of the TIP102 the bits 1 to 3 of this register must always be programmed as '0'.**

Bit	Symbol	Description	Access
7		Write '1'	W
6		Write '0'	W
5:4		Input Trigger mode On TIP102 the output pin 16 of the LS7166 counter chip can be used for interrupt and output trigger impulse generation. 00 = CY# signal (carry) 01 = CYT signal (carry toggle flip flop) 10 = CY signal (carry) 11 = COMP# signal (compare)	W
3:1		Normal count mode	W
0		Binary / BCD mode 1 = BCD mode 0 = **binary mode, should be the normal case**	W

Figure 4-7 : Counter Output Control Register (OCCR)

4.5.4 Quadrature Register (QR)

A write to the Counter Control and Status Register CNTCS1 (CNTCS2) with bit 6 = '1' and bit 7 = '1' will be a write to the Quadrature Register of the LS7166 counter chip.

> **Because the TIP102 was designed to decode quadrature signals of encoders, one of the modes x1, x2 or x4 must be selected for standard operation of the module. Bit 2 to 5 are don't cares.**

Bit	Symbol	Description	Access
7		Write '1'	W
6		Write '1'	W
5:2		Don't care bits	-
1:0		Quadrature mode of the corresponding LS7166 00 = disable quadrature mode 01 = enable x1 quadrature mode 10 = enable x2 quadrature mode 11 = enable x4 quadrature mode	W

Figure 4-8 : Quadrature Register (QR)

4.5.5 Output Status Register (OSR)

A read of the Counter Control and Status Register CNTCS1 (CNTCS2) will be a read of the Output Status Register of the LS7166 counter chip.

Bit	Symbol	Description	Access
7:5		Not used	-
4		UP / DOWN - Count direction indicator in quadrature mode. 0 = when counting down 1 = when counting up	R
3		Sign Bit 0 = when CNTR underflows 1 = when CNTR overflows	R
2		Compare Toggle Flip-Flop: Toggles every time CNTR equals PR.	R
1		Carry Toggle Flip-Flop: Toggles every time CNTR overflows.	R
0		Borrow Toggle Flip-Flop: Toggles every time CNTR underflows.	R

Figure 4-9 : Output Status Register (OSR)

4.6 DAC Data Register (DACDA)

The DAC Data Register DACDA1 (DACDA2) is the write only data register for the ±10V controller output signal of the TIP102. The 2's complement value written into this register is converted to the corresponding output voltage with a range of ±10V.

Bit	Symbol	Description	Access
15	Sign	16 bit DAC data in 2's complement.	W
14:0	Data	Only 16 bit access is supported for this register. A read to this register will return random data.	

Figure 4-10: DAC Data Register (DACDA)

4.7 ADC Control and Status Register (ADCCS)

The ADC Control and Status Register ADCCS1 (ADCCS2) controls the function of the 12 bit ADC.

A data conversion is started by a write cycle to the ADCCS1 (ADCCS2). However the data value of this write is a don't care.

As long as the ADC is busy converting the bit 0 of the ADCCS1 (ADCCS2) will read as '1'.

Bit	Symbol	Description	Access
7:1		These unused bits will be read as '0'.	R/W
0	ADC Busy	ADC Busy 1 = ADC is busy	R/W

Figure 4-11: ADC Control and Status Register (ADCCS)

> **The unused bits 1 to 7 will always be read as '0' when reading the ADC Control and Status Register ADCCS1 (ADCCS2).**

> **After power up the ADC is in a random state and requires two dummy conversions before operating correctly. This is based on the chip design of the ADC. All drivers from TEWS TECHNOLOGIES already include these two dummy conversions.**

4.8 ADC Data Register (ADCDA)

The ADC Data Register ADCDA1 (ADCDA2) holds the conversion result of the 12 bit ADC. It is left shifted by the hardware so the software reads a 16 bit 2's complement value.

Bit	Symbol	Description	Access
15	Sign	12 bit ADC Data in 2's complement, shifted to register bits 15:4.	R
14:4	Data	Only 16 bit access is supported for this register.	
3:0		These unused bits will be read as '0'.	

Figure 4-12: ADC Data Register (ADCDA)

4.9 Configuration Control Register (CONCR)

The Configuration Control Register CONCR1 (CONCR2) controls the operation mode of the reference logic, the encoder configuration and interrupt generation.

> **Writing to this register will clear the reference done flag (bit 6) in the Input and Status Register INPSR1 (INPSR2).**
>
> **The unused bits 5 to 7 will be read as '0' when reading the Configuration Control Register CONCR1 (CONCR2).**

Bit	Symbol	Description	Access	Reset Value
7:5		Not used	-	0
4		Interrupt Enable 1 = a transition on the CY output of the LS7166 counter chip will generate an interrupt. Bit is automatically cleared with the IP_RESET signal.	R/W	0
3		Encoder Difference Signal 1 = enables the analysis of the differential phase signal of a RS422 encoder in the digital filter. In this mode broken encoder wire will be detected and the Encoder Error Status will be set in the Input and Status Register if such an error occurs. **This function requires a transition module with the isolated encoder input option.** Bit is automatically cleared with the IP_RESET signal.	R/W	0
2		Auto Reference Enable 1 = enable This will automatically repeat the selected function of the reference logic and external trigger (bit 0 and bit 1). Bit is automatically cleared with the IP_RESET signal.	R/W	0
1:0		Reference Mode 00 = None - reference logic is disabled 01 = Without reference switch - zero signal of the encoder will trigger the load counter input of the LS7166 counter chip. 10 = With reference switch - zero signal of the encoder is combined with the reference switch input to produce the load counter signal for the LS7166 counter chip. 11 = External trigger - external input signal will generate the load counter pulse to the LS7166 counter chip. For more information see chapter "Reference Logic". These bits will be cleared automatically, when the reference condition or external trigger occurs and bit 2 is not set. Bits are automatically cleared with the IP_RESET signal.	R/W	0

Figure 4-13: Configuration Control Register (CONCR)

4.10 Interrupt Vector Register (INTVEC)

The Interrupt Vector Register INTVEC is a byte wide read/write register. It is shared between both axes, but both axes will create an individual interrupt through the corresponding INTREQx line.

For an interrupt from axis # 1 bit 0 of the interrupt vector will read as '0', for an interrupt from axis #2 it will read as '1'. This is controlled via the IP_ADDRESS line 1.

Example: If the Interrupt Vector Register is loaded with '0x60', axis # 1 will create an interrupt at vector '0x60' and axis # 2 will create an interrupt at vector '0x61'.

Bit	Symbol	Description	Access	Reset Value
7:1		Interrupt Vector loaded by software	R/W	0
0		Interrupt from Axis 1 or 2 1 = interrupt from axis 2 0 = interrupt from axis 1	R/W	0

Figure 4-14: Interrupt Vector Register (INTVEC)

Axis #1 is using the INTREQ0 and axis #2 is using the INTREQ1 interrupt request line of the IP bus.

5 Functional Description

5.1 Quadrature modes of the LS7166

5.1.1 Mode x1

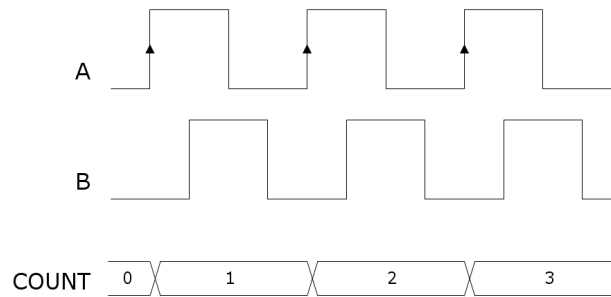In this mode, only the positive edges of the encoder phase signal "A" are counted.

Figure 5-1: LS7166 - Quadrature Mode x1

5.1.2 Mode x2

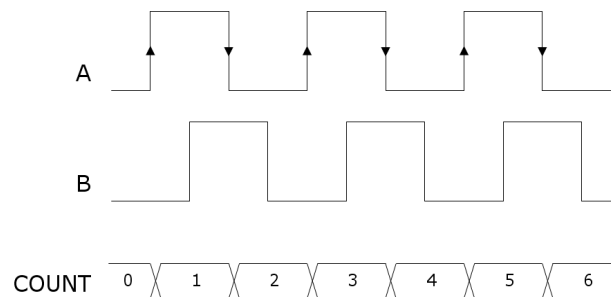In this mode, the positive and also the negative edges of the encoder phase signal "A" are counted.

Figure 5-2: LS7166 - Quadrature Mode x2

5.1.3 Mode x4

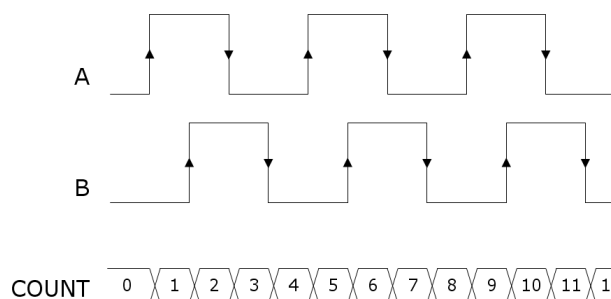In this mode, both edges of both encoder phase signals "A" and "B" are counted.

Figure 5-3: LS7166 - Quadrature Mode x4

5.2 Reference Logic

Due to the nature of measurement systems with incremental encoders, the absolute position of the axes is unknown when the system is powered up. The system has to run through a reference procedure to calibrate the measurement system, in that case the counter, with an absolute position.

The TIP102 has a reference logic, which allows several modes of operation for the reference procedure. The reference logic generates a signal to the load counter input of the LS7166 when the reference condition occurs. This signal will either preset the counter with a value that was previously loaded into the Preset Register of the counter chip, or load the actual value of the counter to the Output Latch of the counter chip, depending on the configuration of the LCTR/LLTC bit in the Input Control Register (ICR).

The desired mode of operation for the reference logic is selected by programming the corresponding bits in the Configuration Control Register (CONCR). An impulse diagram of these modes is sketched in figure 5-1.

5.2.1 Reference Mode - without reference switch

In this mode, the next occurrence of the zero (index) signal of the encoder is used as the source for the reference condition and, therefore, for the load counter signal. Because an incremental encoder usually creates a zero (index) pulse at each turn, this mode is only useful if the absolute position of the next zero (index) pulse is known, or if there is only one such pulse in the operating range of the axis.

5.2.2 Reference Mode - with reference switch

This mode also uses the zero (index) signal of the encoder to generate the reference condition. But it takes an additional Reference Switch (which is an input to the TIP102) to select a single zero (index) signal.

The reference condition in this mode is defined as the first zero (index) pulse of the encoder after a '0' to '1' transition of the reference switch, with the reference switch still in the '1' state.

5.2.3 External Trigger Input

The TIP102 has a trigger input signal ("TRIGGER_INPUT"). This signal can also be used to generate the reference condition.

> **The transition module TIP102-TM-xx has only one set of isolated TRIGGER I/O signals, which is jumper configurable as Trigger Input or Trigger Output (see also chapter "Trigger I/O Jumper Configuration").**

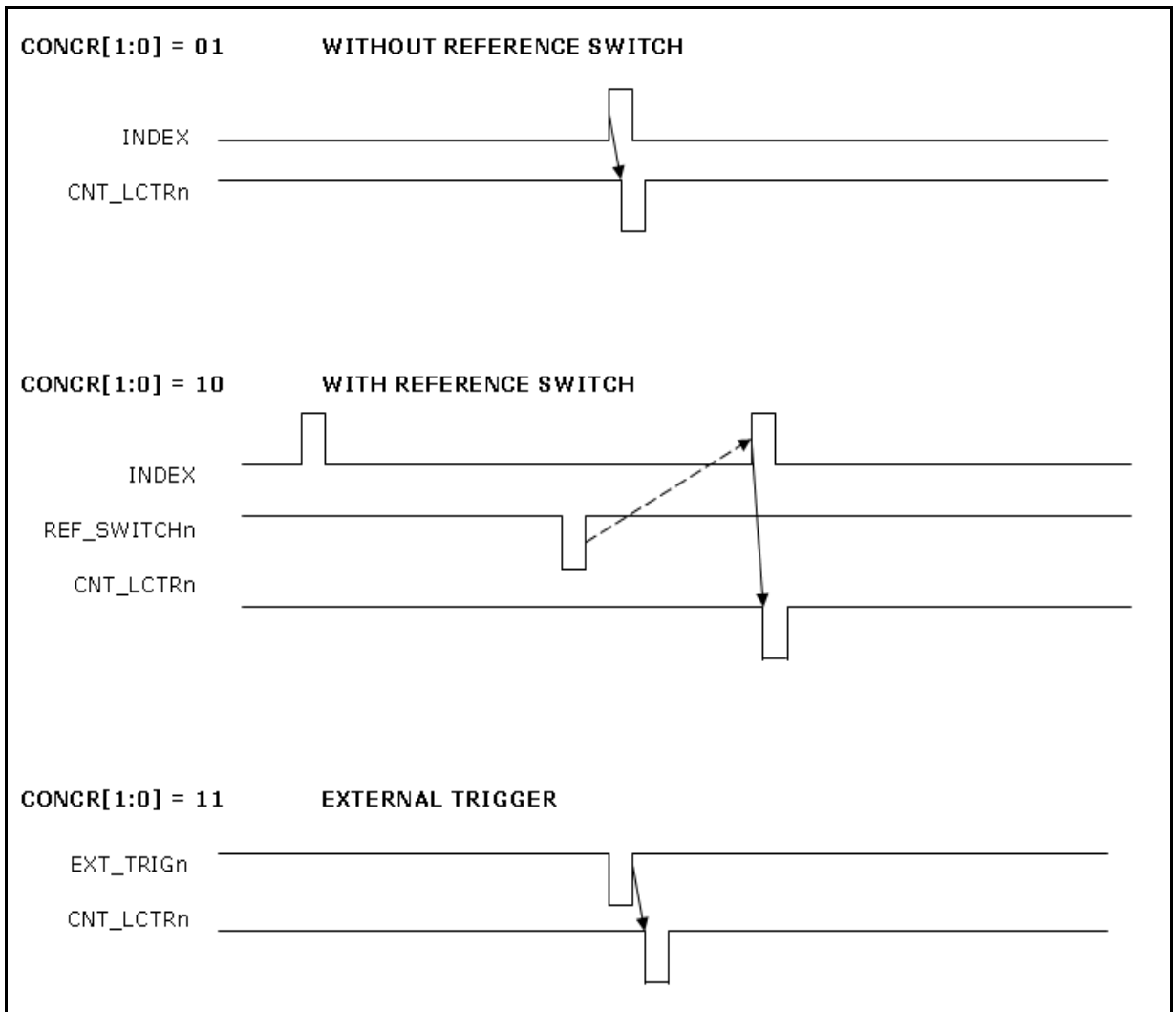The following figure shows the reference modes of the TIP102 in detail:

Figure 5-4: Reference modes of the TIP102

6 Programming Hints

6.1 LS7166 Counter

The following section is intended to give hints on how to initialize the LS7166 counters. This is important because without the proper initialization they cannot operate in the intended way.

> **It is important to initialize the counters first and enable the interrupts in the CONCR afterwards. Otherwise, interrupts might be generated randomly!**

6.1.1 Initialization

The LS7166 counter of the TIP102 requires some basic initialization, before it is able to decode the quadrature counting pulses of the incremental encoder. The following data sequence has to be loaded into the CNTCS1 (CNTCS2) Counter Control and Status Register, in order to initialize it:

- write 0x20 to CNTCS1 (CNTCS2)

  select the counter MCR register, perform a master reset on the LS7166 counter chip

- write 0x48 to CNTCS1 (CNTCS2)

  select the counter ICR register, enable data inputs A/B, configure pin 3 as counter load input (required for the reference logic)

- write 0xB0 to CNTCS1 (CNTCS2)

  select the counter OCCR register, configure pin 16 as compare result output (required for generation of interrupts at defined counter data values)

- write 0xC1, 0xC2 or 0xC3 to CNTCS1 (CNTCS2)

  select the counter QR register, enable quadrature decoding mode X1, X2 or X4

After this initialization, the counter will begin decoding the encoders' quadrature signals.

6.1.2 Reading actual counter data value

The LS7166 has a 24 bit up/down counter. However, the data path to the LS7166 is only 8 bit wide. To read the 24 bit counter data value (8 bit at a time), the following sequence must be programmed:

- write 0x03 to CNTCS1 (CNTCS2)

  select the counter MCR register, latch the actual counter data value into the Output Latch (OL), reset the OL address pointer

- read CNTDA1 (CNTDA2)

  read data byte 0 (LSB), increment OL address pointer

- read CNTDA1 (CNTDA2)

  read data byte 1, increment OL address pointer

- read CNTDA1 (CNTDA2)

> read data byte 2, increment OL address pointer

If the data bytes 0 to 2 are assembled into a 32 bit word the sign bit of the counter has to be extended for further processing, which means bit 7 of data byte 2 into the upper 8 bits of the 32 bit word.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	E	E	E	E	E	E	S																								

BYTE 2   BYTE 1   BYTE 0
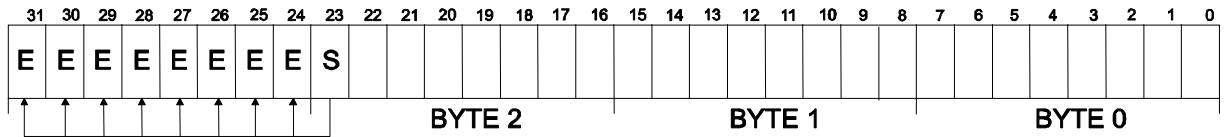
7 Jumper Configurations

7.1 TIP102-xx IP Module

There are no jumpers on the TIP102-xx IP Module! Do never place any jumper on the 8 pin connector block of the TIP102-xx IP Module! This block is solely used for manufacturing and testing purposes.

7.2 TIP102-TM-xx Transition Module

7.2.1 Trigger I/O Jumper Configuration

The Trigger I/O signals at connector X102 (X202) of the transition module must be configured to input or output by the jumper J1 (J200) at the transition module.
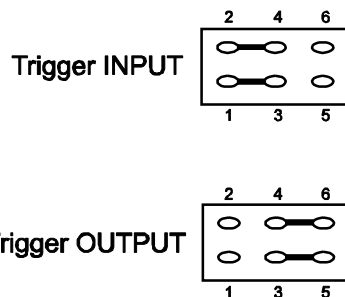
Figure 7-1 : Jumper J1 (J200) configuration for trigger input and output

7.2.2 Encoder Input Jumper Configuration

The TIP102-TM-10 and TIP102-TM-20 transition modules have jumpers to enable or disable the PHASE_A, PHASE_B and INDEX encoder inputs.

If the encoder provides the PHASE_A, PHASE_B and INDEX signals the jumper J2, J3 and J4 (J201, J202 and J203) must be jumpered between pin 1 and 2.

If the encoder does **not** provide the PHASE_A, PHASE_B and INDEX signals the jumper J2, J3 and J4 (J201, J202 and J203) must be jumpered between pin 2 and 3.

7.2.3 TIP102-TM-xx Jumper Layout

Figure 7-2 : Jumper J1 (J200) configuration for trigger output

The jumpers J2, J3 and J4 (J201, J202 and J203) are only present at the TIP102-TM-10 (TIP102-TM-20) transition module.

8 Pin Assignment – I/O Connector

8.1 I/O Connection of TIP102-xx

8.1.1   50 pin IP I/O Connector

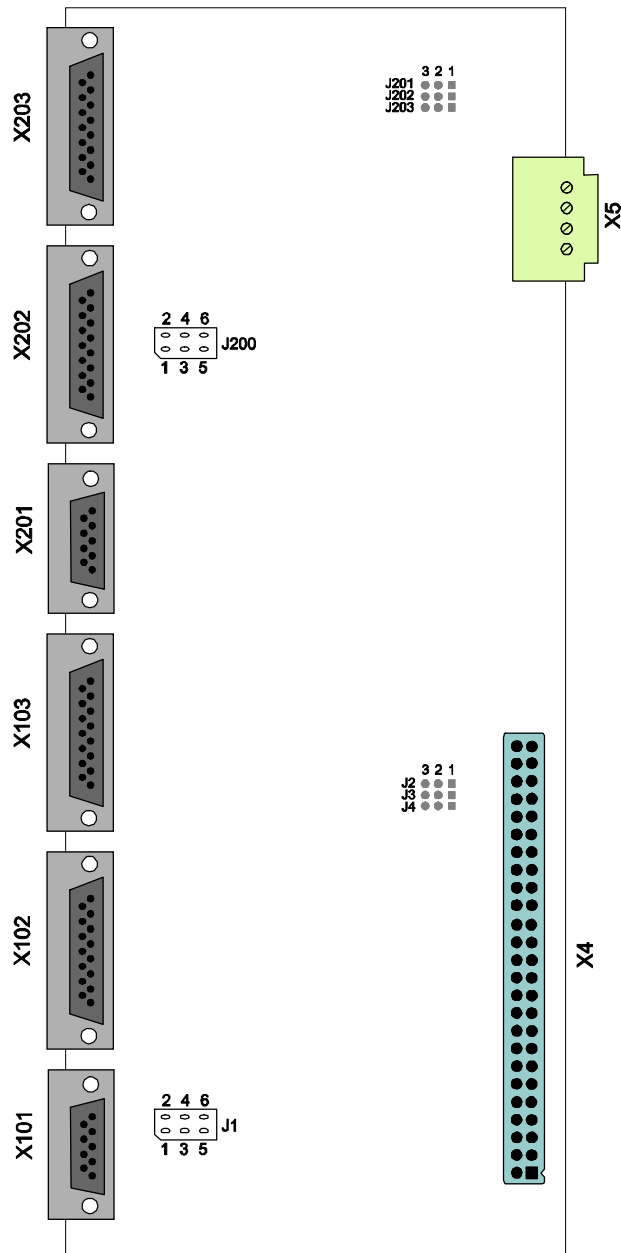| Pin	I/O (Level)	Function	Pin	I/O (Level)	Function
1		+5V (V$_{CC}$)	26	Input	Encoder_Phase_B_Axis_1+
2		+5V (V$_{CC}$)	27	Input	Encoder_Phase_A_Axis_1-
3		GND	28	Input	Encoder_Phase_A_Axis_1+
4		GND	29	Output	Status_LED_Axis_2
5		+12V	30	Output	Servo_Amp_Enable_Axis_2
6		-12V	31		GND
7	Output	Status_LED_Axis_1	32	± 10V (In)	DAC_Output_Axis_2
8	Output	Servo_Amp_Enable_Axis_1	33		DAC_GND
9		GND	34	± 10V (Out)	ADC_Input_Axis_2
10	± 10V (In)	DAC_Output_Axis_1	35		ADC_GND
11		DAC_GND	36		GND
12	± 10V (Out)	ADC_Input_Axis_1	37	Input	Trigger_Input_Axis_2#
13		ADC_GND	38	Output	Trigger_Output_Axis_2#
14		GND	39	Input	General_Input_Axis_2#
15	Input	Trigger_Input_Axis_1#	40	Input	Reference_Switch_Axis_2#
16	Output	Trigger_Output_Axis_1#	41	Input	High_Limit_Switch_Axis_2#
17	Input	General_Input_Axis_1#	42	Input	Low_Limit_Switch_Axis_2#
18	Input	Reference_Switch_Axis_1#	43	Input	Encoder_Error_Axis_2#
19	Input	High_Limit_Switch_Axis_1#	44		NC
20	Input	Low_Limit_Switch_Axis_1#	45	Input	Encoder_Index_Axis_2-
21	Input	Encoder_Error_Axis_1#	46	Input	Encoder_Index_Axis_2+
22		NC	47	Input	Encoder_Phase_B_Axis_2-
23	Input	Encoder_Index_Axis_1-	48	Input	Encoder_Phase_B_Axis_2+
24	Input	Encoder_Index_Axis_1+	49	Input	Encoder_Phase_A_Axis_2-
25	Input	Encoder_Phase_B_Axis_1-	50	Input	Encoder_Phase_A_Axis_2+

Figure 8-1 : 50 pin IP I/O Connector TIP102-xx

8.2 Transition Module I/O Connectors (TIP102-TM-xx)

8.2.1 X101/X201 - DB9 female - Servo Amplifier Signals

Pin	Function	Signal Level	Comment
1	Current_Limit_Switch_1+		Current Limit Switch 1 (floating optocoupler output transistor collector pin) See also pin 6. The switch state is controlled by the matching control input on X102/202 (Pin 11).
2	Current_Limit_Switch_2+		Current Limit Switch 2 (floating optocoupler output transistor collector pin) See also pin 7 The switch state is controlled by the matching control input on X102/202 (Pin 4).
3	Enable_Switch+		Enable Switch (floating optocoupler output transistor collector pin) See also pin 8. The switch state is controlled by OUTCR register bit 0.
4	Shield		
5	DAC_GND		Analog output ground reference See also pin 9.
6	Current_Limit_Switch _1-		Current Limit Switch 1 (floating optocoupler output transistor emitter pin) See also pin 1. The switch state is controlled by the matching control input on X102/202 (Pin 11).
7	Current_Limit_Switch _2-		Current Limit Switch 1 (floating optocoupler output transistor emitter pin) See also pin 2. The switch state is controlled by the matching control input on X102/202 (Pin 4).
8	Enable_Switch-		Enable Switch (floating optocoupler output transistor emitter pin) See also pin 3. The switch state is controlled by OUTCR register bit 0.
9	DAC_Output	+/-10V	Analog output See also pin 5.

Figure 8-2 : X101/X201 - DB9 female - Servo Amplifier Signals

8.2.2 X102/X202 - DB15 male - Power and I/O Signals

Pin	Signal	Level	Comment
1	ENC_VCC		Encoder power supply (source) Direct on-board connection to X103/203 pins 1 & 9 Connect to power supply.
2	ENC_VCC_SENSE		Encoder power supply sense (source) Direct on-board connection to X103/203 pin 3 Connect to power supply sense input (if applicable).
3	Shield		
4	Limit_Switch_2_Control Input	24V	24V control input to activate the Current_Limit_Switch_2 on X101/201 State readable in INPSR register bit 1
5	General_Purpose Input	24V	General purpose 24V input State readable in INPSR register bit 4
6	Trigger_I/O+	Input Configuration: TTL	Bidirectional Trigger I/O signal, direction is configured by jumper See also pin 14. TTL Input configuration : Anode of photodiode When configured as input, the status of this input is reflected by INSPR register bit 3. Output switch configuration : Floating optocoupler output transistor collector pin
7	Shield		
8	ADC_GND		Analog input ground reference See also pin 15.
9	ENC_GND		Encoder power supply ground (source) Direct on-board connection to X103/203 pins 2 & 10 Connect to power supply ground.
10	ENC_GND_SENSE		Encoder power supply sense ground (source) Direct on-board connection to X103/203 pin 11 Connect to power supply sense ground input (if applicable).
11	Limit_Switch_1_Control Input	24V	24V control input to activate the Current_Limit_Switch_1 on X101/201 State readable in INPSR register bit 0
12	Reference Input	24V	Reference 24V Input State readable in INPSR register bit 2

Pin	Signal	Level	Comment
13	Common Return of Input Signals	24V Common Return	Common Return Signal of the following 24V Inputs : General Purpose Input 1 (Pin 12) General Purpose Input 2 (Pin 5) Limit_Switch_1_Control_Input (Pin 11) Limit_Switch_2_Control_Input (Pin 4)
14	Trigger_I/O-	Input Configuration: TTL	Bidirectional Trigger I/O signal Direction is configured by jumper. See also pin 6. TTL Input configuration: Anode of photodiode When configured as input, the status of this input is reflected by INSPR register bit 3. Output switch configuration : Floating optocoupler output transistor collector pin
15	ADC Input	+/-10V	Analog Input See also Pin 8.

Figure 8-3 : X102/X202 - DB15 male - Power and I/O Signals

8.2.3 X103/X203 - DB15 female - Encoder Signals

Pin	Signal	Level	Comment
1	ENC_VCC		Encoder Power Supply Connect to Encoder
2	ENC_GND		Encoder Power Supply Ground Connect to Encoder
3	ENC_VCC_SENSE		Encoder Power Supply Sense Connect to Encoder (if applicable)
4	NC		
5	INDEX-	TTL or RS422 -	Encoder Index Line Connect to Encoder
6	PHASE_B-	TTL or RS422 -	Encoder Phase B Line Connect to Encoder
7	PHASE_A-	TTL or RS422 -	Encoder Phase A Line Connect to Encoder
8	Shield		
9	ENC_VCC		Encoder Power Supply. Connect to Encoder
10	ENC_GND		Encoder Power Supply Ground Connect to Encoder
11	ENC_GND_SENSE		Encoder Power Supply Sense Ground Connect to Encoder (if applicable)
12	ENC_ERROR#	TTL	Encoder Error Input Connect to Encoder (if applicable) State readable in INPSR register bit 5
13	INDEX+	TTL or RS422+	Encoder Index Line Connect to Encoder
14	PHASE_B+	TTL or RS422+	Encoder Phase B Line Connect to Encoder
15	PHASE_A+	TTL or RS422 +	Encoder Phase A Line Connect to Encoder

Figure 8-4 : X103/X203 - DB15 female - Encoder Signals