The Embedded I/O Company

TEWS TECHNOLOGIES

TIP116

4 Channel Quadrature /

General Purpose Counter

Version 1.0

User Manual

Issue 1.0.4

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TIP116-10

4 Channel Quadrature / General Purpose Counter

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
-	Preliminary Issue	March 2003
1.0	First Issue	July 2003
1.1	Revision Update, added OVFL & ROVFL bits	April 2004
1.2	New address TEWS LLC	September 2006
1.3	Interrupt clarification, Quadrature count clarification	January 2007
1.0.4	New notation for HW Engineering Documentation Releases	March 2010

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1 Product Description

The TIP116 IndustryPack® compatible module is primarily designed for motion control applications, but it is also applicable as general purpose counter.

The TIP116 offers four channel quadrature / general purpose counter. Each channel consists of a 32 bit programmable counter, a 32 bit preload register, a 32 bit compare register and a 32 bit data register. The 32 bit counter can be programmed for quadrature, up-/down or direction count. In quadrature count mode the counter is programmable for single, double and quadruple analysis of the encoder signals. Two special count modes are available, a cycling 'Divide-by-N' mode and a 'Single-Cycle' mode.

Additionally four control modes are available via the Z-input. The Z-input can be programmed to load, latch or reset the counter or it can be used as a gate for the counter clock.

The level of the three input signals per channel can be RS422 or TTL. The input signals pass a digital filter for noise suppression before they are fed into the counter.

The TIP116 also provides one RS422 general purpose I/O. It can be configured as a programmable 1, 2, 4 or 8 MHz clock output, as input to simultaneous latch the counters of all channels or as general purpose input/output.

A 16 bit down-counter with preload register acts as an interval timer and allows timing intervals of up to 65ms. It can be used as reference timer for closed loop applications.

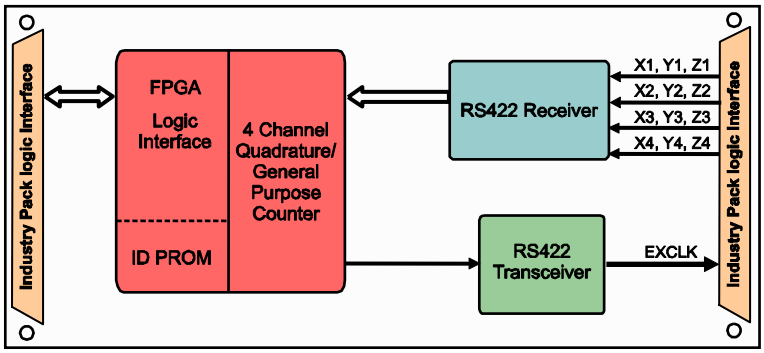

Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I	
I/O Space	Used / no wait states	
Memory Space	Not used	
Interrupts	Int0 used / Int1 not used	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
I/O Interface		
Number of Channels	4 channels with 3 input lines per channel	
Input Levels	RS422 differential and TTL single-ended	
Input Frequency	DC to 4 MHz	
General Purpose I/O	1 RS422 I/O, configurable as programmable 1, 2, 4 or 8 MHz clock output, simultaneous counter latch or general purpose input/output	
Internal Interface		
Interval Timer	Programmable with timing intervals up to 65ms	
Interface Connector	50-conductor flat cable	
Power Requirements	65mA typical @ +5V DC	
Physical Data		
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	823000 h	
Humidity	5 – 95 % non-condensing	
Weight	26 g	

Table 2-1 : Technical Specification

3 ID Prom Contents

Address	Function	Contents
0x01	ASCII ‘I’	**0x49**
0x03	ASCII ‘P’	**0x50**
0x05	ASCII ‘A’	**0x41**
0x07	ASCII ‘C’	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x37**
0x0D	Revision	**0x11**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x0C**
0x17	CRC	**0x19**
0x19 – 0x3F	Not used	**0x00**

Table 3-1 : ID PROM Contents

4 IP Addressing

The TIP116 is controlled by a set of registers, which are directly accessible in the I/O address space of the IP module.

All register of the TIP116 are word (16 bit) or byte (8 bit) accessible (big endian).

4.1 I/O Address Map

Address	Symbol	Size	Bits	Description	Access
0x00	CPR1_HI	word	[31…16]	Counter Preload Register Channel 1	R/W
0x02	CPR 1_LO	word	[15…0]		
0x04	CCP1_HI	word	[31…16]	Counter Compare Register Channel 1	R/W
0x06	CCP 1_LO	word	[15…0]		
0x08	CDR1_HI	word	[31…16]	Counter Data Register Channel 1	R
0x0A	CDR1_LO	word	[15…0]		
0x0C	CONT1	word	[15…0]	Channel Control Register Channel 1	R/W
0x0F	CSR1	byte	[7…0]	Channel Status Register Channel 1	R
	CCR1			Channel Command Register Channel 1	W
0x10	CPR 2_HI	word	[31…16]	Counter Preload Register Channel 2	R/W
0x12	CPR 2_LO	word	[15…0]		
0x14	CCP 2_HI	word	[31…16]	Counter Compare Register Channel 2	R/W
0x16	CCP 2_LO	word	[15…0]		
0x18	CDR2_HI	word	[31…16]	Counter Data Register Channel 2	R
0x1A	CDR2_LO	word	[15…0]		
0x1C	CONT2	word	[15…0]	Channel Control Register Channel 2	R/W
0x1F	CSR2	byte	[7…0]	Channel Status Register Channel 2	R
	CCR2			Channel Command Register Channel 2	W
0x20	CPR 3_HI	word	[31…16]	Counter Preload Register Channel 3	R/W
0x22	CPR 3_LO	word	[15…0]		
0x24	CCP 3_HI	word	[31…16]	Counter Compare Register Channel 3	R/W
0x26	CCP 3_LO	word	[15…0]		
0x28	CDR3_HI	word	[31…16]	Counter Data Register Channel 3	R
0x2A	CDR3_LO	word	[15…0]		
0x2C	CONT3	word	[15…0]	Channel Control Register Channel 3	R/W
0x2F	CSR3	byte	[7…0]	Channel Status Register Channel 3	R
	CCR3			Channel Command Register Channel 3	W
0x30	CPR 4_HI	word	[31…16]	Counter Preload Register Channel 4	R/W
0x32	CPR 4_LO	word	[15…0]		
0x34	CCP 4_HI	word	[31…16]	Counter Compare Register Channel 4	R/W
0x36	CCP 4_LO	word	[15…0]		

Address	Symbol	Size	Bits	Description	Access
0x38	CDR4_HI	word	[31…16]	Counter Data Register Channel 4	R
0x3A	CDR4_LO	word	[15…0]		
0x3C	CONT4	word	[15…0]	Channel Control Register Channel 4	R/W
0x3F	CSR4	byte	[7…0]	Channel Status Register Channel 4	R
	CCR4			Channel Command Register Channel 4	W
0x41	GCR	byte	[7…0]	Global Control/Status Register	R/W
0x43	GPCR	byte	[7…0]	General Purpose I/O Control Register	R/W
0x45	IVEC	byte	[7…0]	Interrupt Vector Register	R/W
0x46	ICR	word	[15…0]	Interrupt Control Register	R/W
0x48	ISR	word	[15…0]	Interrupt Status Register	R/W
0x4B	ITCR	byte	[7…0]	Interval Timer Control Register	R/W
0x4C	ITPRE	word	[15…0]	Interval Timer Preload Register	R/W
0x4E	ITDR	word	[15…0]	Interval Timer Data Register	R
0x50	GISR	word	[15…0]	Global Input Status Register	R

Table 4-1 : Register Set

5 Register Description

The functional description of all registers which are accessed as two 16 bit registers (HI/LO) is combined in a 32 bit register.

5.1 Register Set for Counter Channel 1-4

Each of the four counter channels has a register set of the following six registers.

5.1.1 Counter Preload Register

Bit	Symbol	Description	Access	Reset Value
31:0	CPR	Counter Preload Register The value of this register can be loaded into the counter by: - Setting bit 4 (LCNT) of the Channel Command Register - An impulse on the Z-input when the 'Load on Z'-mode is active - Automatically in the 'Divide-by-N'-mode every time the counter creates a borrow or a carry	R/W	0

Table 5-1 : Counter Preload Register

5.1.2 Counter Compare Register

	Symbol	Description	Access	Reset Value
31:0	CCP	Counter Compare Register Every time the counter matches the Counter Compare Register value, bit 2 (MAT) of the Channel Status Register is set to '1' and, if enabled, an interrupt is generated.	R/W	-1

Table 5-2 : Counter Compare Register

5.1.3 Counter Data Register

Bit	Symbol	Description	Access	Reset Value
31:0	CDR	Counter Data Register This Register contains the Counter Data Value. A read access to the high-word or the highest byte of this register, a 'Latch on Z' or a Simultaneous Counter Latch loads the current counter value into the Counter Data Register. The content of this register is then locked until the lower word or the lowest byte is read. The locking of this register can be observed in the Status Register. When bit 5 (CDLK) of the Channel Status Register is set to '1', this register is locked. The locking of this register can be released manually by writing a '1' to bit 5 (RCDLK) of the Channel Command Register.	R	0

Table 5-3 : Counter Data Register

5.1.4 Channel Control Register

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>15:12</td><td>-</td><td>Reserved</td><td>-</td><td>0</td></tr>
<tr><td>11:9</td><td>POL [2:0]</td><td>Z,Y,X Polarity
The Input Polarity Control can be used to adapt the input to the input source polarity.
<table>
<tr><th>Bit</th><th>Input</th><th>Polarity</th></tr>
<tr><td>11</td><td>Z</td><td>0 = high active, 1 = low active</td></tr>
<tr><td>10</td><td>Y</td><td>0 = high active, 1 = low active</td></tr>
<tr><td>9</td><td>X</td><td>0 = high active, 1 = low active</td></tr>
</table></td><td>R/W</td><td>000</td></tr>
<tr><td>8:7</td><td>QUAD [1:0]</td><td>Quadrature Control
The quadrature inputs can be interpreted as 1x, 2x, or 4x counting.
<table>
<tr><td>0x</td><td>1x</td></tr>
<tr><td>10</td><td>2x</td></tr>
<tr><td>11</td><td>4x</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
<tr><td>6:4</td><td>ZCM [2:0]</td><td>Z Control Mode
The Z Control Mode determines how the counter interprets events on the Z-input.
<table>
<tr><td>000</td><td>No Z-Control</td></tr>
<tr><td>001</td><td>Load on Z</td></tr>
<tr><td>010</td><td>Latch on Z</td></tr>
<tr><td>011</td><td>Gate on Z</td></tr>
<tr><td>100</td><td>Reset on Z</td></tr>
</table></td><td>R/W</td><td>000</td></tr>
<tr><td>3:2</td><td>SCM [1:0]</td><td>Special Count Mode
<table>
<tr><td>00</td><td>No special mode active</td></tr>
<tr><td>01</td><td>Divide-by-N</td></tr>
<tr><td>10</td><td>Single Cycle</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
<tr><td>1:0</td><td>INPUT [1:0]</td><td>Input Mode
The Input Mode determines how the counter interprets the X- and Y- input signals.
<table>
<tr><td>00</td><td>Counter disabled</td></tr>
<tr><td>01</td><td>Quadrature Count</td></tr>
<tr><td>10</td><td>Up/Down Count</td></tr>
<tr><td>11</td><td>Direction Count</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
</table>

Table 5-4 : Channel Control Register

5.1.5 Channel Status Register

Bit	Symbol	Description	Access	Reset Value
7	-	Reserved	-	00
6	OVFL	Counter Data Register Lock Overflow When a Latch Mode event occurs while the Counter Data Register Lock is still active, the data in the Counter Data Register will be retained and this bit will be set to indicate that data was lost.	R	0
5	CDLK	Counter Data Register Lock This bit is set to '1', when the Counter Data Register is locked due to a read access to the high-word/highest byte, a 'Latch on Z' or a Simultaneous Counter Latch. This bit is cleared after a complete read access to the Output Register or by writing a '1' to bit 5 (RCDLK) in the Channel Command Register.	R	0
4	DIR	Count Direction This bit indicates the direction, the counter is counting to. '1' indicates up, '0' indicates down. In the 'Up/Down Count' mode this bit indicates the direction at the last count. In the 'Direction Count' mode this bit corresponds to the Y-input.	R	0
3	SGN	Sign The Sign bit is set to '1' when the counter overflows, and set to '0' when the counter underflows. After reset or power-up this bit should be considered as "don't care" until the first Carry or Borrow occurred.	R	0
2	MAT	Match This bit is set to '1' when the counter value matches the value of the Counter Compare Register. This bit must be reset manually in the Channel Command Register (RMAT).	R	0
1	CRY	Carry This bit is set to '1' when the counter changes from 0xFFFFFFFF to 0x00000000. This bit must be reset manually in the Channel Command Register (RCRY).	R	0
0	BOR	Borrow This bit is set to '1' when the counter changes from 0x00000000 to 0xFFFFFFFF. This bit must be reset manually in the Channel Command Register (RBOR).	R	0

Table 5-5 : Channel Status Register

The Channel Status Register is a read-only register. Write accesses to this address access the Channel Command Register.

5.1.6 Channel Command Register

Bit	Symbol	Description	Access	Reset Value
7	-	Reserved	-	0
6	ROVFL	Reset Counter Data Register Lock Overflow status bit	W	0
5	RCDLK	Release Counter Data Register Lock This resets the CDLK bit in the Channel Status Register and releases the Counter Data Register lock.	W	0
4	LCNT	Load Counter The counter is loaded with the value of the Preload Register.	W	0
3	RCNT	Reset Counter This resets the counter, the status bits RMAT, RCRY, RBOR and the Counter Data Register Lock.	W	0
2	RMAT	Reset Match status bit	W	0
1	RCRY	Reset Carry status bit	W	0
0	RBOR	Reset Borrow status bit	W	0

Table 5-6 : Channel Command Register

Commands are performed by writing a '1' to the according bit.

The Channel Command Register is a write-only register. Read accesses to this address access the Channel Status Register.

5.2 Global Registers

5.2.1 Global Control/Status Register

Bit	Symbol	Description	Access	Reset Value
7:3	-	Reserved	-	-
2	SCRERR	Simultaneous Counter Latch Error '1' indicates that a Simultaneous Counter Latch was issued although a Counter Data Registers was still locked – data is lost. This bit must be reset by writing '1' to it.	R/W	0
1	SCR	Simultaneous Counter Latch Writing '1' loads the Counter Data Registers of all channels with the actual counter value. As long as not all Counter Data Registers have been read, this bit reads as '1'.	R/W	0
0	MIE	Master Interrupt Enable '0' disables any interrupt generation '1' enables interrupt generation	R/W	0

Table 5-7 : Global Control/Status Register

A Simultaneous Counter Latch Error (SCRERR) is issued even if only one of the four Counter Data Registers is locked (resp. the CDLK bit is set in one of the four Channel Status Registers). In event of a Simultaneous Counter Latch Error the Simultaneous Counter Latch will be canceled for all four counter channels and the old data will be retained.

5.2.2 General Purpose I/O Control Register

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>7:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5</td><td>GPDATA</td><td>General Purpose Data
WRITE to this bit, when the General Purpose I/O is configured as output.
READ from this bit, when the General Purpose I/O is configured as input.</td><td>R/W</td><td>0</td></tr>
<tr><td>4:3</td><td>GPCDIV [1:0]</td><td>Clock Output Divider
<table><tr><td>00</td><td>1x = 8 MHz</td></tr><tr><td>01</td><td>2x = 4 MHz</td></tr><tr><td>10</td><td>4x = 2 MHz</td></tr><tr><td>11</td><td>8x = 1 MHz</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>2:1</td><td>GPCNF [1:0]</td><td>General Purpose Configuration
<table><tr><td>00</td><td>General Purpose I/O</td></tr><tr><td>01</td><td>Simultaneous Counter Latch</td></tr><tr><td>10</td><td>Clock Output</td></tr></table>General Purpose I/O:
Use GPDATA to read input data or write output data.
Simultaneous Counter Latch:
The module acts as master, when GPDIR = '1'. Use SCR in the Global Control/Status Register to issue a Simultaneous Counter Latch. It acts as slave, when GPDIR = '0'.
Clock Output:
Use GPCDIV to program the clock output frequency.</td><td>R/W</td><td>0</td></tr>
<tr><td>0</td><td>GPDIR</td><td>General Purpose Input/Output Control
'0 '= Use as output
'1' = Use as input</td><td>R/W</td><td>0</td></tr>
</table>

Table 5-8 : General Purpose I/O Control Register

5.2.3 Interrupt Vector Register

Bit	Symbol	Description	Access	Reset Value
7:0	IVEC	Interrupt Vector	R/W	0

Table 5-9 : Interrupt Vector Register

5.2.4 Interrupt Control Register

Bit	Symbol	Description	Access	Reset Value
15:9	-	Reserved	-	-
8	IRRENTI	Enable Interval Timer Interrupt '1' enables the Interval Timer Interrupt '0' disables the Interval Timer Interrupt	R/W	0
7:4	ICRENL [3:0]	Enable Interrupt on latch '1' enables the Interrupt on latch '0' disables the Interrupt on latch Bit 7 – CH4 latch interrupt enable Bit 6 – CH3 latch interrupt enable Bit 5 – CH2 latch interrupt enable Bit 4 – CH1 latch interrupt enable An interrupt is issued when Counter Data Register is loaded by the Z-input in the 'Latch on Z'-mode	R/W	0000
3:0	ICRENM [3:0]	Enable Interrupt on match '1' enables the Interrupt on match '0' disables the Interrupt on match Bit 3 – CH4 match interrupt enable Bit 2 – CH3 match interrupt enable Bit 1 – CH2 match interrupt enable Bit 0 – CH1 match interrupt enable An interrupt is issued when the Counter Data Register matches the Counter Compare Register	R/W	0000

Table 5-10: Interrupt Control Register

Interrupts on match, interrupts on latch and Timer interrupts are generated only when interrupts are enabled in the Global Control/Status Register (MIE).

5.2.5 Interrupt Status Register

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>15:9</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>8</td><td>ISRT</td><td>Pending Interval Timer Interrupts (Read),
Interrupt acknowledge (Write)
On a read-access this bit indicates a pending Interval Timer interrupt. A pending interrupt is marked with a '1'.
The interrupt is acknowledged by writing a '1' to this bit.</td><td>R/W</td><td>0</td></tr>
<tr><td>7:4</td><td>ISRL [3:0]</td><td>Pending Latch Interrupts (Read),
Interrupt acknowledge (Write)
On a read-access this four bits contain the channels with pending latch interrupts. Channels with pending interrupts are marked with a '1'.
<table><tr><td>Bit 7</td><td>Pending/Acknowledge CH4 latch interrupt</td></tr><tr><td>Bit 6</td><td>Pending/Acknowledge CH3 latch interrupt</td></tr><tr><td>Bit 5</td><td>Pending/Acknowledge CH2 latch interrupt</td></tr><tr><td>Bit 4</td><td>Pending/Acknowledge CH1 latch interrupt</td></tr></table>The interrupts are acknowledged by writing a '1' to the according bit.</td><td>R/W</td><td>0000</td></tr>
<tr><td>3:0</td><td>ISRM [3:0]</td><td>Pending Match Interrupts (Read),
Interrupt acknowledge (Write)
On a read-access this four bits contain the channels with pending match interrupts. Channels with pending interrupts are marked with a '1'.
<table><tr><td>Bit 3</td><td>Pending/Acknowledge CH4 match interrupt</td></tr><tr><td>Bit 2</td><td>Pending/Acknowledge CH3 match interrupt</td></tr><tr><td>Bit 1</td><td>Pending/Acknowledge CH2 match interrupt</td></tr><tr><td>Bit 0</td><td>Pending/Acknowledge CH1 match interrupt</td></tr></table>The interrupts are acknowledged by writing a '1' to the according bit.</td><td>R/W</td><td>0000</td></tr>
</table>

Table 5-11: Interrupt Status Register

5.2.6 Interval Timer Control Register

Bit	Symbol	Description	Access	Reset Value
7:3	-	Reserved	-	-
2:1	ITCDIV [1:0]	Interval Timer Clock Divider 00 = 1x = 8 MHz 01 = 2x = 4 MHz 10 = 4x = 2 MHz 11 = 8x = 1 MHz	R/W	00
0	ITEN	Interval Timer Enable '0' disables the Interval Timer '1' enables the Interval timer	R/W	0

Table 5-12: Interval Timer Control Register

5.2.7 Interval Timer Preload Register

Bit	Symbol	Description	Access	Reset Value
15:0	ITPRE	Interval Timer Preload Register	R/W	0

Table 5-13: Interval Timer Preload Register

5.2.8 Interval Timer Data Register

Bit	Symbol	Description	Access	Reset Value
15:0	ITDR	Interval Timer Data Register This Register contains the actual Timer Value.	R	0

Table 5-14: Interval Timer Data Register

5.2.9 Global Input Status Register

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>15:13</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>12:9</td><td>GISR4 [2:0]</td><td>X-, Y-, Z-Input Status Channel 4
<table><tr><td>Bit</td><td>Input</td></tr><tr><td>11</td><td>Z-Input</td></tr><tr><td>10</td><td>Y-Input</td></tr><tr><td>9</td><td>X-Input</td></tr></table></td><td>R</td><td>000</td></tr>
<tr><td>8:6</td><td>GISR3 [2:0]</td><td>X-, Y-, Z-Input Status Channel 3
<table><tr><td>Bit</td><td>Input</td></tr><tr><td>8</td><td>Z-Input</td></tr><tr><td>7</td><td>Y-Input</td></tr><tr><td>6</td><td>X-Input</td></tr></table></td><td>R</td><td>000</td></tr>
<tr><td>5:3</td><td>GISR2 [2:0]</td><td>X-, Y-, Z-Input Status Channel 2
<table><tr><td>Bit</td><td>Input</td></tr><tr><td>5</td><td>Z-Input</td></tr><tr><td>4</td><td>Y-Input</td></tr><tr><td>3</td><td>X-Input</td></tr></table></td><td>R</td><td>000</td></tr>
<tr><td>2:0</td><td>GISR1 [2:0]</td><td>X-, Y-, Z-Input Status Channel 1
<table><tr><td>Bit</td><td>Input</td></tr><tr><td>2</td><td>Z-Input</td></tr><tr><td>1</td><td>Y-Input</td></tr><tr><td>0</td><td>X-Input</td></tr></table></td><td>R</td><td>000</td></tr>
</table>

Table 5-15: Global Input Status Register

This Register reflects the states of the X-, Y-, and Z-inputs of all channels. Use this register for debug purposes.

6 Functional Description

The TIP116 offers 3 input modes, 2 special count modes and 4 input control modes.

6.1 Input Modes

The input mode determines how the counter interprets the X- and Y input lines:

Input Mode	X-input	Y-input	Z-input
Quadrature Count	Quadrature X	Quadrature Y	Available for Input Control Modes
Up/Down Count	Count UP	Count DOWN	
Direction Count	Count	Count direction (up/down)	

Table 6-1 : Input Modes

Changing the input mode does not affect the counter reading. If no input mode is selected, the counter is disabled.

6.1.1 Quadrature Count

The counter acts as quadrature counter. X-input is quadrature input X, Y-input is quadrature input Y. Input control modes are available with the Z-input. The quadrature inputs can be interpreted as 1x, 2x or 4x counting. 1x lets the counter count once for each full cycle of the quadrature inputs, 2x lets the counter count once for each half cycle of the quadrature inputs and 4x lets the counter count once for each quarter cycle of the quadrature inputs. The count direction (increase or decrease) is determined by the relative phase of the X- and Y-signals. A leading Y signal counts up; a leading X signal counts down.

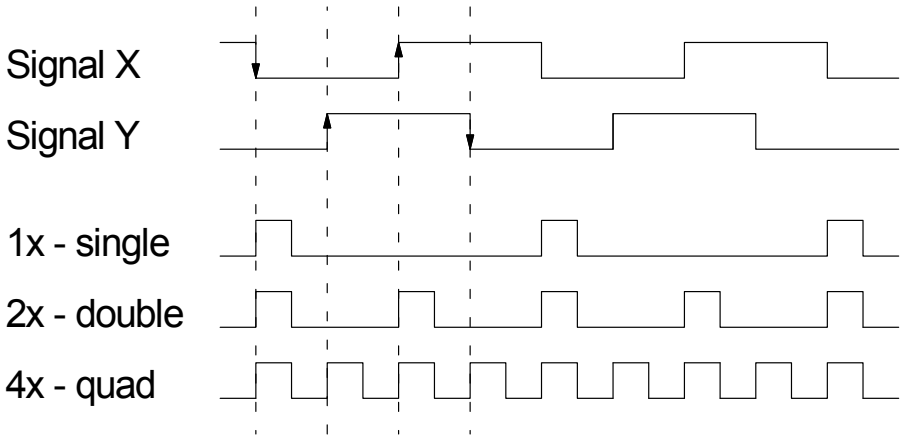

Figure 6-1 : Quadrature Signals

6.1.2 Up/Down Count

The counter acts as up-/down counter. The X-input counts up, the Y-input counts down. Input control modes are available with the Z-input. Counting pulses are generated when a transition from low to

high of either the X- or the Y-input is detected. Simultaneous transitions on the X- and Y-input do not generate a counting pulse.

6.1.3 Direction Count

The counter acts as up-/down counter. The X-input counts, the Y-input determines the count direction. Input control modes are available with the Z-input. Y-input = '1' is up, Y-input = '0' is down.

6.2 Special Count Modes

In normal operation, the counter is a cycling counter. Additional two special count modes are available.

6.2.1 Divide-by-N

The counter is enabled in the Channel Control Register and will run until disabled. The counter is loaded with the content of the preload register every time the counter creates a borrow or a carry.

6.2.2 Single Cycle

The counter is enabled in the Channel Control Register and will start on a manual preload or reset in the Channel Command Register. The counter stops when it creates a borrow or a carry.

6.3 Input Control Modes

The Input Control Mode determines how events on the Z-input are interpreted.

With the exception of the 'Gate on Z' mode, all modes react on a level change on the Z-input. Due to the digital input filtering, a change in the input level is only detected, when the input line is stable for at least 100ns. The following table gives an overview of the control mode events.

Input Control Mode	Polarity	
	high active (CCR[10] = 0)	low active (CCR[10] = 1)
No Z-Control	-	-
Load on Z	Rising edge	Falling edge
Latch on Z	Rising edge	Falling edge
Gate on Z	High level	Low Level
Reset on Z	Rising edge	Falling edge

Table 6-2 : Input Control Mode events

6.3.1 No Z-Control

In this mode the Z-input is ignored. Alternatively the Z-input can be disabled in the Input Enable Register.

6.3.2 Load on Z

An event on the Z-input loads the counter with the content of the Counter Preload Register.

This control mode can be used to establish a known reference position in a mechanical system.

If the 'Single Cycle' mode is active, the event on the Z-input will start the counter.

The counter can also be preloaded by writing '1' to the 'Load Counter' (LCNT) bit in the Channel Command Register.

6.3.3 Latch on Z

An event on the Z-input loads and locks the Counter Data Register with the actual counter value (see “6.4 Counter Data Register Lock” for details). When enabled in the Interrupt Control Register, this also generates an interrupt.

When a ‘Latch on Z’ event occurs while the Counter Data Register Lock is still active, the data in the Counter Data Register will be retained and the Counter Data Register Lock Overflow (OVFL) will be set to indicate that data was lost.

This control mode can be used to capture a position in a mechanical system.

6.3.4 Gate on Z

The signal level on the Z-input enables or disables counting.

When a signal with constant frequency (i.e. the clock output of the TIP116) is connected to the X- and Y-inputs, this control mode can be used to let the counter act as a timer.

6.3.5 Reset on Z

An event on the Z-input resets the counter.

This control mode can be used to establish a known home or reference position in a mechanical system.

The counter can also be reset by writing '1' to the 'Reset Counter' (RCNT) bit in the Channel Command Register.

6.4 Counter Data Register Lock

The Counter Data Register is loaded with the actual counter value and locked on following conditions:

- Read-access to the high-word or the highest byte of the Counter Data Register
- Latch Mode
- General Purpose I/O: Simultaneous Counter Latch
- Simultaneous Counter Latch in the Global Control Register (SCR)

The Counter Data Register is locked until following conditions are met:

- A read-access to the low-word or the lowest byte of the Output Register
- A write '1' to the RCLT bit in the Channel Command Register

Until the lock is released, the Counter Data Register will not load again. The status of the Counter Data Register lock can be monitored in the Channel Status Register (CDLK). When the lock is released, the Counter Data Register retains its value until it is loaded again.

When a Simultaneous Counter Latch is issued although a Counter Data Register is locked, the Simultaneous Counter Latch is canceled and a Simultaneous Counter Latch Error (SCRERR) is issued in the Global Control/Status Register to indicate that data is lost.

When a Latch Mode event occurs while the Counter Data Register Lock is still active, the data in the Counter Data Register will be retained and the Counter Data Register Lock Overflow (OVFL) will be set to indicate that data was lost.

6.5 Interrupts

The TIP116 creates interrupts when the counter reading matches the Counter Compare Register and when the interval timer passes zero. It also creates an interrupt when Counter Data Register is loaded by the Z-input in the 'Latch on Z'-mode. Each interrupt must be enabled individually in the Interrupt Control Register. Additionally, interrupts must be enabled globally in the Global Control Register.

All interrupts are issued on the INTREQ0 output. The channel causing the interrupt can be determined in the Interrupt Status Register. All interrupts are acknowledged in the Interrupt Status Register.

6.6 General Purpose I/O

The TIP116 provides one RS422 general purpose I/O. It can be configured in the General Purpose I/O Control Register:

Configuration	General Purpose I/O Control Register			
	GPDIR	GPCNF	GPCDIV	GPDATA
General Purpose Input	input	General purpose	don't care	Read Input Data
General Purpose Output	output	General purpose	don't care	Write Output Data
Clock Output	output	Clock output	Clock Divider	don't care
Simultaneous Counter Latch Master	output	Simultaneous Counter Latch	don't care	don't care
Simultaneous Counter Latch Slave	input	Simultaneous Counter Latch	don't care	don't care

Table 6-3 : General Purpose I/O Configurations

6.6.1 General Purpose Input/Output

The General Purpose I/O can be configured as input or as output. When configured as input, read the input data from GPDATA, when configured as output, write the output data to GPDATA.

6.6.2 Programmable Clock Output

The clock can be programmed to 8, 4, 2, or 1 MHz frequency. Use GPCDIV in the Global Control Register to configure the desired clock frequency.

In an application, the clock output can be connected with the X-input of a channel which is then gated with the Z-input. This configuration turns that channel into a gated 32 bit timer with a resolution up to 125 ns. Note that the maximum input frequency of the counters is 4 MHz.

6.6.3 Simultaneous Counter Latch

The Simultaneous Counter Latch provides a way to synchronize multiple TIP116 modules or synchronize the TIP116 with external events.

To synchronize the TIP116 with external events, configure the General Purpose I/O as Simultaneous Counter Latch Slave. With a high-pulse of at least 100ns on the GPIO input the Counter Data Registers of all channels are loaded simultaneously with the actual counter reading.

To synchronize multiple TIP116, configure one module as Simultaneous Counter Latch Master and the other modules as Simultaneous Counter Latch Slaves. Connect the GPIO of the master with the GPIO of the slaves. To issue a Simultaneous Counter Latch, write to the SCR bit in the Global Control/Status Register of the master. The Simultaneous Counter Latch is then passed on the connected Simultaneous Counter Latch Slaves.

The Simultaneous Counter Latch (SCR) in the Global Control/Status Register operates independent of the configuration of the General Purpose I/O, except in the described case when the General Purpose I/O is configured as Simultaneous Counter Latch Master.

6.7 Interval Timer

The interval timer is a 16 bit preloadable counter with a programmable clock. On activation, the counter loads from Interval Timer Preload Register und starts counting down. When the counter reaches zero, it generates an interrupt (if enabled), is automatically preloaded again and continues counting.

With the 16 bit preload register and the programmable clock interval times up to 65ms are possible. Calculate the interval times after following formula:

Interval Time = Value of ITPL * Clock period

ITC_CL	Clock frequency	Clock period
00	8 MHz	125ns
01	4 MHz	250ns
10	2 MHz	500ns
11	1 MHz	1µs

Table 6-4 : Output Clock Periods

The interval timer can be used as reference timer in closed loop applications.

6.8 Digital Input Filtering

To avoid false counts caused by noisy input signals, the X- Y- and Z-inputs are digital filtered. A change in the input level is only detected, when the input line is stable for at least 100ns.

6.9 Input Wiring

The following schematic shows the principle input wiring for one encoder signal.

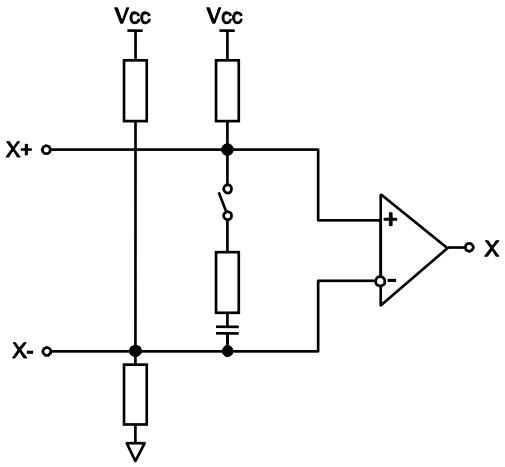

Figure 6-2 : Input Wiring

The 120Ω termination resistor is switchable via DIP switches. For single-ended/TTL signals the switch must be left open (default), for differential/RS422 signals the switch should be closed.

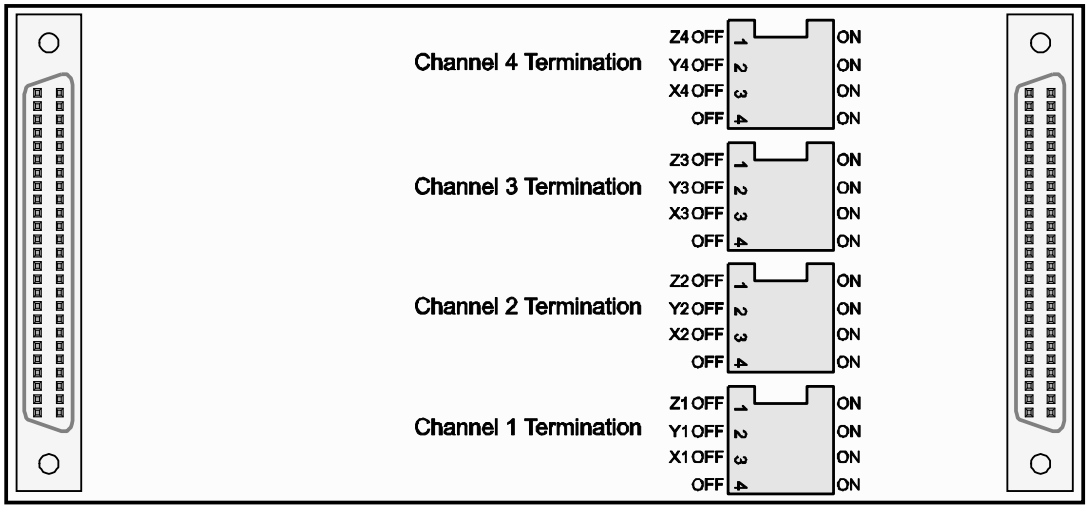

Figure 6-3 : Termination Resistor DIP Switches

6.9.1 Single-Ended / TTL

The following schematic shows the principle input wiring for one single-ended/TTL encoder signal. For single-ended/TTL input, leave the inverting input (X-) open and connect the TTL signal to the non-inverting input (X+).

The120Ω termination resistor must be switched off when using single-ended/TTL input signals!

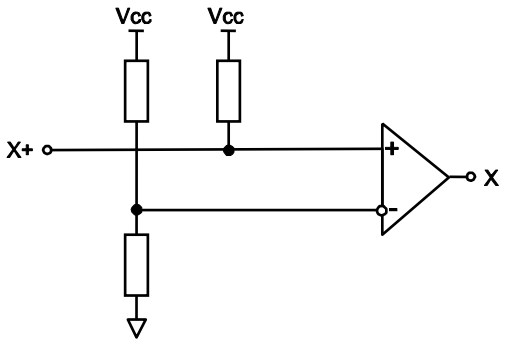

Figure 6-4 : Single-ended Input Wiring

The switching point lies at approx. 1.6V, with a hysteresis of about 0.4 mV.

6.9.2 Differential / RS422

The following schematic shows the principle input wiring for one differential/RS422 encoder signal. RS422 input signals should be terminated. The encoder input is fail-safe based, so that unused inputs can be left open.

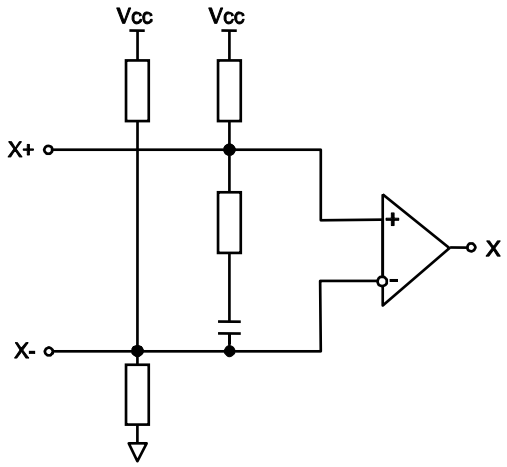

Figure 6-5 : Differential Input Wiring

It is recommended to terminate differential/RS 422 input signals.

7 Pin Assignment – I/O Connector

Pin	Signal	RS422	TTL input
1	Channel 1 X+	X1+	X1
2	GND		GND
3	Channel 1 Y+	Y1+	Y1
4	GND		GND
5	Channel 1 Z+	Z1+	Z1
6	GND		GND
7	Channel 2 X+	X2+	X2
8	GND		GND
9	Channel 2 Y+	Y2+	Y2
10	GND		GND
11	Channel 2 Z+	Z2+	Z2
12	GND		GND
13	Channel 3 X+	X3+	X3
14	GND		GND
15	Channel 3 Y+	Y3+	Y3
16	GND		GND
17	Channel 3 Z+	Z3+	Z3
18	GND		GND
19	Channel 4 X+	X4+	X4
20	GND		GND
21	Channel 4 Y+	Y4+	Y4
22	GND		GND
23	Channel 4 Z+	Z4+	Z4
24	GND		GND
25	GPIO+	RS422+	

Pin	Signal	RS422	TTL input
26	GND		GND
27	Channel 1 X-	X1-	No connect
28	GND		GND
29	Channel 1 Y-	Y1-	No connect
30	GND		GND
31	Channel 1 Z-	Z1-	No connect
32	GND		GND
33	Channel 2 X-	X2-	No connect
34	GND		GND
35	Channel 2 Y-	Y2-	No connect
36	GND		GND
37	Channel 2 Z-	Z2-	No connect
38	GND		GND
39	Channel 3 X-	X3-	No connect
40	GND		GND
41	Channel 3 Y-	Y3-	No connect
42	GND		GND
43	Channel 3 Z-	Z3-	No connect
44	GND		GND
45	Channel 4 X-	X4-	No connect
46	GND		GND
47	Channel 4 Y-	Y4-	No connect
48	GND		GND
49	Channel 4 Z-	Z4-	No connect
50	GPIO-	RS422-	

Table 7-1 : Pin Assignment I/O Connector