The Embedded I/O Company

TIP150

2 Channel Synchro / Resolver-To-Digital Converter

Version 1.1

User Manual

Issue 1.1.9

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TIP150-40R

2 Channel Tracking RDC,
Converter Accuracy 4 arcmin +1LSB

TIP150-41R

2 Channel Tracking RDC,
Converter Accuracy 2 arcmin +1LSB

Signal Conditioning Adapter

TIP150-A1-xx Resolver Interface

TIP150-A2-xx Resolver Interface with Reference Oscillator

TIP150-A3-xx High Precision Synchro/Resolver Interface

TIP150-A4-xx High Precision Synchro/Resolver Interface with Reference Oscillator

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	September 1995
1.0	Hardware Version 1.1	December 1996
1.2	General Revision	January 2003
1.3	New address TEWS LLC	September 2006
1.4	New Hardware Revision	November 2006
1.5	Added Binary Data to Angle relation table	August 2008
1.1.6	New Notation for User Manual	January 2010
1.1.7	Adapted for new RDC19224 Chip Rev. D - Max Reference Signal Frequency 10kHz - Error BIT threshold changed in Status Register Description - General Update for Table 3-1 Tracking Rate Characteristics …	August 2019
1.1.8	Single channel order options -30R and -31R have been discarded	September 2019
1.1.9	Update Block Diagram	September 2019

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1 Product Description

The TIP150 is an IndustryPack® module providing two channels of a Tracking Synchro / Resolver-To-Digital Converter. The resolution programming allows selection of 10, 12, 14 or 16 bit conversion. This combines the high tracking rate of a 10 bit converter with the precision of a 16 bit converter.

Two converter accuracies are available: TIP150-40 with 4 arcmin +1LSB converter accuracy for both channels and TIP150-41 with 2 arcmin +1LSB converter accuracy for both channels.

The TIP150 IndustryPack® module requires an additional signal conditioning adapter (TIP150-Ay-xx) per channel. The customer specific signal conditioning adapters provide an easy interface for the different types of synchro and resolver. For more details please see the Signal Conditioning Adapter section in this manual.

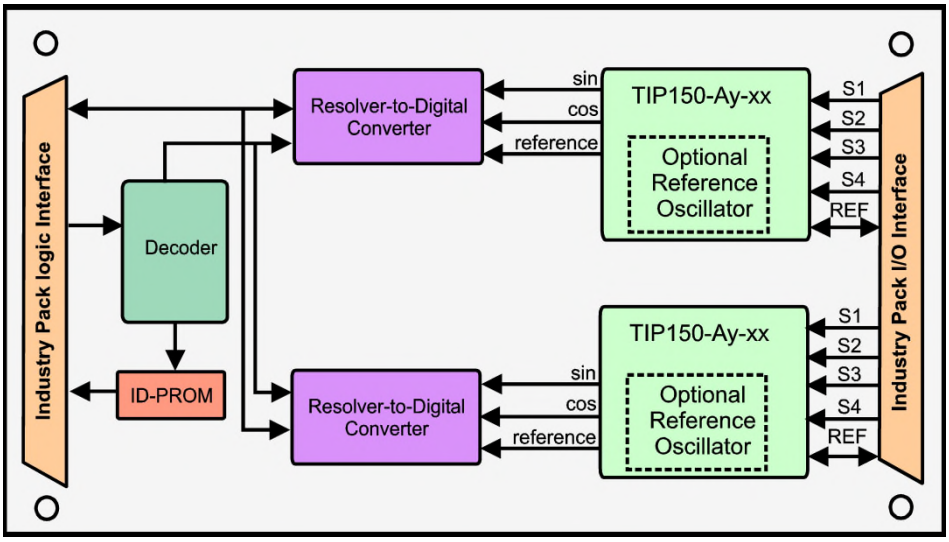

Figure 1-1 : Block Diagram

2 Technical Specification

TIP150-xx	
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995 (8MHz)
Interface Connector	50-conductor flat cable
Wait States	IDSEL# : no wait states IOSEL# to control registers : no wait states IOSEL# to data register : 2 wait states
Number of I/O Channels	TIP150-4x : 2
Accuracy of RDC	TIP150-40 : 4 arcmin +1LSB TIP150-41 : 2 arcmin +1LSB
Power Requirements	TIP150-4x with TIP150-A2-07 adapters 140mA typical @ +5V 15mA typical @ +12V , no load 32mA typical @ -12V, no load
Temperature Range	Operating : 0 °C to +70 °C Storage : -25°C to +125°C
MTBF	1166000 h (TIP150-4x module only) 818000 h (e.g.TIP150-4x with TIP150-A2-07 adapters)
Humidity	5 – 95 % non-condensing
Weight	30 g

Table 2-1 : Technical Specification TIP150

TIP150-A1-xx (Signal Conditioning Adapter)	
Input Voltage	Configured by resistors
Input Frequency	DC to 10 KHz
TIP150-A2-xx (Signal Conditioning Adapter)	
Input Voltage	Configured by resistors
Input Frequency	2 KHz to 10 KHz, dependent of configuration of on board reference oscillator
Reference Oscillator	2 KHz to 10 KHz, max. 11.8Vrms 70mA configured on Signal Conditioning Adapter by resistors
TIP150-A3-xx (Signal Conditioning Adapter)	
Input Voltage	11.8Vrms or 90.0Vrms, selected by high precision matching resistor array
Input Frequency	DC to 10 KHz
TIP150-A4-xx (Signal Conditioning Adapter)	
Input Voltage	11.8Vrms, high precision matching resistor array

Input Frequency	2 KHz to 10 KHz, dependent of configuration of on board reference oscillator
Reference Oscillator	2 KHz to 10 KHz, max. 11.8Vrms 70mA configured on Signal Conditioning Adapter by resistors

Table 2-2 : Technical Specification TIP150 Adapter

3 Functional Description

The TIP150 provides two Resolver-To-Digital Converter channels. The input signals are adapted by Signal Conditioning Adapters (TIP150-Ay-xx) plugged on the TIP150.

A Signal Conditioning Adapter is required for each channel of the TIP150.

Four types of Signal Conditioning Adapters are available:

- TIP150-A1-xx Resolver Interface Signal Conditioning Adapter
- TIP150-A2-xx Resolver Interface Signal Conditioning Adapter with on board reference oscillator
- TIP150-A3-xx High precision Synchro/Resolver Interface Signal Conditioning Adapter
- TIP150-A4-xx High precision Synchro/Resolver Interface Signal Conditioning Adapter with on board reference oscillator

TIP150-4x modules (2 channels) support the mode of synchronous status and data latch for each channel or synchronous data and status latch for both channels simultaneous.

3.1 Tracking Rate Characteristics

Tracking Rate, Reference Frequency limits and Velocity Scaling are depending on the resolution configured for the Resolver-Digital-Converter (RDC).

Resolution				
10 bit	**12 bit**	**14 bit**	**16 bit**	**Unit**
282				Bandwidth (Hz)
282	126.9	61.0	15.3	Max Tracking Rate (RPS*)
10	10	7	4	Max Reference Frequency (kHz)
0.0036	0.0143	0.0573	0.229	Velocity Voltage Scaling Factor (V/RPS*)

* RPS (rotations per second)

Table 3-1 : Tracking Rate Characteristics for Converter Options

3.2 Automatically Resolution Change

If the Build-In-Test bits of the converter indicate an error, the resolution bits RES0 and RES1 of the Channel Control Register which normally control the resolution will be ignored and the resolution is changed from its programmed value one step down to a lower resolution. This allows the converter to settle out faster. After the converter has settled out, the resolution is switched back to the programmed resolution.

For example:

If 12 bit resolution is programmed and Build-In-Test indicates an error the resolution changes to 10 bit until the converter settled out.

If 14 bit resolution is programmed and Build-In-Test indicates an error the resolution changes to 12 bit until the converter settled out.

If 16 bit resolution is programmed and Build-In-Test indicates an error the resolution changes to 14 bit until the converter settled out.

3.3 Binary Angle Relationships

Resolution in Bits	2^n	LSB as % of full scale	Degrees/Bit	Minutes/Bit	Radians/Bit
10	1024	0.09765625	0.3515625	21.09375	0.00613592
12	4096	0.02441406	0.0878906	5.27344	0.00153398
14	16384	0.00610352	0.0219727	1.31836	0.00038350
16	65536	0.00152588	0.0054932	0.32959	0.00009587

Table 3-2 : Binary Angle Relationships

Angle in degrees = $\frac{Data \cdot 360°}{2^{16}}$

Angle in minutes = $\frac{Data \cdot 21600'}{2^{16}}$

Angle in radians = $\frac{Data \cdot 2\pi}{2^{16}}$

(Data read is always 16bit left aligned. For less than 16bit resolution, least significant data bits are set to '0').

4 ID PROM Contents

Address	Function	Contents
0x01	ASCII ‘I’	0x49
0x03	ASCII ‘P’	0x50
0x05	ASCII ‘A’	0x41
0x07	ASCII ‘C’	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x14
0x0D	Revision	0x11
0x0F	Reserved	0x00
0x11	Driver-ID low byte	0x00
0x13	Driver-ID high byte	0x00
0x15	Number of bytes used	0x0D
0x17	CRC	TIP150-40R : 0x4F TIP150-41R : 0x6E
0x19	Board Option –xx	TIP150-40R : 0x28 TIP150-41R : 0x29
0x1B	Not used	0x00
…		…
0x3F		0x00

Table 4-1 : ID PROM Contents

5 IP Addressing

5.1 I/O Addressing

The complete register set of the TIP150 is accessible in the IP I/O space.

The control registers are automatically cleared by assertion of IP_RESET#.

Address	Symbol	Description	Size (Bit)	Access
0x00	DATA_RDC1	Channel 1 Data Register	16	R
0x03	STATUS_RDC1	Channel 1 Status Register	8	R
0x05	CONTR_RDC1	Channel 1 Control Register	8	R/W
0x06	Reserved			
0x08	DATA_RDC2	Channel 2 Data Register	16	R
0x0B	STATUS_RDC1	Channel 2 Status Register	8	R
0x0D	CONTR_RDC2	Channel 2 Control Register	8	R/W
0x0E	Reserved			

Table 5-1 : Register Set

5.2 Channel 1 Data Register (Address 0x00)

The Channel 1 Data Register DATA_RDC1 contains the converted data value of the Resolver or Synchro. When the resolution is set to less than 16 bits, all unused bits are read as ’0’. The conversion result is always MSB aligned. The resolution is controlled by the Channel 1 Control Register. If the Build-In-Test bit of the Channel 1 Status Register is read as ’1’, the resolution changes from its programmed value one step down to a lower resolution. This allows the converter to settle out faster.

Bit	Symbol	Description	Access	Reset Value
15:0		16 bit RDC value Left aligned. For resolution of 10, 12 or 14 bits, unused data bits are read as ‘0’	R	

Table 5-2 : Channel 1 Data Register DATA_RDC1 (Address 0x00)

For example:

If 12 bit resolution is programmed: Data Register = 0xXXX0

If 16 bit resolution is programmed: Data Register = 0xXXXX

5.3 Channel 1 Status Register (Address 0x03)

The Channel 1 Status Register STATUS_RDC1 is a byte wide read register and indicates the data conversion status of the converter for channel 1.

Bit	Symbol	Description	Access	Reset Value
7:2		Always read as '0'	R	
1	LOS	Loss of Signal Read as '1' indicates that both sin and cos input of the on board oscillator are less than 800mV peak. Only valid for TIP150 modules with Signal Conditioning Adapters with Reference Oscillator (TIP150-A2-xx, TIP150-A4-xx). For other Signal Conditioning Adapters (TIP150-A1-xx, TIP150-A3-xx) always read as '0'.	R	
0	BIT	Built-In-Test Read as '1' indicates an error : • If the difference between input and output angels exceeds approximately 180 LSBs (of the selected resolution). This condition will occur during a large step and reset after the converter settles out. • For an over velocity condition, because the converter loop cannot maintain input-output or/and if the converter malfunctions where it cannot maintain the loop at a null. • If both, sin and cos input voltages are less than 800mV peak or if the differential reference voltage is less than 20mV peak. As long as BIT is read as '1' the resolution for the RDC is changed from the programmed value to the next lower resolution.	R	

Table 5-3 : Channel 1 Status Register STATUS_RDC1 (Address 0x03)

5.4 Channel 1 Control Register (Address 0x05)

The Channel 1 Control Register CONTR_RDC1 is a byte wide read/write register.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>7:6</td><td></td><td>Always read as ‘0’. Write access has no effect</td><td>R/W</td><td></td></tr>
<tr><td>5:4</td><td></td><td>Don’t care</td><td>R/W</td><td></td></tr>
<tr><td>3</td><td>ESC</td><td>Synchronous Conversion Channel 1 and Channel 2
1 = Enabled
Read access to the Channel 1 Data Register starts the conversion for channel 1 and 2, latches the Status Register for channel 1 and 2 and provides the data for channel 1. Latching the Status Register ensures that the Status Registers reflect the state at data read time. The status of both Status Registers will remain latched until a read access to the Channel 2 Status Register.</td><td>R/W</td><td>0</td></tr>
<tr><td>2</td><td>ESL</td><td>Synchronous Status Latch
1 = Status will be latched at the time reading the Channel 1 Data Register, ensuring that the Channel 1 Status Register reflects the state at data read time. The status will remain latched until it is read.
To use this mode of operation, bit 3 (ESC) must be set to ‘0’.</td><td>R/W</td><td>0</td></tr>
<tr><td>1</td><td>RES1</td><td rowspan="2">Resolution Selection
Used to program the resolution of the converter :<table><tr><th>RES1</th><th>RES0</th><th>Resolution</th></tr><tr><td>0</td><td>0</td><td>10 bits</td></tr><tr><td>0</td><td>1</td><td>12 bits</td></tr><tr><td>1</td><td>0</td><td>14 bits</td></tr><tr><td>1</td><td>1</td><td>16 bits</td></tr></table></td><td rowspan="2">R/W</td><td rowspan="2">00</td></tr>
<tr><td>0</td><td>RES0</td></tr>
</table>

Table 5-4 : Channel 1 Control Register CONTR_RDC1 (Address 0x05)

After reset all bits are set to ‘0’, default conditions are 10 bit conversion, no synchronous conversion.

5.5 Channel 2 Data Register (Address0x08)

The Channel 2 Data Register DATA_RDC2 contains the converted data value of the Synchro or Resolver. When the resolution is set to less than 16 bits, all unused bits are read as ’0’. The conversion result is always MSB aligned. The resolution is controlled by the Channel 2 Control Register. If the Build-In-Test bit of the Channel 2 Status Register is read as ’1’, the resolution changes from its programmed value one step down to a lower resolution. This allows the converter to settle out faster.

Bit	Symbol	Description	Access	Reset Value
15:0		16 bit RDC value Left aligned. For resolution of 10, 12 or 14 bits, unused data bits are read as ‘0’	R	

Table 5-5 : Channel 2 Data Register DATA_RDC2 (Address 0x08)

For example:

If 12 bit resolution is programmed: Data Register = 0xXXX0

If 16 bit resolution is programmed: Data Register = 0xXXXX

5.6 Channel 2 Status Register (Address 0x0B)

The Channel 2 Status Register STATUS_RDC2 is a byte wide read register and indicates the data conversion status of the converter for channel 2.

Bit	Symbol	Description	Access	Reset Value
7:2		Always read as '0'	R	
1	LOS	Loss of Signal Read as '1' indicates that both sin and cos input of the on board oscillator are less than 800mV peak. Only valid for TIP150 modules with Signal Conditioning Adapters with Reference Oscillator (TIP150-A2-xx, TIP150-A4-xx). For all other Signal Conditioning Adapters (TIP150-A1-xx, TIP150-A3-xx) read as '0'.	R	
0	BIT	Built-In-Test Read as '1' indicates an error : • If the difference between input and output angels exceeds approximately 180 LSBs (of the selected resolution). This condition will occur during a large step and reset after the converter settles out. • For an over velocity condition, because the converter loop cannot maintain input-output or/and if the converter malfunctions where it cannot maintain the loop at a null. • If both, sin and cos input voltages are less than 800mV peak or if the differential reference voltage is less than 20mV peak. As long as BIT is read as '1' the resolution for the RDC is changed from the programmed value to the next lower resolution.	R	

Table 5-6 : Channel 2 Status Register STATUS_RDC2 (Address 0x0B)

5.7 Channel 2 Control Register (Address 0x0D)

The Channel 2 Control Register CONTR_RDC2 is a byte wide read/write register.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>7:6</td><td></td><td>Always read as ‘0’. Write access has no effect</td><td>R/W</td><td></td></tr>
<tr><td>5:3</td><td></td><td>Don’t care</td><td>R/W</td><td></td></tr>
<tr><td>2</td><td>ESL</td><td>Synchronous Status Latch
1 = Status will be latched at the time reading the Channel 2 Data Register, ensuring that the Channel 2 Status Register reflects the state at data read time. The status will remain latched until it is read.
To use this mode of operation, bit3 (ESC) of the Channel 1 Control Register must be set to ‘0’.</td><td>R/W</td><td>0</td></tr>
<tr><td>1</td><td>RES1</td><td rowspan="2">Resolution Selection
Used to program the resolution of the converter :
<table><tr><th>RES1</th><th>RES0</th><th>Resolution</th></tr><tr><td>0</td><td>0</td><td>10 bits</td></tr><tr><td>0</td><td>1</td><td>12 bits</td></tr><tr><td>1</td><td>0</td><td>14 bits</td></tr><tr><td>1</td><td>1</td><td>16 bits</td></tr></table></td><td rowspan="2">R/W</td><td rowspan="2">00</td></tr>
<tr><td>0</td><td>RES0</td></tr>
</table>

Table 5-7 : Channel 2 Control Register CONTR_RDC2 (Address 0x0D)

After reset all bits are set to ‘0’, default conditions are 10 bit conversion, no synchronous conversion.

6 Operating Modes

If bit 2 and bit 3 of the Control Register(s) are set to ’0’, the Status Register(s) reflect the actual conditions of the converter. It is recommended to use a mode which latches the status of the data reading.

6.1 Operating with Synchronous Status Latch

Operating with synchronous status latch for each channel separately is selected if bit 2 of the respective Channel Control Register is set to ’1’. In this case the Channel Status Register latches the status at Data Register read time. The latch is released by a read access to the Status Register.

Sequence:

Read Data Register (read data and latch the status for the data read)

Read Status Register (read latched status and release status latch)

Check Build-In-Test Status Register bit 0 (if bit 0 was read as ’0’, the data value is valid)

To use this mode, bit 3 of the Channel 1 Control Register must be set to ’0’.

6.2 Operating with Synchronous Conversion

Operating with synchronous conversion for Channel 1 and Channel 2 is selected if bit 3 of the Channel 1 Control Register (CONTR_RDC1) is set to ’1’. In this case the value of channel 2 is converted simultaneously with channel 1 and both Status Registers are latched at Data Register read time. To release the latches of the channel 1 and channel 2 Status Registers the user must read the Status Register of Channel 2 (STATUS_RDC2).

Sequence:

Read Channel 1 Data Register (start conversion for channel 1 and 2, latch the status for channel 1 and 2, read data for channel 1)

Read Channel 1 Status Register (read latched status for channel 1)

Read Channel 2 Data Register (read data for channel 2)

Read Channel 2 Status Register (read latched status for channel 2 and release status latches for channel 1 and 2)

Check Build-In-Test (bit 0) of both Status registers (if bit 0 was read as ’0’, the data value is valid)

7 Signal Conditioning Adapter

For the TIP150 the concept of Signal Conditioning Adapters is used. This makes it easy to use the TIP150 with various types of Resolver and Synchro.

Four different kinds of Signal Conditioning Adapters are available:

TIP150-A1-xx Resolver Signal Conditioning Adapter

TIP150-A2-xx Resolver Signal Conditioning Adapter with reference signal source

TIP150-A3-xx High precision Resolver/Synchro Signal Conditioning Adapter

TIP150-A4-xx High precision Resolver/Synchro Signal Conditioning Adapter with reference signal source

The A1, A3 Signal Conditioning Adapters require a reference signal from the resolver/synchro as an input.

The A2, A4 Signal Conditioning Adapters generate the reference signal to be used for the resolver/synchro on board and automatically compensate the phase error generated by the resolver/synchro.
The maximum reference output voltage available is 11.8Vrms. Maximum output current is 70mA. Reference signal frequencies 2kHz ... 10kHz are available.

The -xx option specifies the signal input voltage, single ended or differential input signal mode, reference input voltage (A1, A3 adapters) or reference output voltage and frequency (A2, A4 adapters).
Ask for the actual list of signal conditioning adapters or for your special requirement.

The TIP150-A1-xx signal conditioning adapters are configured by resistors for the resolver sin, cos input signal voltage and the reference input signal voltage. For the resolver sin, cos input signals, single ended and differential signal input options are available.

The TIP150-A2-xx signal conditioning adapters are configured by resistors for the resolver sin, cos signal input voltage and the reference output signal voltage and frequency. All TIP150-A2 adapters operate in single ended signal input mode for the resolver sin, cos input signals (the resolver sin- and cos- signals are connected to AGND, the resolver sin+, cos+ signal inputs become referenced to AGND).

The TIP150-A3-xx and TIP150-A4-xx signal conditioning adapters are configured by a high precision resistor network for 11.8Vrms or 90Vrms resolver/synchro signal input and are configured by resistors for the reference signal voltage.

7.1 Adapter Connections

The Signal Conditioning Adapters TIP150-Ay-xx are used to link the TIP150-xx IP I/O connector to the on board Resolver-To-Digital Converter.

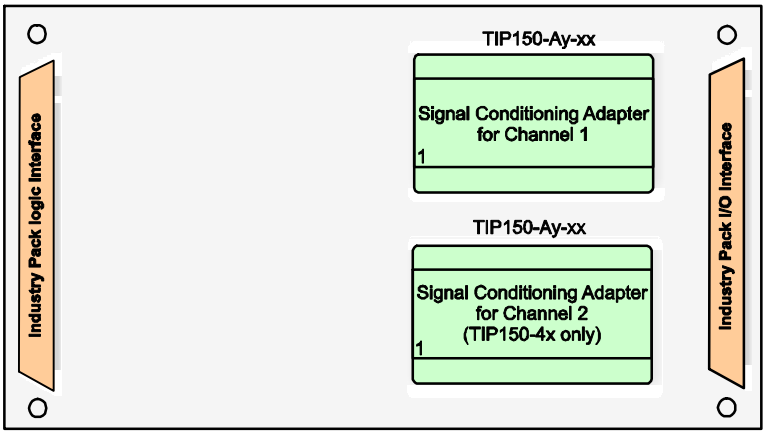

Figure 7-1 : TIP150 Adapter Board Placement

7.1.1 Signal Conditioning Adapter Pin Out

Pin	Signal	Function
1	+REF	RDC Ref+ Input Signal
2	-5V	Power Supply
3	AGND	Analog Ground
4	AGND	Analog Ground
5	S3	S3 (Sin+) Input from Resolver / Synchro
6	-12V	Power Supply
7	SIN	RDC Sin I/O Signal
8	GND	Digital Ground
9	-S	RDC Sin- Input Signal
10	+12V	Power Supply
11	-REF	RDC Ref- Input Signal
12	EXC-	Reference Signal- Output (A2, A4 Adapters only)
13	-REF_EXT	External Reference Signal - Input (A1, A3 Adapters only)
14	+REF_EXT	External Reference Signal + Input (A1, A3 Adapters only)
15	EXC+	Reference Signal+ Output (A2, A4 Adapters only)
16	S4	S4 (Cos-) Input from Resolver / Synchro
17	COS	RDC Cos I/O Signal
18	-C	RDC Cos - Input Signal

Pin	Signal	Function
19	S1	S1 (SIn-) Input from Resolver / Synchro
20	+C	RDC Cos+ Input Signal
21	S2	S2 (Cos+) Input from Resolver / Synchro
22	LOS	Loss of Signal (error signal from on board reference oscillator) (A2, A4 Adapters only)
23	+S	RDC Sin+ Input Signal
24	+5V	Power Supply

Table 7-1 : Signal Conditioning Adapter Pin Out

8 Installation Hints

8.1 Module Height

Due to the concept of Signal Conditioning Adapters (TIP150-Ay-xx) the TIP150 uses the maximum board height which is allowed by the IP specification.

To avoid damage of the carrier board and / or of the TIP150 please make sure that there are no conductive components like ceramic PGA's underneath the IP socket used for the TIP150.

8.2 Single Ended Signal Conditioning Adapters

Some TIP150-A1-xx, all TIP150-A2-xx and some TIP150-A4-xx signal conditioning adapters are specified as single ended for the resolver sin, cos signal inputs.

These single ended signal conditioning adapters require the resolver sin and cos input signals to be referenced to AGND. This is done by connecting the resolver signals sin+, sin-, cos+, cos- to the TIP150-xx I/O connector with an additional AGND connection for the sin- and cos- input signals.

Single ended signal conditioning adapters shipped from Q2 2003 onward, provide an on board AGND connection for the sin-, cos- I/O pins. For these single ended adapters the resolver sin-, cos- signals are connected to AGND by the adapter and the resolver sin+, cos+ signals become referenced to AGND.

Single ended signal conditioning adapters shipped before Q2 2003 require an additional external AGND connection for the sin-, cos- I/O pins in addition to the connected resolver sin-, cos- signals. E.g. for such a single ended adapter on channel 1, connect the resolver sin- signal and I/O pin 3 (AGND) to I/O pin 2 (sin-) and connect the resolver cos- signal and I/O pin 6 (AGND) to I/O pin 5 (cos-).

The reference input signal (A1, A3 adapters) does not require an external AGND connection for single ended signal conditioning adapters.

9 I/O Pin Assignment

9.1 50 pin IP I/O Connector

Pin	Function Resolver / Synchro	Direction	Comment
1	Resolver 1 S3 (Sin+) / Synchro 1 S3	Input	
2	Resolver 1 S1 (Sin-) / Synchro 1 S1	Input	see note below
3	AGND		
4	Resolver 1 S2 (Cos+) / Synchro 1 S2	Input	
5	Resolver 1 S4 (Cos-) / N.C.	Input	see note below
6	AGND		
7	Resolver / Synchro 1 REF+	Input	Excitation voltage input A1, A3 Adapter only Leave unconnected for A2, A4 Adapter
8	Resolver / Synchro 1 REF-	Input	
9	AGND		
10	Resolver / Synchro 1 VEL	Output	Velocity Voltage Output
11	NC		
12	AGND		
13	Resolver / Synchro 1 EXC+	Output	Excitation voltage output A2, A4 Adapter only
14	Resolver / Synchro 1 EXC-	Output	
15	AGND		
16	NC		
17	NC		
18	NC		
19	NC		
20	NC		
21	NC		
22	NC		
23	NC		
24	NC		
25	Resolver 2 S3 (Sin+) / Synchro 2 S3	Input	
26	Resolver 2 S1 (Sin-) / Synchro 2 S1	Input	see note below
27	AGND		
28	Resolver 2 S2 (Cos+) / Synchro 2 S3	Input	
29	Resolver 2 S4 (Cos-) / N.C.	Input	see note below
30	AGND		
31	Resolver / Synchro 2 REF+	Input	Excitation voltage input A1, A3 Adapter only Leave unconnected for A2, A4 Adapter
32	Resolver / Synchro 2 REF-	Input	

Pin	Function Resolver / Synchro	Direction	Comment
33	AGND		
34	Resolver / Synchro 2 VEL	Output	Velocity Voltage Output
35	NC		
36	AGND		
37	Resolver / Synchro 2 EXC+	Output	Excitation voltage output A2, A4 Adapter only
38	Resolver / Synchro 2 EXC-	Output	
39	AGND		
40	NC		
41	NC		
42	NC		
43	NC		
44	NC		
45	NC		
46	NC		
47	NC		
48	NC		
49	NC		
50	NC		

Table 9-1 : Pin Assignment I/O Connector

Signal conditioning adapters specified as single ended for the resolver sin, cos signal inputs may require an additional AGND connection on the TIP150 I/O connector.

Single ended signal conditioning adapters shipped from Q2 2003 onward, provide an on board AGND connection for I/O pins 2, 5 (or 26, 29).
On these adapters the resolver sin-, cos- signals plugged on I/O pins 2, 5 (or 26, 29) are connected to AGND by the adapter. The resolver signals sin+, cos+ plugged on I/O pins 1, 4 (or 26, 29) become referenced to AGND.

Single Ended Signal Conditioning Adapters shipped before Q2 2003 require an additional external AGND connection for I/O pins 2, 5 (or 26, 29).
E.g. for a single ended adapter on channel 1, connect the resolver sin- signal and I/O pin 3 (AGND) to I/O pin 2 (sin-) and connect the resolver cos- signal and I/O pin 6 (AGND) to I/O pin 5 (cos-).