The Embedded I/O Company

TEWS TECHNOLOGIES

TIP600

16 Channel Digital Inputs

Version 1.1

User Manual

Issue 1.1.6

August 2014

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7
25469 Halstenbek, Germany www.tews.com
Phone: +49-(0)4101-4058-0
Fax: +49-(0)4101-4058-19
e-mail: info@tews.com

TIP600-10R

16 isolated digital inputs

This document contains information, which is proprietary to TEWS TECHNOLOGIES GmbH. Any reproduction without written permission is forbidden.

TEWS TECHNOLOGIES GmbH has made any effort to ensure that this manual is accurate and complete. However TEWS TECHNOLOGIES GmbH reserves the right to change the product described in this document at any time without notice.

TEWS TECHNOLOGIES GmbH is not liable for any damage arising out of the application or use of the device described herein.

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

©2014 by TEWS TECHNOLOGIES GmbH

All trademarks mentioned are property of their respective owners.

Issue	Description	Date
1.0	First Issue	July 1994
1.1	Technical Specification	April 1996
1.2	General Revision	April 2003
1.3	Added Description for IP Interrupt Line used	June 2004
1.4	New address TEWS LLC	September 2006
1.1.5	New notation of User Manual Issue	March 2009
1.1.6	General Revision	August 2014

Table of Contents

List of Figures

List of Tables

1 Product Description

The TIP600 is an IndustryPack® compatible module providing 16 digital inputs for 24 volt high level input voltages.

The 16 digital inputs are galvanically isolated by optocouplers. The individual inputs are potential free in relation to each other and can be activated in both polarities.

All inputs have an electronic debounce circuit with a programmable debounce time.

The TIP600 uses the Z8536 programmable I/O controller. It is configured to take advantage of the Z8536 interrupt handling capability. All inputs can generate an interrupt. The signal edge handling is programmable. For systems with particularly fast reaction, each input can be assigned to its own interrupt vector.

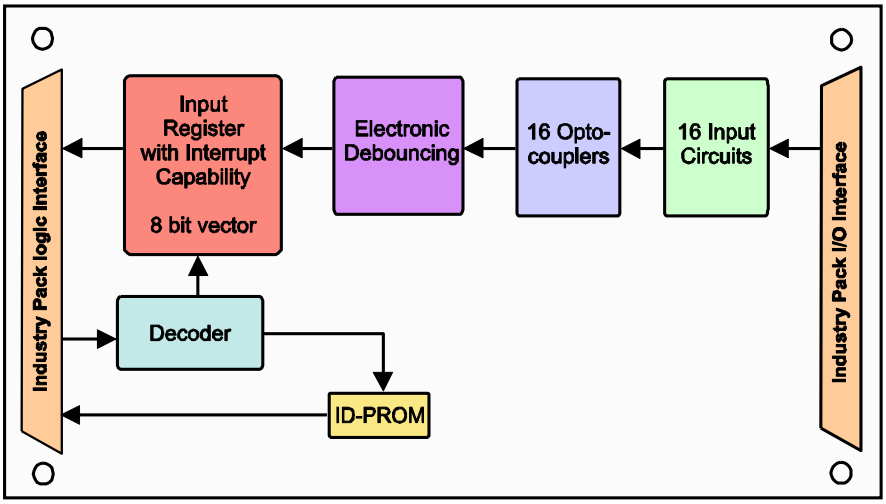

Figure 1-1 : Block Diagram

2 Technical Specification

Logic Interface	Single Size IndustryPack® Logic (8MHz)	
I/O Interface	50-conductor flat cable	
Number of Inputs	16, each input can generate an interrupt at programmable signal transition	
Input Isolation	All channels are isolated completely independent from each other	
Input Voltage	24V DC	
Input Current	4.2mA typical @+24V	
Input Switching Level	12V typical (minimum 9V, maximum 13V)	
Input Signal Debouncing	Electronic debouncing with programmable debounce time (9µs to 520ms)	
Interrupts	Each input can generate an interrupt at programmable signal transition. Interrupts are mapped to the IP INTREQ0# line. The IP INTREQ1# line is not used.	
Wait States	IDPROM: 0 wait state I/O (Z85536 CIO): minimum 4 wait states	
Power Requirements	230mA typical @+5V (all inputs active)	
Temperature Range	Operating Storage	0 °C to +70 °C -45°C to +125°C
MTBF	360925h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	27 g	
Transition Module	Optional (TIP001-TM-10)	

Table 2-1 : Technical Specification

3 ID PROM Content

Offset	Function	Content
0x01	ASCII ‘I’	0x49
0x03	ASCII ‘P’	0x50
0x05	ASCII ‘A’	0x41
0x07	ASCII ‘C’	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x04
0x0D	Revision	0x10
0x0F	Reserved	0x00
0x11	Driver-ID Low - Byte	0x00
0x13	Driver-ID High - Byte	0x00
0x15	Number of bytes used	0x0C
0x17	CRC	0xB6

Table 3-1 : ID PROM Content

4 IP Addressing

4.1 I/O Addressing

The TIP600 is accessed in the I/O space through the following set of four direct accessible registers implemented in the on board Z8536 I/O port controller:

Address	Symbol	Description	Size (Bit)
0x01	PORTC	Port C	8
0x03	PORTB	Port B input lines 1 to 8	8
0x05	PORTA	Port A input lines 9 to 16	8
0x07	CIOCSR	CIO Command and Status Register	8

Table 4-1 : Register Set

4.2 Indirect Addressable Registers

In addition to the above mentioned direct access registers the Z8536 CIO has 48 indirect addressable registers. These indirect addressable registers are used for the mode specification and for the control of the ports, and the counter/timers.

Not all of the indirect addressable registers are required for the operation of the TIP600.

Ind. ADDR	Name	Function	Size
0x00	MICR	Master Interrupt Control	8
0x01	MCCR	Master Configuration Control	8
0x02	PAIV	Port A Interrupt Vector	8
0x03	PBIV	Port B Interrupt Vector	8
0x04	CTIV	Counter / Timer Interrupt Vector	8
0x05	PCDP	Port C Data Path Polarity	8
0x06	PCDD	Port C Data Direction	8
0x07	PCSC	Port C Special I/O Control	8
0x08	PACS	Port A Control / Status	8
0x09	PBCS	Port B Control / Status	8
0x0A	C1CSR	Counter / Timer 1 Command / Status	8
0x0B	C2CSR	Counter / Timer 2 Command / Status	8
0x0C	C3CSR	Counter / Timer 3 Command / Status	8
0x0D	PADR	Port A Data Register	8
0x0E	PBDR	Port B Data Register	8
0x0F	PCDR	Port C Data Register	8
0x10	CT1CM	Counter / Timer 1 Current Count MSB	8
0x11	CT1CL	Counter / Timer 1 Current Count LSB	8
0x12	CT2CM	Counter / Timer 2 Current Count MSB	8
0x13	CT2CL	Counter / Timer 2 Current Count LSB	8
0x14	CT3CM	Counter / Timer 3 Current Count MSB	8

Ind. ADDR	Name	Function	Size
0x15	CT3CL	Counter / Timer 3 Current Count LSB	8
0x16	CT1PM	Counter /Timer 1 Preload MSB	8
0x17	CT1PL	Counter /Timer 1 Preload LSB	8
0x18	CT2PM	Counter /Timer 2 Preload MSB	8
0x19	CT2PL	Counter /Timer 2 Preload LSB	8
0x1A	CT3PM	Counter /Timer 3 Preload MSB	8
0x1B	CT3PL	Counter /Timer 3 Preload LSB	8
0x1C	CT1MO	Counter /Timer 1 Mode Specification	8
0x1D	CT2MO	Counter /Timer 2 Mode Specification	8
0x1E	CT3MO	Counter /Timer 3 Mode Specification	8
0x1F	CTCV	Counter /Timer Current Vector	8
0x20	PAMO	Port A Mode Specification	8
0x21	PAHS	Port A Handshake Specification	8
0x22	PADP	Port A Data Path Polarity	8
0x23	PADD	Port A Data Direction	8
0x24	PASC	Port A Special I/O Control	8
0x25	PAPP	Port A Pattern Polarity	8
0x26	PAPT	Port A Pattern Transition	8
0x27	PAPM	Port A Pattern Mask	8
0x28	PBMO	Port B Mode Specification	8
0x29	PBHS	Port B Handshake Specification	8
0x2A	PBDP	Port B Data Path Polarity	8
0x2B	PBDD	Port B Data Direction	8
0x2C	PBSC	Port B Special I/O Control	8
0x2D	PBPP	Port B Pattern Polarity	8
0x2E	PBPT	Port B Pattern Transition	8
0x2F	PBPM	Port B Pattern Mask	8

Table 4-2 : Z8536 CIO Indirect Addressable Registers

The access to the indirect addressable register is controlled by a state machine and a hidden pointer register. The state machine takes 3 different states, RESET state, state ”0” or state ”1”.

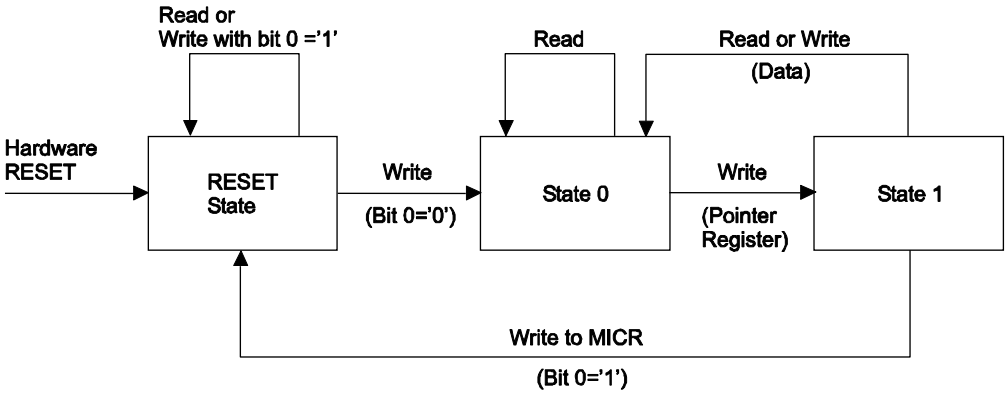

Figure 4-1 : CIO State Machine

A hardware reset will put the state machine into the RESET state. In the RESET state it is only possible to read or write the RESET bit (bit 0) in the Master Interrupt Control Register (MICR). A write access with the RESET bit (bit 0) = 0 will put the state machine into state ”0”.

Writing in state ”0” loads the internal pointer register with the internal register address to select the chosen register. This will put also the state machine into state ”1”.

A read or write access in state ”1” will transfer data from or to the internal register which was selected by the pointer register. Any access to the internal registers puts the state machine back into state ”0”.

Any read in state ”0” returns the contents of the last register pointed to. Therefore, a register can be read continuously without writing to the pointer again.

Outside the RESET state any read will put the state machine into state ”0”. So a dummy read can be used to bring the state machine in this known state.

If the state machine is in state ”1”, some of the Z8536 CIO internal operations are disabled. So the state machine should not be left in state ”1” longer as necessary.

Direct accesses to the data register PORTA, PORTB and PORTC have no consequence for the status of the state machine.

5 Functional Description

5.1 Digital Inputs

5.1.1 Optical Isolation

The TIP600-10R provides 16 digital inputs. The standard signal level for these inputs is 24V DC. The switching level of the inputs is between 9 and 13 volts. All input channels are isolated by AC optocoupler and are also isolated against each other. The use of AC optocoupler makes the operation of the inputs independent from signal polarity.

5.1.2 Digital Filtering

A digital filter circuit is provided for input switch debouncing. The debounce time is programmable by port C and counter/timer 3 of the Z8536 CIO in a range from 9 µs to 520 ms.

As long as bit 3 of port C is set to “1”, which is also the default setting after a reset, the TIP600 operates with a minimum debounce time of 9 µs.

To use a programmed debounce time the preload register of counter/timer 3 must be loaded with a value, which is computed by the following formula:

Preload value = debounce time in ms * 125

The programmable debounce time is enabled by setting bit 3 of port C to “0”.

5.1.3 Input and Interrupt Logic

The input and interrupt logic is implemented in the Z8536 port controller circuit. The digitally filtered input signals are connected with port A and port B of the Z8536. The input lines 1 to 8 are wired to port B and the input lines 9 to 16 are wired to port A.

Interrupt generation can be individually programmed for each channel and input transition.

A software initialization of the Z8536 is required before the input states can be read at port A and port B.

6 Programming

After power up or system reset the Z8536 CIO is in its initial state and the I/O ports A, B, C are disabled and configured to output direction. For normal operation of the TIP600 a minimum software initialization is required.

6.1 Required Software Initialization

The input lines of the TIP600 are connected to the port B of the Z8536 CIO. This port has to be configured as input and because of the inverting function of the optocouplers the input polarity has to be set to inverting.

To perform this required software initialization sees the following procedure:

- write 0x00 to CIOCSR
  write 0x01 to CIOCSR
  write 0x00 to CIOCSR
  this sequence puts the CIO Z8536 into a known (reset) state
- write 0x23 to CIOCSR
  this selects the Port A Data Direction Register (PADD) for the next operation
- write 0xFF to CIOCSR
  writing 0xFF into PADD will configure all bits of port A as inputs
- write 0x22 to CIOCSR
  this selects the Port A Data Path Polarity Register (PADP) for the next operation
- write 0xFF to CIOCSR
  writing 0xFF into PADP will configure all bits of port A to be inverted
- write 0x2B to CIOCSR
  this selects the Port B Data Direction Register (PBDD) for the next operation
- write 0xFF to CIOCSR
  writing 0xFF into PBDD will configure all bits of port B as inputs
- write 0x2A to CIOCSR
  this selects the Port B Data Path Polarity Register (PBDP) for the next operation
- write 0xFF to CIOCSR
  writing 0xFF into PBDP will configure all bits of port B to be inverted
- write 0x01 to CIOCSR
  this selects the Master Configuration Control Register (MCCR) for the next operation
- write 0x84 to CIOCSR
  writing 0x84 into MCCR will enable port A and B

After this sequence the directly accessible port registers PORTA and PORTB can be used for reading the actual status of the TIP600 input.

6.2 Programming of debounce time

On the TIP600 port C and counter timer 3 of the Z8536 are wired in way, that they can be used to generate a programmable debounce time.

For programming debounce time proceed as follow:

- write 0x1E to CIOCSR
  this selects the Counter/Timer 3 Mode Specification Register (CT3MO) for the next operation
- write 0xE0 to CIOCSR
  writing 0xE0 into CT3MO will configure counter/timer 3 to continuous cycle, external output, external clock
- write 0x1A to CIOCSR
  this selects the Counter/Timer 3 Preload MSB Register (CT3PM) for the next operation
- write 0xF0 to CIOCSR
  writing 0x04 into CT3PM will load the first half of the debounce time of '0x04E2' which is just an example for approximately 10 ms
- write 0x1B to CIOCSR
  this selects the Counter/Timer 3 Preload LSB Register (CT3PL) for the next operation
- write 0xE2 to CIOCSR
  writing 0xE2 into CT3PL will load the second half of the debounce time of '0x04E2' which is just an example for approximately 10 ms
- write 0x06 to CIOCSR
  this selects the Port C Data Direction Register (PCDD) for the next operation
- write 0x02 to CIOCSR
  writing 0x02 into PCDD configures bit 1 as an input for counter
- write 0x01 to CIOCSR
  this selects the Master Configuration Control Register (MCCR) for the next operation
- write 0x94 to CIOCSR
  writing 0x94 into MCCR will enable port A, B and C and counter/timer 3
- write 0x0F to CIOCSR
  this selects the Port C Data Register (PCDR) for the next operation
- write 0x70 to CIOCSR
  writing 0x70 into PCDR configures bit 3 as an writable output
- write 0x0C to CIOCSR
  this selects the Counter/Timer 3 Command and Status Register (C3CSR) for the next operation
- write 0x06 to CIOCSR
  writing 0x06 into C3CSR runs counter timer 3
- write 0x00 to PORTC
  writing 0x00 to PORTC will enable the programmable debounce time

7 Installation

7.1 Input Wiring

Each input is optically isolated from the logic circuit. Each input is independent of the other inputs and can be wired different. Each input has two connections at the IP I/O connector, Input x + and Input x -. However the TIP600 has AC optocoupler at the input side. Therefore the polarity of the input signal may be in either way.

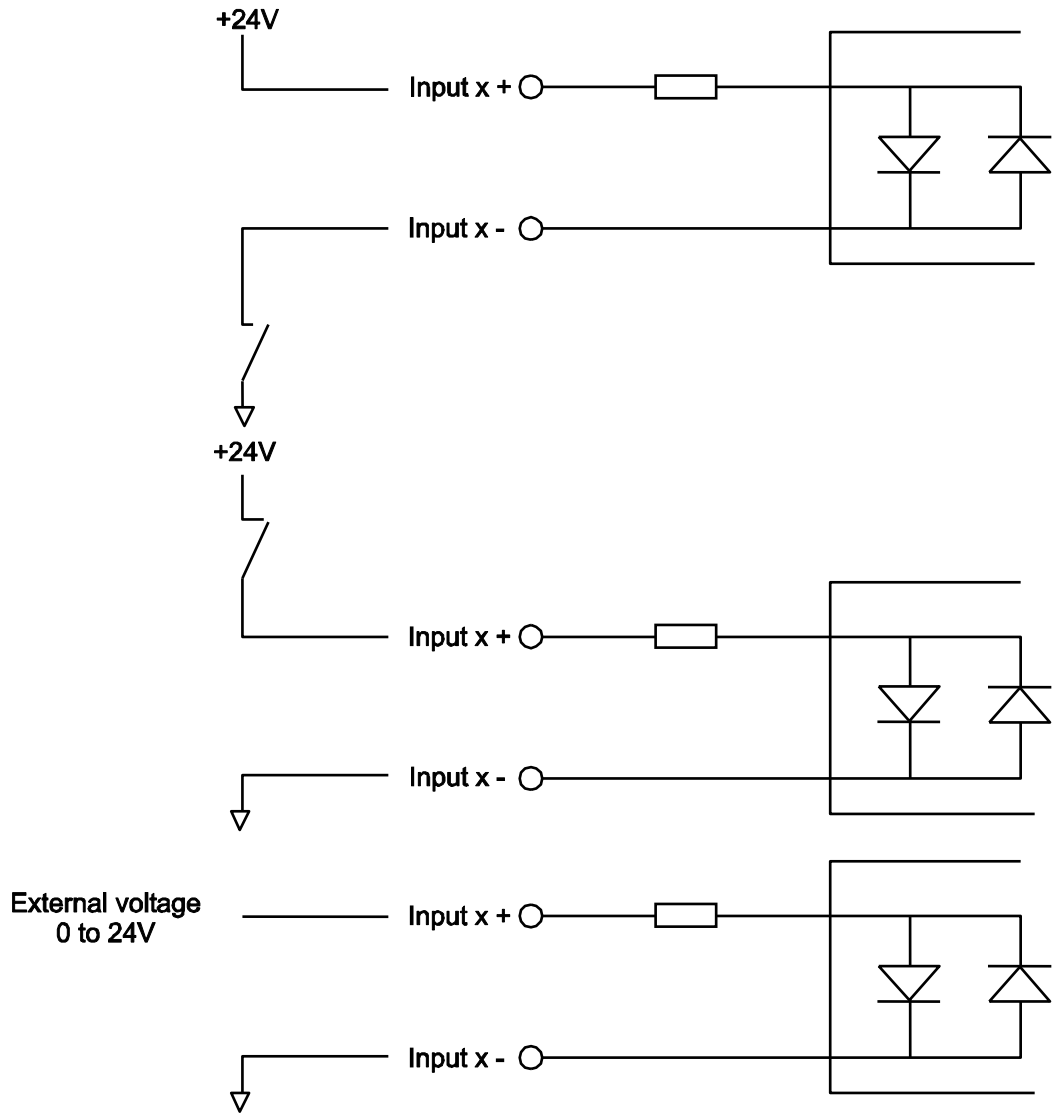

Figure 7-1 : Input Wiring Options

8 Pin Assignment – I/O Connector

Pin	Function
1	Input 1 +
2	Input 1 -
3	Input 2 +
4	Input 2 -
5	Input 3 +
6	Input 3 -
7	Input 4 +
8	Input 4 -
9	Input 5 +
10	Input 5 -
11	Input 6 +
12	Input 6 -
13	Input 7 +
14	Input 7 -
15	Input 8 +
16	Input 8 -
17	Input 9 +
18	Input 9 -
19	Input 10 +
20	Input 10 -
21	Input 11 +
22	Input 11 -
23	Input 12 +
24	Input 12 -
25	Input 13 +
26	Input 13 -
27	Input 14 +
28	Input 14 -
29	Input 15 +
30	Input 15 -
31	Input 16 +
32	Input 16 -

Table 8-1 : Input I/O Connection