The Embedded I/O Company

TEWS TECHNOLOGIES

TIP812-20

SERCOS IP with 2 Encoder Interfaces

Version 1.0

User Manual

Issue 1.0.4

August 2014

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7
25469 Halstenbek, Germany www.tews.com
Phone: +49-(0)4101-4058-0
Fax: +49-(0)4101-4058-19
e-mail: info@tews.com

TIP812-20

SERCOS Controller IP with 2 Encoder Interfaces

TIP812-TM-20

Transition Module with SERCOS RS485 + optical transceiver and encoder signal receiver

TIP812-TM-21

Transition Module with SERCOS RS485 + optical transceiver and optical isolated encoder signal receiver

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	January 1998
1.1	General Revision	June 2003
1.2	SERCON816 Sercos Controller	October 2004
1.3	New address TEWS LLC	September 2006
1.0.4	General Revision	August 2014

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1 Product Description

The TIP812-20 IP provides a complete SERCOS bus interface using the SERCON816 SERCOS interface controller in SERCON410B compatible mode, plus two encoder interface ports (incremental encoder, X4 Quadrature input, 8 bit encoder counter) to support hand wheel functionality.

For the SERCOS interface the TIP812-20 supports both physical interfaces, RS485 and optical fiber. The RS485 and optical transceivers are located on the TIP812-TM-2x Transition Module which is required for the TIP812-20.

The encoder interface on the TIP812-20 supports RS422 or TTL signals. The encoder interface receivers are located on the TIP812-TM-20 Transition Module.

On the TIP812-TM-21 Transition Module the encoder interface is optically isolated from the system logic.

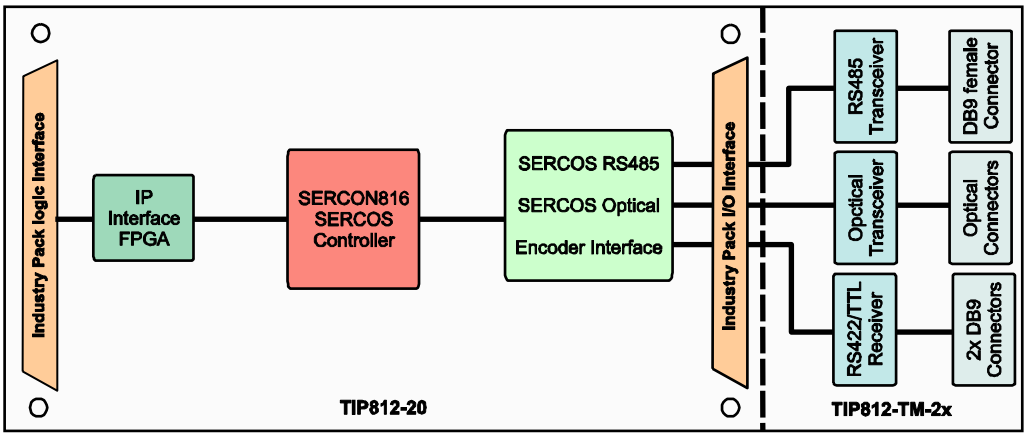

Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I	
I/O Space	Used (0 wait states)	
Memory Space	Used (1 wait state)	
Interrupts	INT0 used (SERCON816 INT0), INT1 used (SERCON816 INT1)	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
On Board Devices		
SERCOS Controller	TIP812-20 : SERCON816 (SERCON410B compatible mode only)	
RS485 Transceiver	TIP812-TM-2x : ADM485-AR	
Optical Transceiver	TIP812-TM-2x : HFBR-1604, HFBR-2602	
Encoder Counter (2 Ports)	X4 Quadrature 8 bit Up/Down counter for incremental encoders with overflow/underflow flags.	
I/O Interface		
Physical Interface	TIP812-TM-2x : SERCOS RS485 interface, SERCOS optical fiber interface, encoder RS422 / TTL interface (optically isolated for TIP812-TM-21)	
Interface Connector	TIP812-20 : 50-conductor flat cable for TIP812-TM-2x TIP812-TM-2x : DB9 (SERCOS RS485 interface), HFBR-1604/2602 (SERCOS optical interface), 2 x DB9 (encoder interface)	
Physical Data		
Power Requirements	TIP812-20: 75mA typical @ +5V DC TIP812-TM-2x: 45mA typical @ +5V DC	
Temperature Range	Operating Storage	-40 °C to +85 °C -45°C to +125°C
MTBF	TIP812-20 : 751000 h TIP812-TM-20 : 501000 h TIP812-TM-21 : 526000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	TIP812-20: 50 g TIP812-TM-2x: 200 g	

Figure 2-1 : Technical Specification

3 Functional Description

The TIP812-20 SERCOS IP implements a SERCOS communication interface by using the SERCON816 controller in SERCON410B compatible mode. The SERCOS interface is a digital interface for communication between systems which have to exchange information cyclically at short, fixed intervals (65µsec to 65msec). It is appropriate for the synchronous operation of distributed control or test equipment (e.g. connection between drives and numeric control).

A SERCOS interface communication system consists of one master and several slaves. These units are connected by an optical fiber ring. This ring starts and ends at the master. The slaves regenerate and repeat their received data or send their own telegrams. By this method the telegrams sent by the master are received by all slaves while the master receives data telegrams from the slaves. The optical fiber assures a reliable high-speed data transmission with excellent noise immunity.

The TIP812-20 SERCOS IP interface contains all the hardware-related functions of the SERCOS interface and considerably reduces the hardware costs and the computing time requirements of the host CPU. It is the direct link between the electric-optical receiver and transmitter and the host CPU that executes the control algorithms. The TIP812-20 SERCOS IP can be used for both, SERCOS interface masters and slaves.

The serial interface operates at data rates up to 4 Mbaud. A dual ported RAM (1024 * 16 bit) is used for control and communication data exchange between the TIP812-20 SERCOS IP and the host CPU. The organization of the memory is flexible.

The telegram processing of cyclic data is automatically controlled by the TIP812-20 IP. The transmission of service channel information over several communication cycles is executed automatically.

Furthermore the TIP812-20 implements two 8 bit – X4 Quadrature mode counter for incremental encoder signals.

Since this is an X4 Quadrature Counter, the signal change of any Encoder Signal Phase (A or B) will be counted. In case of a leading Phase A signal the counting-direction is up, otherwise down. Overflow and underflow conditions are signed by flags.

4 ID ROM Contents

Offset	Description	Value
0x01	ASCII ‘I’	0x49
0x03	ASCII ‘P’	0x50
0x05	ASCII ‘A’	0x41
0x07	ASCII ‘C’	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x15
0x0D	Revision	0x10
0x0F	Reserved	0x00
0x11	Driver-ID Low-byte	0x00
0x13	Driver-ID High-byte	0x00
0x15	Number of bytes used	0x0D
0x17	CRC	0x22
0x19	Version	0x14

Figure 4-1 : ID ROM Contents

5 IP Addressing

The TIP812-20 IP is accessed through a set of direct accessible registers.

The SERCON816 registers and other additional registers are accessible in the IP I/O address space.

The lower 1024 * 16 bit of the SERCON816 dual ported RAM area is accessible in the IP MEM address space (SERCON410B compatible mode).

5.1 SERCON816 Registers

Offset	Symbol	Description	Size (bit)
0x00	VERSION	See SERCON816 Reference Manual	16
0x02	REG01	See SERCON816 Reference Manual	16
0x04	REG02	See SERCON816 Reference Manual	16
0x06	REG03	See SERCON816 Reference Manual	16
0x08	REG04	See SERCON816 Reference Manual	16
0x0A	REG05	See SERCON816 Reference Manual	16
0x0C	REG06	See SERCON816 Reference Manual	16
0x0E	REG07	See SERCON816 Reference Manual	16
0x10	REG08	See SERCON816 Reference Manual	16
0x12	REG09	See SERCON816 Reference Manual	16
0x14	REG0A	See SERCON816 Reference Manual	16
0x16	REG0B	See SERCON816 Reference Manual	16
0x18	REG0C	See SERCON816 Reference Manual	16
0x1A	REG0D	See SERCON816 Reference Manual	16
0x1C	REG0E	See SERCON816 Reference Manual	16
0x1E	TSCYC0	See SERCON816 Reference Manual	16
0x20	TSCYC1	See SERCON816 Reference Manual	16
0x22	TCYCDEL	See SERCON816 Reference Manual	16
0x24	TCNTLT	See SERCON816 Reference Manual	16
0x26	TCNTST	See SERCON816 Reference Manual	16
0x28	TCYCSTART	See SERCON816 Reference Manual	16
0x2A	JTSCYC1	See SERCON816 Reference Manual	16
0x2C	JTSCYC2	See SERCON816 Reference Manual	16
0x2E	PROGERR	See SERCON816 Reference Manual	16
0x30	JTRDEL1	See SERCON816 Reference Manual	16
0x32	JTRDEL2	See SERCON816 Reference Manual	16
0x34	TINT0	See SERCON816 Reference Manual	16
0x36	TINT1	See SERCON816 Reference Manual	16
0x38	TINT2	See SERCON816 Reference Manual	16
0x3A	TINT3	See SERCON816 Reference Manual	16
0x3C	TDIVCLK	See SERCON816 Reference Manual	16

Offset	Symbol	Description	Size (bit)
0x3E	DTDIVCLK	See SERCON816 Reference Manual	16
0x40	REG20	See SERCON816 Reference Manual	16
0x42	THTPT	See SERCON816 Reference Manual	16
0x44	THT	See SERCON816 Reference Manual	16
0x46	THWPT	See SERCON816 Reference Manual	16
0x48	THW	See SERCON816 Reference Manual	16
0x4A	REG25	See SERCON816 Reference Manual	16
0x4C	THR	See SERCON816 Reference Manual	16
0x4E	FIFO	See SERCON816 Reference Manual	16

Figure 5-1 : SERCON816 Registers

5.2 Additional Registers

Offset	Description	Size (bit)	Access
0x50	Encoder Counter 1	16	R/W
0x52	Encoder Counter 2	16	R/W
…	-	-	-
0x61	Interrupt Vector	8	R/W
…	-	-	-
0x71	Master Synchronization CLK Enable	8	R/W

Figure 5-2 : Additional Registers

5.2.1 Encoder Counter Register

Bit	Description
15:10	Unused. Always read as '0'.
9	Underflow Flag Underflow flag for the 8 bit counter. If an underflow occurs while the overflow flag is set, the overflow flag will be cleared and the underflow flag will not be set.
8	Overflow Flag Overflow flag for the 8 bit counter. If an overflow occurs while the underflow flag is set, the underflow flag will be cleared and the overflow flag will not be set.
7:0	8 Bit Encoder Counter Value Since this is an X4 Quadrature counter, the signal change of any Encoder Signal Phase (A or B) will be counted. In case of a leading Phase A signal the counting direction is up, otherwise down. In case of read-access the overflow and underflow flags are cleared (after read-out), while the encoder counter value remains unchanged. Any write-access to an Encoder Counter Register clears the 8 bit encoder counter value and the overflow and underflow flag.

Figure 5-3 : Encoder Counter Register

5.2.2 Interrupt Vector Register

The Interrupt Vector Register is used for reading the IP modules interrupt vector during an interrupt acknowledge cycle.

Bit	Description
7:1	Higher 7 bits of interrupt vector. Must be set by the user.
0	Ignored for write access. Indicates interrupt source for interrupt acknowledge cycle (if indicated by the carrier board on address line A1) : 0 : IntReq0# (SERCON816 INT0 signal) 1 : IntReq1# (SERCON816 INT1 signal)

Figure 5-4 : Interrupt Vector Register

5.2.3 Master Sync Clock Enable Register

Used for the RS485 interface only. Not used for the optical interface.

Bit	Description
7:1	Ignored for write access. Undefined for read access.
0	Controls the transmission of the SERCON Master Sync Clock (SERCON816 CON_CLK signal) for the RS485 interface. 0 : Sync Clock transmission disabled 1 : Sync Clock transmission enabled

Figure 5-5 : Master Sync Clock Enable Register

6 Jumper Configuration

6.1 IP Module Configuration

There are no jumper configuration features on the TIP812-20 IP.

6.2 Transition Module Configuration

Jumpers J1, J2, J3 are for the SERCOS RS485 interface only.

Jumper J4 selects the SERCOS interface type (RS485 or optical).

Jumper	Comment	Installed	Function
J1	SERCOS RS485 Interface X1 Pin 1 Assignment (Shield)	1-2	X1 Pin 1 = X1 Pin 5 (RGND)
		2-3	X1 Pin 1 = DB Case
J2	SERCOS RS485 Interface Master Sync CLK Termination	1-2	Termination ON (120Ω)
		2-3	Termination OFF
J3	SERCOS RS485 Interface Data Termination	1-2	Termination ON (120Ω)
		2-3	Termination OFF
J4	SERCOS Interface Select	1-3, 2-4	RS485 Interface
		5-7, 6-8	Optical Fiber Interface

Figure 6-1 : Jumper Configuration

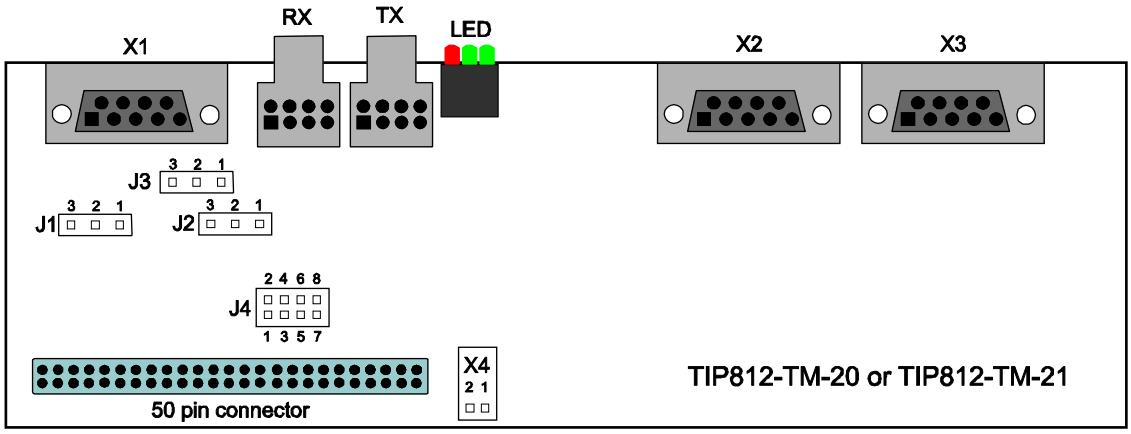

Figure 6-2 : Jumper Location

7 Pin Assignment

7.1 TIP812-20 IP Module

7.1.1 50 pin I/O Connector (IP)

Pin	Symbol	Description
25	ENC1A	Encoder 1 Signal Phase A
26	ENC1B	Encoder 1 Signal Phase B
27	ENC2A	Encoder 2 Signal Phase A
28	ENC2B	Encoder 2 Signal Phase B
30	TxD1	SERCOS Serial Interface Transmit (RS485)
31	RxD	SERCOS Serial Interface Receive
32	TxD_	SERCOS Serial Interface Transmit (Optical)
33	TxD_	SERCOS Serial Interface Transmit (Optical)
35	GND	System Logic Ground
36	GND	System Logic Ground
37	GND	System Logic Ground
38	+5V	System Logic VCC
39	+5V	System Logic VCC
40	+5V	System Logic VCC
42	IDLE#	SERCOS Data Transmission Enable
43	MASTER_SYNC	SERCOS Master Synchronization Clock Enable
44	CON_CLK	SERCOS Synchronization CLK Output
45	CYC_CLK	SERCOS Synchronization CLK Input
47	ERROR#	SERCOS LED Control
48	TRANSMIT_ACTIVE#	SERCOS LED Control
49	RECEIVE_ACTIVE#	SERCOS LED Control

Figure 7-1 : 50 pin I/O Connector (IP)

7.2 TIP812-2x Transition Module

7.2.1 50 pin I/O Connector (TM)

See 50 pin I/O Connector (IP) of TIP812-20.

7.2.2 Transition Module Connectors

SERCOS RS485 DB9 Female (X1)		
Pin-No.	**Function**	**Signal Level**
1	Shield	
2	NC	
3	SERCOS DATA Signal –	RS485
4	SERCOS MASTER SYNC CLK Signal –	RS485
5	RGND (coupled with 100 Ohm to system logic GND)	
6	NC	
7	NC	
8	SERCOS DATA Signal +	RS485
9	SERCOS MASTER SYNC CLK Signal +	RS485
Encoder-1 DB9 Female (X3)		
Pin-No.	**Function**	**Signal Level**
1	GND_ENC [2)]	
2	NC	
3	NC	
4	Encoder 1 PHASE B Signal +	RS422 / TTL
5	Encoder 1 PHASE A Signal +	RS422 / TTL
6	VCC_ENC	
7	NC	
8	Encoder 1 PHASE B Signal – [1)]	RS422 / --
9	Encoder 1 PHASE A Signal – [1)]	RS422 / --
Encoder-2 DB9 Female (X2)		
Pin-No.	**Function**	**Signal Level**
1	GND_ENC [2)]	
2	NC	
3	NC	
4	Encoder 2 PHASE B Signal +	RS422 / TTL
5	Encoder 2 PHASE A Signal +	RS422 / TTL
6	VCC_ENC	
7	NC	
8	Encoder 2 PHASE B Signal – [1)]	RS422 / --
9	Encoder 2 PHASE A Signal – [1)]	RS422 / --

Encoder Power Supply Source Connector (X4)		
Pin-No.	**Function**	**Signal Level**
1	GND_ENC [2)]	(Fused Max. 30V, 1A)
2	VCC_ENC	

Figure 7-2 : Transition Module Connectors

[1)] For the use of single-ended encoder signals with the TIP812-TM-20 encoder TTL interface, these pins must not be externally connected.

[2)] For the TIP812-TM-20 encoder RS422 / TTL interface, this signal is connected to System Logic GND on board.