

TIP813

LON Bus Interface based on Neuron Chip 3150

Version 1.0

User Manual

Issue 1.5

September 2006

D75813802

TEWS TECHNOLOGIES GmbH

Am Bahnhof 7
25469 Halstenbek, Germany
www.tews.com

Phone: +49-(0)4101-4058-0
Fax: +49-(0)4101-4058-19
e-mail: info@tews.com

TEWS TECHNOLOGIES LLC

9190 Double Diamond Parkway,
Suite 127, Reno, NV 89521, USA
www.tews.com

Phone: +1 (775) 850 5830
Fax: +1 (775) 201 0347
e-mail: usasales@tews.com

TIP813-10

LON bus RS485 interface

TIP813-TM-10

Transition Module for TIP813-10, optically isolated RS485

TIP813-20

LON bus 1.25 Mbit transformer interface

TIP813-21

LON bus 78 kbit transformer interface

TIP813-30

LON bus 78 kbit LON interface FTT-10A

This document contains information, which is proprietary to TEWS TECHNOLOGIES GmbH. Any reproduction without written permission is forbidden.

TEWS TECHNOLOGIES GmbH has made any effort to ensure that this manual is accurate and complete. However TEWS TECHNOLOGIES GmbH reserves the right to change the product described in this document at any time without notice.

TEWS TECHNOLOGIES GmbH is not liable for any damage arising out of the application or use of the device described herein.

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an 'Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W Write Only

R Read Only

R/W Read/Write

R/C Read/Clear

R/S Read/Set

©1995-2006 by TEWS TECHNOLOGIES GmbH

IndustryPack is a registered trademark of SBS Technologies, Inc

Issue	Description	Date
1.0	First Issue	July 1995
1.1	TIP813-TM-10 added	November 1995
1.2	Revision B	May 1997
1.3	TIP813-10 added	September 1999
1.4	General Revision	August 2003
1.5	New address TEWS LLC	September 2006

Table of Contents

1	PRODUCT DESCRIPTION	6
2	TECHNICAL SPECIFICATION.....	7
3	ID PROM CONTENTS	8
4	IP ADDRESSING.....	9
	4.1 I/O Addressing.....	9
	4.1.1 Semaphore Flag Register	9
	4.1.2 Local Reset Register.....	9
	4.1.3 Reset Status Register	10
	4.1.4 Interrupt Control Register.....	10
	4.1.5 Vector Register	10
	4.2 Memory Space Addressing.....	11
5	INSTALLATION TIP813	12
	5.1 Configuration of TIP813-10	12
	5.2 Configuration of TIP813-2x	12
	5.3 Configuration of TIP813-30	13
	5.3.1 LON Ports	14
6	INSTALLATION TIP813-TM-10.....	15
	6.1 Configuration of the TIP813-10.....	15
	6.2 Configuration of the TIP813-TM-10	15
	6.3 User Information TIP813-TM-10	15
7	PIN ASSIGNMENT – I/O CONNECTOR	16
	7.1 I/O Connection of TIP813-10	16
	7.2 I/O Connection of TIP813-2x	17
	7.3 I/O Connection of TIP813-30	18

Table of Figures

FIGURE 1-1 : BLOCK DIAGRAM.....	6
FIGURE 2-1 : TECHNICAL SPECIFICATION.....	7
FIGURE 3-1 : ID PROM CONTENTS	8
FIGURE 4-1 : REGISTER MAP	9
FIGURE 4-2 : LOCAL RESET REGISTER (LOCRES)	9
FIGURE 4-3 : RESET STATUS REGISTER (RESSTA)	10
FIGURE 4-4 : INTERRUPT CONTROL REGISTER (INTCSR)	10
FIGURE 4-5 : VECTOR REGISTER (VECTOR).....	10
FIGURE 5-1 : TIP813-10 INTERFACE CONFIGURATION	12
FIGURE 5-2 : TIP813-10 JUMPER LOCATION.....	12
FIGURE 5-3 : TIP813-30 TERMINATION AND LON PORT CONFIGURATION	13
FIGURE 5-4 : TIP813-30 JUMPER LOCATION.....	13
FIGURE 5-5 : LON PORT CONFIGURATION	14
FIGURE 6-1 : CONFIGURATION TIP813-TM-10	15
FIGURE 7-1 : PIN ASSIGNMENT I/O CONNECTOR TIP813-10.....	16
FIGURE 7-2 : PIN ASSIGNMENT I/O CONNECTOR TIP813-20 AND TIP813-21	17
FIGURE 7-3 : PIN ASSIGNMENT I/O CONNECTOR TIP813-30.....	18

1 Product Description

The TIP813 is an IndustryPack® compatible module and provides a complete LON interface using the NEURON Chip 3150.

The communication is handled via a 4Kbyte Dual Port RAM. A 32Kbyte EPROM is used to store the protocol firmware of the NEURON Chip 3150 and the application program. All modules have the protocol firmware and the MIP/DPR host interface software preinstalled.

Four kinds of on board physical interface are available:

- The TIP813-10 supports standard RS485 and power line interface
- The TIP813-20 supports a transformer-coupled 1.25Mbit interface
- The TIP813-21 supports a transformer-coupled 78kbit interface
- The TIP813-30 supports the free topology twisted pair interface based on the ECHELON FTT-10A transceiver

The complete network communication port of the NEURON Chip is routed to the IndustryPack I/O connector of the TIP813-10. This allows high flexibility to interface other physical media, i.e. optically isolated RS485 or power line interface by a separate transition module. The TIP813-TM-10 transition module with the TIP813-10 supports optically isolated standard RS485 on DB-9 connector.

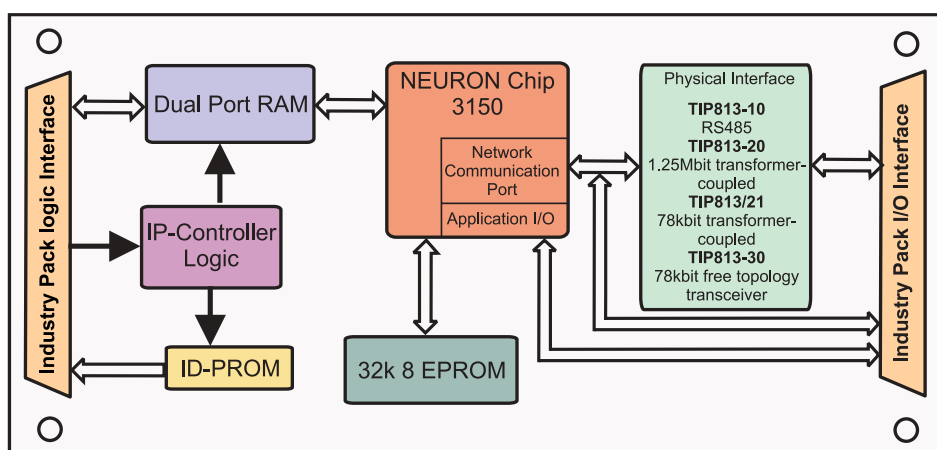


Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface	
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995
ID ROM Data	Format I
I/O Space	Used (no wait states)
Memory Space	Used (4kbyte) (no wait states)
Interrupts	Intreq0# used, Intreq1# not used
DMA	Not supported
Clock Rate	8MHz
Module Type	Type I
Functional Data	
LON Controller	NEURON Chip 3150
Firmware	MIP/DPR of ECHELON in EPROM, Run-Time-License included
Interface Type	TIP813-10: RS485 or direct connect TIP813-10 with TIP813-TM-10: optically isolated RS485 TIP813-20: Transformer coupled 1.25Mbit TIP813-21: Transformer coupled 78kbit TIP813-30: FFT-10A Transceiver
Network Speed	Selectable by software
Connecting Pins	500mA maximum current for each line
Interface Connector	50-conductor flat cable
Physical Data	
Power Requirements	TIP813-10: 230mA typical @ +5V DC TIP813-TM-10: 150mA typical @ +5V DC TIP813-20: 230mA typical @ +5V DC TIP813-21: 230mA typical @ +5V DC TIP813-30: 160mA typical @ +5V DC
Temperature Range	Operating 0 °C to +70 °C Storage -45°C to +125°C
MTBF	TIP813-10: 572000h TIP813-30: 603000h
Humidity	5 – 95 % non-condensing

Figure 2-1 : Technical Specification

3 ID Prom Contents

Offset	Function	Content
0x01	ASCII 'I'	0x49
0x03	ASCII 'P'	0x50
0x05	ASCII 'A'	0x41
0x07	ASCII 'C'	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x0E
0x0D	Revision	0x10
0x0F	Reserved	0x00
0x11	Driver-ID Low - Byte	0x00
0x13	Driver-ID High - Byte	0x00
0x15	Number of bytes used	0x0D
0x17	CRC	0xC6 (TIP813-10) 0x39 (TIP813-20) 0x18 (TIP813-21) 0x73 (TIP813-30)
0x19	Version	0x0A (TIP813-10) 0x14 (TIP813-20) 0x15 (TIP813-21) 0x1E (TIP813-30)

Figure 3-1 : ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP813 is accessible in the I/O space of the IP.

Address	Symbol	Description	Size (Bit)	Access
0x01	SEMFLG1	Semaphore Flag 1	8	
0x03	SEMFLG2	Semaphore Flag 2	8	
0x05	SEMFLG3	Semaphore Flag 3	8	
0x07	SEMFLG4	Semaphore Flag 4	8	
0x09	SEMFLG5	Semaphore Flag 5	8	
0x0B	SEMFLG6	Semaphore Flag 6	8	
0x0D	SEMFLG7	Semaphore Flag 7	8	
0x0F	SEMFLG8	Semaphore Flag 8	8	
0x11	LOCRES	Local Reset Register	8	W
0x21	RESSTA	Reset Status Register	8	R/C
0x31	INTCSR	Interrupt Control Register	8	W
0x41	VECTOR	Vector Register	8	R/W

Figure 4-1 : Register Map

4.1.1 Semaphore Flag Register

The Semaphore Flag Registers SEMFLG1 to SEMFLG8 are implemented in the TIP813 IDT71342 dual ported RAM device. The MIP/DPR firmware of the TIP813 makes use of these semaphores to synchronize the access to the data structure in the dual ported RAM between the host software and the MIP/DPR firmware (see also the Microprocessor Interface Program (MIP) User's Guide of ECHELON).

4.1.2 Local Reset Register

The write only Local Reset Register can be used to initiate a reset of the TIP813 under host software control.

A local reset will restart the MIP/DPR firmware of the TIP813.

Bit	Symbol	Description	Access	Reset Value
7:1		Not used		
0		0 : Run 1 : Activate local reset The local reset remains active until this bit is cleared by the host software.	W	0

Figure 4-2 : Local Reset Register (LOCRES)

4.1.3 Reset Status Register

The Reset Status Register is used to latch the reset event in bit 0. This flag is useful as a reset indication to the host software because the TIP813 can also be reset by network messages.

Bit	Symbol	Description	Access	Reset Value
7:1		Not used		
0		Reset Status 0 : Run 1 : Reset occurred This flag can be reset by a write to this register.	R/C	

Figure 4-3 : Reset Status Register (RESSTA)

4.1.4 Interrupt Control Register

The write only Interrupt Control Register is used to control the interrupt generation of the TIP813.

Bit	Symbol	Description	Access	Reset Value
7:1		Not used		
0		Interrupt Enable Control 0 : Interrupts disabled 1 : Interrupts enabled If set to '1', the MIP/DPR firmware can generate an interrupt to indicate the transfer of messages.	W	0

Figure 4-4 : Interrupt Control Register (INTCSR)

4.1.5 Vector Register

The Vector Register is a read/write register, which must be programmed with the required interrupt vector when interrupts are used with the TIP813.

Bit	Symbol	Description	Access	Reset Value
7:0		Interrupt Vector loaded by software	R/W	0x00

Figure 4-5 : Vector Register (VECTOR)

4.2 Memory Space Addressing

The TIP813 has a 4Kbit * 8 dual ported RAM. This RAM is used to exchange messages and commands between the host software and the MIP/DPR firmware running on the TIP813. The data structure is initialized by the MIP/DPR firmware as defined in the Microprocessor Interface Program (MIP) User's Guide of ECHELON.

5 Installation TIP813

5.1 Configuration of TIP813-10

The TIP813-10 LON IP is supporting two physical network layers RS485 and Direct Connect. There are two jumper blocks (J1 and J2) with five jumpers each which must be configured for the required physical layer.

Physical Interface	Jumper block J1	Jumper block J2
RS485	All jumper removed	All jumper installed
Direct Connect	All jumper installed	All jumper removed

Figure 5-1 : TIP813-10 interface configuration

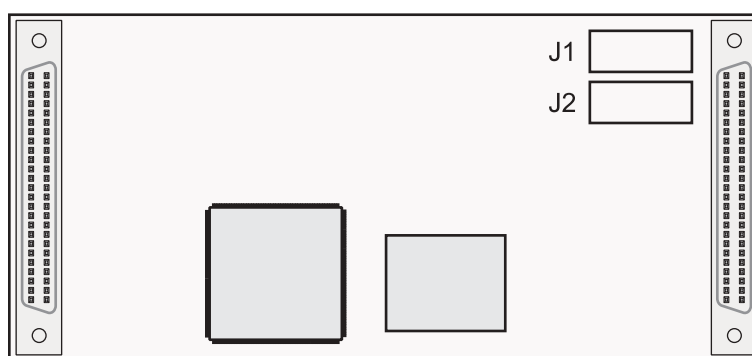


Figure 5-2 : TIP813-10 jumper location

5.2 Configuration of TIP813-2x

For the TIP813-20 and TIP813-21 there is no jumper to configure.

5.3 Configuration of TIP813-30

The TIP813-30 supports a configuration for the LON bus termination and possibility to disable one LON port.

The jumper block 'J1' configures the termination mode of the TIP813-30.

Termination	1 – 2	3 - 4
Termination with 52.5 ohms for singly-terminated bus topology	Close	Close
Termination with 105ohms for doubly-terminated bus topology	Open	Close
Termination with 105ohms for doubly-terminated bus topology	Close	Open
No termination on board	Open	Open

The jumper 'J2' and 'J3' can be used to disable the second LON port of the TIP813-30.

Function	J2	J3
LON Port 2 enable	Close	Close
LON Port 2 disable	Open	Open

The default condition is no termination and LON port 2 disabled.

Figure 5-3 : TIP813-30 Termination and LON Port configuration

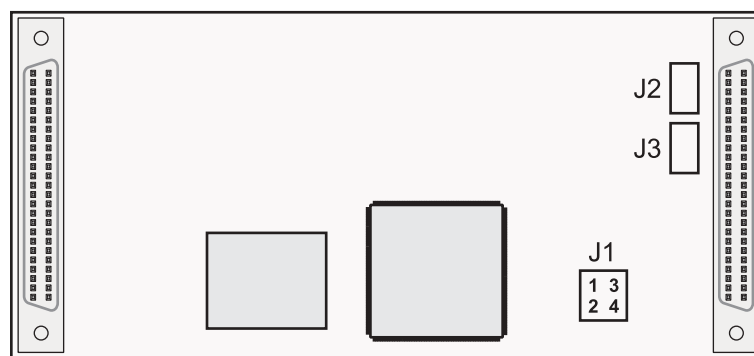


Figure 5-4 : TIP813-30 jumper location

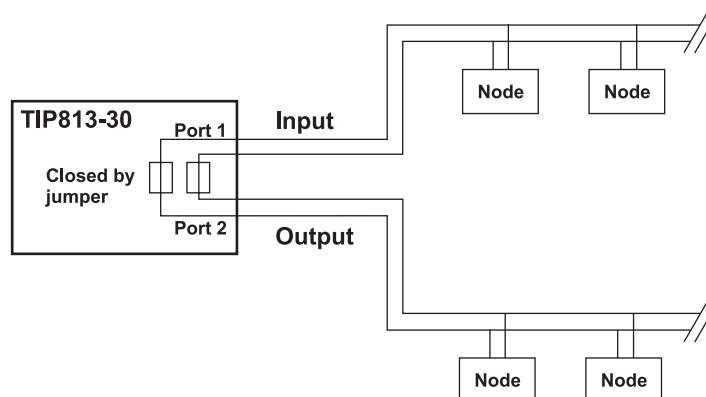
5.3.1 LON Ports

- The TIP813-30 supports one LON bus channel with two ports at the local connector (Port1 and Port2). The standard local connector is a 50-conductor flat cable. The pinning of this flat cable supports a direct connection to two DB9 connectors.
- In addition to NET_A and NET_B seven extra pins are routed on board from Port 1 to Port 2. These pins could be used for user specific signals (max. 500mA). But the main reason is the reduction of the stub-length between TIP813-30 and the LON-Net or a Transition Module. So the first LON port is used as 'LON Input' and the second port as 'LON Output'.
- If Port 2 is not used for the application, it must be disabled by open the connection for NET_A and NET_B (two jumpers, one for each net). This is necessary to cut off the unused LON-Net leads from Port 2.

The Port 1 is always enabled and two different LON connections are available.

Examples:

Port 1 and Port 2 enabled:



Only Port 1 enabled and Port 2 completely inactive:

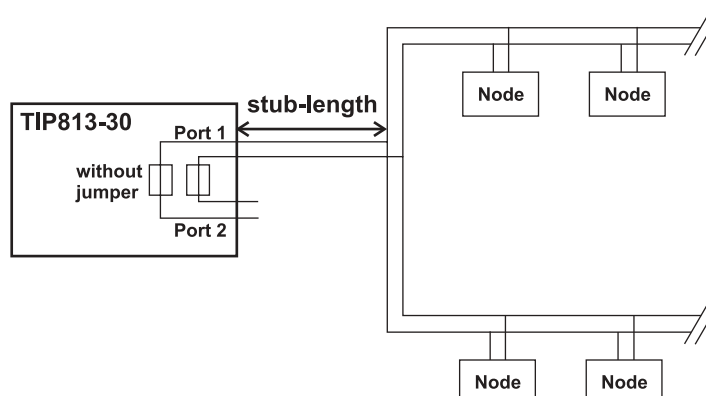


Figure 5-5 : LON Port Configuration

6 Installation TIP813-TM-10

The TIP813-TM-10 Transition Module will be connected with a 50-pin flat cable to the IP I/O interface of the TIP813-10. The TIP813-TM-10 supports isolated RS485 on a DB9 connector.

6.1 Configuration of the TIP813-10

All jumpers of the jumper blocks J1 and J2 of the TIP813-10 must be removed if using the TIP813-10 with the TIP813-TM-10 Transition Module (removing all jumpers on the TIP813-10 disables the physical interface of the TIP813-10).

6.2 Configuration of the TIP813-TM-10

If jumper J1 on the Transition Module TIP813-TM-10 is installed, the RS485 is terminated by a 120 ohm resistor. Jumper J1 must only be installed if the TIP813-TM-10 is located at one end of the RS485 bus.

Resistor R1 connects the DB9 connector case to the board CASE_GND.

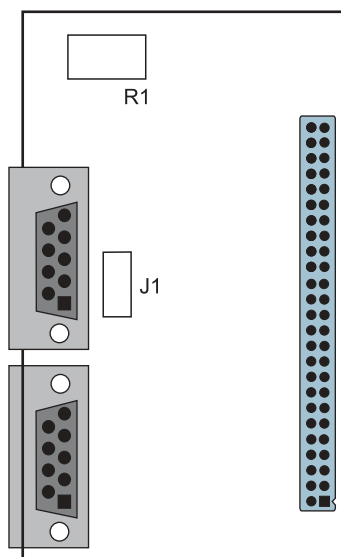


Figure 6-1 : Configuration TIP813-TM-10

6.3 User Information TIP813-TM-10

The 'Service' LED located in the TIP813-TM-10 front panel is switched on by the TIP813-10 firmware when the NEURON Chip has not been configured with network address information.

Pushing the 'Service Request' button in the TIP813-TM-10 front panel causes the TIP813-10 NEURON Chip to transmit a network management message containing its 48 bit unique ID on the network. This information may then be used by a network management device to install and configure the node.

7 Pin Assignment – I/O Connector

7.1 I/O Connection of TIP813-10

Pin	Function	Comment	Pin	Function	Comment
1	GND		26	Not used	
2	+5V		27	Not used	
3	GND		28	Not used	
4	+12V		29	Not used	
5	GND		30	Not used	
6	-12V		31	Not used	
7	Not used		32	Not used	
8	SERVICE#	Service request pin	33	LON_DIRECT +	
9	Not used		34	LON_DIRECT -	
10	I/O9	Parallel I/O Port of 3150	35	GND	
11	I/O8	Parallel I/O Port of 3150	36	GND	
12	I/O7	Parallel I/O Port of 3150	37	LON_DIRECT +	
13	I/O6	Parallel I/O Port of 3150	38	LON_DIRECT -	
14	I/O5	Parallel I/O Port of 3150	39	GND	
15	I/O4	Parallel I/O Port of 3150	40	GND	
16	I/O3	Parallel I/O Port of 3150	41	Not used	
17	I/O2	Parallel I/O Port of 3150	42	Not used	
18	I/O1	Parallel I/O Port of 3150	43	LON_RS485 +	
19	I/O0	Parallel I/O Port of 3150	44	LON_RS485 -	
20	Not used		45	GND	
21	CP4	Communication Port of 3150	46	GND	
22	CP3	Communication Port of 3150	47	LON_RS485 +	
23	CP2	Communication Port of 3150	48	LON_RS485 -	
24	CP1	Communication Port of 3150	49	GND	
25	CP0	Communication Port of 3150	50	GND	

Figure 7-1 : Pin Assignment I/O Connector TIP813-10

7.2 I/O Connection of TIP813-2x

Pin	Function	Comment	Pin	Function	Comment
1	GND		26	Case GND	Pin must be connected to CASE Ground !
2	+5V		27	Case GND	Pin must be connected to CASE Ground !
3	GND		28	Not used	
4	SERVICE	Service request pin	29	Not used	
5	I/O 0	Parallel I/O Port LON controller	30	Not used	
6	Not used		31	Not used	
7	Not used		32	Not used	
8	Not used		33	Miscellaneous	Connected to pin 42
9	Not used		34	Miscellaneous	Connected to pin 43
10	Not used		35	LON_DATA B	
11	Not used		36	LON_DATA A	
12	Not used		37	Miscellaneous	Connected to pin 46
13	Not used		38	miscellaneous	Connected to pin 47
14	Not used		39	miscellaneous	Connected to pin 48
15	Not used		40	Miscellaneous	Connected to pin 49
16	Not used		41	Miscellaneous	Connected to pin 50
17	Not used		42	Miscellaneous	Connected to pin 33
18	Not used		43	Miscellaneous	Connected to pin 34
19	Not used		44	LON_DATA B	
20	Not used		45	LON_DATA A	
21	Not used		46	Miscellaneous	Connected to pin 37
22	Not used		47	Miscellaneous	Connected to pin 38
23	Not used		48	Miscellaneous	Connected to pin 39
24	Not used		49	Miscellaneous	Connected to pin 40
25	Not used		50	miscellaneous	Connected to pin 41

Figure 7-2 : Pin Assignment I/O Connector TIP813-20 and TIP813-21

7.3 I/O Connection of TIP813-30

Pin	Function	Comment	Pin	Function	Comment
1	GND		26	Case GND	Pin must be connected to CASE Ground !
2	+5V		27	Case GND	Pin must be connected to CASE Ground !
3	GND		28	Not used	
4	SERVICE	Service request pin	29	Not used	
5	I/O 0	Parallel I/O Port LON controller	30	Not used	
6	Not used		31	Not used	
7	Not used		32	Not used	
8	Not used		33	Miscellaneous	Connected to pin 42 Port 1
9	Not used		34	Miscellaneous	Connected to pin 43 Port 1
10	Not used		35	NET_B	Port 1
11	Not used		36	NET_A	Port 1
12	Not used		37	Miscellaneous	Connected to pin 46 Port 1
13	Not used		38	Miscellaneous	Connected to pin 47 Port 1
14	Not used		39	Miscellaneous	Connected to pin 48 Port 1
15	Not used		40	Miscellaneous	Connected to pin 49 Port 1
16	Not used		41	Miscellaneous	Connected to pin 50 Port 1
17	Not used		42	Miscellaneous	Connected to pin 33 Port 2
18	Not used		43	Miscellaneous	Connected to pin 34 Port 2
19	Not used		44	NET_B	Port 2
20	Not used		45	NET_A	Port 2
21	Not used		46	Miscellaneous	Connected to pin 37 Port 2
22	Not used		47	Miscellaneous	Connected to pin 38 Port 2
23	Not used		48	Miscellaneous	Connected to pin 39 Port 2
24	Not used		49	Miscellaneous	Connected to pin 40 Port 2
25	Not used		50	Miscellaneous	Connected to pin 41 Port 2

Figure 7-3 : Pin Assignment I/O Connector TIP813-30

The pins 33, 34, 37, 38, 39, 40, 41 and the corresponding pins (42, 43, 46, 47, 48, 49, and 50) are not used by the TIP813. These connections are for external applications.