The Embedded I/O Company

TEWS TECHNOLOGIES

TIP815

ARCNET Controller

Version 1.0

User Manual

Issue 1.0.8

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TIP815-10R

ARCNET Traditional Hybrid Interface (2.5 Mbps) (20 MHz Clock Source)

TIP815-11R

ARCNET Traditional Hybrid Interface (2.5 Mbps) (40 MHz Clock Source)

TIP815-20R

ARCNET RS485 Interface (2.5 Mbps)

TIP815-21R

ARCNET RS485 Interface (5 Mbps)

Style Conventions

Hexadecimal characters are specified with prefix 0x, (i.e. 0x029E means hexadecimal value 029E)

For signals on hardware products, an "Active Low" is represented by the Signal Name with a following "#" (i.e. IP_RESET#)

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	June 1994
1.1	Revised	July 1995
1.2	5 Mbps Version added	November 1995
1.3	Hardware Rev. C	May 1997
1.4	Hardware Rev. E	September 2002
1.5	New address TEWS LLC	September 2006
1.6	TIP815-11 max data rate changed to 2.5 Mbps (Hybrid parameters have changed along with RoHS transition)	January 2007
1.0.7	New notation of User Manual Issue	September 2009
1.0.8	General Revision	August 2014

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1 Product Description

The TIP815 is an IndustryPack® compatible module with a complete ARCNET interface using the controller COM20020. The COM20020 contains the ARCNET controller with transceiver and Dual Port RAM. Various network topologies are supported (Star, Tree, and Bus).

The TIP815-10R/-11R are designed for Coax and Twisted Pair ARCNET networks. A high impedance local area network driver hybrid is used to interface to both jumper selectable physical layers. The host CPU and the controller are galvanically isolated from the network cable by the hybrids pulse transformer.

The TIP815-20R/-21R versions are designed for RS485 networks. The RS485 is optically isolated from the controller and the power for the RS485 transceiver is provided by a DC/DC converter.

Two speed grades of the TIP815 are available: the TIP815-10R/-11R/-20R offer 2.5 Mbps and the TIP815-21R offers communications up to 5 Mbps.

The on board 8 bit SMD switch located on the IP can be used as source for the hardware depend ARCNET Node ID. The switch signals are also available at the IP's 50 pin I/O connector.

The TIP815 is ideal suited for industrial / factory automation and automotive applications.

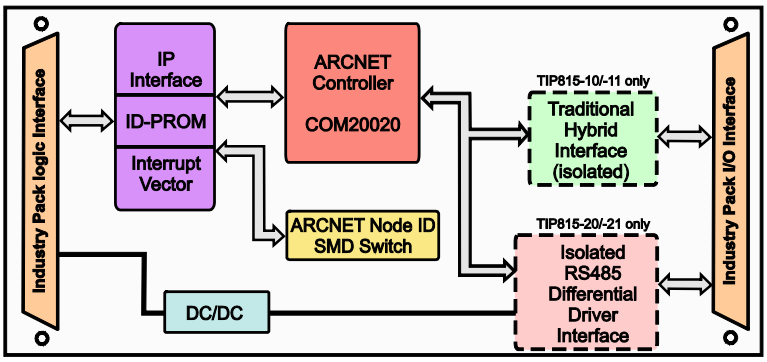

Figure 1-1 : Block Diagram TIP815

2 Technical Specification

Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995
ID ROM Data	Format I
I/O Space	Used with no wait states
Memory Space	Not used
Interrupts	IntReq0 used
DMA	Not supported
Clock Rate	8 MHz
Module Type	Type I
On board Devices	
Controller	COM20020 ULANC Rev. D Universal Local Area Network Controller with 2kx8 on board RAM
I/O Interface	
Interface Connector	50-conductor flat cable
Physical Network	for TIP815–10R/–11R : Coax 90 ohms or Twisted Pair (jumper selectable), galvanic isolation for TIP815–20R/–21R : RS485, galvanic isolation
Network Speed	TIP815–10R and –20 (20MHz Clock Source): 2.5 Mbps, 1.25 Mbps, 625 Kbps or 312.5 Kbps software selectable TIP815-11R (40 MHz Clock Source): 2.5 Mbps, 1.25 Mbps, 625 Kbps software selectable TIP815–21R (40 MHz Clock Source): 5 Mbps, 2.5 Mbps, 1.25 Mbps or 625 Kbps software selectable
Physical Data	
Power Requirements	TIP815–10R/–11R: 120mA typical @ 5V -25mA typical @ -12V TIP815–20R/–21R: 265mA typical @ 5V
Temperature Range	Operating 0 °C to +70 °C Storage -40°C to +85 °C
MTBF	tbd.
Humidity	5 – 95 % non-condensing

Table 2-1 : Technical Specification

3 ID PROM Content

Address	Function	Content
0x01	ASCII ‘I’	0x49
0x03	ASCII ‘P’	0x50
0x05	ASCII ‘A’	0x41
0x07	ASCII ‘C’	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x12
0x0C	Revision	0x10
0x0F	Reserved	0x00
0x11	Driver-ID Low-Byte	0x00
0x13	Driver-ID High-Byte	0x00
0x15	Number of bytes used	0x0D
0x17	CRC	0xC5 for TIP815-10R 0xE4 for TIP815-11R 0x3A for TIP815-20R 0x1B for TIP815-21R
0x19	Board Option	0x0A for TIP815-10R 0x0B for TIP815-11R 0x14 for TIP815-20R 0x15 for TIP815-21R
0x1B to 0x3F	Reserved	undefined

Table 3-1 : ID PROM Content

4 IP Addressing

4.1 I/O Space Addressing

The TIP815 provides nine 8 bit wide registers accessible in the IP I/O space.

Address	Symbol	Register Name	Size
0x01	STIMCR	Status/Interrupt Mask	8 bit
0x03	DICOCR	Diagnostic/Command	8 bit
0x05	APTRHI	Address Pointer High	8 bit
0x07	APTRLO	Address Pointer Low	8 bit
0x09	DATA	Data Register	8 bit
0x0A	SUBADR	Sub Address Register	8 bit
0x0D	CONFIG	Configuration	8 bit
0x0F	IDREG	Network ID Register	8 bit
0x41	SWITCH	Switch Register	8 bit
0x61	VECTOR	Interrupt Vector Register	8 bit

Table 4-1 : I/O Space Registers

4.1.1 COM20020 Registers

The registers STIMCR, DICOCR, APTRHI, APTRLO, DATA, SUBADR, CONFIG and IDREG are implemented in the COM20020 ARCNET controller chip.

4.1.2 Switch Register

The Switch Register is a byte wide read only register. Its value is that of the 8 pos. switch, which is located on the IP. The software can read this register to obtain the node ID of the TIP815 from the switch and then configure the ARCNET controller accordingly.

Bit Number	Bit Symbol	Access	Description
7 (MSB)	SWITCH_BYTE	R	Value corresponds to the SMD switch value
6			
5			
4			
3			
2			
1			
0 (LSB)			

Table 4-2 : Switch Register

4.1.3 Interrupt Vector Register

The Interrupt Vector Register is a byte wide read/write register. The Interrupt Vector Register contains the interrupt vector for interrupts to the IP host CPU.

The value of the Interrupt Vector Register could be read/write during I/O cycle and also be read during an interrupt acknowledge cycle.

Bit Number	Bit Symbol	Access	Description
7 (MSB)	VEC_BYTE	R/W	Interrupt Vector for IP Host CPU
6			
5			
4			
3			
2			
1			
0 (LSB)			

Table 4-3 : Interrupt Vector Register

Only the IP INTREQ0 interrupt channel is used. The IP INTREQ1 interrupt channel is unused.

The reset value of the Interrupt Vector Register is 0x00.

4.2 Memory Space Addressing

Not used by the TIP815

5 Programming

5.1 Initialization of the Hardware

The COM20020 ARCNET controller, which is used on the TIP815 IP, is able to work with different CPU bus structures. The COM20020 learns the used bus structure by monitoring the first bus cycles which address the COM20020.

To initialize the COM20020 controller to the right CPU bus structure, the software must generate the following accesses to the COM20020 directly after a system reset:

1. Write 0x55 to the DICOCR register at byte offset 0x03
2. Read the DICOCR register at byte offset 0x03

If the COM20020 is not initialized with the above listed sequence after a reset, the ARCNET IP will not operate.

5.2 Programming the COM20020 Controller

For programming the COM20020 ARCNET controller please references the COM20020 Data Book.

6 Installation

6.1 Configuration of the TIP815-10R/-11R

The TIP815-10R/-11R must be configured by the jumper J1 for the TIP815 V1.0 Rev. A-D and jumper J2 for the TIP815 V1.0 Rev. E for the desired physical layer coax or twisted pair of the network. See the following table for the corresponding jumper settings.

6.1.1 TIP815 V1.0 Rev.A-D

Coax Cable (jumper installed)	Twisted Pair Cable (jumper installed)
J1 1—3 J1 1—4	J1 3—5 J1 4—6

Table 6-1 : Jumper Configuration (TIP815 V1.0 Rev.A-D)

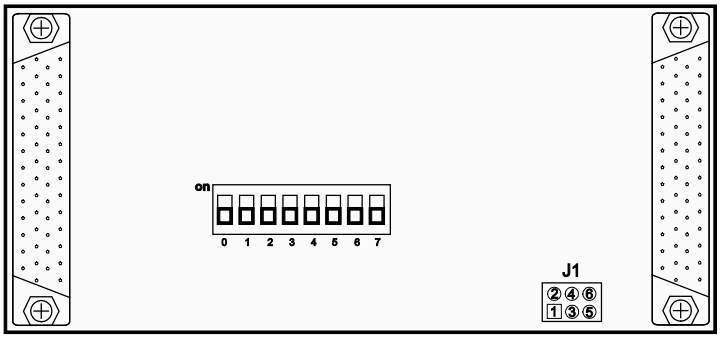

Figure 6-1 : Jumper Location / Switch Location (TIP815 V1.0 Rev.A-D)

6.1.2 TIP815 V1.0 Rev.E

Coax Cable (jumper installed)	Twisted Pair Cable (jumper installed)
J2 1—3 J2 1—4	J2 3—5 J2 4—6

Table 6-2 : Jumper Configuration (TIP815 V1.0 Rev.E)

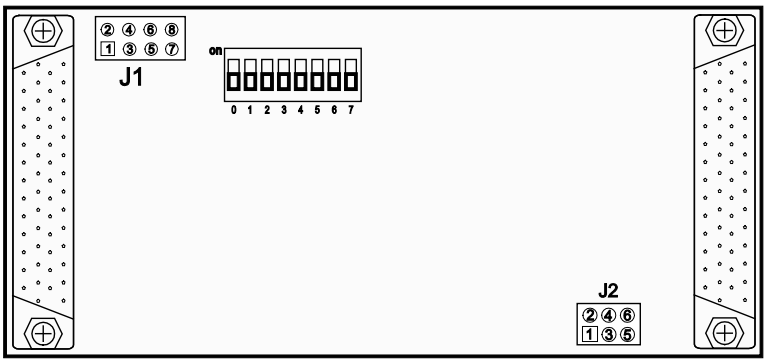

Figure 6-2 : Jumper Location / Switch Location (TIP815 V1.0 Rev.E)

6.2 General Installation Notes

6.2.1 Switch Register

All TIP815 board options TIP815-10R/-11R and TIP815-20R/-21R have an 8 bit switch located on the IP (see figure 6-2 for older revisions and figure 6-4 for revision E). This switch can be read by the software at initialization time and its value can be used to program the node ID of the IP's ARCNET controller. A switch in position OFF represents a logical 1; a switch in position ON represents a logical 0. Default configuration for the local switch is all switches in the OFF position. The switch signals are also available at the 50pin I/O connector.

If the switch setting is provided by the external I/O connector, the local SMD switches must all be switched off.

6.3 Network Cabling

6.3.1 Coax

RG62 is the most popular ARCNET cable. Other cable types can be used, but RG62 has the best electrical characteristics as well as a low cost. It is the first choice even for difficult, electrically noisy environments. It is also simple to install and terminate.

6.3.2 Twisted Pair and RS485

For a Twisted Pair or RS485 network a twisted pair cable with an impedance of 100 ohms @ 1 MHz should be used. It can be AWG 22, 24 or 26.

To reduce the stub length of the TIP815 to a minimum, the twisted pair signals (phase A and B) and the RS485 signals (isolated +RS485 and –RS485) are each connected twice to the IP I/O connector. This means that the Twisted Pair Bus and the RS485 Bus are routed through the TIP815.

All network signal lines must be terminated at both extremes of the cable with a resistor connected between Phase A and Phase B for twisted pair or between signal +RS485 and –RS485. Resistor values should be equal to the impedance of the twisted pair cables.

7 Pin Assignment – I/O Connector

7.1 50 pin I/O flat cable

I/O Pin Number	Function	Signal Name
1	External Case Ground	CASE
2	External Case Ground	CASE
3	Coaxial Signal	CENTER COAXIAL
4	Coaxial Shield	SHIELD COAXIAL
5		
6		
7	External SMD Switch bit 0	DIP0
8	External SMD Switch bit 1	DIP1
9	External SMD Switch bit 2	DIP2
10	External SMD Switch bit 3	DIP3
11	External SMD Switch bit 4	DIP4
12	External SMD Switch bit 5	DIP5
13	External SMD Switch bit 6	DIP6
14	External SMD Switch bit 7	DIP7
15		
16		
17		
18	Isolated RS485 Ground	GND_A
19	Isolated RS485 Signal -	ARCNET_L
20	Isolated RS485 Signal +	ARCNET_H
21	Isolated RS485 Ground	GND_A
22		
23		
24		
25		
26	External Case Ground	CASE
27	Twisted Pair Phase A	PHASE A
28	Twisted Pair Phase B	PHASE B
29	Twisted Pair Phase A	PHASE A
30	Twisted Pair Phase B	PHASE B
31		
32		
33	+5V Supply Voltage	VCC
34	Ground	GND
35	Ground	GND

I/O Pin Number	Function	Signal Name
36	ARCNET Controller PULSE2#	PULSE2#
37	ARCNET Controller PULSE1#	PULSE1#
38	ARCNET Controller TXEN#	TXEN#
39	ARCNET Controller RXIN	RXIN
40		
41		
42		
43	Isolated RS485 Ground	GND_A
44	Isolated RS485 Signal -	ARCNET_L
45	Isolated RS485 Signal +	ARCNET_H
46	Isolated RS485 Ground	GND_A
47		
48		
49		
50		

Table 7-1 : I/O Pin Assignment

7.2 IP Connector Orientation

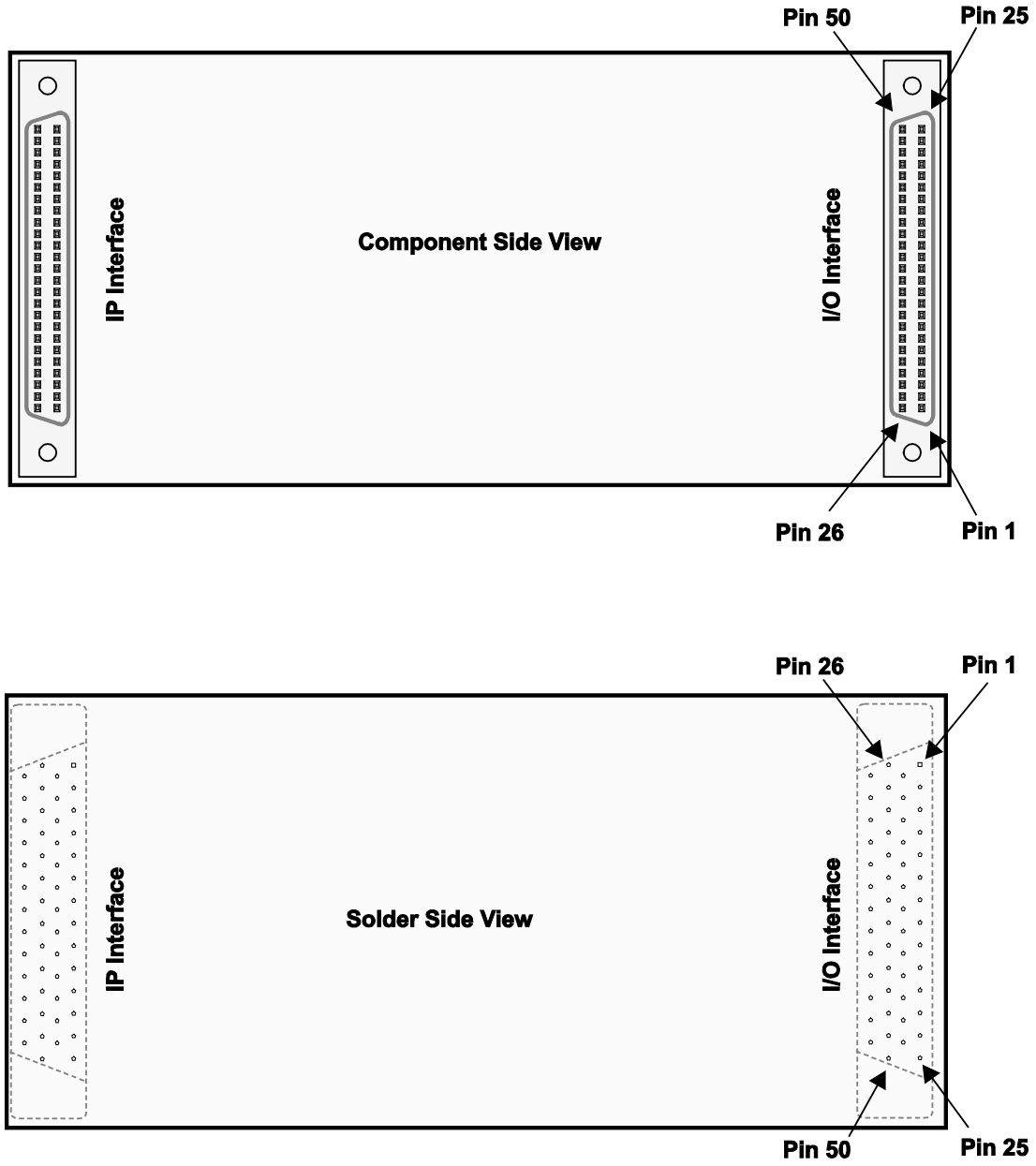

Figure 7-1 : IP Connector Orientation