The Embedded I/O Company

TEWS TECHNOLOGIES

TIP818

Fault tolerant CAN Bus IP

Version 1.0

User Manual

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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7
25469 Halstenbek, Germany www.tews.com
Phone: +49-(0)4101-4058-0
Fax: +49-(0)4101-4058-19
e-mail: info@tews.com

TIP818-10

Fault tolerant CAN bus IP

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	September 1998
1.1	General Revision	October 2003
1.2	New address TEWS LLC	September 2006
1.0.3	General Revision	August 2014

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1 Product Description

The TIP818 is an IndustryPack® compatible module and provides a complete CAN bus interface using the Intel 82527 CAN controller. The Intel 82527 CAN controller supports the standard data and remote frame as well as the extended data and remote frame according to CAN specification 2.0 part A and part B. It has the capability to transmit, receive and perform message filtering on extended and standard messages.

The TIP818 provides a 16 bit bus interface which permits word and byte accesses to the internal registers of the CAN controller.

The physical interface is a fault tolerant CAN transceiver, which supports the communication between the CAN protocol controller and the physical bus. The interface is optically isolated from the CAN controller.

The fault tolerant CAN transceiver supports transmission capability on either bus wire, if one of the bus wires is corrupted. The failure detection logic automatically selects a suitable transmission mode.

The TIP818 is designed for fault tolerant CAN applications (based on Philips fault tolerant CAN transceiver TJA1053 or similar types) with up to 32 nodes and a baud rate up to 125 kbaud.

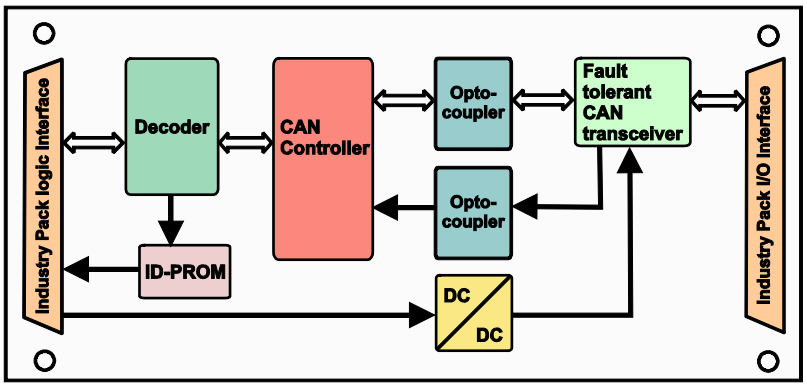

Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I	
I/O Space	Used with no wait states	
Memory Space	Used with minimum 1 wait state	
Interrupts	INTREQ0 and INTREQ1 are used	
DMA	Not supported	
Clock Rate	8MHz	
Module Type	Type I	
On Board Devices		
CAN Controller	Intel 82527	
Number of Channels	1	
Physical Interface	Fault tolerant CAN Transceiver based on Philips TJA1053 Transceiver	
Isolation	CAN bus isolated by optocouplers	
Transfer Rate	Baud rate up to 125 kbaud	
Nodes	Up to 32	
Interface Connector	50-conductor flat cable	
Power Requirements	100mA typical @ +5V DC	
Physical Data		
Temperature Range	Operating Storage	-40 °C to +85 °C -40°C to +125°C
MTBF	573647h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	31 g	

Figure 2-1 : Technical Specification

3 ID Prom Contents

Address	Function	Contents
0x01	ASCII ‘I’	**0x49**
0x03	ASCII ‘P’	**0x50**
0x05	ASCII ‘A’	**0x41**
0x07	ASCII ‘C’	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x29**
0x0D	Revision	**0x10**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x0D**
0x17	CRC	**0xB6**
0x19	Version -10	**0x0A**

Figure 3-1 : ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP818 is accessible in the I/O space of the IP.

TIP818 Address Range: IP_memory_base_address + (0x0000 to 0x01FF)

TIP818 Registers:

CAN Controller:	IP_memory_base_address + (0x0000 to 0x00FF)
Interrupt Vector Register	P_memory_base_address + (0x0101)
Transceiver Status Register:	IP_memory_base_address + (0x0103)
Transceiver Interrupt Status Register:	IP_memory_base_address + (0x0105)
Transceiver Interrupt Enable Register:	IP_memory_base_address + (0x0107)

4.2 Memory Address Map

Address	Function	Size
CAN Controller		
0x0000	Control Register	byte
0x0001	Status Register	byte
0x0002	CPU Interface Register	byte
0x0003	Reserved	byte
0x0004 – 0005	High Speed Read Register	word
0x0006 – 0007	Global Mask – Standard	word
0x0008 – 000B	Global Mask – Extended	word
0x000C – 000F	Message 15 Mask	word
0x0010 – 001D	Message 1	word
0x001E	Message 1	byte
0x001F	CLKOUT Register	byte
0x0020 – 002D	Message 2	word
0x002E	Message 2	byte
0x002F	Bus Configuration Register	byte
0x0030 – 003D	Message 3	word
0x003E	Message 3	byte
0x003F	Bit Timing Register 0	byte
0x0040 – 004D	Message 4	word
0x004E	Message 4	byte
0x004F	Bit Timing Register 1	byte
0x0050 – 005D	Message 5	word
0x005E	Message 5	byte

Address	Function	Size
0x005F	Interrupt Register	byte
0x0060 – 006D	Message 6	word
0x006E	Message 6	byte
0x006F	Reserved	byte
0x0070 – 007D	Message 7	word
0x007E	Message 7	byte
0x007F	Reserved	byte
0x0080 – 008D	Message 8	word
0x008E	Message 8	byte
0x008F	Reserved	byte
0x0090 – 009D	Message 9	word
0x009E	Message 9	byte
0x009F	P1CONF	byte
0x00A0 – 00AD	Message A	word
0x00AE	Message A	byte
0x00AF	P2CONF	byte
0x00B0 – 00BD	Message B	word
0x00BE	Message B	byte
0x00BF	P1IN	byte
0x00C0 – 00CD	Message C	word
0x00CE	Message C	byte
0x00CF	P2IN	byte
0x00D0 – 00DD	Message D	word
0x00DE	Message D	byte
0x00DF	P1OUT	byte
0x00E0 – 00ED	Message E	word
0x00EE	Message E	byte
0x00EF	P2OUT	byte
0x00F0 – 00FD	Message F	word
0x00FE	Message F	byte
0x00FF	Serial Reset Address	byte
Interrupt & Status Register		
0x0101	Interrupt Vector Register	byte
0x0103	Transceiver Status Reg.	byte
0x0105	Transceiver Interrupt Status Reg.	byte
0x0107	Transceiver Interrupt Enable Reg.	byte

Figure 4-1 : Memory Address Map

4.3 Interrupt Vector Register

The Interrupt Vector Register is a byte wide read/write register. There are two interrupt sources on the TIP818, CAN controller interrupts and CAN transceiver interrupts. All bits are read as '0' after reset.

Bit	Symbol	Description	Access	Reset Value
7:1	IV7 … IV1	Interrupt Vector 7-1 are the upper bits of the interrupt vector.	R/W	
0	IS	Interrupt Source bit will be overwritten in interrupt acknowledge cycles with an indication of the interrupt source. 1 = CAN transceiver interrupt 0 = CAN controller interrupt	R/W	

Figure 4-2 : Interrupt Vector Register (Address 0x0101)

4.3.1 CAN controller Interrupts

The Intel 82527 CAN controller can generate interrupts on interrupt request line INTREQ0# of the IP bus.

4.3.2 CAN Transceiver Interrupts

The Philips fault tolerant CAN transceiver can detect fault conditions on the physical CAN bus lines. As an indication of such faults the fault tolerant CAN transceiver can generate interrupts on interrupt request line INTREQ1# of the IP bus.

4.4 Transceiver Interrupt Enable Register

The Transceiver Interrupt Enable Register is a byte wide read/write register. This register enables or disables the assertion of interrupts from the fault tolerant CAN transceiver.

Bit	Symbol	Description	Access	Reset Value
7:1				
0		Transceiver Interrupt Enable bit 1= enabled 0 = disabled	R/W	

Figure 4-3 : Transceiver Interrupt Enable Register (Address 0x0107)

4.5 Transceiver Interrupt Status Register

The Transceiver Interrupt Status Register is a byte wide read/write register. After enabling the transceiver interrupt with the Transceiver Interrupt Enable Register the transceiver interrupt status is indicated in the Transceiver Interrupt Status Register.

Any write access to this register clears the interrupt status. Write to this register for interrupt removal service.

Bit	Symbol	Description	Access	Reset Value
7:1				
0		Transceiver Interrupt Status bit 1= transceiver interrupt pending 0 = no transceiver interrupt pending	R/W	

Figure 4-4 : Transceiver Interrupt Status Register (Address 0x0105)

4.6 Transceiver Status Register

The Transceiver Status Register is a byte wide read/write register. To work without transceiver interrupts the Transceiver Status Register indicates the real status of the fault signal signalized by the fault tolerant CAN transceiver. Poll this register to detect a fault signalized by the fault tolerant CAN transceiver.

Bit	Symbol	Description	Access	Reset Value
7:1				
0		Transceiver Status bit 1= transceiver fault detected 0 = no transceiver fault detected	R/W	

Figure 4-5 : Transceiver Status Register (Address 0x0103)

5 CAN Controller Programming

For programming the Intel 82527 CAN bus controller please refer to the Intel 82527 Data Book.

6 CAN Transceiver Failure Detection

The failure detector of the CAN transceiver is active in the normal operation mode and detects the following single bus failures and switches to an appropriate mode:

1. CANH wire interrupted
2. CANL wire interrupted
3. CANH short-circuited to battery
4. CANL short-circuited to ground
5. CANH short-circuited to ground
6. CANL short-circuited to battery
7. CANL mutually shorted to CANH

The differential receiver threshold is set at –2.9V. This ensures correct reception in the normal operating modes and in the event of failures 1, 2 and 5 with a noise margin as high as possible. These failures, or recovery from them, do not destroy ongoing transmissions.

Failures 3 and 6 are detected by comparators connected to CANH and CANL, respectively. If the comparator threshold is exceeded for a certain period of time, the reception is switched to the single-wire mode.

This time is needed to avoid false triggering by external RF fields. Recovery from these failures is detected automatically after a certain time-out (filtering) and no transmission is lost. The CANH driver and the RTH pin are switched off in the event of failure 3.

Failures 4 and 7 initially result in a permanent dominant level at RXD. After a time-out, the CANL driver and the RTL pin are switched off. Only a weak pull-up at RTL remains. Reception continues by switching to the single-wire mode via CANH. When failures 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold level for a certain period of time, reception and transmission switch back to the differential mode.

If any of the seven wiring failures occur, the output NERR will be made LOW. On error recovery, NERR will be made HIGH again.

During all single-wire transmissions, the EMC performance (both immunity and emission) is worse than in the differential mode. Integrated receive filters suppress any HF noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression. In the single-wire mode, low frequency noise cannot be distinguished from the required signal.

7 Termination

A standard CAN termination with a 120 ohms resistor between CANL and CANH can't be used. Therefore it is not possible to connect the TIP818 with a standard CAN bus system with standard termination. The TIP818 then always indicate a transceiver fault.

8 Pin Assignment – I/O Connector

The 50 pin flat cable from the IP carrier board is split into two 9 pin sections.

The IP I/O lines 01-09 fit directly to a DB9 male connector. The assignment of such a DB9 connector meets the suggestion of the CiA (CAN in Automation). The IP I/O lines 01-09 are connected on board with the IP I/O lines 10-18. By this it is very easy to connect the TIP818 to the CAN bus.

I/O line	Pin No. of DB9	Description according to CiA	
01	1	Reserved	
02	6	(GND)	Optional Input Ground
03	2	CAN_L bus line	Fault tolerant CAN
04	7	CAN_H bus line	Fault tolerant CAN
05	3	GND	Ground
06	8	Reserved	(error line)
07	4	Reserved	
08	9	(V+)	Optional Input Power
09	5	Reserved	
10	1	Reserved	
11	6	(GND)	Optional Input Ground
12	2	CAN_L bus line	Fault tolerant CAN
13	7	CAN_H bus line	Fault tolerant CAN
14	3	GND	Ground
15	8	Reserved	(error line)
16	4	Reserved	
17	9	(V+)	Optional Input Power
18	5	Reserved	

Figure 8-1 : Pin Assignment I/O Connector