The Embedded I/O Company

TEWS TECHNOLOGIES

TMPE623

Reconfigurable FPGA with Digital I/O PCIe Mini Card

Version 1.0

User Manual

Issue 1.0.4

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TMPE623-10R

Artix-7 7A50T FPGA, 26 TTL I/O

TMPE623-11R

Artix-7 7A50T FPGA, 13 Differential EIA-422 / EIA-485 I/O

TMPE623-12R

Artix-7 7A50T FPGA, 13 Differential M-LVDS I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	December 2017
1.0.1	Updated SPI-Flash Type in the Technical Specifications Added Power Requirements & MTBF Added Note about the "Quad-Enable" bit of the SPI-Flash Updated Appendix A	April 2018
1.0.2	Clarified variant dependent usage of the Digital I/O Interface Updated Figure 4-2	March 2020
1.0.3	Corrected “Mating Part” number for the I/O connector (X2)	April 2020
1.0.4	Clarified SPI-Flash	September 2021

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1 Product Description

The TMPE623 is a standard full PCI Express Mini Card, providing a user programmable Xilinx Artix-7 7A50T FPGA.

Depending on the order option the TMPE623 offers 26 ESD-protected 5V-tolerant TTL lines or 13 differential I/O lines using ESD-protected EIA-422 / EIA-485 compatible line transceivers or Multipoint-LVDS transceivers.

All I/O lines are individually programmable as input or output. TTL I/O lines can be set to high, low, or tristate. Each TTL I/O line has a pull-resistor to a common programmable pull voltage that can be set so +3.3 V, +5 V and GND. Differential I/O lines are terminated, EIA-422 / EIA-485 lines with 120 Ω, M-LVDS lines with 100 Ω. The I/O signals are accessible through a 30 pin Pico-Clasp latching connector.

The User FPGA is configured by a SPI flash. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using the Vivado ILA). With the TA308 Programming Kit direct JTAG access to the FPGA is possible, using the Xilinx Platform Cable USB.

User applications for the TMPE623 with 7A50T FPGA can be developed using the design software Vivado Design Suite HL WebPACK Edition, which can be downloaded free of charge from www.xilinx.com.

TEWS offers a well-documented basic FPGA Example Application design. It includes a constraints file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TMPE623. It implements PCIe to register mapping and basic I/O. It comes as a Xilinx Vivado Design Suite project with source code and as a ready-to-download bit stream.

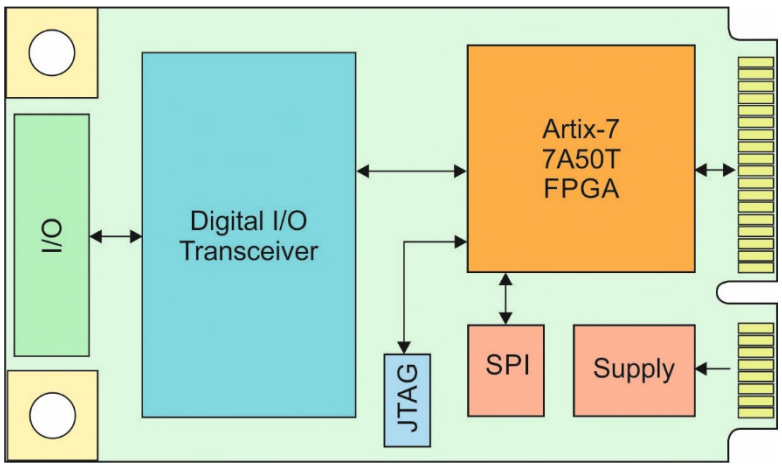


Figure 1-1: Block Diagram

2 Technical Specification

Interface				
Mechanical Interface	PCI Express Mini Card conforming to PCI Express Mini Card Electromechanical Specification, Revision 2.0 Card Type: Full-Mini Card (50.95 x 30 mm)			
Electrical Interface	PCI Express x1 Link conforming to PCI Express Base Specification, Revision 2.0 The TMPE623 does not support the USB interface			
Main On-Board Devices				
User configurable FPGA	XC7A50T-2 (Xilinx)			
SPI-Flash	Macronix MX25L12835F (or compatible) 128 Mbit SPI-Flash covered by the Vivado “mx25l12845g” device settings. (contains TMPE623 FPGA Example)			
I/O Interface				
Digital I/O Channels	TMPE623-10R: 26 ESD-protected 5 V-tolerant TTL lines TMPE623-11R: 13 differential EIA-422 / EIA-485 lines TMPE623-12R: 13 differential M-LVDS lines			
Digital I/O Transceiver	TMPE623-10R: 74LVC2G241 (or compatible) TMPE623-11R: 65HVD75D (or compatible) TMPE623-12R: 65LVDM176D (or compatible)			
I/O Connector	30 pol. Pico-Clasp latching connector			
Physical Data				
Power Requirements	Depends on FPGA design With TMPE623 FPGA Example Design running, without external load:			
		TMPE623-10R	TMPE623-11R	TMPE623-12R
	+3.3 Vaux:	300 mA	500 mA	400 mA
	+1.5 V:	200 mA	200 mA	200 mA
Temperature Range	Operating	refer to “Thermal Management” chapter		
	Storage	-40°C to +85°C		
MTBF	1.200.000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.			
Humidity	5 – 95 % non-condensing			
Weight	TMPE623-1xR: 13 g			

Table 2-1: Technical Specification

3 Handling and Operating Instructions

3.1 ESD Protection

The PCI Express Mini Card module is sensitive to static electricity. Packing, unpacking and all other module handling has to be done in an ESD/EOS protected Area.

3.2 Height Restrictions

The I/O connector and the heatsink exceed the available PCI Express Mini Card components height. Check carefully if your application provides enough spacing for a TMPE623.

3.3 Thermal Considerations

Due to its small size and high density, the TMPE623 can generate a lot of heat.

Forced air cooling is recommended during operation. If forced air cooling is not possible, another equivalent cooling mechanism must be applied. Without adequate cooling, damage to the device can occur.

4 Functional Description

This chapter gives a brief overview of the various module functions.

4.1 User FPGA Overview

The FPGA is an Artix-7 in a CSG325 package.

Artix-7	Slices	Flip-Flops	DSP48A1 Slices	Block RAM (Kb)	GTP Transceivers
7A50T-2	8150	65200	120	2700	4

Table 4-1: TMPE623 FPGA Feature Overview

The FPGA is equipped with 4 I/O banks and 4 Gigabit (GTP) Transceivers. One of the GTPs can be connected to an Endpoint Block for PCI Express.

Bank	V_{CCO}	V_{REF}	Signals	Remarks
Bank 0	3.3 V	none	Configuration	
Bank 14	3.3 V	none	I/O Interface	
Bank 15	3.3 V	none	I/O Interface	+Configuration
Bank 34	3.3 V	none	I/O Interface	
GTP Bank	**Description**			**Remarks**
Bank 216	GTP0: PCIe Endpoint Block GTP1: Not used GTP2: Not used GTP3: Not used			

Table 4-2: FPGA Bank Usage

4.2 User FPGA Gigabit Transceiver (GTP)

The TMPE623 provides one GTP as 7 Series FPGAs Integrated Block for PCI Express.

GTP	Signal	FPGA Pins	Connected to
GTP0 (X0Y0)	MGTPTX	H1 / H2	used for FPGA Integrated Block for PCI Express
	MGTPRX	E3 / E4	
GTP1 (X0Y1)	MGTPTX	F1 / F2	Not used
	MGTPRX	A3 / A4	
GTP2 (X0Y2)	MGTPTX	D1 / D2	Not used
	MGTPRX	C5 / C6	
GTP3 (X0Y3)	MGTPTX	B1 / B2	Not used
	MGTPRX	G3 / G4	

Table 4-3: FPGA GTP Connections

The 100 MHz MGT clock MGTREFCLK0 (FPGA Integrated Block for PCI Express) is connected directly to the PCI Express Mini Card reference clock. MGTREFCLK1is not used on the TMPE623.

GTP	Signal	FPGA Pins	Connected to
MGTREFCLK0	MGTREFCLK	D5 / D6	100 MHz (backplane clock)
MGTREFCLK1	MGTREFCLK	B5 / B6	not connected

Table 4-4: Gigabit Transceiver Reference Clocks

4.3 User FPGA Configuration

The Artix-7 FPGA can be configured by the following interfaces:

- Master Serial SPI Flash Configuration Interface
- JTAG Interface via JTAG Header

On delivery the SPI configuration Platform Flash contains the TEWS example application for the TMPE623 Artix-7 device.

4.3.1 SPI-Flash

The TMPE623 provides a 128-Mbit serial Flash memory, which is used as the default FPGA configuration source. After configuration the flash is accessible from the FPGA, so it also can be used for additional code or user data storage. The SPI-Flash is connected via Quad (x4) SPI interface to Artix-7 configuration interface.

The SPI-Flash is a Macronix MX25L12835F (or compatible) covered by the Vivado “mx25l12845g” device settings. The device ID is 0xC22018.

SPI-Flash Signal	Bank	V_{CCO}	Pin	Description / Artix-7
CLK	0	3.3 V	E8	Serial Clock (CCLK)
CS#	14	3.3 V	L15	Chip Select (CS0_B)
DI (bit0)	14	3.3 V	K16	Serial Data input (MOSI) / MISO[0]
DO (bit1)	14	3.3 V	L17	Serial Data output (DIN) / MISO[1]
WP# (bit2)	14	3.3 V	J15	MISO[2]
HOLD# (bit3)	14	3.3 V	J16	MISO[3]

Table 4-5: FPGA SPI-Flash Connections

To use the Quad (x4) SPI interface during configuration, a non-volatile “Quad-Enable” bit must be set in the SPI Flash. The Vivado Hardware Manager sets this bit automatically when a bitstream is programmed into the SPI Flash, and resets this bit when the SPI-Flash is erased. The TMPE623 is delivered with the “Quad-Enable” bit set.

4.3.2 Configuration via JTAG

For direct FPGA configuration, FPGA read back or in-system diagnostics with ChipScope, the JTAG connector can be used to access the FPGA JTAG port. Also an indirect SPI-Flash programming is possible via the JTAG connector.

4.3.3 Generate Artix-7 Configuration Data

For a PCIe FPGA design it is important to meet the PCIe 100 ms T_{PVPERL} startup requirements. To achieve this, it is necessary to use the maximum configuration speed and the x4 SPI Bus Width.

To use the maximum configuration speed, the TMPE623 must be configured to use the 100 MHz external master clock as CCLK.

To use this configuration feature, the following configuration option must be set:

```
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN           div-1 [current_design]
set_property CONFIG_VOLTAGE                              3.3   [current_design]
set_property CFGBVS                                      VCCO  [current_design]
```

To use the maximum data transfer speed of the User FPGA SPI Configuration Flash the SPI Configuration Bus Width must be set to the x4.

```
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH               4     [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE              YES   [current_design]
set_property CONFIG_MODE                                 SPIx4 [current_design]
```

Without these options, the configuration time for the Artix-7 FPGA exceeds the maximum PCIe bus setup time.

4.4 Clocking

4.4.1 FPGA Clock Sources

The following table lists the available clock sources on the TMPE623:

FPGA Clock-Pin Name	FPGA Pin Number	Source	Description
MGTREFCLK0_101	D5 / D6	PCI Express Mini Card Slot	100 MHz PCIe Reference clock
IO_L3N_T0_DQS_EMCCLK_14	K18	External oscillator	100 MHz External master configuration clock
IO_L12P_T1_MRCC_14	P14	External oscillator	100 MHz External user clock

Table 4-6: Available FPGA Clock Sources

The 100 MHz EMCCLK is used as configuration clock and is necessary to meet the PCIe 100 ms T_{PVPERL} startup requirements. While this clock is not on a clock capable pin, it can be used as internal clock source by setting the CLOCK_DEDICATED_ROUTE FALSE constraint:

```
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets EMC_CLK]
```

This will result in a couple of warning during synthesis and implementation.

4.5 Digital I/O Interface

Each of the 26 digital I/O channels provides input and output data signals and an output enable signal to the digital buffers.

Signal Name	Pin Number	Direction	IO Standard	IO Bank	Drive [mA]	Slew Rate
DI<0>	A10	IN	LVCMOS33	14	4	SLOW
DI<1>	A15	IN	LVCMOS33	14	4	SLOW
DI<2>	H14	IN	LVCMOS33	14	4	SLOW
DI<3>	D11	IN	LVCMOS33	14	4	SLOW
DI<4>	F15	IN	LVCMOS33	14	4	SLOW
DI<5>	B17	IN	LVCMOS33	14	4	SLOW
DI<6>	D14	IN	LVCMOS33	14	4	SLOW
DI<7>	D13	IN	LVCMOS33	14	4	SLOW
DI<8>	B14	IN	LVCMOS33	14	4	SLOW
DI<9>	G16	IN	LVCMOS33	14	4	SLOW
DI<10>	G15	IN	LVCMOS33	14	4	SLOW
DI<11>	C12	IN	LVCMOS33	14	4	SLOW
DI<12>	U14	IN	LVCMOS33	14	4	SLOW
DI<13>	K15	IN	LVCMOS33	14	4	SLOW

Signal Name	Pin Number	Direction	IO Standard	IO Bank	Drive [mA]	Slew Rate
DI<14>	T13	IN	LVCMOS33	14	4	SLOW
DI<15>	T15	IN	LVCMOS33	14	4	SLOW
DI<16>	T17	IN	LVCMOS33	14	4	SLOW
DI<17>	K17	IN	LVCMOS33	14	4	SLOW
DI<18>	T14	IN	LVCMOS33	14	4	SLOW
DI<19>	V12	IN	LVCMOS33	14	4	SLOW
DI<20>	V11	IN	LVCMOS33	14	4	SLOW
DI<21>	R15	IN	LVCMOS33	14	4	SLOW
DI<22>	V8	IN	LVCMOS33	14	4	SLOW
DI<23>	J5	IN	LVCMOS33	14	4	SLOW
DI<24>	K2	IN	LVCMOS33	14	4	SLOW
DI<25>	L5	IN	LVCMOS33	14	4	SLOW
DO<0>	D15	OUT	LVCMOS33	14	4	SLOW
DO<1>	B10	OUT	LVCMOS33	14	4	SLOW
DO<2>	D16	OUT	LVCMOS33	14	4	SLOW
DO<3>	B15	OUT	LVCMOS33	14	4	SLOW
DO<4>	E15	OUT	LVCMOS33	14	4	SLOW
DO<5>	C16	OUT	LVCMOS33	14	4	SLOW
DO<6>	F14	OUT	LVCMOS33	14	4	SLOW
DO<7>	C17	OUT	LVCMOS33	14	4	SLOW
DO<8>	D10	OUT	LVCMOS33	14	4	SLOW
DO<9>	D18	OUT	LVCMOS33	14	4	SLOW
DO<10>	H17	OUT	LVCMOS33	14	4	SLOW
DO<11>	G17	OUT	LVCMOS33	14	4	SLOW
DO<12>	V14	OUT	LVCMOS33	14	4	SLOW
DO<13>	L14	OUT	LVCMOS33	14	4	SLOW
DO<14>	R13	OUT	LVCMOS33	14	4	SLOW
DO<15>	N18	OUT	LVCMOS33	14	4	SLOW
DO<16>	V16	OUT	LVCMOS33	14	4	SLOW
DO<17>	U15	OUT	LVCMOS33	14	4	SLOW
DO<18>	P15	OUT	LVCMOS33	14	4	SLOW
DO<19>	T12	OUT	LVCMOS33	14	4	SLOW
DO<20>	U9	OUT	LVCMOS33	14	4	SLOW
DO<21>	U16	OUT	LVCMOS33	14	4	SLOW
DO<22>	M6	OUT	LVCMOS33	14	4	SLOW
DO<23>	R7	OUT	LVCMOS33	14	4	SLOW
DO<24>	P1	OUT	LVCMOS33	14	4	SLOW
DO<25>	J6	OUT	LVCMOS33	14	4	SLOW
OE<0>#	B16	OUTPUT	LVCMOS33	14	4	SLOW

Signal Name	Pin Number	Direction	IO Standard	IO Bank	Drive [mA]	Slew Rate
OE<1>#	G14	OUTPUT	LVCMOS33	14	4	SLOW
OE<2>#	C11	OUTPUT	LVCMOS33	14	4	SLOW
OE<3>#	C14	OUTPUT	LVCMOS33	14	4	SLOW
OE<4>#	E13	OUTPUT	LVCMOS33	14	4	SLOW
OE<5>#	C13	OUTPUT	LVCMOS33	14	4	SLOW
OE<6>#	F17	OUTPUT	LVCMOS33	14	4	SLOW
OE<7>#	A17	OUTPUT	LVCMOS33	14	4	SLOW
OE<8>#	E17	OUTPUT	LVCMOS33	14	4	SLOW
OE<9>#	C18	OUTPUT	LVCMOS33	14	4	SLOW
OE<10>#	H16	OUTPUT	LVCMOS33	14	4	SLOW
OE<11>#	E16	OUTPUT	LVCMOS33	14	4	SLOW
OE<12>#	M17	OUTPUT	LVCMOS33	14	4	SLOW
OE<13>#	J14	OUTPUT	LVCMOS33	14	4	SLOW
OE<14>#	P18	OUTPUT	LVCMOS33	14	4	SLOW
OE<15>#	L18	OUTPUT	LVCMOS33	14	4	SLOW
OE<16>#	T18	OUTPUT	LVCMOS33	14	4	SLOW
OE<17>#	V17	OUTPUT	LVCMOS33	14	4	SLOW
OE<18>#	U11	OUTPUT	LVCMOS33	14	4	SLOW
OE<19>#	U12	OUTPUT	LVCMOS33	14	4	SLOW
OE<20>#	V9	OUTPUT	LVCMOS33	14	4	SLOW
OE<21>#	U10	OUTPUT	LVCMOS33	14	4	SLOW
OE<22>#	J4	OUTPUT	LVCMOS33	14	4	SLOW
OE<23>#	M5	OUTPUT	LVCMOS33	14	4	SLOW
OE<24>#	K3	OUTPUT	LVCMOS33	14	4	SLOW
OE<25>#	L3	OUTPUT	LVCMOS33	14	4	SLOW

Table 4-7: Digital I/O Interface

The IN[25:0] signals reflect the IO_[25:0] line state. They are always active.

The OUT[25:0] signals set the IO_[25:0] state when the corresponding I/O transmitters are enabled.

The OE[25:0] signals enable or disable the I/O transmitters. A pull-down resistor disables the I/O transmitters when the OE pins are not driven.

For the TMPE623-11R and -12R order options (differential I/O only) not all signals are used and driven. The user FPGA logic design should implement FPGA internal pull-down or pull-up resistors on the according IN lines for the TMPE623-11R and -12R order options to keep these signals from floating.

TMPE623 Variant	Signal to I/O Mapping on X2	Unused Signals
TMPE623-10R	DI/DO/OEx = IO_x	None
TMPE623-11R & TMPE623-12R	DI/DO/OEx with even numbers (0, 2, …) = IO_x	DI/DO/OE with odd numbers (1, 3, …)

Table 4-8: Digital I/O Interface Usage for TMPE623 Variants

4.5.1 TTL I/O Interface

Each I/O line is buffered by a 74LVC2G241. The 74LVC2G241 is a tri-state buffer that provides TTL compatible inputs with 5 V-tolerance. The outputs can be set to tri-state with an output enable signal and provide a 47 Ω serial resistor and a 4.7 kΩ pull resistor. The pull resistor guarantees a valid logic level when the outputs are tristate and not driven externally. The pull voltage can be set to 3.3 V, 5 V or GND. When set to 5 V, the outputs must not be driven, but set to tristate for a valid high level.

A TVS array protects against ESD shocks.

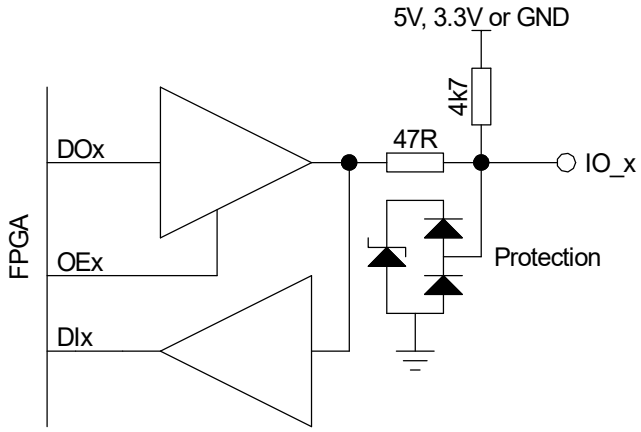


Figure 4-1: TTL I/O Interface

Especially the TTL I/Os are quite prone to crosstalk and ringing. Keep that in mind when developing FPGA code for the TTL I/Os and use appropriate counter measurements like input debouncing or a time-shifted output update scheme.

With the pull voltage set to 5 V, the digital I/O can weakly drive a higher voltage than 3.3 V by setting the output to tri-state. This can be useful when connecting to a standard 5 V CMOS logic input, where a high level of minimum 3.5 V is required. Drive DO constant low and use OE to toggle the output.

With the pull voltage set to GND, a pull-down functionality is implemented. Drive DO constant high and use OE to toggle the output.

Pull Option	DO	OE	Output	Remark
No pull-up or pull-down	0	1	0	Driven Low
	1	1	1	Driven to 3.3 V
Pull-up to 3.3 V	0	1	0	Driven Low
	1	1	1	Driven to 3.3 V
	-	0	1	Pulled to 3.3 V
Pull-up to 5 V	0	1	0	Driven Low
	-	0	1	Pulled to 5 V
Pull-down to GND	-	0	0	Pulled to GND
	1	1	1	Driven to 3.3 V

Table 4-9: I/O Pull Options

If the pull resistors float, the user should keep in mind that the I/O Lines are still connected via their pull resistors.

The normal behavior is that the User FPGA code controls the I/O Pull Configuration depending on User FPGA I/O Function. The SEL signals are connected to an analog multiplexer. With this multiplexer the desired voltage can be adjusted directly from the User FPGA. The user must ensure that valid signals are always driven.

CNT Lines	Description	Artix-7 Pins
SEL[1:0]	11: pull-down 10: pull-up to 3.3 V 01: pull-up to 5 V 00: No pull-up or pull-down	V6, V7

Table 4-10: I/O Pull Configuration

4.5.1.1 Output Level & Output Current

Because of the 47 ohm series resistor, there is a reduced high-level voltage at the I/O pin when the output buffer sources a noticeable current to the external load while driving a high-level. To maintain a proper TTL high level, the recommended maximum I/O source current is 15 mA.

There is also an increased low-level voltage at the I/O pin when the output buffer sinks a noticeable current from the external load while driving a low-level. To maintain a proper TTL low level, the recommended maximum I/O sink current is 6 mA.

For achieving a 5 V CMOS high-level voltage (V_{OH} >= 3.5 V), the external load should be high impedance. If there would be a low impedance path to ground on the I/O load, this may result in a voltage divider with the on-board pull resistor, significantly reducing the high-level voltage at the I/O pin. To maintain a proper 5 V CMOS high level, the I/O load (leakage) current should not exceed 250 µA.

4.5.2 Differential I/O Interface

EIA-485 variants use an ESD-protected SN65HVD75 EIA-422 / EIA-485 transceiver and provide a 120 Ω termination resistor. LVDS variants use a SN65MLVD176 M-LVDS transceiver and provide a 100 Ω termination resistor.

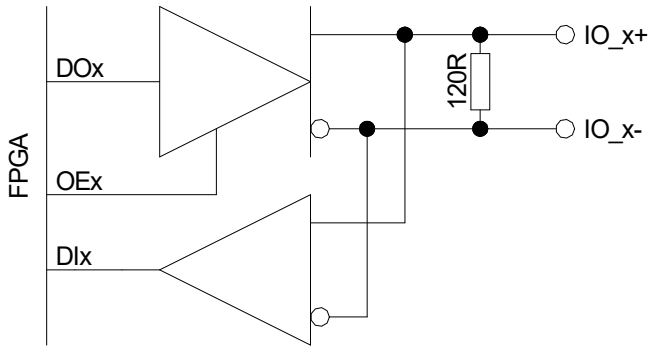


Figure 4-2 : Differential I/O Interface

Please note that each TMPE623 M-LVDS line provides its own termination. If more than four lines are connected together some termination resistors must be removed.

The actual data transmission rate depends on factors like connection, cable length, FPGA design etc.

4.6 User GPIO

The TMPE623 has some optional general purpose I/O and debug signals connected to the FPGA. The required signaling standard is LVCMOS33.

The FPGA is connected to the status indicator signals of the PCI Express Mini Card Slot:

Signal	Bank	V_{CCO}	Pin	Description
LED_WWAN#	34	3.3 V	V2	WWAN status indicator
LED_WPAN#	34	3.3 V	V4	WPAN status indicator
LED_WLAN#	34	3.3 V	V3	WLAN status indicator

Table 4-11: FPGA General Purpose I/O

4.7 I²C-EEPROM

The TMPE623 provides an Atmel AT24C04 4-kbit I²C memory. As factory default the EEPROM contains basic TMPE623 ID values (similar to PCI IDs) and the module serial number in EUI-64 format. The former can be used to identify the module and its variant when a custom PCIe implementation sit used, the latter can be used to support the PCIe Device Serial Number Capability.

Offset	Description	Size (Bit)
0x000-0x1EF	Unused	-
0x1F0	Vendor ID (0x1498)	16
0x1F2	Device ID (0xA26F)	16
0x1F4	Subsystem Vendor ID (0x1498)	16
0x1F6	Subsystem ID (-10 = 0xA00A, -11 = 0xA00B, -12 = 0xA00C)	16
0x1F8	Module Serial Number The Module Serial Number is stored as EUI-64 (i.e. Sn. 1234567 = 0x0001060001234567).	64

Table 4-12: I2C EEPROM Address Map

The device address is “1010000”.

SPI-Flash Signal	Bank	V_{CCO}	Pin	Description
PROM_SCL	34	3.3 V	R1	Serial Clock
PROM_SDA	34	3.3 V	U1	Serial Data

Table 4-13: FPGA I²C-EEPROM Connections

4.8 I²C Temperature Sensor

The TMPE623 provides an NXP SE95 13-bit temperature sensor. The device address is “1001000”.

SPI-Flash Signal	Bank	V_{CCO}	Pin	Description
SCL_SE95	15	3.3 V	F18	Serial Clock
SDA_SE95	15	3.3 V	M18	Serial Data
OS	15	3.3 V	E18	“Overtemperature Shutdown”

Table 4-14: FPGA I²C Temperature Sensor Connections

4.9 Thermal Management

All components used on the TMPE623 are rated for the industrial temperature range of -40°C to +85°C. The actual temperature range the TMPE623 can be used in is highly dependent on the FPGA design, the load of the modules I/O circuitry and the applied cooling method.

The module has several hot spots including differential transceivers, power supplies and the FPGA. The TMPE623 is equipped with a basic heatsink that helps to evenly spread the heat and provides a mounting base for additional cooling such as additional passive heatsinks, heat pipes or active cooling.

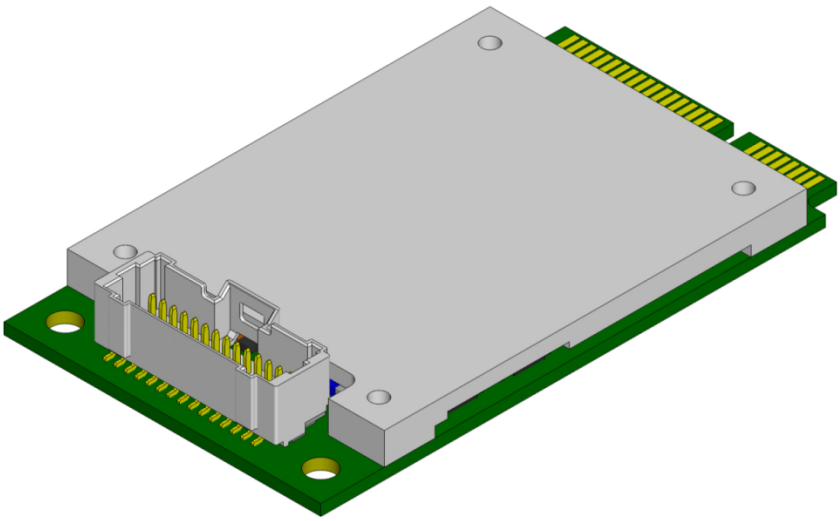


Figure 4-3 : TMPE623 with Heatsink

Mounting a heatsink will violate the Mini PCIe Card component envelope. Check carefully if your system provides enough spacing for a TMPE623 with mounted heatsink. In space constrained systems mounting a heatsink may not be possible. In this case forced air cooling must be applied during operation.

Use the Xilinx XPower Estimator (XPE) or the Vivado Power Report to determine whether additional cooling requirements such as forced air cooling apply. It is also strongly recommended to use the internal temperature monitoring of the Artix-7 and the on-board temperature sensor to monitor the temperature.

As an indication: With the example application running in a standard PC enclosure at 25°C the TMPE623 current requirement is 500 mA @ 3.3 V and 200 mA @ 1.5 V, resulting in a TMPE623 board temperature of about 50°C and an internal temperature of the Artix-7 FPGA of about 60°C.

5 Design Help

5.1 Example Design

TEWS offers an FPGA Example design which consists of a well-documented basic example. It includes a constraints file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TMPE623. It implements a PCIe endpoint with register mapping and basic I/O functions. It comes as a Xilinx Vivado Design Suite project with source code and as a ready-to-download bit stream. This Example design can be used as a starting point for own projects.

5.2 FPGA MultiBoot

The Artix-7 FPGAs provide the “MultiBoot” capability. It allows the FPGA to selectively reconfigure itself with a new bitstream stored in the attached SPI configuration flash. The reconfiguration can be triggered by the FPGA application itself or during the initial FPGA configuration when an error occurs (Fallback Multiboot). The latter can be used to implement safe in-field updates: if an update fails, a “golden” bitstream is loaded that allows to handle the error or to retry the update.

The TMPE623 provides a SPI configuration flash that is large enough to hold multiple FPGA configuration bitstreams. This allows the use of the Artix-7 MultiBoot feature. On delivery the TMPE623 is programmed with a fallback multiboot example.

Refer to Xilinx UG470 “7 Series FPGAs Configuration User Guide” for more details.

6 Installation

To install the PCI Express Mini Card, insert it, slightly slanted, into the connector and fold it down. If the carrier board has spring latches, gently push the card down until the spring latch locks in place. Otherwise secure the card with screws.

To remove the card, remove the screws or pull the spring latch away from the card until it pops up. The card can then be removed from the connector.

The I/O connector exceeds the available PCI Express Mini Card components height. Check carefully if you application provides enough spacing for a TMPE623.

6.1 A Remark About Slot Supplies

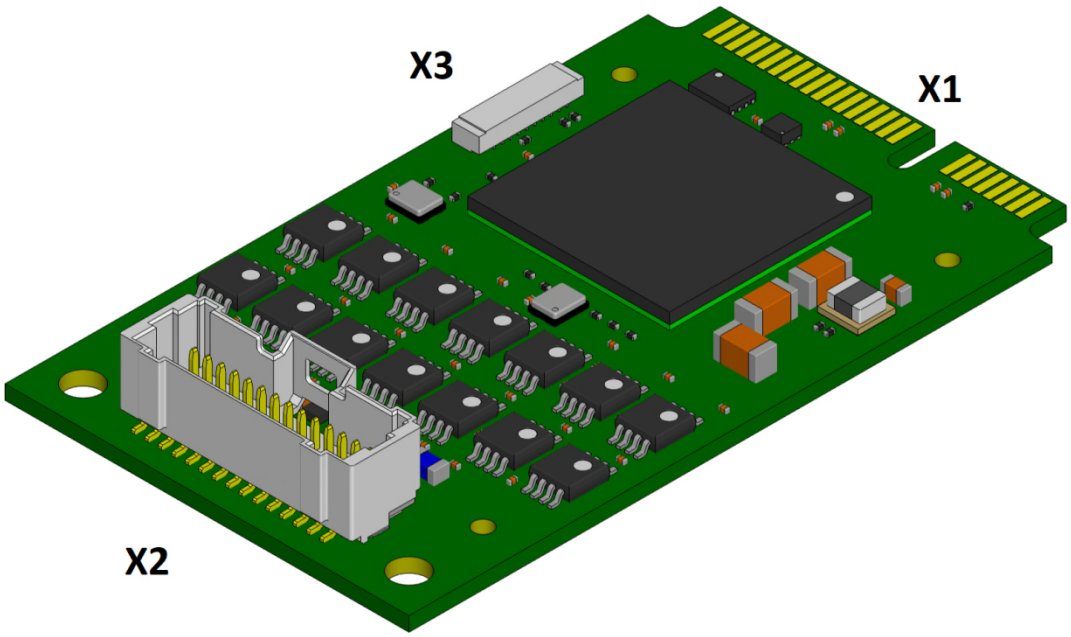
A PCI Express Mini Card slot is powered by two supplies, 1.5V and 3.3Vaux. While the 1.5V is powered on and off with the rest of the system, the 3.3Vaux supply is typically powered by the systems auxiliary power, which is available even when the system is off. Keep this in mind when installing or removing a PCI Express Mini Card and make sure that the system is turned off completely.

After initial power-up, the FPGA on the TMPE623 is not configured until all power supplies are available. But when the system is turned off, the FPGA remains configured as long as the slot is powered with the systems auxiliary power. In this case, a “power cycle” may not have the expected results.

7 I/O Connectors

This chapter provides information about user accessible on-board connectors

7.1 Overview



X1	System Connector
X2	I/O Connector
X3	JTAG Connector

Figure 7-1: I/O Connector Overview

7.2 Board Connectors

7.2.1 System Connector (X1)

Pin-Count	52
Connector Type	Card-edge
Source & Order Info	none

Table 7-1: System Connector

Signal names in grey are not used by the card.

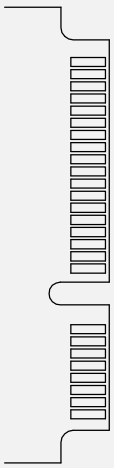
Description	Pin		Pin	Description
W_DISABLE2#	51		52	+3.3 Vaux
Reserved	49		50	GND
Reserved	47		48	+1.5 V
Reserved	45		46	LEP_WPAN#
GND	43		44	LEP_WLAN#
+3.3 Vaux	41		42	LEP_WWAN#
+3.3 Vaux	39		40	GND
GND	37		38	USB_D+
GND	35		36	USB_D-
PETp0	33		34	GND
PETn0	31		32	SMB_DATA
GND	29		30	SMB_CLK
GND	27		28	+1.5 V
PERp0	25		26	GND
PERn0	23		24	+3.3 Vaux
GND	21		22	PERST#
UIM_IC_DP	19		20	W_DISABLE1#
UIM_IC_DM	17		18	GND
Mechanical Key				Mechanical Key
GND	15		16	UIM_SPU
REF_CLK+	13		14	UIM_RESET
REF_CLK-	11		12	UIM_CLK
GND	9		10	UIM_DATA
CLKREQ#	7		8	UIM_PWR
COEX2	5		6	+1.5 V
COEX1	3		4	GND
WAKE#	1		2	+3.3 Vaux

Table 7-2: System Connector Pin Assignment

7.2.2 I/O Connector (X2)

Pin-Count	30
Connector Type	Molex Pico-Clasp, dual row straight header, with lock
Source & Order Info	501190-3017
Mating Part	501189-3010

Table 7-3: I/O Connector

The I/O connector exceeds the available PCI Express Mini Card components height. Check carefully if you application provides enough spacing for a TMPE623.

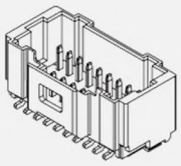
Pin Assignment						
Description		**Pin**		**Pin**	**Description**	
Single-En.	**Diff.**				**Single-En.**	**Diff.**
GND	GND	1		2	GND	GND
I/O_0	I/O_0+	3		4	I/O_1	I/O_0-
I/O_2	I/O_2+	5		6	I/O_3	I/O_2-
I/O_4	I/O_4+	7		8	I/O_5	I/O_4-
I/O_6	I/O_6+	9		10	I/O_7	I/O_6-
I/O_8	I/O_8+	11		12	I/O_9	I/O_8-
I/O_10	I/O_10+	13		14	I/O_11	I/O_10-
I/O_12	I/O_12+	15		16	I/O_13	I/O_12-
I/O_14	I/O_14+	17		18	I/O_15	I/O_14-
I/O_16	I/O_16+	19		20	I/O_17	I/O_16-
I/O_18	I/O_18+	21		22	I/O_19	I/O_18-
I/O_20	I/O_20+	23		24	I/O_21	I/O_20-
I/O_22	I/O_22+	25		26	I/O_23	I/O_22-
I/O_24	I/O_24+	27		28	I/O_25	I/O_24-
GND	GND	29		30	GND	GND

Table 7-4: I/O Connector Pin Assignment

I/O_x signals correspond to the DIx/DOx/OEx FPGA pins.

7.2.3 JTAG Connector (X3)

Pin-Count	10
Connector Type	JST XRS 10pol 0.6 mm Pitch IDC Connector
Source & Order Info	SM10B-XSRS-ETB
Mating Part	10XSR-36S

Table 7-5: JTAG Connector

The TMPE623 provides a JTAG connector to access the FPGA's JTAG port.

TEWS provides a "Programming Kit" (TA308) which includes a XSR cable and an adapter module that provides a Xilinx USB Programmer II compatible 2 mm shrouded header.

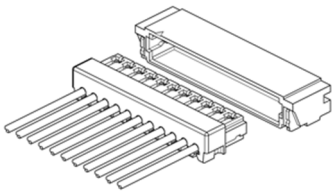
	Pin	Description
	1	GND
	2	TCK
	3	TMS
	4	TDI
	5	TDO
	6	GND
	7	GPIO0
	8	GPIO1
	9	PRESENT#
	10	V_{REF}

Table 7-6: JTAG Connector Pin Assignment

GPIO0 is connected to FPGA DONE

GPIO1 is connected to Power Good (covers FPGA V_{CORE} and 5 V)

PRESENT# is not used by the TMPE623.

V_{REF} is 3.3 V

Figure 7-2: TMPE623 connected to a Programmer via TA308

8 Appendix A

This appendix contains the signal to pin assignments for the Artix-7 FPGA.

```
### Pin and location constraints

## ############################################################################################ ##
## PCIe
## ############################################################################################ ##

# PCIe Lanes
set_property LOC GTPE2_CHANNEL_X0Y0 [get_cells
{PCIE_FW_UNIT_INST/B_XIL_PCIE_EP.I_PCIE_EP/U0/inst/gt_top_i/pipe_wrapper_i/pipe_lane[0].gt_wrapper_i
/gtp_channel.gtpe2_channel_i}]
set_property PACKAGE_PIN    H1        [get_ports PER0_N]
set_property PACKAGE_PIN    H2        [get_ports PER0_P]
set_property PACKAGE_PIN    E3        [get_ports PET0_N]
set_property PACKAGE_PIN    E4        [get_ports PET0_P]

# PCIe Reference Clock
set_property PACKAGE_PIN    D5        [get_ports REFCLK_N]
set_property PACKAGE_PIN    D6        [get_ports REFCLK_P]

# PERST
set_property -dict { PACKAGE_PIN K1   IOSTANDARD LVCMOS33                      }  [get_ports
PERST_n]


## ############################################################################################ ##
## Front I/O
## ############################################################################################ ##

# Setting Pin locations, IOSTANDARD, and SLEW and DRIVE for Outputs only
set_property -dict { PACKAGE_PIN B16  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[0]}]
set_property -dict { PACKAGE_PIN G14  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[1]}]
set_property -dict { PACKAGE_PIN C11  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[2]}]
set_property -dict { PACKAGE_PIN C14  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[3]}]
set_property -dict { PACKAGE_PIN E13  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[4]}]
set_property -dict { PACKAGE_PIN C13  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[5]}]
set_property -dict { PACKAGE_PIN F17  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[6]}]
set_property -dict { PACKAGE_PIN A17  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[7]}]
set_property -dict { PACKAGE_PIN E17  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[8]}]
set_property -dict { PACKAGE_PIN C18  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[9]}]
set_property -dict { PACKAGE_PIN H16  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[10]}]
set_property -dict { PACKAGE_PIN E16  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[11]}]
set_property -dict { PACKAGE_PIN M17  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[12]}]
set_property -dict { PACKAGE_PIN J14  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[13]}]
set_property -dict { PACKAGE_PIN P18  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[14]}]
set_property -dict { PACKAGE_PIN L18  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[15]}]
set_property -dict { PACKAGE_PIN T18  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[16]}]
set_property -dict { PACKAGE_PIN V17  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[17]}]
set_property -dict { PACKAGE_PIN U11  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[18]}]
```

```
set_property -dict { PACKAGE_PIN U12  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[19]}]
set_property -dict { PACKAGE_PIN V9   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[20]}]
set_property -dict { PACKAGE_PIN U10  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[21]}]
set_property -dict { PACKAGE_PIN J4   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[22]}]
set_property -dict { PACKAGE_PIN M5   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[23]}]
set_property -dict { PACKAGE_PIN K3   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[24]}]
set_property -dict { PACKAGE_PIN L3   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{OE[25]}]

set_property -dict { PACKAGE_PIN A10  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[0]}]
set_property -dict { PACKAGE_PIN A15  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[1]}]
set_property -dict { PACKAGE_PIN H14  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[2]}]
set_property -dict { PACKAGE_PIN D11  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[3]}]
set_property -dict { PACKAGE_PIN F15  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[4]}]
set_property -dict { PACKAGE_PIN B17  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[5]}]
set_property -dict { PACKAGE_PIN D14  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[6]}]
set_property -dict { PACKAGE_PIN D13  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[7]}]
set_property -dict { PACKAGE_PIN B14  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[8]}]
set_property -dict { PACKAGE_PIN G16  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[9]}]
set_property -dict { PACKAGE_PIN G15  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[10]}]
set_property -dict { PACKAGE_PIN C12  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[11]}]
set_property -dict { PACKAGE_PIN U14  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[12]}]
set_property -dict { PACKAGE_PIN K15  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[13]}]
set_property -dict { PACKAGE_PIN T13  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[14]}]
set_property -dict { PACKAGE_PIN T15  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[15]}]
set_property -dict { PACKAGE_PIN T17  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[16]}]
set_property -dict { PACKAGE_PIN K17  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[17]}]
set_property -dict { PACKAGE_PIN T14  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[18]}]
set_property -dict { PACKAGE_PIN V12  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[19]}]
set_property -dict { PACKAGE_PIN V11  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[20]}]
set_property -dict { PACKAGE_PIN R15  IOSTANDARD LVCMOS33                      }  [get_ports
{DI[21]}]
set_property -dict { PACKAGE_PIN V8   IOSTANDARD LVCMOS33                      }  [get_ports
{DI[22]}]
set_property -dict { PACKAGE_PIN J5   IOSTANDARD LVCMOS33                      }  [get_ports
{DI[23]}]
set_property -dict { PACKAGE_PIN K2   IOSTANDARD LVCMOS33                      }  [get_ports
{DI[24]}]
set_property -dict { PACKAGE_PIN L5   IOSTANDARD LVCMOS33                      }  [get_ports
{DI[25]}]

set_property -dict { PACKAGE_PIN D15  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[0]}]
set_property -dict { PACKAGE_PIN B10  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[1]}]
set_property -dict { PACKAGE_PIN D16  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
```

```
{DO[2]}]
set_property -dict { PACKAGE_PIN B15  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[3]}]
set_property -dict { PACKAGE_PIN E15  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[4]}]
set_property -dict { PACKAGE_PIN C16  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[5]}]
set_property -dict { PACKAGE_PIN F14  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[6]}]
set_property -dict { PACKAGE_PIN C17  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[7]}]
set_property -dict { PACKAGE_PIN D10  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[8]}]
set_property -dict { PACKAGE_PIN D18  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[9]}]
set_property -dict { PACKAGE_PIN H17  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[10]}]
set_property -dict { PACKAGE_PIN G17  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[11]}]
set_property -dict { PACKAGE_PIN V14  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[12]}]
set_property -dict { PACKAGE_PIN L14  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[13]}]
set_property -dict { PACKAGE_PIN R13  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[14]}]
set_property -dict { PACKAGE_PIN N18  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[15]}]
set_property -dict { PACKAGE_PIN V16  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[16]}]
set_property -dict { PACKAGE_PIN U15  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[17]}]
set_property -dict { PACKAGE_PIN P15  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[18]}]
set_property -dict { PACKAGE_PIN T12  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[19]}]
set_property -dict { PACKAGE_PIN U9   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[20]}]
set_property -dict { PACKAGE_PIN U16  IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[21]}]
set_property -dict { PACKAGE_PIN M6   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[22]}]
set_property -dict { PACKAGE_PIN R7   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[23]}]
set_property -dict { PACKAGE_PIN P1   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[24]}]
set_property -dict { PACKAGE_PIN J6   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{DO[25]}]

set_property -dict { PACKAGE_PIN V7   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{PULL_SEL[0]}]
set_property -dict { PACKAGE_PIN V6   IOSTANDARD LVCMOS33  SLEW SLOW  DRIVE  4  }  [get_ports
{PULL_SEL[1]}]


## ############################################################################################ ##
## I2C Interfaces
## ############################################################################################ ##

# Setting Pin locations, IOSTANDARD, and SLEW
set_property -dict { PACKAGE_PIN R1   IOSTANDARD LVCMOS33  SLEW SLOW           }  [get_ports
PROM_SCL]
set_property -dict { PACKAGE_PIN U1   IOSTANDARD LVCMOS33  SLEW SLOW           }  [get_ports
PROM_SDA]
set_property -dict { PACKAGE_PIN F18  IOSTANDARD LVCMOS33  SLEW SLOW           }  [get_ports
SE95_SCL]
set_property -dict { PACKAGE_PIN H18  IOSTANDARD LVCMOS33  SLEW SLOW           }  [get_ports
SE95_SDA]
set_property -dict { PACKAGE_PIN E18  IOSTANDARD LVCMOS33                      }  [get_ports
SE95_OS]


## ############################################################################################ ##
## SPI Interface
```

```
## ########################################################################################################## ##

# CCLK runs through STARTUPE2
#set_property PACKAGE_PIN   E8        [get_ports CCLK]

# Setting Pin locations, IOSTANDARD, and SLEW
set_property -dict { PACKAGE_PIN L15  IOSTANDARD LVCMOS33                      }  [get_ports
SPI_CS_n]
set_property -dict { PACKAGE_PIN K16  IOSTANDARD LVCMOS33                      }  [get_ports
SPI_DI]
set_property -dict { PACKAGE_PIN L17  IOSTANDARD LVCMOS33                      }  [get_ports
SPI_DO]
set_property -dict { PACKAGE_PIN J15  IOSTANDARD LVCMOS33                      }  [get_ports
SPI_WP_n]
set_property -dict { PACKAGE_PIN J16  IOSTANDARD LVCMOS33                      }  [get_ports
SPI_HOLD_n]


## ########################################################################################################## ##
## Section: Miscellaneous
## ########################################################################################################## ##

# XADC inputs
set_property -dict { PACKAGE_PIN D8   IOSTANDARD LVCMOS33                      }  [get_ports
VAUXP0]
set_property -dict { PACKAGE_PIN C8   IOSTANDARD LVCMOS33                      }  [get_ports
VAUXN0]
set_property -dict { PACKAGE_PIN B9   IOSTANDARD LVCMOS33                      }  [get_ports
VAUXP1]
set_property -dict { PACKAGE_PIN A9   IOSTANDARD LVCMOS33                      }  [get_ports
VAUXN1]
set_property -dict { PACKAGE_PIN D9   IOSTANDARD LVCMOS33                      }  [get_ports
VAUXP8]
set_property -dict { PACKAGE_PIN C9   IOSTANDARD LVCMOS33                      }  [get_ports
VAUXN8]
set_property -dict { PACKAGE_PIN B12  IOSTANDARD LVCMOS33                      }  [get_ports
VAUXP2]
set_property -dict { PACKAGE_PIN A12  IOSTANDARD LVCMOS33                      }  [get_ports
VAUXN2]
set_property -dict { PACKAGE_PIN A13  IOSTANDARD LVCMOS33                      }  [get_ports
VAUXP10]
set_property -dict { PACKAGE_PIN A14  IOSTANDARD LVCMOS33                      }  [get_ports
VAUXN10]


# 100 MHz External Configuration Master Clock
set_property -dict { PACKAGE_PIN K18  IOSTANDARD LVCMOS33                      }  [get_ports
EMC_CLK]
# Allow connection from non-clockable pin to clock nets
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets EMC_CLK]


# 100 MHz External User Clock
set_property -dict { PACKAGE_PIN P14  IOSTANDARD LVCMOS33                      }  [get_ports
USR_CLK]


# LEDs
set_property -dict { PACKAGE_PIN V2   IOSTANDARD LVCMOS33  SLEW SLOW           }  [get_ports
LED_WWAN]
set_property -dict { PACKAGE_PIN V4   IOSTANDARD LVCMOS33  SLEW SLOW           }  [get_ports
LED_WPAN]
set_property -dict { PACKAGE_PIN V3   IOSTANDARD LVCMOS33  SLEW SLOW           }  [get_ports
LED_WLAN]


# PCIe Mini Card SMBus
set_property PROHIBIT TRUE  [get_sites M1]
set_property PROHIBIT TRUE  [get_sites N1]


## ########################################################################################################## ##
## Basic timing constraints
```

```
## ############################################################################################################ ##

# PCIe Reference Clock
create_clock -period 10.000 [get_ports REFCLK_P]

# 100 MHz External Configuration Master Clock
create_clock -period 10.000 [get_ports EMC_CLK]

# 100 MHz External User Clock
create_clock -period 10.000 [get_ports USR_CLK]


## ############################################################################################################ ##
## Configuration constraints
## ############################################################################################################ ##

# General Config Settings
set_property CFGBVS                             VCCO      [current_design]
set_property CONFIG_VOLTAGE                     3.3       [current_design]
set_property BITSTREAM.GENERAL.COMPRESS         FALSE     [current_design]


# Boot from external Clock
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN  div-1     [current_design]


# SPI x4 Settings
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE     YES       [current_design]
set_property CONFIG_MODE                        SPIx4     [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH      4         [current_design]
```