The Embedded I/O Company

TEWS TECHNOLOGIES

TMPE627

Reconfigurable FPGA with AD/DA & Digital I/O PCIe Mini Card

Version 1.0

User Manual

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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

TMPE627-10R

14 TTL I/O, 4 AD, 4 DA, Artix-7 7A50T FPGA

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	June 2017
1.0.1	Corrected typos	October 2017
1.0.2	Changed Document Title Added “A Remark About Slot Supplies”	January 2018
1.0.3	Clarified unipolar ADC input ranges	February 2020
1.0.4	Corrected “Mating Part” number for the I/O connector (X2)	April 2020
1.0.5	Corrected minor formatting errors & typos Clarified exact FPGA part number Clarified the ADC input filter	April 2021
1.0.6	Clarified SPI-Flash	September 2021

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1 Product Description

The TMPE627 is a standard full PCI Express Mini Card, providing a user programmable Xilinx Artix-7 7A50T FPGA.

The TMPE627 provides 14 ESD-protected 5 V-tolerant TTL lines. All I/O lines are individually programmable as input or output. TTL I/O lines can be set to high, low, or tristate. Each TTL I/O line has a pull-resistor to a common programmable pull voltage that can be set so +3.3 V, +5 V and GND.

The DAC offers 4 channels of 16 bit analog outputs with software selectable output voltage ranges of 0-5 V, 0-10 V, 0-10.8 V, ±5 V, ±10 V or ±10.8 V. The output voltage range can be individually set per channel. The conversion time is typ. 10 µs and the DAC outputs are capable to drive a load of 2 kΩ, with a capacitance up to 4000 pF.

The 16 bit ADC offers 4 input channels that can be operated in single-ended or differential mode. It offers software selectable input voltage ranges of 0-5.12 V, 0-10 V, 0-10.24 V, ±5 V, ±5.12 V, ±10 V and ±10.24 V with a sampling rate of up to 200 ksps.

Each TMPE627 is factory calibrated. The calibration information is stored in an on-board serial EEPROM unique to each TMPE627 module.

The I/O signals are accessible through a 30 pin Pico-Clasp latching connector.

The User FPGA is configured by a SPI flash. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using the Vivado ILA). With the TA308 Programming Kit direct JTAG access to the FPGA is possible, using the Xilinx Platform Cable USB.

User applications for the TMPE627 with 7A50T FPGA can be developed using the design software Vivado Design Suite HL WebPACK Edition, which can be downloaded free of charge from www.xilinx.com.

TEWS offers a well-documented basic FPGA Example Application design. It includes a constraints file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TMPE627. It implements PCIe to register mapping and basic I/O. It comes as a Xilinx Vivado Design Suite project with source code and as a ready-to-download bit stream.

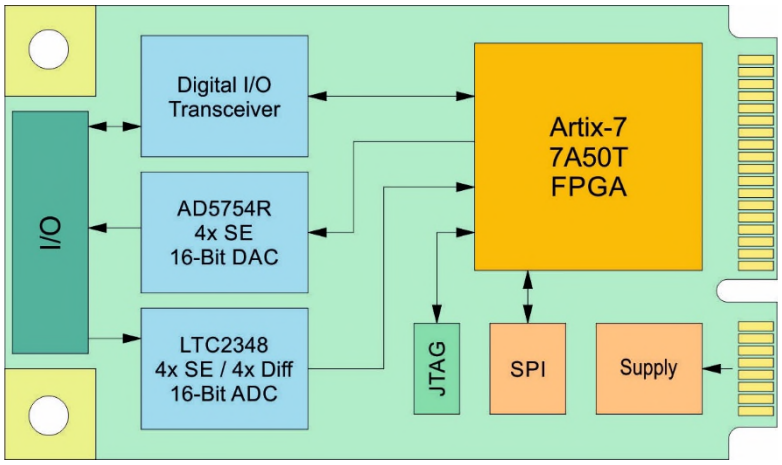


Figure 1-1: Block Diagram

2 Technical Specification

Interface		
Mechanical Interface	PCI Express Mini Card conforming to PCI Express Mini Card Electromechanical Specification, Revision 2.0 Card Type: Full-Mini Card (50.95 x 30 mm)	
Electrical Interface	PCI Express x1 Link conforming to PCI Express Base Specification, Revision 2.0 The TMPE627 does not support the USB interface	
Main On-Board Devices		
User configurable FPGA	TMPE627-10R: XC7A50T-2CSG325I (Xilinx)	
SPI-Flash	Micron N25Q128A (or compatible) 128 Mbit SPI-Flash covered by the Vivado “mt25ql128” device settings. (contains TMPE627 FPGA Example)	
ADC	LTC2348 (Linear Technologies)	
DAC	AD5754R (Analog Devices)	
I/O Interface		
Digital I/O Channels	14 ESD-protected 5 V-tolerant TTL lines	
Digital I/O Transceiver	74LVC2G241 (or compatible)	
Analog Inputs	4x 16-bit, 200 ksps, simultaneous sampling differential/single-ended ADC	
Analog Input Voltage	Software selectable: 0-5.12 V, 0-10 V, 0-10.24 V, ±5 V, ±5.12 V, ±10 V, ±10.24 V	
Analog Output Channels	4x 16-bit, 10 µs settling, single-ended DAC	
Analog Output Voltage	Software selectable: 0-5 V, 0-10 V, 0-10.8V, ±5 V, ±10 V, ±10.8 V	
I/O Connector	30 pol. Pico-Clasp latching connector	
Physical Data		
Power Requirements	Depends on FPGA design With TMPE627 FPGA Example Design running, DACs driving the ADCs and into a 2 kΩ load: +3.3 Vaux: 650 mA typical +1.5 V: 200 mA typical	
Temperature Range	Operating	refer to “Thermal Management” chapter
	Storage	-40°C to +85°C
MTBF	987.000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	13 g	

Table 2-1: Technical Specification

3 Handling and Operating Instructions

3.1 ESD Protection

The PCI Express Mini Card module is sensitive to static electricity. Packing, unpacking and all other module handling has to be done in an ESD/EOS protected Area.

3.2 Height Restrictions

The I/O connector and the heatsink will exceed the available PCI Express Mini Card components height. Check carefully if your application provides enough spacing for a TMPE627.

3.3 Thermal Considerations

Due to its small size and high density, the TMPE627 can generate a lot of heat.

Forced air cooling is recommended during operation. If forced air cooling is not possible, another equivalent cooling mechanism must be applied. Without adequate cooling, damage to the device can occur.

4 Functional Description

This chapter gives a brief overview of the various module functions.

4.1 User FPGA Overview

The FPGA is an Artix-7 in a CSG325 package.

Artix-7	Slices	Flip-Flops	DSP48A1 Slices	Block RAM (Kb)	GTP Transceivers
7A50T	8150	65200	120	2700	4

Table 4-1: TMPE627 FPGA Feature Overview

The FPGA is equipped with 4 I/O banks and 4 Gigabit (GTP) Transceivers. One of the GTPs can be connected to an Endpoint Block for PCI Express.

Bank	V_{CCO}	V_{REF}	Signals	Remarks
Bank 0	3.3 V	none	Configuration	
Bank 14	3.3 V	none	I/O Interface	
Bank 15	3.3 V	none	I/O Interface	+Configuration
Bank 34	3.3 V	none	I/O Interface	
GTP Bank	**Description**			**Remarks**
Bank 216	GTP0: PCIe Endpoint Block GTP1: Not used GTP2: Not used GTP3: Not used			

Table 4-2: FPGA Bank Usage

4.2 User FPGA Gigabit Transceiver (GTP)

The TMPE627 provides one GTP as 7 Series FPGAs Integrated Block for PCI Express.

GTP	Signal	FPGA Pins	Connected to
GTP0 (X0Y0)	MGTPTX	H1 / H2	used for FPGA Integrated Block for PCI Express
	MGTPRX	E3 / E4	
GTP1 (X0Y1)	MGTPTX	F1 / F2	Not used
	MGTPRX	A3 / A4	
GTP2 (X0Y2)	MGTPTX	D1 / D2	Not used
	MGTPRX	C5 / C6	
GTP3 (X0Y3)	MGTPTX	B1 / B2	Not used
	MGTPRX	G3 / G4	

Table 4-3: GTP Connections

The 100 MHz MGT clock MGTREFCLK0 (FPGA Integrated Block for PCI Express) is connected directly to the PCI Express Mini Card reference clock. MGTREFCLK1is not used on the TMPE627.

GTP	Signal	FPGA Pins	Connected to
MGTREFCLK0	MGTREFCLK	D5 / D6	100 MHz (backplane clock)
MGTREFCLK1	MGTREFCLK	B5 / B6	not connected

Table 4-4: Gigabit Transceiver Reference Clocks

4.3 User FPGA Configuration

The Artix-7 FPGA can be configured by the following interfaces:

- Master Serial SPI Flash Configuration Interface
- JTAG Interface via JTAG Header

On delivery the SPI configuration Platform Flash contains the TEWS example application for the TMPE627 Artix-7 device.

4.3.1 SPI-Flash

The TMPE627 provides a 128-Mbit serial Flash memory, which is used as the default FPGA configuration source. After configuration the flash is accessible from the FPGA, so it also can be used for additional code or user data storage. The SPI-Flash is connected via Quad (x4) SPI interface to Artix-7 configuration interface.

The SPI-Flash is a Micron N25Q128A (or compatible) covered by the Vivado “mt25ql128” device settings. The device ID is 0x20BA18.

SPI-Flash Signal	Bank	V_{CCO}	Pin	Description / Artix-7
CLK	0	3.3 V	E8	Serial Clock (CCLK)
CS#	14	3.3 V	L15	Chip Select (CS0_B)
DI (bit0)	14	3.3 V	K16	Serial Data input (MOSI) / MISO[0]
DO (bit1)	14	3.3 V	L17	Serial Data output (DIN) / MISO[1]
WP# (bit2)	14	3.3 V	J15	MISO[2]
HOLD# (bit3)	14	3.3 V	J16	MISO[3]

Table 4-5: FPGA SPI-Flash Connections

4.3.2 Configuration via JTAG

For direct FPGA configuration, FPGA read back or in-system diagnostics with ChipScope, the JTAG connector can be used to access the FPGA JTAG port. Also an indirect SPI-Flash programming is possible via the JTAG Chain.

4.3.3 Generate Artix-7 Configuration Data

To use the maximum configuration speed, the TMPE627 must be configured to use the 100 MHz external master clock as CCLK.

To use this configuration feature, the following configuration option must be set:

```
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN          div-1 [current_design]
set_property CONFIG_VOLTAGE                             3.3   [current_design]
set_property CFGBVS                                     VCCO  [current_design]
```

To use the maximum data transfer speed of the User FPGA SPI Configuration Flash the SPI Configuration Bus Width must be set to the x4.

```
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH              4     [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE             YES   [current_design]
set_property CONFIG_MODE                                SPIx4 [current_design]
```

Without this option, the configuration time for the Artix-7 FPGA exceed the maximum PCIe bus setup time.

4.4 Clocking

4.4.1 FPGA Clock Sources

The following table lists the available clock sources on the TMPE627:

FPGA Clock-Pin Name	FPGA Pin Number	Source	Description
MGTREFCLK0_101	D5 / D6	PCI Express Mini Card Slot	100 MHz PCIe Reference clock
IO_L3N_T0_DQS_EMCCLK_14	K18	External oscillator	100 MHz External master configuration clock

Table 4-6: Available FPGA clocks

4.5 Digital I/O Interface

Each of the 14 digital I/O channels provides an input and output data signal and an output enable signal to the digital buffers.

Signal Name	Pin Number	Direction	IO Standard	IO Bank	Drive [mA]	Slew Rate
DI<0>	N18	IN	LVCMOS33	14	4	SLOW
DI<1>	U10	IN	LVCMOS33	14	4	SLOW
DI<2>	J14	IN	LVCMOS33	14	4	SLOW
DI<3>	N17	IN	LVCMOS33	14	4	SLOW
DI<4>	M17	IN	LVCMOS33	14	4	SLOW
DI<5>	U17	IN	LVCMOS33	14	4	SLOW
DI<6>	R17	IN	LVCMOS33	14	4	SLOW
DI<7>	P18	IN	LVCMOS33	14	4	SLOW
DI<8>	U12	IN	LVCMOS33	14	4	SLOW
DI<9>	T17	IN	LVCMOS33	14	4	SLOW
DI<10>	U11	IN	LVCMOS33	14	4	SLOW
DI<11>	U14	IN	LVCMOS33	14	4	SLOW
DI<12>	P15	IN	LVCMOS33	14	4	SLOW
DI<13>	U9	IN	LVCMOS33	14	4	SLOW
DO<0>	V12	OUT	LVCMOS33	14	4	SLOW
DO<1>	L18	OUT	LVCMOS33	14	4	SLOW
DO<2>	T13	OUT	LVCMOS33	14	4	SLOW
DO<3>	L14	OUT	LVCMOS33	14	4	SLOW
DO<4>	M14	OUT	LVCMOS33	14	4	SLOW
DO<5>	R18	OUT	LVCMOS33	14	4	SLOW
DO<6>	P16	OUT	LVCMOS33	14	4	SLOW
DO<7>	P14	OUT	LVCMOS33	14	4	SLOW
DO<8>	V13	OUT	LVCMOS33	14	4	SLOW
DO<9>	T15	OUT	LVCMOS33	14	4	SLOW
DO<10>	R13	OUT	LVCMOS33	14	4	SLOW
DO<11>	V14	OUT	LVCMOS33	14	4	SLOW
DO<12>	U15	OUT	LVCMOS33	14	4	SLOW
DO<13>	T14	OUT	LVCMOS33	14	4	SLOW
OE<0>#	V9	OUTPUT	LVCMOS33	14	4	SLOW
OE<1>#	K17	OUTPUT	LVCMOS33	14	4	SLOW
OE<2>#	T12	OUTPUT	LVCMOS33	14	4	SLOW
OE<3>#	M16	OUTPUT	LVCMOS33	14	4	SLOW
OE<4>#	T18	OUTPUT	LVCMOS33	14	4	SLOW
OE<5>#	N16	OUTPUT	LVCMOS33	14	4	SLOW
OE<6>#	K15	OUTPUT	LVCMOS33	14	4	SLOW

Signal Name	Pin Number	Direction	IO Standard	IO Bank	Drive [mA]	Slew Rate
OE<7>#	M15	OUTPUT	LVCMOS33	14	4	SLOW
OE<8>#	V11	OUTPUT	LVCMOS33	14	4	SLOW
OE<9>#	N14	OUTPUT	LVCMOS33	14	4	SLOW
OE<10>#	U16	OUTPUT	LVCMOS33	14	4	SLOW
OE<11>#	V17	OUTPUT	LVCMOS33	14	4	SLOW
OE<12>#	R15	OUTPUT	LVCMOS33	14	4	SLOW
OE<13>#	V16	OUTPUT	LVCMOS33	14	4	SLOW
SEL<0>	R2	OUTPUT	LVCMOS33	34	4	SLOW
SEL<1>	V8	OUTPUT	LVCMOS33	34	4	SLOW

Table 4-7: Digital I/O Interface

4.5.1 TTL I/O Interface

Each I/O line is buffered by a 74LVC2G241. The 74LVC2G241 is a tri-state buffer that provides TTL compatible inputs with 5 V-tolerance. The outputs can be set to tri-state with an output enable signal and provide a 47 Ω serial resistor and a 4.7 kΩ pull resistor. The pull resistor guarantees a valid logic level when the outputs are tristate and not driven externally. The pull voltage can be set to 3.3 V, 5 V or GND. When set to 5 V, the outputs must not be driven, but set to tristate for a valid high level.

A TVS array protects against ESD shocks.

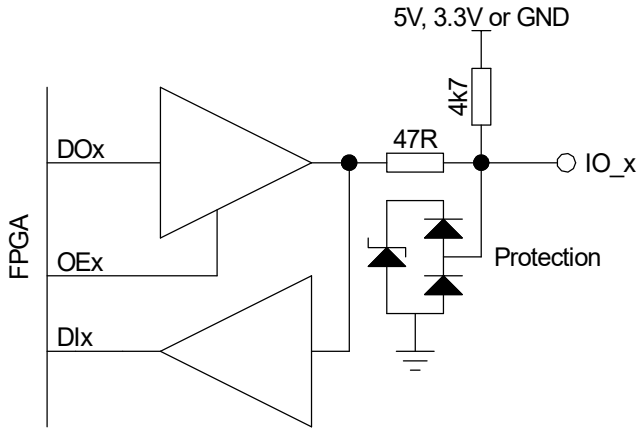


Figure 4-1: TTL I/O Interface

With the pull voltage set to 5 V, the digital I/O can weakly drive a higher voltage than 3.3 V by setting the output to tri-state. This can be useful when connecting to a standard 5 V CMOS logic input, where a high level of minimum 3.5 V is required. Drive DO constant low and use OE to toggle the output.

With the pull voltage set to GND, a pull-down functionality is implemented. Drive DO constant high and use OE to toggle the output.

Pull Option	DO	OE	Output	Remark
No pull-up or pull-down	0	1	0	
	1	1	1	
Pull-up to 3.3 V	0	1	0	
	1	1	1	Driven to 3.3 V
	-	0	1	Pulled to 3.3 V
Pull-up to 5 V	0	1	0	
	-	0	1	Pulled to 5 V
Pull-down to GND	-	0	0	Pulled to GND
	1	1	1	

Table 4-8: I/O Pull Options

If the pull resistors float, the user should keep in mind that the I/O Lines are still connected via their pull resistors.

The normal behavior is that the User FPGA code controls the I/O Pull Configuration depending on User FPGA I/O Function. The SEL signals are connected to an analog multiplexer. With this multiplexer the desired voltage can be adjusted directly from the User FPGA. The user must ensure that valid signals are always driven.

CNT Lines	Description	Artix-7 Pins
SEL[1:0]	11: pull-down 10: pull-up to 3.3 V 01: pull-up to 5 V 00: No pull-up or pull-down	V8, R2

Table 4-9: I/O Pull Configuration

4.5.1.1 Output Level & Output Current

Because of the 47 ohm series resistor, there is a reduced high-level voltage at the I/O pin when the output buffer sources a noticeable current to the external load while driving a high-level. To maintain a proper TTL high level, the recommended maximum I/O source current is 15 mA.

There is also an increased low-level voltage at the I/O pin when the output buffer sinks a noticeable current from the external load while driving a low-level. To maintain a proper TTL low level, the recommended maximum I/O sink current is 6 mA.

For achieving a 5 V CMOS high-level voltage (V_{OH} >= 3.5 V), the external load should be high impedance. If there would be a low impedance path to ground on the I/O load, this may result in a voltage divider with the on-board pull resistor, significantly reducing the high-level voltage at the I/O pin. To maintain a proper 5 V CMOS high level, the I/O load (leakage) current should not exceed 250 µA.

4.6 User GPIO

The TMPE627 has some optional general purpose I/O and debug signals connected to the FPGA. The required signaling standard is LVCMOS33.

The FPGA is connected to the status indicator of the PCI Express Mini Card Slot:

Signal	Bank	V_{CCO}	Pin	Description
LED_WWAN#	34	3.3 V	U1	WWAN status indicator
LED_WPAN#	34	3.3 V	V3	WPAN status indicator
LED_WLAN#	34	3.3 V	V2	WLAN status indicator

Table 4-10: FPGA General Purpose I/O

4.7 ADC Interface

The LTC2348 provide a pin-selectable SPI and LVDS serial interface. When the LVDS interface is active, the inputs at the ADC are terminated with internal 100 Ω differential termination resistors.

Signal	Bank	V_{CCO}	Pin	Description
PD	15	3.3 V	B17	Power Down Input
LVDS/CMOS#	15	3.3 V	B16	I/O Mode Select
CNV	15	3.3 V	C12	Conversion Start
BUSY	15	3.3 V	D18	Busy Output
CS#	15	3.3 V	G16	Chip Select
SDI	15	3.3 V	G17	Data Input
SDO0	15	3.3 V	A17	Data Output 0
SDO1 / SDI+	15	3.3 V	D13	Data Output 1 / LVDS Data Input+
SDO2 / SDI-	15	3.3 V	C13	Data Output 2 / LVDS Data Input-
SDO3 / SCKI+	15	3.3 V	E13	Data Output 3 / LVDS Clock Input+
SCKI / SCKI-	15	3.3 V	D14	Clock Input / LVDS Clock Input-
SCKO / SCKO+	15	3.3 V	E15	Clock Output / LVDS Clock Output+
SDO4 / SCKO-	15	3.3 V	D15	Data Output 4 / LVDS Clock Output-
SDO5 / SDO+	15	3.3 V	E16	Data Output 5 / LVDS Data Output+
SDO6 / SDO-	15	3.3 V	D16	Data Output 6 / LVDS Data Output-
SDO7	15	3.3 V	C18	Data Output 7

Table 4-11: ADC I/O Interface

Associated with the ADC are two additional signals. These are fault flags, provided by the ADC input overvoltage protection. During normal operation the flags are high. During an overvoltage condition the flags are pulled low.

Signal	Bank	V_{CCO}	Pin	Description
FF_12	15	3.3 V	B11	Fault flag for ADC channels 1 & 2
FF_34	15	3.3 V	E17	Fault flag for ADC channels 3 & 4

Table 4-12: ADC Fault Flag

4.7.1 ADC

Protection	4 kV ESD HMB rating on analog input channels ±55 V power-off and overvoltage protection
Input Impedance	>1 GΩ
Input Capacitance	5 pF
Common-Mode Input Range	±11 V

Table 4-13: ADC Electrical Interface

All analog inputs are connected through 1st order low-pass filter, an overvoltage protection device and a high input impedance buffer amplifier to the ADC. The -3dB cutoff frequency of the input filter is approx. 100 kHz.

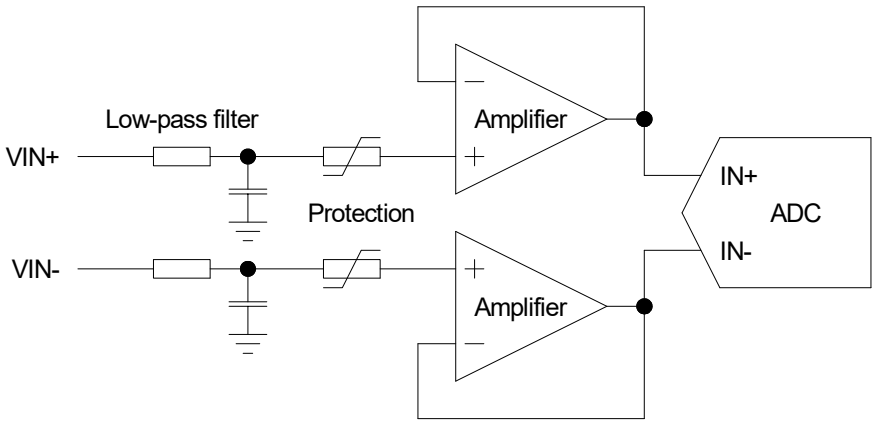


Figure 4-2: ADC Input Circuit

The absolute input voltage limit for the analog inputs is ±11 V relative to ground for each pin. The common mode range is limited by the buffer amplifier.

Input Range (by datasheet)	Full scale range	Absolute input voltage[1]	Binary Format
±10.24 V	20.48 V	±5.12 V	Two's Complement
±10 V	20 V	±5 V	Two's Complement
±5.12 V	10.24 V	±2.56 V	Two's Complement
±5 V	10 V	±2.5 V	Two's Complement
0 V to 10.24 V	10.24 V	10.24 V	Straight Binary
0 V to 10 V	10 V	10 V	Straight Binary
0 V to 5.12 V	5.12 V	5.12 V	Straight Binary

[1]Differential, Antiphase Inputs with a Zero Common Mode

Table 4-14: ADC Input Ranges

Due to the wide common mode input voltage range the differential signal can be almost anywhere in the allowed range, i.e. in the "±10 V" input range a ±5 V differential signal can have an offset (or common mode voltage, (VIN+ + VIN–)/2) of 8 V without problem.

The unipolar input ranges are intended for input signals where VIN+ remains over VIN-. Usually VIN- is connected to AGND and VIN+ is used as a standard single-ended input. However, the input signals are

allowed to swing with an arbitrary relationship to each other, provided each pin remains within the common mode range and VIN+ remains over VIN-.

ADC Input Schemes

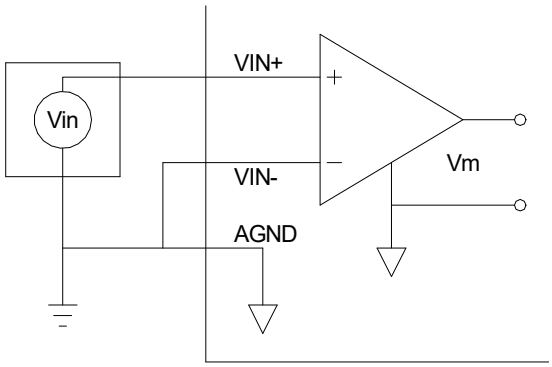
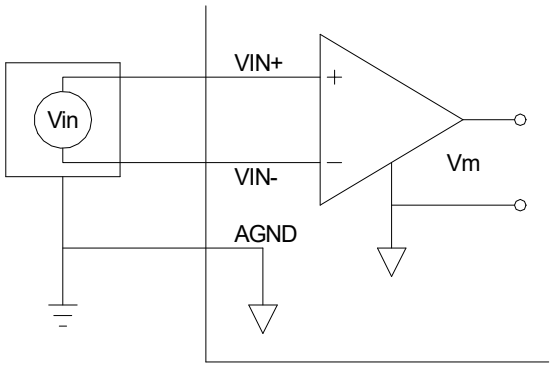
Single-Ended with Ground Reference	Differential with Ground Reference
	

Table 4-15: ADC Input Schemes

If signals without a ground reference should be connected, use the single-ended input scheme or connect VIN+ and VIN- to AGND with a resistor to prevent the signal source to float out of the ADC's common-mode range. In most cases the VIN- connection suffices.

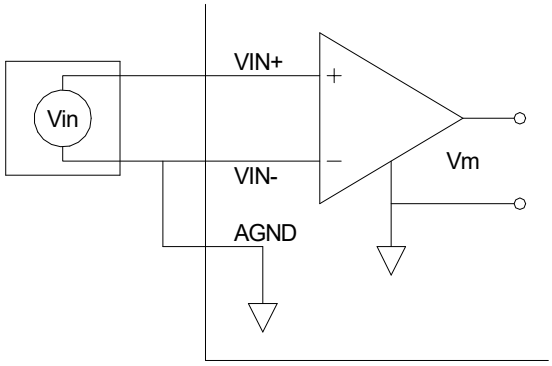
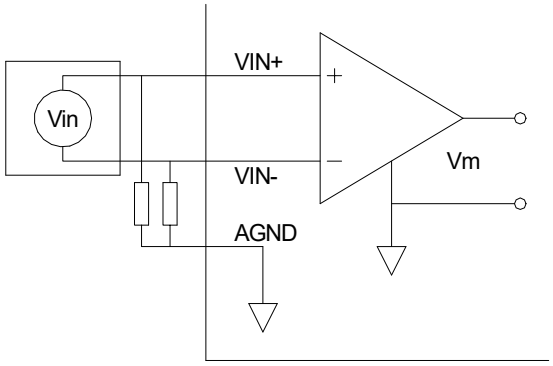
Single-Ended without Ground Reference	Differential without Ground Reference
	

Table 4-16: ADC Input Schemes

Unused ADC channels should be connected to AGND.

4.8 DAC Interface

The DAC signals are accessible through the I/O bank 15 of the Artix-7 FPGA.

Signal	Bank	V_{CCO}	Pin	Description
SCLK	15	3.3 V	F17	Serial Clock Input
SDIN	15	3.3 V	C11	Serial Data Input
SDO	15	3.3 V	A15	Serial Data Output
SYNC#	15	3.3 V	D10	Frame synchronization signal
LDAC#	15	3.3 V	G14	Load DAC
CLR#	15	3.3 V	F14	Sets the DAC registers to zero-scale or midscale code
BIN2S	15	3.3 V	B15	DAC coding for a bipolar output range

Table 4-17: DAC I/O Interface

4.8.1 DAC

All analog outputs are directly connected to DAC pins.

Protection	3.5 kV ESD HMB rating on analog input channels
DC Output Impedance	0.5 Ω
Load	2 kΩ
Capacitive Load	4000 pF

Table 4-18: DAC Electrical Interface

4.8.2 DAC Overcurrent Protection

Generally the DAC's "Automatic Channel Power-Down" overcurrent protection feature should be used instead of the current limit clamp. This minimizes the effect of a fault on a DAC output because of the limited power supply.

In case of an overload condition, the DAC channel is powered down and its output is clamped to ground with a resistance of ~4 kΩ. This condition is indicated by the OCx bit set to '1' and the PUx set to '0'. The channel can be powered up again by setting the PUx bit back to '1' after the overload condition is relieved.

4.9 I²C-EEPROM

The TMPE627 provides an Atmel AT24C04 4-kbit I²C memory, which is used to store the ADC and DAC correction data.

Although the EEPROM is not write-protected it should be generally treated as a read-only resource for FPGA designs.

Refer to “4.12.2 Correction EEPROM” for details about the stored data. The device address will be “1010000”.

SPI-Flash Signal	Bank	V_{CCO}	Pin	Description
SCL	34	3.3 V	R1	Serial Clock
SDA	34	3.3 V	T2	Serial Data

Table 4-19: FPGA I²C-EEPROM Connections

4.10 I²C Temperature Sensor

The TMPE627 provides an NXP SE95 13-bit temperature sensor. The device address will be “1001000”.

SPI-Flash Signal	Bank	V_{CCO}	Pin	Description
SCL_SE95	15	3.3 V	H16	Serial Clock
SDA_SE95	15	3.3 V	F15	Serial Data
OS	15	3.3 V	H18	“Overtemperature Shutdown”

Table 4-20: FPGA I²C Temperature Sensor Connections

4.11 Thermal Management

All components used on the TMPE627 are rated for the industrial temperature range of -40°C to +85°C. The actual temperature range the TMPE627 can be used in is highly dependent on the FPGA design, the load of the modules I/O circuitry and the applied cooling method.

The module has several hot spots including operational amplifiers, ADC and DAC, power supplies and the FPGA. The TMPE627 is equipped with a basic heatsink that help to evenly spread the heat and provides a mounting base for additional cooling such as additional passive heatsinks, heat pipes or active cooling.

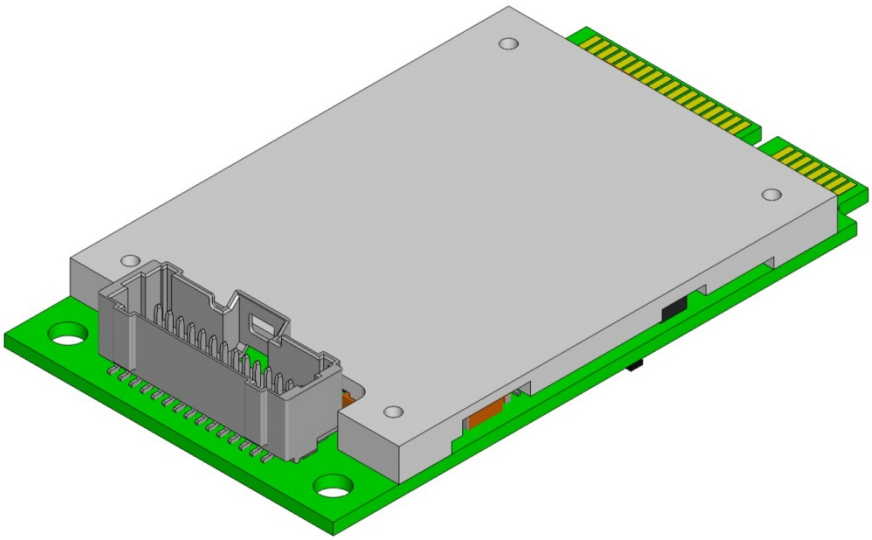


Figure 4-3: TMPE627 with Heat Sink

Mounting a heatsink will violate the Mini PCIe Card component envelope. Check carefully if your system provides enough spacing for a TMPE627 with mounted heatsink. In space constrained systems mounting a heatsink may not be possible. In this case forced air cooling must be applied during operation.

Use the Xilinx XPower Estimator (XPE) or the Vivado Power Report to determine whether additional cooling requirements such as forced air cooling apply. It is also strongly recommended to use the internal temperature monitoring of the Artix-7 and the on-board temperature sensor to monitor the temperature.

As an indication: With the example application running in a standard PC enclosure at 25°C the TMPE627 current requirement is 650 mA @ 3.3 V and 200 mA @ 1.5 V, resulting in a TMPE627 board temperature of about 50°C and an internal temperature of the Artix-7 FPGA of about 60°C.

4.12 ADC & DAC Correction

There are two errors that affect the DC accuracy of the ADCs and DACs.

Offset Error:

The Offset Error is the deviation from an ideal zero. For ADCs it is the data value when converting with the input connected to its own ground in single-ended mode, or with shorted inputs in differential mode. For DACs it is the difference between the ideal and actual DAC output with zero code as digital input. This error can be corrected by subtracting the known error from the datum.

Gain Error:

The Gain Error is the deviation in slope of the ideal ADC or DAC transfer characteristic. This error can be corrected by multiplying the datum with the correction factor.

The TMPE627 provides offset and gain correction values for each channel and voltage range. The correction values are based on a linear regression.

The correction values are obtained during factory calibration and are stored in an on-board EEPROM as 2-complement 2-byte-wide values in the range from -32768 to +32767. To achieve a higher accuracy, they are scaled to ¼ LSB.

4.12.1 Off-Module Correction

The correction can be done off-module in software, using the following correction formula:

$$Data = Value \cdot \left(1 - \frac{Gain_{corr}}{2^{\mathrm{Re}\,solution}} \cdot \frac{1}{4}\right) - Offset_{corr} \cdot \frac{1}{4}$$

Figure 4-4: Correction Formula

Data is the corrected result (for AD channels this is the ADC input value, for DA channels this is the value that has to be written to the DAC to achieve the desired output value).

Value is the uncorrected datum (for AD channels this is the ADC reading, for DA channels this is the desired output value).

$Gain_{corr}$ and $Offset_{corr}$ are the correction values stored in the Calibration Value ROM.

Resolution is the data converter resolution in bit (for the TMPE627 it is 16 for both AD and DA)

Floating point arithmetic or scaled integer arithmetic must be used to avoid rounding errors in computing above formula.

Due to inherent device deviation, the extremes of the full scale range may not be fully reachable, even after calibration.

4.12.2 Correction EEPROM

The correction values are determined at factory and are stored in the I²C-EEPROM.

There is an offset correction value and a gain correction value for each ADC and DAC channel at each voltage range. To achieve a higher accuracy, they are scaled to ¼ LSB.

Offset	Description	Voltage Range	Size (Bit)
0x000	ADC Channel 1 $Offset_{CORR}$	5.12 V	16
0x002	ADC Channel 1 $Gain_{CORR}$	5.12 V	16
0x004	ADC Channel 2 $Offset_{CORR}$	5.12 V	16
0x006	ADC Channel 2 $Gain_{CORR}$	5.12 V	16
0x008	ADC Channel 3 $Offset_{CORR}$	5.12 V	16
0x00A	ADC Channel 3 $Gain_{CORR}$	5.12 V	16
0x00C	ADC Channel 4 $Offset_{CORR}$	5.12 V	16
0x00E	ADC Channel 4 $Gain_{CORR}$	5.12 V	16
0x010	ADC Channel 1 $Offset_{CORR}$	±5 V	16
0x012	ADC Channel 1 $Gain_{CORR}$	±5 V	16
0x014	ADC Channel 2 $Offset_{CORR}$	±5 V	16
0x016	ADC Channel 2 $Gain_{CORR}$	±5 V	16
0x018	ADC Channel 3 $Offset_{CORR}$	±5 V	16
0x01A	ADC Channel 3 $Gain_{CORR}$	±5 V	16
0x01C	ADC Channel 4 $Offset_{CORR}$	±5 V	16
0x01E	ADC Channel 4 $Gain_{CORR}$	±5 V	16
0x020	ADC Channel 1 $Offset_{CORR}$	±5.12 V	16
0x022	ADC Channel 1 $Gain_{CORR}$	±5.12 V	16
0x024	ADC Channel 2 $Offset_{CORR}$	±5.12 V	16
0x026	ADC Channel 2 $Gain_{CORR}$	±5.12 V	16
0x028	ADC Channel 3 $Offset_{CORR}$	±5.12 V	16
0x02A	ADC Channel 3 $Gain_{CORR}$	±5.12 V	16
0x02C	ADC Channel 4 $Offset_{CORR}$	±5.12 V	16
0x02E	ADC Channel 4 $Gain_{CORR}$	±5.12 V	16
0x030	ADC Channel 1 $Offset_{CORR}$	10 V	16
0x032	ADC Channel 1 $Gain_{CORR}$	10 V	16
0x034	ADC Channel 2 $Offset_{CORR}$	10 V	16
0x036	ADC Channel 2 $Gain_{CORR}$	10 V	16
0x038	ADC Channel 3 $Offset_{CORR}$	10 V	16
0x03A	ADC Channel 3 $Gain_{CORR}$	10 V	16
0x03C	ADC Channel 4 $Offset_{CORR}$	10 V	16
0x03E	ADC Channel 4 $Gain_{CORR}$	10 V	16
0x040	ADC Channel 1 $Offset_{CORR}$	10.24 V	16
0x042	ADC Channel 1 $Gain_{CORR}$	10.24 V	16

Offset	Description	Voltage Range	Size (Bit)
0x044	ADC Channel 2 $Offset_{CORR}$	10.24 V	16
0x046	ADC Channel 2 $Gain_{CORR}$	10.24 V	16
0x048	ADC Channel 3 $Offset_{CORR}$	10.24 V	16
0x04A	ADC Channel 3 $Gain_{CORR}$	10.24 V	16
0x04C	ADC Channel 4 $Offset_{CORR}$	10.24 V	16
0x04E	ADC Channel 4 $Gain_{CORR}$	10.24 V	16
0x050	ADC Channel 1 $Offset_{CORR}$	±10 V	16
0x052	ADC Channel 1 $Gain_{CORR}$	±10 V	16
0x054	ADC Channel 2 $Offset_{CORR}$	±10 V	16
0x056	ADC Channel 2 $Gain_{CORR}$	±10 V	16
0x058	ADC Channel 3 $Offset_{CORR}$	±10 V	16
0x05A	ADC Channel 3 $Gain_{CORR}$	±10 V	16
0x05C	ADC Channel 4 $Offset_{CORR}$	±10 V	16
0x05E	ADC Channel 4 $Gain_{CORR}$	±10 V	16
0x060	ADC Channel 1 $Offset_{CORR}$	±10.24 V	16
0x062	ADC Channel 1 $Gain_{CORR}$	±10.24 V	16
0x064	ADC Channel 2 $Offset_{CORR}$	±10.24 V	16
0x066	ADC Channel 2 $Gain_{CORR}$	±10.24 V	16
0x068	ADC Channel 3 $Offset_{CORR}$	±10.24 V	16
0x06A	ADC Channel 3 $Gain_{CORR}$	±10.24 V	16
0x06C	ADC Channel 4 $Offset_{CORR}$	±10.24 V	16
0x06E	ADC Channel 4 $Gain_{CORR}$	±10.24 V	16
0x070-0x7F	Reserved	-	-
0x080	DAC Channel 1 $Offset_{CORR}$	5 V	16
0x082	DAC Channel 1 $Gain_{CORR}$	5 V	16
0x084	DAC Channel 2 $Offset_{CORR}$	5 V	16
0x086	DAC Channel 2 $Gain_{CORR}$	5 V	16
0x088	DAC Channel 3 $Offset_{CORR}$	5 V	16
0x08A	DAC Channel 3 $Gain_{CORR}$	5 V	16
0x08C	DAC Channel 4 $Offset_{CORR}$	5 V	16
0x08E	DAC Channel 4 $Gain_{CORR}$	5 V	16
0x090	DAC Channel 1 $Offset_{CORR}$	10 V	16
0x092	DAC Channel 1 $Gain_{CORR}$	10 V	16
0x094	DAC Channel 2 $Offset_{CORR}$	10 V	16
0x096	DAC Channel 2 $Gain_{CORR}$	10 V	16
0x098	DAC Channel 3 $Offset_{CORR}$	10 V	16
0x09A	DAC Channel 3 $Gain_{CORR}$	10 V	16
0x09C	DAC Channel 4 $Offset_{CORR}$	10 V	16
0x09E	DAC Channel 4 $Gain_{CORR}$	10 V	16

Offset	Description	Voltage Range	Size (Bit)
0x0A0	DAC Channel 1 $Offset_{CORR}$	±5 V	16
0x0A2	DAC Channel 1 $Gain_{CORR}$	±5 V	16
0x0A4	DAC Channel 2 $Offset_{CORR}$	±5 V	16
0x0A6	DAC Channel 2 $Gain_{CORR}$	±5 V	16
0x0A8	DAC Channel 3 $Offset_{CORR}$	±5 V	16
0x0AA	DAC Channel 3 $Gain_{CORR}$	±5 V	16
0x0AC	DAC Channel 4 $Offset_{CORR}$	±5 V	16
0x0AE	DAC Channel 4 $Gain_{CORR}$	±5 V	16
0x0B0	DAC Channel 1 $Offset_{CORR}$	±10 V	16
0x0B2	DAC Channel 1 $Gain_{CORR}$	±10 V	16
0x0B4	DAC Channel 2 $Offset_{CORR}$	±10 V	16
0x0B6	DAC Channel 2 $Gain_{CORR}$	±10 V	16
0x0B8	DAC Channel 3 $Offset_{CORR}$	±10 V	16
0x0BA	DAC Channel 3 $Gain_{CORR}$	±10 V	16
0x0BC	DAC Channel 4 $Offset_{CORR}$	±10 V	16
0x0BE	DAC Channel 4 $Gain_{CORR}$	±10 V	16
0x0C0	DAC Channel 1 $Offset_{CORR}$	10.8 V	16
0x0C2	DAC Channel 1 $Gain_{CORR}$	10.8 V	16
0x0C4	DAC Channel 2 $Offset_{CORR}$	10.8 V	16
0x0C6	DAC Channel 2 $Gain_{CORR}$	10.8 V	16
0x0C8	DAC Channel 3 $Offset_{CORR}$	10.8 V	16
0x0CA	DAC Channel 3 $Gain_{CORR}$	10.8 V	16
0x0CC	DAC Channel 4 $Offset_{CORR}$	10.8 V	16
0x0CE	DAC Channel 4 $Gain_{CORR}$	10.8 V	16
0x0D0	DAC Channel 1 $Offset_{CORR}$	±10.8 V	16
0x0D2	DAC Channel 1 $Gain_{CORR}$	±10.8 V	16
0x0D4	DAC Channel 2 $Offset_{CORR}$	±10.8 V	16
0x0D6	DAC Channel 2 $Gain_{CORR}$	±10.8 V	16
0x0D8	DAC Channel 3 $Offset_{CORR}$	±10.8 V	16
0x0DA	DAC Channel 3 $Gain_{CORR}$	±10.8 V	16
0x0DC	DAC Channel 4 $Offset_{CORR}$	±10.8 V	16
0x0DE	DAC Channel 4 $Gain_{CORR}$	±10.8 V	16
0x0E0-0x1EF	Reserved	-	-
0x1F0	Vendor ID (0x1498)		16
0x1F2	Device ID (0xA273)		16
0x1F4	Subsystem Vendor ID (0x1498)		16
0x1F6	Subsystem ID (0xA00A)		16

Offset	Description	Voltage Range	Size (Bit)
0x1F8	Module Serial Number The Module Serial Number is stored as EUI-64 (i.e. Sn. 1234567 = 0x0001060001234567). It can be used to support the PCIe Device Serial Number Capability	-	64

Table 4-21: Correction Value Space Address Map

5 Design Help

5.1 Example Design

TEWS offers this FPGA Example design which consists of well documented basic example. It includes an constraints file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TMPE627. It implements a PCIe endpoint with register mapping and basic I/O functions. It comes as a Xilinx Vivado Design Suite project with source code and as a ready-to-download bit stream. A user manual is included. This Example design can be used as a starting point for own projects.

5.2 FPGA MultiBoot

The Artix-7 FPGAs provide the “MultiBoot” capability. It allows the FPGA to selectively reconfigure itself with a new bitstream stored in the attached SPI configuration flash. The reconfiguration can be triggered by the FPGA application itself or during the initial FPGA configuration when an error occurs (Fallback Multiboot). The latter can be used to implement safe in-field updates: if an update fails, a “golden” bitstream is loaded that allows to handle the error or to retry the update.

The TMPE627 provides a SPI configuration flash that is large enough to hold multiple FPGA configuration bitstreams. This allows the use of the Artix-7 MultiBoot feature.

Refer to Xilinx UG470 “7 Series FPGAs Configuration User Guide” for more details.

6 Installation

To install the PCI Express Mini Card, insert it, slightly slanted, into the connector and fold it down. If the carrier board has spring latches, gently push the card down until the spring latch locks in place. Otherwise secure the card with screws.

To remove the card, remove the screws or pull the spring latch away from the card until it pops up. The card can then be removed from the connector.

The I/O connector will exceed the available PCI Express Mini Card components height. Check carefully if you application provides enough spacing for a TMPE627.

6.1 A Remark About Slot Supplies

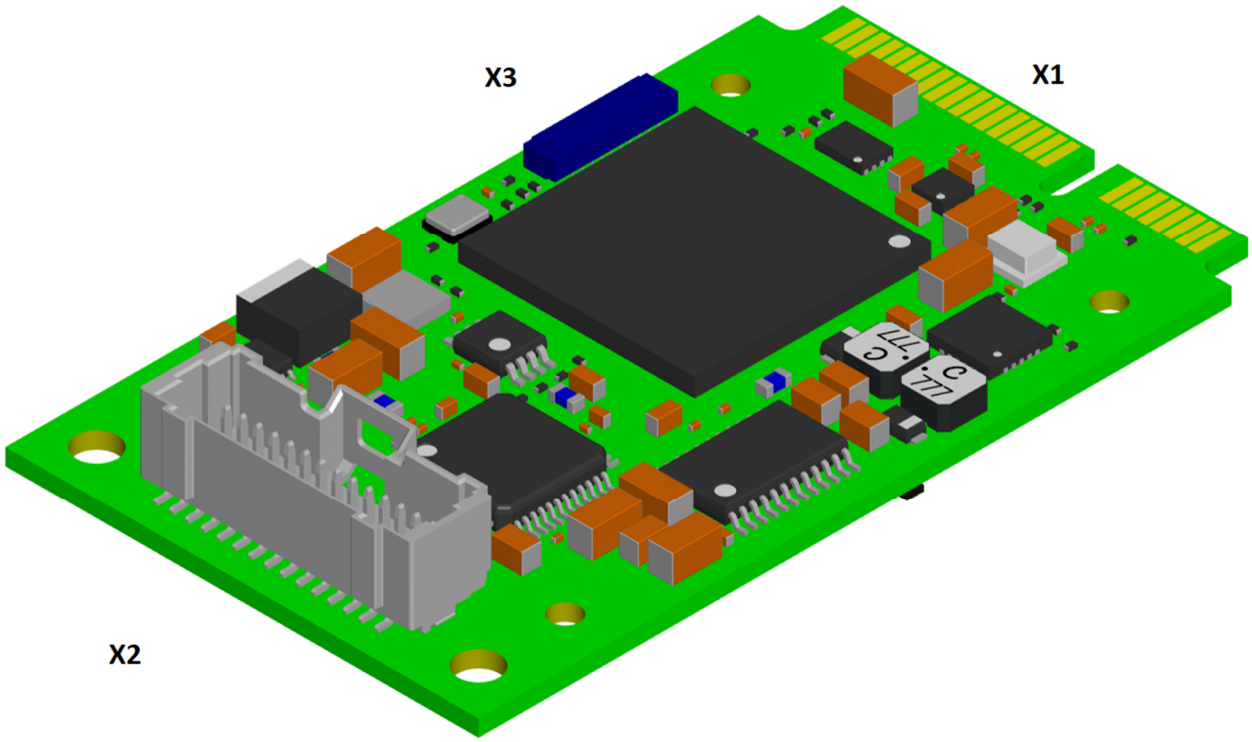
A PCI Express Mini Card slot is powered by two supplies, 1.5V and 3.3Vaux. While the 1.5V is powered on and off with the rest of the system, the 3.3Vaux supply is typically powered by the systems auxiliary power, which is available even when the system is off. Keep this in mind when installing or removing a PCI Express Mini Card and make sure that the system is turned off completely.

After initial power-up, the FPGA on the TMPE627 is not configured until all power supplies are available. But when the system is turned off, the FPGA remains configured as long as the slot is powered with the systems auxiliary power. In this case, a “power cycle” may not have the expected results.

7 I/O Connectors

This chapter provides information about user accessible on-board connectors

7.1 Overview



X1	System Connector
X2	I/O Connector
X3	JTAG Connector

Figure 7-1: I/O Connector Overview

7.2 Board Connectors

7.2.1 System Connector (X1)

Pin-Count	52
Connector Type	Card-edge
Source & Order Info	none

Signal names in grey are not used by the card.

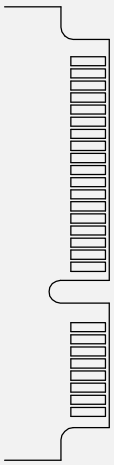
Description	Pin		Pin	Description
W_DISABLE2#	51		52	+3.3 Vaux
Reserved	49		50	GND
Reserved	47		48	+1.5 V
Reserved	45		46	LEP_WPAN#
GND	43		44	LEP_WLAN#
+3.3 Vaux	41		42	LEP_WWAN#
+3.3 Vaux	39		40	GND
GND	37		38	USB_D+
GND	35		36	USB_D-
PETp0	33		34	GND
PETn0	31		32	SMB_DATA
GND	29		30	SMB_CLK
GND	27		28	+1.5 V
PERp0	25		26	GND
PERn0	23		24	+3.3 Vaux
GND	21		22	PERST#
UIM_IC_DP	19		20	W_DISABLE1#
UIM_IC_DM	17		18	GND
Mechanical Key				Mechanical Key
GND	15		16	UIM_SPU
REF_CLK+	13		14	UIM_RESET
REF_CLK-	11		12	UIM_CLK
GND	9		10	UIM_DATA
CLKREQ#	7		8	UIM_PWR
COEX2	5		6	+1.5 V
COEX1	3		4	GND
WAKE#	1		2	+3.3 Vaux

Figure 7-2: Preliminary System Connector Pin Assignment

7.2.2 I/O Connector (X2)

Pin-Count	30
Connector Type	Molex Pico-Clasp, dual row straight header, with lock
Source & Order Info	501190-3017
Mating Part	501189-3010

The I/O connector will exceed the available PCI Express Mini Card components height. Check carefully if you application provides enough spacing for a TMPE627.

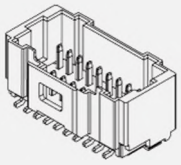
Pin Assignment						
Description		**Pin**		**Pin**	**Description**	
Single-En.	**Diff.**				**Single-En.**	**Diff.**
ADC 1	ADC 1+	1		2	Connect to GND	ADC 1-
ADC 2	ADC 2+	3		4	Connect to GND	ADC 2-
ADC 3	ADC 3+	5		6	Connect to GND	ADC 3-
ADC 4	ADC 4+	7		8	Connect to GND	ADC 4-
DAC 1	-	9		10	DAC 2	-
DAC 3	-	11		12	DAC 4	-
GND	GND	13		14	GND	GND
I/O_0	-	15		16	I/O_1	-
I/O_2	-	17		18	I/O_3	-
I/O_4	-	19		20	I/O_5	-
I/O_6	-	21		22	I/O_7	-
I/O_8	-	23		24	I/O_9	-
I/O_10	-	25		26	I/O_11	-
I/O_12	-	27		28	I/O_13	-
GND	GND	29		30	GND	GND

Figure 7-3: I/O Connector Pin Assignment

I/O_x signals correspond to the DIx/DOx/OEx FPGA pins.

7.2.3 JTAG Connector (X3)

Pin-Count	10
Connector Type	JST XRS 10pol 0,6 mm Pitch IDC Connector
Source & Order Info	SM10B-XSRS-ETB
Mating Part	10XSR-36S

The TMPE627 provides a JTAG connector to access the FPGA's JTAG port.

TEWS provides a "Programming Kit" (TA308) which includes a XSR cable and an adapter module that provides a Xilinx USB Programmer II compatible 2 mm shrouded header.

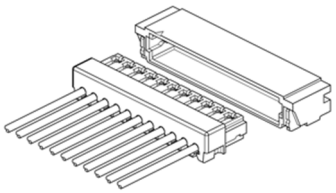
	Pin	Description
	1	GND
	2	TCK
	3	TMS
	4	TDI
	5	TDO
	6	GND
	7	GPIO0
	8	GPIO1
	9	PRESENT#
	10	V_{REF}

Figure 7-4: XRS Connector Pin Assignment

GPIO0 is connected to FPGA DONE

GPIO1 is connected to Power Good (covers FPGA V_{CORE} and 5 V)

PRESENT# is not used by the TMPE627.

V_{REF} is 3.3 V

Figure 7-5: TMPE627 connected to a Programmer via TA308

8 Appendix A

This appendix contains the signal to pin assignments for the Artix-7 FPGA.

```
## ############################################################################################## ##
## PCIe
## ############################################################################################## ##

# PCIe Lanes
set_property    LOC                                                    GTPE2_CHANNEL_X0Y0        [get_cells
{PCIE_FW_UNIT_INST/B_XIL_PCIE_EP.I_PCIE_EP/U0/inst/gt_top_i/pipe_wrapper_i/pipe_lane[0].gt_wrapper_i
/gtp_channel.gtpe2_channel_i}]
set_property PACKAGE_PIN    H2        [get_ports PER0_P]
set_property PACKAGE_PIN    H1        [get_ports PER0_N]
set_property PACKAGE_PIN    E4        [get_ports PET0_P]
set_property PACKAGE_PIN    E3        [get_ports PET0_N]

# PCIe Reference Clock
set_property PACKAGE_PIN    D6        [get_ports REFCLK_P]
set_property PACKAGE_PIN    D5        [get_ports REFCLK_N]

# PERST
set_property IOSTANDARD     LVCMOS33  [get_ports PERST_n]
set_property PACKAGE_PIN    K1        [get_ports PERST_n]


## ############################################################################################## ##
## Front I/O
## ############################################################################################## ##

set_property IOSTANDARD     LVCMOS33  [get_ports OE*]
set_property IOSTANDARD     LVCMOS33  [get_ports DI*]
set_property IOSTANDARD     LVCMOS33  [get_ports DO*]
set_property IOSTANDARD     LVCMOS33  [get_ports PULL_*]
# Setting SLEW and DRIVE for Outputs only
set_property SLEW           SLOW      [get_ports OE*]
set_property DRIVE          4         [get_ports OE*]
set_property SLEW           SLOW      [get_ports DO*]
set_property DRIVE          4         [get_ports DO*]
set_property SLEW           SLOW      [get_ports PULL_*]
set_property DRIVE          4         [get_ports PULL_*]

set_property PACKAGE_PIN    V9        [get_ports {OE[0]}]
set_property PACKAGE_PIN    K17       [get_ports {OE[1]}]
set_property PACKAGE_PIN    T12       [get_ports {OE[2]}]
set_property PACKAGE_PIN    M16       [get_ports {OE[3]}]
set_property PACKAGE_PIN    T18       [get_ports {OE[4]}]
set_property PACKAGE_PIN    N16       [get_ports {OE[5]}]
set_property PACKAGE_PIN    K15       [get_ports {OE[6]}]
set_property PACKAGE_PIN    M15       [get_ports {OE[7]}]
set_property PACKAGE_PIN    V11       [get_ports {OE[8]}]
set_property PACKAGE_PIN    N14       [get_ports {OE[9]}]
set_property PACKAGE_PIN    U16       [get_ports {OE[10]}]
set_property PACKAGE_PIN    V17       [get_ports {OE[11]}]
set_property PACKAGE_PIN    R15       [get_ports {OE[12]}]
set_property PACKAGE_PIN    V16       [get_ports {OE[13]}]

set_property PACKAGE_PIN    N18       [get_ports {DI[0]}]
set_property PACKAGE_PIN    U10       [get_ports {DI[1]}]
set_property PACKAGE_PIN    J14       [get_ports {DI[2]}]
set_property PACKAGE_PIN    N17       [get_ports {DI[3]}]
set_property PACKAGE_PIN    M17       [get_ports {DI[4]}]
set_property PACKAGE_PIN    U17       [get_ports {DI[5]}]
set_property PACKAGE_PIN    R17       [get_ports {DI[6]}]
set_property PACKAGE_PIN    P18       [get_ports {DI[7]}]
set_property PACKAGE_PIN    U12       [get_ports {DI[8]}]
set_property PACKAGE_PIN    T17       [get_ports {DI[9]}]
set_property PACKAGE_PIN    U11       [get_ports {DI[10]}]
set_property PACKAGE_PIN    U14       [get_ports {DI[11]}]
set_property PACKAGE_PIN    P15       [get_ports {DI[12]}]
set_property PACKAGE_PIN    U9        [get_ports {DI[13]}]
```

```
set_property PACKAGE_PIN    V12       [get_ports {DO[0]}]
set_property PACKAGE_PIN    L18       [get_ports {DO[1]}]
set_property PACKAGE_PIN    T13       [get_ports {DO[2]}]
set_property PACKAGE_PIN    L14       [get_ports {DO[3]}]
set_property PACKAGE_PIN    M14       [get_ports {DO[4]}]
set_property PACKAGE_PIN    R18       [get_ports {DO[5]}]
set_property PACKAGE_PIN    P16       [get_ports {DO[6]}]
set_property PACKAGE_PIN    P14       [get_ports {DO[7]}]
set_property PACKAGE_PIN    V13       [get_ports {DO[8]}]
set_property PACKAGE_PIN    T15       [get_ports {DO[9]}]
set_property PACKAGE_PIN    R13       [get_ports {DO[10]}]
set_property PACKAGE_PIN    V14       [get_ports {DO[11]}]
set_property PACKAGE_PIN    U15       [get_ports {DO[12]}]
set_property PACKAGE_PIN    T14       [get_ports {DO[13]}]

set_property PACKAGE_PIN    R2        [get_ports {PULL_SEL[0]}]
set_property PACKAGE_PIN    V8        [get_ports {PULL_SEL[1]}]


## ############################################################################################ ##
## ADC
## ############################################################################################ ##

set_property IOSTANDARD     LVCMOS33  [get_ports ADC_*]
set_property IOSTANDARD     LVCMOS33  [get_ports FF_*]
# Setting SLEW and DRIVE for Outputs only
set_property SLEW           SLOW      [get_ports ADC_CNV]
set_property SLEW           SLOW      [get_ports ADC_CS_n]
set_property SLEW           SLOW      [get_ports ADC_LVDS_CMOS_n]
set_property SLEW           SLOW      [get_ports ADC_PD]
set_property SLEW           SLOW      [get_ports ADC_SCKI_SCKI_N]
set_property SLEW           SLOW      [get_ports ADC_SDI]
set_property DRIVE          4         [get_ports ADC_CNV]
set_property DRIVE          4         [get_ports ADC_CS_n]
set_property DRIVE          4         [get_ports ADC_LVDS_CMOS_n]
set_property DRIVE          4         [get_ports ADC_PD]
set_property DRIVE          4         [get_ports ADC_SCKI_SCKI_N]
set_property DRIVE          4         [get_ports ADC_SDI]

set_property PACKAGE_PIN    C12       [get_ports ADC_CNV]
set_property PACKAGE_PIN    D18       [get_ports ADC_BUSY]
set_property PACKAGE_PIN    B17       [get_ports ADC_PD]
set_property PACKAGE_PIN    G16       [get_ports ADC_CS_n]
set_property PACKAGE_PIN    B16       [get_ports ADC_LVDS_CMOS_n]
set_property PACKAGE_PIN    G17       [get_ports ADC_SDI]
set_property PACKAGE_PIN    A17       [get_ports ADC_SDO0]
set_property PACKAGE_PIN    D13       [get_ports ADC_SDO1_SDI_P]
set_property PACKAGE_PIN    C13       [get_ports ADC_SDO2_SDI_N]
set_property PACKAGE_PIN    E13       [get_ports ADC_SDO3_SCKI_P]
set_property PACKAGE_PIN    D14       [get_ports ADC_SCKI_SCKI_N]
set_property PACKAGE_PIN    E15       [get_ports ADC_SCKO_SCKO_P]
set_property PACKAGE_PIN    D15       [get_ports ADC_SDO4_SCKO_N]
set_property PACKAGE_PIN    E16       [get_ports ADC_SDO5_SDO_P]
set_property PACKAGE_PIN    D16       [get_ports ADC_SDO6_SDO_N]
set_property PACKAGE_PIN    C18       [get_ports ADC_SDO7]
set_property PACKAGE_PIN    B11       [get_ports FF_12]
set_property PACKAGE_PIN    E17       [get_ports FF_34]


## ############################################################################################ ##
## DAC
## ############################################################################################ ##

set_property IOSTANDARD     LVCMOS33  [get_ports DAC_*]
# Setting SLEW and DRIVE for Outputs only
set_property SLEW           SLOW      [get_ports DAC_BIN2S]
set_property SLEW           SLOW      [get_ports DAC_CLR_n]
set_property SLEW           SLOW      [get_ports DAC_LDAC_n]
set_property SLEW           SLOW      [get_ports DAC_SCLK]
set_property SLEW           SLOW      [get_ports DAC_SDIN]
set_property SLEW           SLOW      [get_ports DAC_SYNC_n]
set_property DRIVE          4         [get_ports DAC_BIN2S]
```

```
set_property DRIVE          4         [get_ports DAC_CLR_n]
set_property DRIVE          4         [get_ports DAC_LDAC_n]
set_property DRIVE          4         [get_ports DAC_SCLK]
set_property DRIVE          4         [get_ports DAC_SDIN]
set_property DRIVE          4         [get_ports DAC_SYNC_n]

set_property PACKAGE_PIN    C11       [get_ports DAC_SDIN]
set_property PACKAGE_PIN    F17       [get_ports DAC_SCLK]
set_property PACKAGE_PIN    D10       [get_ports DAC_SYNC_n]
set_property PACKAGE_PIN    A15       [get_ports DAC_SDO]
set_property PACKAGE_PIN    G14       [get_ports DAC_LDAC_n]
set_property PACKAGE_PIN    F14       [get_ports DAC_CLR_n]
set_property PACKAGE_PIN    B15       [get_ports DAC_BIN2S]


## ########################################################################################### ##
## I2C Interfaces
## ########################################################################################### ##

set_property IOSTANDARD     LVCMOS33  [get_ports PROM*]
set_property IOSTANDARD     LVCMOS33  [get_ports SE95*]
# Setting SLEW and DRIVE for Outputs only
set_property SLEW           SLOW      [get_ports PROM*]
set_property SLEW           SLOW      [get_ports SE95_SCL]
set_property SLEW           SLOW      [get_ports SE95_SDA]

set_property PACKAGE_PIN    R1        [get_ports PROM_SCL]
set_property PACKAGE_PIN    T2        [get_ports PROM_SDA]
set_property PACKAGE_PIN    H16       [get_ports SE95_SCL]
set_property PACKAGE_PIN    F15       [get_ports SE95_SDA]
set_property PACKAGE_PIN    H18       [get_ports SE95_OS]


## ########################################################################################### ##
## SPI Interface
## ########################################################################################### ##

set_property IOSTANDARD     LVCMOS33  [get_ports SPI*]

# CCLK runs through STARTUPE2
#set_property PACKAGE_PIN   R16       [get_ports CCLK]

set_property PACKAGE_PIN    L15       [get_ports SPI_CS_n]
set_property PACKAGE_PIN    K16       [get_ports SPI_DI]
set_property PACKAGE_PIN    L17       [get_ports SPI_DO]
set_property PACKAGE_PIN    J15       [get_ports SPI_WP_n]
set_property PACKAGE_PIN    J16       [get_ports SPI_HOLD_n]


## ########################################################################################### ##
## Section: Miscellaneous
## ########################################################################################### ##

# XADC inputs
set_property IOSTANDARD     LVCMOS33  [get_ports VAUX*]
set_property PACKAGE_PIN    B9        [get_ports VAUXP1]
set_property PACKAGE_PIN    A9        [get_ports VAUXN1]
set_property PACKAGE_PIN    A13       [get_ports VAUXP10]
set_property PACKAGE_PIN    A14       [get_ports VAUXN10]
set_property PACKAGE_PIN    D9        [get_ports VAUXP8]
set_property PACKAGE_PIN    C9        [get_ports VAUXN8]
set_property PACKAGE_PIN    D8        [get_ports VAUXP0]
set_property PACKAGE_PIN    C8        [get_ports VAUXN0]
set_property PACKAGE_PIN    B12       [get_ports VAUXP2]
set_property PACKAGE_PIN    A12       [get_ports VAUXN2]
set_property PACKAGE_PIN    A10       [get_ports VAUXN9]
set_property PACKAGE_PIN    B10       [get_ports VAUXP9]


# 100 MHz External Configuration Master Clock
set_property IOSTANDARD     LVCMOS33  [get_ports EMC_CLK]
set_property PACKAGE_PIN    K18       [get_ports EMC_CLK]
# Allow connection from non-clockable pin to clock nets
```

```
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets EMC_CLK]


# LEDs
set_property IOSTANDARD     LVCMOS33  [get_ports LED_W*]
set_property SLEW           SLOW      [get_ports LED_W*]
set_property PACKAGE_PIN    P1        [get_ports LED_WWAN]
set_property PACKAGE_PIN    V3        [get_ports LED_WPAN]
set_property PACKAGE_PIN    V2        [get_ports LED_WLAN]


# PCIe Mini Card SMBus
set_property PROHIBIT       TRUE      [get_sites M1]
set_property PROHIBIT       TRUE      [get_sites N1]




# PCIe Reference Clock
create_clock -period 10.000 [get_ports REFCLK_P]

# 100 MHz External Configuration Master Clock
create_clock -period 10.000 [get_ports EMC_CLK]




### General Config Settings
set_property CFGBVS                             VCCO      [current_design]
set_property CONFIG_VOLTAGE                     3.3       [current_design]
set_property BITSTREAM.GENERAL.COMPRESS         FALSE     [current_design]


### Boot from external Clock
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN  div-1     [current_design]


### SPI x4 Settings
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE     YES       [current_design]
set_property CONFIG_MODE                        SPIx4     [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH      4         [current_design]
```