The Embedded I/O Company

TPCE200

4 Slot IndustryPack® Carrier for PCI Express

Version 1.0

User Manual

Issue 1.0.1

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TPCE200-10R

PCI Express x1 Carrier for four IndustryPack® modules, +12V Power Supply from PCIe Connector

TPCE200-11R

PCI Express x1 Carrier for four IndustryPack® modules, +12V Power Supply via PCIe Graphics Connector

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0.0	Initial Issue	June 2013
1.0.1	Correction of Subsystem ID in PCI Configuration Space Header	November 2013

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1 Product Description

The TPCE200 is a standard height PCI Express, Revision 2.0 compatible module that provides four slots for up to four single-size or two double-size IndustryPack (IP) modules used to build modular, flexible and cost effective I/O solutions for all kinds of applications like process control, medical systems, telecommunication and traffic control.

Four 50 pin, 0.1 inch flat ribbon cable connectors provide access to all IP I/O lines. LED status indicators for IP acknowledge, +5V and ±12V are provided.

The IP clock speed is selectable between 8MHz and 32MHz for each IP slot separately.

One memory space is provided for each IP, allowing linear addressing for 16-Bit memory on the IP.

The IP power lines are fuse protected by self-healing fuses and RF filtered. The operating temperature range is -40°C to +85°C.

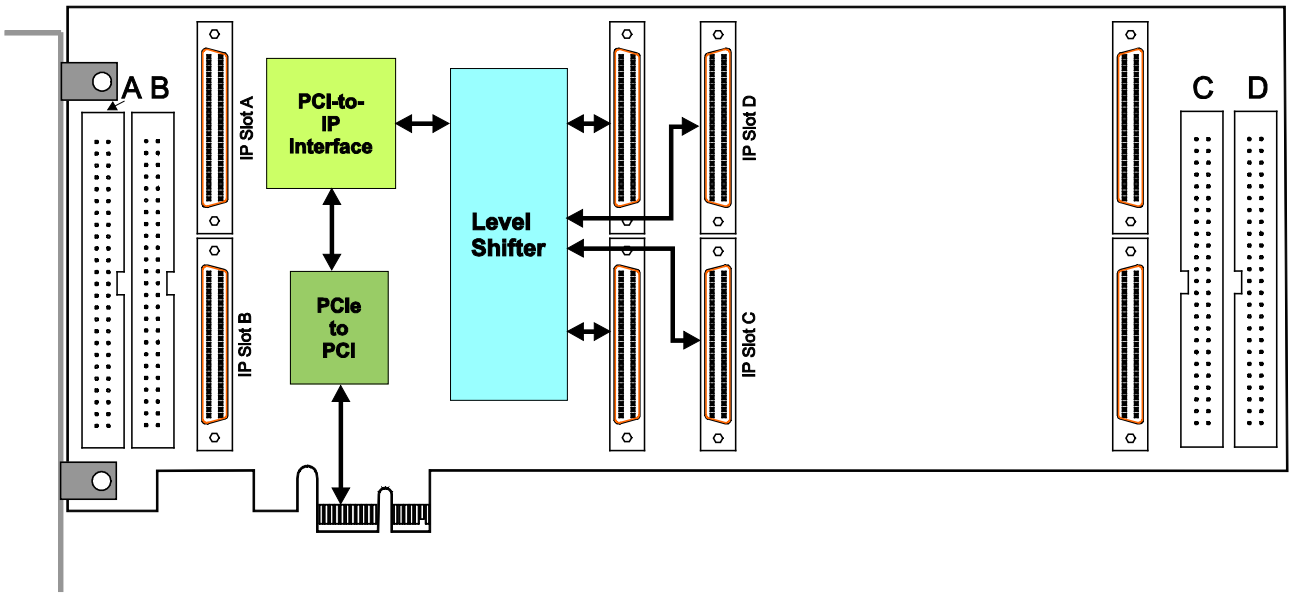


Figure 1-1 : TPCE200 Block Diagram

2 Technical Specification

PCI Express Interface		
PCI Express	PCI Express x1, Revision 2.0 Standard Height Full Length	
IP Interface		
IP Interface	According to IndustryPack specification ANSI / VITA 4-1995 8-/16-Bit Access 8/32 MHz selectable per IP slot	
IP Slots	4 single-size IP slots (A, B, C, D) IP slots A+B and IP slots C+D may be used for two double-size IP modules	
IP Interrupt Mapping	Routing of all IP interrupts to Legacy PCI INTA Local interrupt status register	
IP Power Supply	Resettable fuses and RF-filtering on all IP power lines	
IP LEDs	One IP module activity LED for each IP slot One IP module +5V power supply LED for each IP slot One IP module +12V power supply LED for all IP slots One IP module -12V power supply LED for all IP slots	
IP DMA	Not supported	
IP 32-Bit Access	Not supported	
Main Onboard Devices		
PCI Express to PCI Bridge	XIO2001 (Texas Instruments)	
PCI Target Device	XC6SLX9 (Xilinx)	
Physical Data		
Power Requirements	170mA @ +3.3V DC 160mA @ +12V DC **Additional power is required by the IP Modules!**	
Maximum Power for IP Slots	The maximum power available for the IP slots is variant dependent. Please see chapter “Power Limits for IP Modules” for detailed information.	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	TPCE200-10R: 338.000 h TPCE200-11R: 315.000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	TPCE200-10R: 173 g TPCE200-11R: 176 g	

Table 2-1 : Technical Specification

3 Handling and Operating Instructions

3.1 ESD Protection

The TPCE200 is sensitive to static electricity. Packing, unpacking and all other handling of the TPCE200 has to be done in an ESD/EOS protected Area.

3.2 Installation of IP Modules

Before mounting IP Modules on the TPCE200, be sure that the system is powered off. Also, do not mount any IP Modules when the TPCE200 is mounted in the system.

3.3 Current Limits for IP Modules

The PCIe specification limits the power for PCIe add-in cards. These limitations have implications for the use of IP modules.
Refer to the chapter "Current Limits for IP Modules" for details.

3.4 Installation of TPCE200-11R

For the TPCE200-11R variant, it is imperative to always connect a PCI Express VGA power cable to the TPCE200, even if no IP modules are mounted.

3.5 Installation of TPCE200-xxR

Be sure to lock the TPCE200 front panel and the system case with a screw.

4 Installation

4.1 Installation of IP Modules

Installing IP Modules on the TPCE200 is done by simply snapping them into the IP slot. The connectors are keyed, so the modules can only be installed correctly. After an IP has been installed, it can be fastened to the carrier board by screws. This is usually only necessary in high vibration or shock environments. Screws and spacers are required to fix a single IP on the TPCE200. They can be ordered from TEWS TECHNOLOGIES separately (Part number: TIPxxx-HK).

Before installing IP Modules, be sure that the power supply for the TPCE200 is turned off! Also, do not mount any IP Modules when the TPCE200 is mounted in the system.

The component is sensitive to Electrostatic Discharge (ESD). Use an anti-static mat connected to a wristband when handling or installing the components.

4.1.1 Current Limits for IP Modules

The following current limits have to be taken into account when choosing the appropriate TPCE200 for the power requirements of the IP modules.

TPCE200	Power Supply	Current Limits
TPCE200-10R	+5V	Max. 2A for all slots combined
	+12V	Max. 200mA for all slots combined
	-12V	Max. 100mA for all slots combined
TPCE200-11R	+5V	Max. 2A per IP slot
	+12V	Max. 500mA total, max. 200mA for a single IP slot
	-12V	Max. 300mA total, max. 200mA for a single IP slot

Table 4-1 : Current Limits for the IP Modules

4.1.2 IP Power Supply Filters

The TPCE200 provides RF filtering and decoupling capacitors on all IP power lines.

There are 3 power supply filters for each IP slot, one for the +12V supply pin, one for the -12V supply pin and one for the two +5V supply pins.

4.1.3 IP Power Supply Fuses

There is a self-healing fuse for the +5V supply at each IP slot.

IP 5V Fuse Operating Current Rating I_hold (Ampere) @ TA								
-40°C	-20°C	0°C	23°C	40°C	50°C	60°C	70°C	85°C
3.08	2.71	2.35	2.00	1.80	1.60	1.50	1.40	1.25

Table 4-2 : IP +5V Fuse Operating Current Rating

There are self-healing fuses for the +12V supply and for the -12V supply at each IP slot.

IP +12V/-12V Fuse Operating Current Rating I_hold (Ampere) @ TA								
-40°C	**-20°C**	**0°C**	**23°C**	**40°C**	**50°C**	**60°C**	**70°C**	**85°C**
0.30	0.27	0.24	0.20	0.18	0.16	0.14	0.12	0.11

Table 4-3 : IP +12V/-12V Fuse Operating Current Rating

4.1.4 IP I/O Interface

All pins of the IP slot I/O connectors are routed to 50-pin flat cable connectors for I/O access; with a maximum current rating of 0.5A per pin.

4.2 TPCE200 Module Installation

4.2.1 General

The TPCE200 is a full length PCI Express Card with an x1 Connector. It is necessary to fix the front panel of the TPCE200 to the system case with a screw.

Also, be sure not to mount any IP Modules or I/O cables when the TPCE200 is mounted in the mainboard slot. Take it out of the slot prior to mounting any modules or cables.

4.2.2 TPCE200-11R only

For the TPCE200-11R variant, it is imperative to always connect a PCI Express VGA power cable to the TPCE200, even if no IP modules are mounted.

5 Indicators

5.1 LED Indicators

The TPCE275 provides a couple of board-status LEDs as shown below.

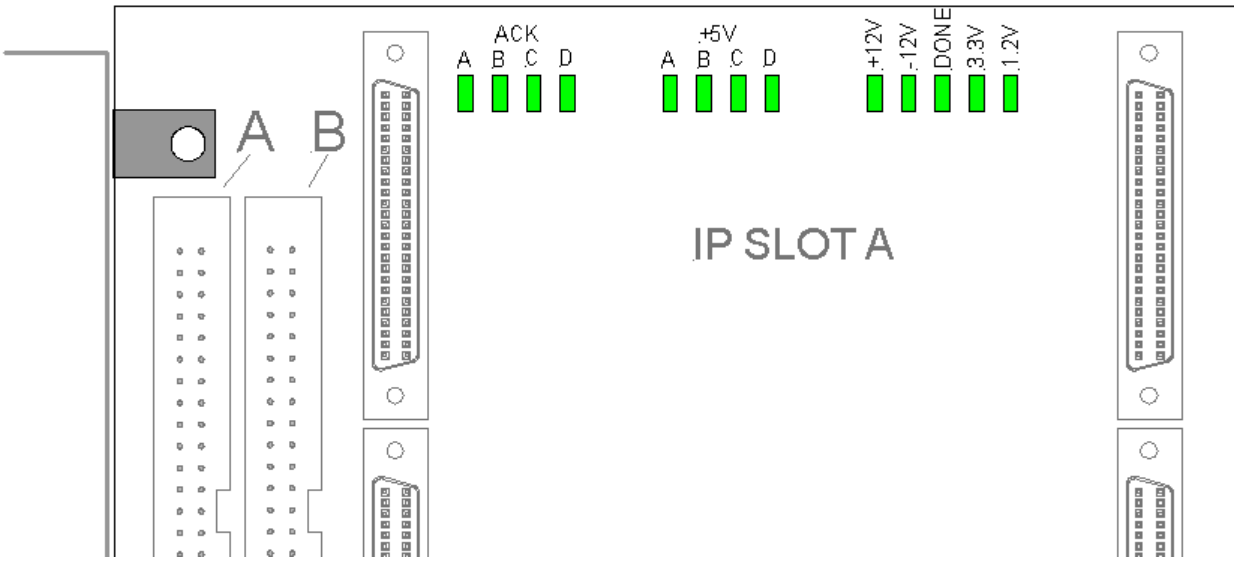


Figure 5-1 : Onboard LED Placement

LED	Color	State	Description
ACK x (A, B, C, D)	Green	On	Access Acknowledge or IP Reset active
		Off	No IP Access
+5V x (A, B, C, D)	Green	On	+5V IP Power Supply OK
		Off	+5V IP Power Supply FAILURE
+12V	Green	On	+12V IP Power Supply OK
		Off	+12V IP Power Supply FAILURE
-12V	Green	On	-12V IP Power Supply OK
		Off	-12V IP Power Supply FAILURE
DONE	Green	On	FPGA configured
		Off	FPGA NOT configured
3.3V	Green	On	3.3V Power Supply OK
		Off	3.3V Power Supply FAILURE
1.2V	Green	On	1.2V Power Supply OK
		Off	1.2V Power Supply FAILURE

Table 5-1 : Onboard LED Description

6 Address Map

6.1 PCI Configuration Space

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				Initial Values (Hex Values)
	31 24	23 16	15 8	7 0	
0x00	Device ID (TPCE200)		Vendor ID (TEWS Technologies)		70C8 1498
0x04	Status		Command		0200 0046
0x08	Class Code			Revision ID	068000 01
0x0C	BIST	Header Type	Latency Timer	Cacheline Size	00 00 00 00
0x10	**Base Address Register 0 (BAR0)** (IP Interface Control/Status Register)				FFFF FF00(1) (256 Byte)
0x14	**Base Address Register 1 (BAR1)** (IP Interface ID, I/O, INT Space)				FFFF FC00(1) (1 Kbyte)
0x18	**Base Address Register 2 (BAR2)** (IP Interface MEM Space)				FE00 0000(1) (32 Mbyte)
0x1C	Base Address Register 3 (BAR3)				00000000
0x20	Base Address Register 4 (BAR4)				00000000
0x24	Base Address Register 5 (BAR5)				00000000
0x28	PCI CardBus Information Structure Pointer				00000000
0x2C	Subsystem ID 0x700A = TPCE200-10R 0x700B = TPCE200-11R		Subsystem Vendor ID 0x1498 (TEWS Technologies)		**s.l.** 1498
0x30	Expansion ROM Base Address				00000000
0x34	Reserved			Cap. Ptr.	000000 00
0x38	Reserved				00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	00 00 01 00
0x40-0xFF	Reserved				00000000

Table 6-1 : PCI Configuration Space Header

Notes:

(1) Readback value after writing all 1's

6.2 Base Address Register Configuration

Base Address Register (BAR)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	MEM	256	16	Little	IP Interface Control/Status Registers
1	MEM	1K	16	Little	IP Slots A-D ID, I/O, INT Space (8-/16-Bit)
2	MEM	32M	16	Little	IP Slots A-D MEM Space (8-/16-Bit)

Table 6-2 : Base Address Register Configuration

Note: The TPCE200 will convert 32-Bit transfer-size accesses to the actual port width. E.g. an aligned 32-Bit write to a 16-Bit port is automatically splitted into two 16-Bit writes.

6.2.1 BAR 0 – IP Interface Control/Status Address Map

Offset (Base = PCI Base Address 0)	Size (Bit)	Register
0x00	16	FPGA Revision Register
0x02	16	IP A Control Register
0x04	16	IP B Control Register
0x06	16	IP C Control Register
0x08	16	IP D Control Register
0x0A	16	IP Reset Register
0x0C	16	IP Status Register
0x0E	16	Reserved
0x10 - 0xFF	1920	Reserved

Table 6-3 : IP Interface Control/Status Register Map

6.2.2 BAR 1 – IP Slots A-D ID, I/O, INT Space Address Map

Offset (Base = PCI Base Address 1)		Size (Byte)	IP Slot	IP Space
Start	End			
0x0000_0000	0x0000_007F	128	A	I/O
0x0000_0080	0x0000_00BF	64	A	ID
0x0000_00C0	0x0000_00FF	64	A	INT
0x0000_0100	0x0000_017F	128	B	I/O
0x0000_0180	0x0000_01BF	64	B	ID
0x0000_01C0	0x0000_01FF	64	B	INT
0x0000_0200	0x0000_027F	128	C	I/O
0x0000_0280	0x0000_02BF	64	C	ID
0x0000_02C0	0x0000_02FF	64	C	INT
0x0000_0300	0x0000_037F	128	D	I/O
0x0000_0380	0x0000_03BF	64	D	ID
0x0000_03C0	0x0000_03FF	64	D	INT

Table 6-4 : BAR 1 – IP Slots A-D ID, I/O, INT Space Address Map

The TPCE200 supports read and write cycles to the IP ID, I/O, INT and MEM spaces. A PCI access to the TPCE200 will always be terminated in every case. If the IP module supports access to the desired space, data will be written to/read from the IP. If the IP module does not support the access, it will not generate an ACK signal. In this case, the local IP interface control logic will terminate the access after a timeout of 8µs and set the "Timeout Bit" in the IP Status Register.

A read access to the IP INT space initiates an IP interrupt acknowledge cycle. A read access with address A1=0 (i.e. 0x0000_0xC0) initiates an interrupt acknowledge cycle for IP INT0#, a read access with address A1=1 (i.e. 0x0000_0xC2) initiates an interrupt acknowledge cycle for IP INT1#. The read access returns the interrupt vector. This feature is helpful for IP modules that require an interrupt acknowledge cycle to remove their pending interrupt request.

6.2.3 BAR 2 – IP Slots A-D MEM Space Address Map

Offset (Base = PCI Base Address 2)		Size (Byte)	IP Slot	IP Space
Start	End			
0x0000_0000	0x007F_FFFF	8 M	A	MEM (16-Bit)
0x0080_0000	0x00FF_FFFF	8 M	B	MEM (16-Bit)
0x0100_0000	0x017F_FFFF	8 M	C	MEM (16-Bit)
0x0180_0000	0x01FF_FFFF	8 M	D	MEM (16-Bit)

Table 6-5 : IP MEM Space Address Map

The TPCE200 supports read and write cycles to the IP ID, I/O, INT and MEM spaces. A PCI access to the TPCE200 will always be terminated in every case. If the IP module supports access to the desired space, data will be written to/read from the IP. If the IP module does not support the access, it will not generate an ACK signal. In this case, the local IP interface control logic will terminate the access after a timeout of 8µs and set the "Timeout Bit" in the IP Status Register

7 Functional Description

7.1 IP Interface Control/Status Register Description

7.1.1 Revision ID Register (Offset 0x00)

The Revision ID Register shows the revision of the onboard IP FPGA logic.

Bit	Name	Description
15 (MSB)	-	Read: Undefined Write: No Effect
14		
13		
12		
11		
10		
9		
8		
7	REV_ID	Read: FPGA Logic Revision ID Write: No Effect
6		
5		
4		
3		
2		
1		
0 (LSB)		

Table 7-1 : IP Interface Revision ID Register

7.1.2 IP Control Registers (Offsets 0x02, 0x04, 0x06, 0x08)

The IP Control Registers are used to control IP interrupts, recovery time and clock rate on the IP interface.

There is one IP Control Register for each IP Slot (A-D).

Bit	Name	Description
15 (MSB)	-	Read: Undefined Write: No Effect. Should be written with 0's
14		
13		
12		
11		
10		
9		
8	SEL_MODE	0 : Single IP Select Cycle 1 : Extended IP Select Cycle (i.e. Hold States) IP x select signal is held active until the first IP Acknowledge Cycle is detected. May be required by some IP modules.
7	INT1_EN	0 : IP x Interrupt 1 Disabled 1 : IP x Interrupt 1 Enabled
6	INT0_EN	0 : IP x Interrupt 0 Disabled 1 : IP x Interrupt 0 Enabled
5	INT1_SENSE	0 : IP x Interrupt 1 Level Sensitive 1 : IP x Interrupt 1 Edge Sensitive
4	INT0_SENSE	0 : IP x Interrupt 0 Level Sensitive 1 : IP x Interrupt 0 Edge Sensitive
3	ERR_INT_EN	0 : IP x Error Interrupt Disabled 1 : IP x Error Interrupt Enabled
2	TIME_INT_EN	0 : IP x Timeout Interrupt Disabled 1 : IP x Timeout Interrupt Enabled
1	RECOVER	0 : IP x Recovery Time Disabled 1 : IP x Recovery Time Enabled
0 (LSB)	CLKRATE	0 : IP x Clock Rate 8 MHz 1 : IP x Clock Rate 32 MHz

Table 7-2 : IP Interface Control Registers

After reset, all bits in the IP Control Registers are cleared.

If the IP recovery time feature is enabled for an IP slot, the next IP cycle for this slot is delayed by the internal control logic until the IP recovery time of approx. 1µs is expired. The recovery timer starts at the end of the cycle before.

7.1.3 IP Reset Register (Offset 0x0A)

The IP Reset Register is used to assert the IP RESET# signal for all IP slots at the same time and to detect when the IP reset phase is done.

Bit	Name	Description
15 (MSB)	-	Read: Undefined Write: No Effect. Should be written with 0's
14		
13		
12		
11		
10		
9		
8		
7		
6		
5		
4		
3		
2		
1		
0 (LSB)	IP_RESET	Read: 0 : IP RESET# Signal is De-asserted 1 : IP RESET# Signal is Asserted Write: 0 : No Effect 1 : Assert IP RESET# Signal for all IP slots (signal will be negated automatically after 200ms)

Table 7-3 : IP Interface Reset Register

During a PCIe reset, the IP RESET# signal will also be asserted. The IP RESET# duration will always be at least 200ms, no matter the PCIe reset time.

7.1.4 IP Status Register (Offset 0x0C)

The IP Status Register is used to read IP timeout, error and interrupt status for the IP slots.

Bit	Name	Description	
		Read Access	Write Access
15 (MSB)	TIME_D	0 : No Timeout on IP_D 1 : IP_D Timeout has occurred	0 : No Effect 1 : Clear IP_D Timeout Status
14	TIME_C	0 : No Timeout on IP_C 1 : IP_C Timeout has occurred	0 : No Effect 1 : Clear IP_C Timeout Status
13	TIME_B	0 : No Timeout on IP_B 1 : IP_B Timeout has occurred	0 : No Effect 1 : Clear IP_B Timeout Status
12	TIME_A	0 : No Timeout on IP_A 1 : IP_A Timeout has occurred	0 : No Effect 1 : Clear IP_A Timeout Status
11	ERR_D	0 : No Error on IP_D 1 : IP_D ERROR# Signal Asserted	No Effect
10	ERR_C	0 : No Error on IP_C 1 : IP_C ERROR# Signal Asserted	No Effect
9	ERR_B	0 : No Error on IP_B 1 : IP_B ERROR# Signal Asserted	No Effect
8	ERR_A	0 : No Error on IP_A 1 : IP_A ERROR# Signal Asserted	No Effect
7	INT1_D	0 : No Interrupt 1 Request on IP_D 1 : Active IP_D Interrupt 1 Request	0 : No Effect 1 : Clear Edge Sensitive IP_D Interrupt 1 Status
6	INT0_D	0 : No Interrupt 0 Request on IP_D 1 : Active IP_D Interrupt 0 Request	0 : No Effect 1 : Clear Edge Sensitive IP_D Interrupt 0 Status
5	INT1_C	0 : No Interrupt 1 Request on IP_C 1 : Active IP_C Interrupt 1 Request	0 : No Effect 1 : Clear Edge Sensitive IP_C Interrupt 1 Status
4	INT0_C	0 : No Interrupt 0 Request on IP_C 1 : Active IP_C Interrupt 0 Request	0 : No Effect 1 : Clear Edge Sensitive IP_C Interrupt 0 Status
3	INT1_B	0 : No Interrupt 1 Request on IP_B 1 : Active IP_B Interrupt 1 Request	0 : No Effect 1 : Clear Edge Sensitive IP_B Interrupt 1 Status
2	INT0_B	0 : No Interrupt 0 Request on IP_B 1 : Active IP_B Interrupt 0 Request	0 : No Effect 1 : Clear Edge Sensitive IP_B Interrupt 0 Status
1	INT1_A	0 : No Interrupt 1 Request on IP_A 1 : Active IP_A Interrupt 1 Request	0 : No Effect 1 : Clear Edge Sensitive IP_A Interrupt 1 Status
0 (LSB)	INT0_A	0 : No Interrupt 0 Request on IP_A 1 : Active IP_A Interrupt 0 Request	0 : No Effect 1 : Clear Edge Sensitive IP_A Interrupt 0 Status

Table 7-4 : IP Interface Status Register

The IP timeout time is app. 8µs.

An IP timeout occurs if the IP module fails to generate the IP ACK# signal within the IP timeout time. An IP timeout is only reported in the Status Register. For timed out read accesses, the returned data is all 'F'.

7.2 Interrupts

7.2.1 Interrupt Sources

The TPCE200 provides the following main interrupt sources:

- IP_A_INTREQ#[1:0]
- IP_B_INTREQ#[1:0]
- IP_C_INTREQ#[1:0]
- IP_D_INTREQ#[1:0]

All the IP interrupts are low active and may be set to level or edge sensitive by the IP Control Registers.

7.2.2 Interrupt Mapping

The IP Interface address map provides an interrupt status register as well as register bits for interrupt enable control.

If any of the interrupt bits is set in the IP Status Register and the corresponding interrupt enable bit is set in the IP Control Register, the Spartan-6 INTA# line on the local PCI bus is asserted which is translated into Assert_INTx or Deassert_INTx messages on the PCI Express interface.

7.2.3 Interrupt Handling

Upon detecting interrupts, software should check the IP Status Register to determine which IP interrupts are active.

For edge sensitive IP interrupts, the interrupt is cleared by writing a ‘1’ to the corresponding bit in the IP Status register. For level sensitive IP interrupts, interrupt clearing is scope of the IP module used.

8 Pin Assignments

8.1 J1x – IP Interface Connector (x = A, B, C, D)

Pin-Count	50
Connector Type	AMPLIMITE 0.50 Series
Source & Order Info	5173280-3 (Tyco)

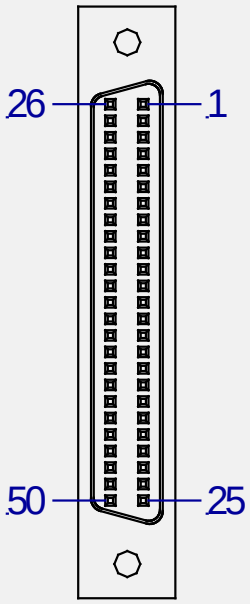
Signal	Pin	Connector view	Pin	Signal
GND	**26**		**1**	GND
IP_x_+5V	**27**		**2**	IP_x_CLK
IP_R/W#	**28**		**3**	IP_RESET#
IP_x_IDSEL#	**29**		**4**	IP_xy_D00 [1]
IP_x_DMAREQ0# [2]	**30**		**5**	IP_xy_D01 [1]
IP_x_MEMSEL#	**31**		**6**	IP_xy_D02 [1]
IP_x_DMAREQ1# [2]	**32**		**7**	IP_xy_D03 [1]
IP_x_INTSEL#	**33**		**8**	IP_xy_D04 [1]
IP_x_DMAACK# [2]	**34**		**9**	IP_xy_D05 [1]
IP_x_IOSEL#	**35**		**10**	IP_xy_D06 [1]
IP_x_RESERVED0	**36**		**11**	IP_xy_D07 [1]
IP_A1	**37**		**12**	IP_xy_D08 [1]
IP_x_DMAEND# [2]	**38**		**13**	IP_xy_D09 [1]
IP_A2	**39**		**14**	IP_xy_D10 [1]
IP_x_ERROR#	**40**		**15**	IP_xy_D11 [1]
IP_A3	**41**		**16**	IP_xy_D12 [1]
IP_x_INTREQ0#	**42**		**17**	IP_xy_D13 [1]
IP_A4	**43**		**18**	IP_xy_D14 [1]
IP_x_INTREQ1#	**44**		**19**	IP_xy_D15 [1]
IP_A5	**45**		**20**	IP_x_BS0#
IP_x_STROBE#	**46**		**21**	IP_x_BS1#
IP_A6	**47**		**22**	IP_x_-12V
IP_x_ACK#	**48**		**23**	IP_x_+12V
IP_x_RESERVED1	**49**		**24**	IP_x_+5V
GND	**50**		**25**	GND

Table 8-1 : IP J1x Pin Assignment

Notes:

1) "xy" means either IP Slots A+C, or IP Slots B+D.

2) DMA is not supported by the TPCE200; these signals are pulled high to 5V.

8.2 J2x – IP I/O Connector (x = A, B, C, D)

Pin-Count	50
Connector Type	AMPLIMITE 0.50 Series
Source & Order Info	5173280-3 (Tyco)

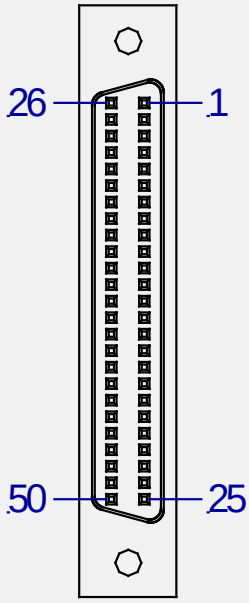
Signal	Pin	Connector view	Pin	Signal
I/O 26	**26**		**1**	I/O 1
I/O 27	**27**		**2**	I/O 2
I/O 28	**28**		**3**	I/O 3
I/O 29	**29**		**4**	I/O 4
I/O 30	**30**		**5**	I/O 5
I/O 31	**31**		**6**	I/O 6
I/O 32	**32**		**7**	I/O 7
I/O 33	**33**		**8**	I/O 8
I/O 34	**34**		**9**	I/O 9
I/O 35	**35**		**10**	I/O 10
I/O 36	**36**		**11**	I/O 11
I/O 37	**37**		**12**	I/O 12
I/O 38	**38**		**13**	I/O 13
I/O 39	**39**		**14**	I/O 14
I/O 40	**40**		**15**	I/O 15
I/O 41	**41**		**16**	I/O 16
I/O 42	**42**		**17**	I/O 17
I/O 43	**43**		**18**	I/O 18
I/O 44	**44**		**19**	I/O 19
I/O 45	**45**		**20**	I/O 20
I/O 46	**46**		**21**	I/O 21
I/O 47	**47**		**22**	I/O 22
I/O 48	**48**		**23**	I/O 23
I/O 49	**49**		**24**	I/O 24
I/O 50	**50**		**25**	I/O 25

Table 8-2 : IP J2 I/O Connectors (onboard)

8.3 J1 – IP Strobe Signal Header

The Strobe Header may be used to connect the Strobe signals of mounted IP modules.

Pin-Count	4
Connector Type	Std. 2-row 4 Pin Header
Source & Order Info	-

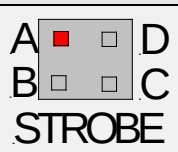
Signal	Pin	Connector view	Pin	Signal
IP_A_STROBE#	**1**		**2**	IP_D_STROBE#
IP_B_STROBE#	**3**		**4**	IP_C_STROBE#

Table 8-3 : J1 IP Strobe Signal Header

8.4 X1, X2, X3, X4 – I/O Connectors (50-Pin Flat Cable)

Pin-Count	50
Connector Type	Flat Cable Connector
Source & Order Info	Tyco 5104340

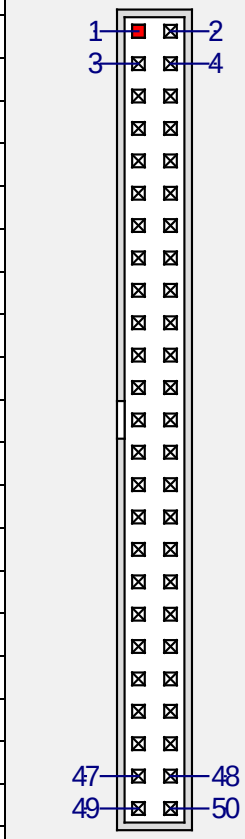
Pin Assignment				
Description	**Pin**	**Connector View**	**Pin**	**Description**
I/O 1	**1**		**2**	I/O 2
I/O 3	**3**		**4**	I/O 4
I/O 5	**5**		**6**	I/O 6
I/O 7	**7**		**8**	I/O 8
I/O 9	**9**		**10**	I/O 10
I/O 11	**11**		**12**	I/O 12
I/O 13	**13**		**14**	I/O 14
I/O 15	**15**		**16**	I/O 16
I/O 17	**17**		**18**	I/O 18
I/O 19	**19**		**20**	I/O 20
I/O 21	**21**		**22**	I/O 22
I/O 23	**23**		**24**	I/O 24
I/O 25	**25**		**26**	I/O 26
I/O 27	**27**		**28**	I/O 28
I/O 29	**29**		**30**	I/O 30
I/O 31	**31**		**32**	I/O 32
I/O 33	**33**		**34**	I/O 34
I/O 35	**35**		**36**	I/O 36
I/O 37	**37**		**38**	I/O 38
I/O 39	**39**		**40**	I/O 40
I/O 41	**41**		**42**	I/O 42
I/O 43	**43**		**44**	I/O 44
I/O 45	**45**		**46**	I/O 46
I/O 47	**47**		**48**	I/O 48
I/O 49	**49**		**50**	I/O 50

Table 8-4 : X1, X2, X3, X4 - I/O Connector Pin Assignment