The Embedded I/O Company

TEWS TECHNOLOGIES

TPCE646

Reconfigurable MPSoC with 32 x 16 bit Analog Output, 8 x 16 bit Analog Input and 25Gbps MGT Rear I/O

Version 1.0

User Manual

Issue 1.0.1

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TPCE646-10R

8 x Analog In, 32 x Analog Out, Front I/O and 64 direct rear FPGA I/O Lines,

XCZU11EG-1FFVC1760I Zynq™ UltraScale+™ MPSoC,

PL 4 GB DDR4, PS 4GB DDR4

TPCE646-11R

8 x Analog In, 32 x Analog Out, Front I/O and 64 direct rear FPGA I/O Lines,

XCZU17EG-1FFVC1760I Zynq™ UltraScale+™ MPSoC,

PL 4 GB DDR4, PS 4GB DDR4

TPCE646-12R

8 x Analog In, 32 x Analog Out, Front I/O and 64 direct rear FPGA I/O Lines,

XCZU19EG-1FFVC1760I Zynq™ UltraScale+™ MPSoC,

PL 4 GB DDR4, PS 4GB DDR4

Issue	Description	Date
1.0.0	Issue	December 2025
1.0.1	Extension description: BMC Register and minor corrections	May 2026

Table of Contents

List of Figures

List of Tables

1 Product Description

The TPCE646 is a X8 PCIe compatible module providing a user configurable AMD Zynq™ UltraScale+™ MPSoC with 32 DAC output channels and 8 ADC input channels.

The TPCE646 DAC output channels are based on the Dual 16 bit AD5547 DAC. Each DAC output is designed as a single-ended bipolar ±10 V analog output.

The TPCE646 ADC input channels are based on the Dual 16 bit 5Msps Differential-Input LTC2323-16 ADC. The TPCE646 provides 8 ADC channels. Each of the 8 channels has a resolution of 16 bit and can work at up to 5Msps. The analog input circuit is designed to allow input voltages up to ±10 V on each input-pin (results in ±20Vpp differential voltage range).

Additionally, the TPCE646 provides four differential LVDS I/O lanes on the front I/O interface.

For customer specific I/O extension or inter-board communication, the TPCE646 provides 64 MPSoC I/Os on a rear I/O connector (directly connected) and 8 PL Multi-Gigabit-Transceiver on Samtec Firefly connectors (two quad interfaces). Digital rear I/O lines can be configured as 64 single ended LVCMOS18 or as 32 differential LVDS interfaces

The PL memory interface of the Zynq™ UltraScale+™ MPSoC is connected to a 4GB, 64 bit wide DDR4 SDRAM and the PS memory interface is connected to a 4GB, 64 bit wide DDR4 SDRAM.

For communication of the Zynq™ UltraScale+™ MPSoC PS, a rear I/O Ethernet port, a USB to UART channel based on an FTDI chip and a PCIe X4 interface multiplexed with the X8 PCIe interface are available.

The Zynq™ UltraScale+™ MPSoC is configured by two dual QSPI flash devices. Depending on the device size it might be required to use the AMD Tandem Configuration Feature for PCIe conforming configuration. The QSPI flash device is in-system programmable. A microSD card slot is available as an alternative configuration source. An in-circuit PL and PS debugging option is available via a JTAG header.

User applications for the TPCE646 with Zynq™ UltraScale+™ MPSoC can be developed using the design software Vivado™ and Vitis™. Licenses for the development tools are required.

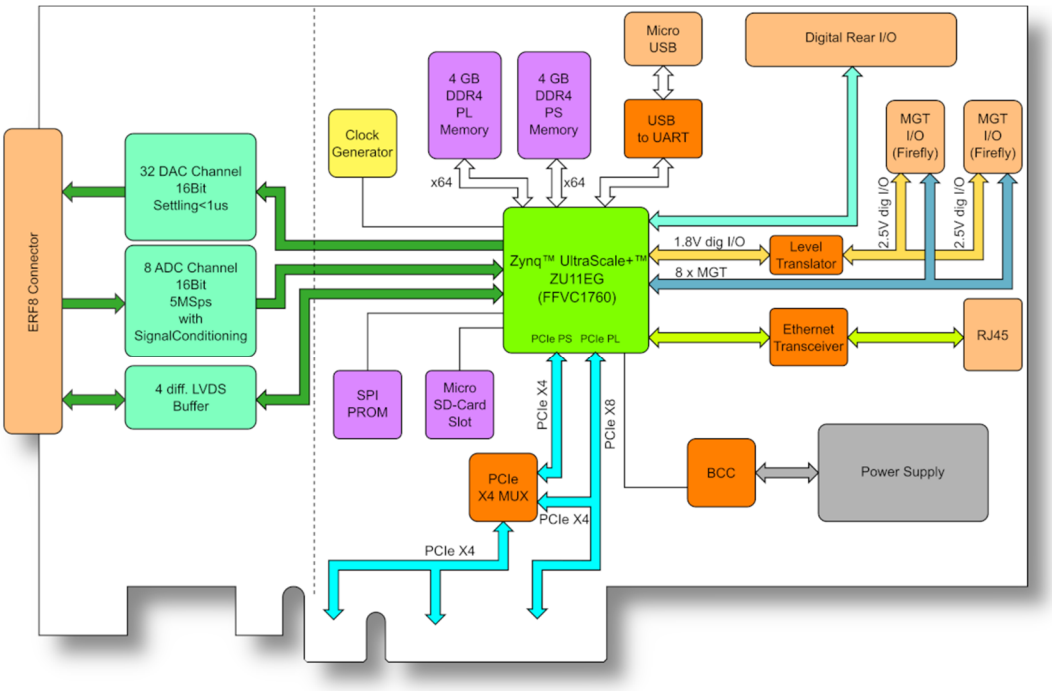


Figure 1 1: Block Diagram TPCE646-10R

2 Technical Specification

PCIe Interface		
Mechanical Interface	Peripheral Component Interconnect Express (PCIe) PCI Express CEM R3.0 Standard Height, shortened Half Length PCI Express Add-in Card (98.4mm x 153.50mm)	
Electrical Interface	PCI Express x8 Gen 3 comply with the PCI Express Base Specification, rev3.1.	
On-Board Devices		
Zynq™ UltraScale+™ MPSoC	TPCE646-10R: XCZU11EG-1FFVC1760I TPCE646-11R: XCZU17EG-1FFVC1760I TPCE646-12R: XCZU19EG-1FFVC1760I	
SPI-Flash	2 x MT25QU512ABB8E12 (Micron)	
DDR4 RAM	8 x MT40A512M16TB-062E (Micron) 8Gb x 16 bit	
Board Management Controller	LCMXO3LF-9400E (Lattice)	
ADC	LTC2323IUFD-16 (Analog Devices)	
DAC	AD5547BRUZ (Analog Devices)	
Ethernet Controller	DP83867IS (Texas)	
UART	FT2232H-56Q (FTDI)	
I/O Interface		
A/D Channels	8 Differential 16 bit A/D Channels Input Voltage Ranges: Differential: ±20.68 V Single-Ended: ±10.34 V All analog inputs are connected via an impedance converter and a second operation amplifier for level adjustment and filtering to the differential ADC inputs. The -3 dB limit of this input stage is at approx. 8MHz	
D/A Channels	32 Single-Ended 16 bit D/A Channels Output Configuration per BMC Device via SPI Interface from MPSoC (Zynq™ UltraScale+™). Single-Ended Output Voltage Ranges: ±10 V, ±5.0 V, ±2.5 V, Output Range configurable per D/A channel. Simultaneous Conversion for all D/A Channels.	
	Maximum single-ended Output Voltage – Vout Maximum Output Drive Current for each Output Maximum Capacitive Load for each Output Typical Settling Time for a 10 mA / 1000 pF Load	±10 V 10 mA 1000 pF < 1 µs
Digital Front I/O Channels	4 digital M-LVDS compatible I/O Lines	

<table>
<tr><td>Digital Rear I/O Channels</td><td>64 direct MPSoC I/O lines to Rear I/O connector
Can be used as single-ended or differential I/O
MPSoC I/O Standard: LVCMOS18 and LVDS
2 x 4 GTY (Gigabit Transceiver Ultra High-Speed) lines
Each line consists of one differential RX and TX pair.
Transmission speeds of up to 25Gbps are possible.</td></tr>
<tr><td colspan="2">I/O Connector</td></tr>
<tr><td>Front I/O</td><td>Front I/O Samtec - ERF8_050_01_L_D_RA_L_TR</td></tr>
<tr><td>Digital Rear I/O</td><td>80 pin High-Speed Ground Plane Header (QSE-040-01-L-D-A) (Samtec)</td></tr>
<tr><td>GTY Rear I/O</td><td>2 x 38 pin Firefly Micro Flyover Connector (UEC5-019-1-H-D-RA-2-A) (Samtec)</td></tr>
<tr><td colspan="2">Physical Data</td></tr>
<tr><td>Power Requirements</td><td>Depends on User MPSoC design
With TPCE646 Board Reference Design / without external load<table><tr><td></td><td>typical @ +12 V Auxiliary Power</td></tr><tr><td>TPCE646-10R</td><td>1.5 A (18 W)</td></tr></table></td></tr>
<tr><td>Temperature Range</td><td>Operating
Storage</td><td>-40°C to +60°C
-40°C to +85°C</td></tr>
<tr><td>MTBF</td><td>TPCE646-10R: 104.000 h
MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C.
The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.</td></tr>
<tr><td>Humidity</td><td>5 – 95 % non-condensing</td></tr>
<tr><td>Weight</td><td>TPCE646-xxR: 300 g</td></tr>
</table>

Table 2-1 : Technical Specification

3 Handling and Operation Instruction

3.1 ESD Protection

The TPCE646 is sensitive to static electricity. Packing, unpacking and all other handling of the TPCE646 has to be done in an ESD/EOS protected Area.

3.2 Thermal Considerations

Forced air cooling is required during operation. Without forced air cooling, damage to the device can occur.

Please also note chapter "Thermal Management".

3.3 Power Supply

The TPCE646 always requires the PCI Express 2 x 4 auxiliary power supply for operation.
This is the only external supply used on the TPCE646.

4 BMC (Board Management Controller)

4.1 Hardware Power Up Configuration

An important part of the hardware configuration of the TCPE646 is made via the DIP switch preselection.

Important configurations

- Main configuration source of User MPSoC
- PCIe Routing
- I2C Bus Routing

DIP-Switch S1

Switch	Position		Configuration
1	**OFF**		All X8 PCIe Lanes are mapped to User MPSoC PL MGT Bank 225 / 226
	ON		The first 4 PCIe Lanes are mapped to User MPSoC PS MGT Bank 505
3:2	**OFF**	**OFF**	PS JTAG Configuration
	OFF	ON	Configuration Mode is the QSPI “Master Quad-SPI (32b) Mode.
	ON	**OFF**	Not used
	ON	ON	Alternative Configuration Mode SD 2.0
4	-		Not used

Table 4-1 : Hardware Configuration DIP-Switch S1

DIP-Switch S2

Switch	Position	Configuration
1	**OFF**	I2C Bridge between BMC and Zynq™ I2C is register controlled via “I2C_BRDG_MODE_EN”
	ON	I2C Bridge is always active
2	**OFF**	BMC is master of TEMP-I2C Bus.
	ON	User MPSoC PS or PL are master of the TEMP-I2C bus forwarding of the main onboard I2C bus to the TEMP-I2C bus.
3	-	Not used
4	-	Not used

Table 4-2 : Hardware Configuration DIP-Switch S2

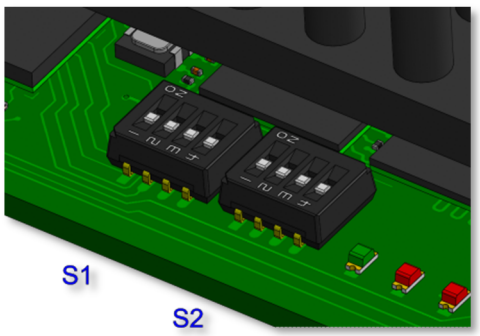


Figure 4-1 : Configuration Switch Overview

4.2 SPI Interface to BMC

The BMC handles the programming of the Si5338 clock generator, enables and monitors the User MPSoC Power Supply, board temperature, power up configuration of the User MPSoC and the default programming of the reference voltages for the DAC output voltage range.

There is an SPI interface for in-system reprogramming capability that is accessible from the User MPSoC. Its structure is shown below.

4.2.1 SPI Configuration BMC Register Space

SPI Register Address	Register Name	Size (bit)
0x00	DAC Control / Status Register	32
0x04	DAC Output Voltage Range Register Channel 0 - 15	32
0x08	DAC Output Voltage Range Register Channel 16 - 31	32
0x0C – 0x0F	Reserved	-
0x10	DAC Reference Voltage Registers - DAC Channel 0	32
0x14	DAC Reference Voltage Registers - DAC Channel 1	32
0x18	DAC Reference Voltage Registers - DAC Channel 2	32
0x1C	DAC Reference Voltage Registers - DAC Channel 3	32
0x20	DAC Reference Voltage Registers - DAC Channel 4	32
0x24	DAC Reference Voltage Registers - DAC Channel 5	32
0x28	DAC Reference Voltage Registers - DAC Channel 6	32
0x2C	DAC Reference Voltage Registers - DAC Channel 7	32
0x30	DAC Reference Voltage Registers - DAC Channel 8	32
0x34	DAC Reference Voltage Registers - DAC Channel 9	32
0x38	DAC Reference Voltage Registers - DAC Channel 10	32
0x3C	DAC Reference Voltage Registers - DAC Channel 11	32
0x40	DAC Reference Voltage Registers - DAC Channel 12	32
0x44	DAC Reference Voltage Registers - DAC Channel 13	32
0x48	DAC Reference Voltage Registers - DAC Channel 14	32
0x4C	DAC Reference Voltage Registers - DAC Channel 15	32
0x50	DAC Reference Voltage Registers - DAC Channel 16	32
0x54	DAC Reference Voltage Registers - DAC Channel 17	32
0x58	DAC Reference Voltage Registers - DAC Channel 18	32
0x5C	DAC Reference Voltage Registers - DAC Channel 19	32
0x60	DAC Reference Voltage Registers - DAC Channel 20	32
0x64	DAC Reference Voltage Registers - DAC Channel 21	32
0x68	DAC Reference Voltage Registers - DAC Channel 22	32
0x6C	DAC Reference Voltage Registers - DAC Channel 23	32
0x70	DAC Reference Voltage Registers - DAC Channel 24	32

0x74	DAC Reference Voltage Registers - DAC Channel 25	32
0x78	DAC Reference Voltage Registers - DAC Channel 26	32
0x7C	DAC Reference Voltage Registers - DAC Channel 27	32
0x80	DAC Reference Voltage Registers - DAC Channel 28	32
0x84	DAC Reference Voltage Registers - DAC Channel 29	32
0x88	DAC Reference Voltage Registers - DAC Channel 30	32
0x8C	DAC Reference Voltage Registers - DAC Channel 31	32
0x90 – 0x9F	Reserved	-
0xA0	Extended Control and Status Register	32
0xA4	Reserved	32
0xA8	Power Supply Control and Status Register	32
0xAC	Power Supply Extended Status Register	32
0xB0	Fan Control Status Register	32
0xB4	Fan Detection Period Register	32
0xB8	Fan Detection Revolution Limit Register	32
0xBC	Fan PWM User adjusted Period Register	32
0xC0	Fan Error Revolution Limit Register	32
0xC4	Fan Revolution (Speed) Register	32
0xC8 – 0xCC	Reserved	-
0xD0	User Application Device Control and Status Register	32
0xD4 – 0xEC	Reserved	-
0xF0	TPCE646 Board Temperature	32
0xF4	TPCE646 I/O Temperature	32
0xF8	TPCE646 Serial Number	32
0xFC	BMC Firmware ID	32

Table 4-3 : SPI Configuration BMC Register Space

5 Terms and Definitions

5.1 Register bit Access Types

Register Bit Access Type		Description
R	Read	The bit is readable by software (not writeable)
W	Write	The bit is writeable by software (not readable)
R/W	Read/Write	The bit is readable and writeable by software
R/W1C (R/C)	Read/Clear	The bit is readable by software The bit is set by firmware Software may clear the bit by writing a '1'
R/W1S (R/S)	Read/Set	The bit is readable by software Software may set this bit to '1' The bit is cleared by firmware

Table 5-1 : Register bit Access Types

For future software compatibility: Reserved bits shall be written '0'.

5.2 Signal Direction Types

Signal Direction Types as stated in Pin Assignment tables.

Signal Direction (Dir)	Description
I	Input Externally driven signal into the PMC
O	Output Signal driven out by PMC
I/O	Bi-Directional Signal
OD	Open Drain Output Signal driven low or tri-stated by PMC

Table 5-2 : Signal Direction Types

5.3 Style Conventions

Hexadecimal values are shown with prefix 0x (i.e. 0x029E).

Binary values are shown with prefix 0b (i.e. 0b0110).

"Active Low" signals are shown with a # suffix (i.e. RESET#).

6 Register Description

6.1 User MPSoC

The User MPSoC register description depends on the user application and is not part of this specification.

6.2 BMC

6.2.1 DAC Reference Voltages (Background)

Background information for register offsets 0x0 – 0x8C:

The TPCE646 DAC output (AD5547) consists of two independent DACs, which are combined in one device/package.

The output voltage range of a AD5547 DAC channel is determined by two applied reference voltages VREF and VOFF. On the TPCE646, these reference voltages are configurable for each individual DAC channel via the analog output channels of on-board Reference DAC devices.

For the generation of the reference voltages for the 32 TPCE646 DAC outputs, four serial Reference DAC devices are present on the TPCE646. Each Reference DAC features 16 analog outputs, providing the reference voltages for four of the AD5547 devices or 8 TPCE646 DAC channels.

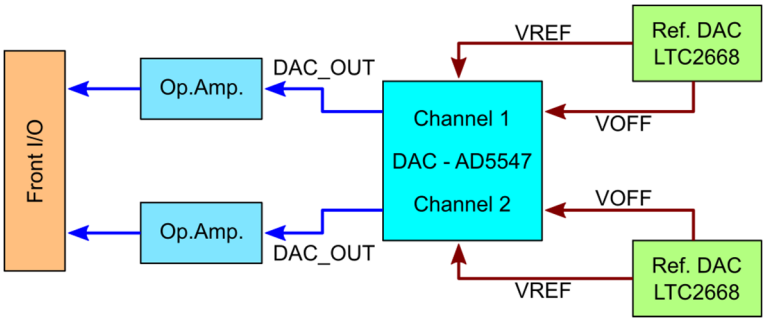


Figure 6-1 : DAC and Ref. DAC Schemata

6.2.2 DAC Control and Status Register – 0x00

This register is used to program the reference voltages (i.e. the output voltage ranges) of the TPCE646 DAC channels after the DAC output voltage ranges have been pre-configured via registers 0x04, 0x08 (and 0x10 to 0x8C for individual ranges).

Bit	Symbol	Description	Access	Reset Value
31:24	-	Range for RefDAC 3 (Structure like RefDAC 0, exception: shared DAC_REF_CLR)		0
23:16	-	Range for RefDAC 2 (Structure like RefDAC 0, exception: shared DAC_REF_CLR)		0
15:08	-	Range for RefDAC 1 (Structure like RefDAC 0, exception: shared DAC_REF_CLR)		0
7:6	-	Reserved		0
5	DAC_REF_OUTP_UPD	DAC Reference Update Initiate Reference DAC output update with current DAC channel output voltage range pre-configuration (see registers 0x4, 0x8) Self-Clearing	R/S	0
4	DAC_REF_CLR	DAC Reference Clear Performs an asynchronous clear on the Reference DAC device, including post-reset/power-on setup with currently adjusted output voltage configuration *Fundamental Device Reset -* *Using this bit always affects all 4 Reference DACs.* Self-Clearing	R/S	0
3	DAC_REF_OVRTMP	DAC Reference Over Temperature Status information provided by the Reference DAC device. Reset/cleared by an output update operation.	R	0
2	-	Reserved		
1	DAC_REF_OUTPSTTLE	DAC Reference Output Settle Internal generated settling pulse (set to approx. 20.5us) 0 when reference voltages have settled (after an update)	R	0
0	DAC_REF_IOBSY	DAC Reference I/O Busy Indicates that • Controller is not in idle • Span-Configuration update is pending • Reference voltage update is pending • Internal synchronization is pending	R	0

Table 6-1 : DAC Reference Control and Status Register

6.2.3 DAC Output Voltage Range Register – 0x04

This register is used to pre-configure the output voltage range of the TPCE646 DAC channels (0 to 15).

Bit	Symbol	Description	Access	Reset Value
31:30	DAC_15_OR	Output Voltage range selection for DAC channel 15 00 : ±10 V range (default value) 01 : ±5 V range 10 : ±2.5 V range 11 : individual range selection	R/W	0b00
…	-	…	…	…
1:0	DAC_0_OR	Output Voltage range selection for DAC channel 0 00 : ±10V range (default value) 01 : ±5V range 10 : ±2.5V range 11 : individual range selection	R/W	0b00

Table 6-2 : DAC Output Voltage Range Register

For individual voltage range selection, the DAC channel's reference voltages (VREF, VOFF) must be configured in the corresponding DAC Reference Voltage register.

6.2.4 DAC Output Voltage Range Register – 0x08

This register is used to pre-configure the output voltage range of the TPCE646 DAC channels (16 to 31).

Bit	Symbol	Description	Access	Reset Value
31:30	DAC_31_OR	Output Voltage range selection for DAC channel 31 00 : ±10 V range (default value) 01 : ±5 V range 10 : ±2.5 V range 11 : individual range selection	R/W	0b00
…	-	…	…	…
1:0	DAC_16_OR	Output Voltage range selection for DAC channel 16 00 : ±10 V range (default value) 01 : ±5 V range 10 : ±2.5 V range 11 : individual range selection	R/W	0b00

Table 6-3 : DAC Output Voltage Range Register

For individual voltage range selection, the DAC channel's reference voltages (VREF, VOFF) must be configured in the corresponding Reference Voltage register.

6.2.5 DAC Reference Voltage Registers – 0x10 to 0x8C

The DAC Reference Voltage Registers are used to define the output voltage range for each TPCE646 DAC output channel that is configured for an individual output voltage range.

Steps are:

1. Determine the VREF and VOFF voltage values for the individual output voltage range
2. Determine the corresponding VREF and VOFF data values for the Reference DAC
3. Program the VREF and VOFF data values to the corresponding Reference Voltage Register

The output voltage range of a TPCE646 DAC channel is calculated with two reference values (VREF and VOFF) as follows:

Vrange_low = -1 * VOFF

Vrange_high = -1 * VOFF - 2 * VREF

See the following Examples:

VOFF	VREF	Vrange_low	Vrange_high	Voltage Range	Note
+10 V (0xFFFF)	-10 V (0x0000)	-10 V	+10 V	-10V … +10 V	typical range
+5 V (0xC000)	-5 V (0x4000)	-5 V	+5 V	-5V … +5 V	typical range
+1.25 V (0x2000)	-5 V (0x4000)	-1.25 V	+8.75 V	-1.25 V … + 8.75 V	asymmetric range
-5 V (0x4000)	+5 V (0xC000)	+5 V	-5 V	+5 V … -5 V	changes sign

Table 6-4 : VREF, VOFF to Voltage Range Examples

Thus, any desired output voltage can be generated. However, in any case, it is important to ensure that the voltages Vout1 and Vout2 are never set above +10 V or below -10 V. Voltages above these limits cannot be generated and lead to incorrect outputs.

The following table shows the Reference DAC data coding for the VREF and VOFF voltages.

Voltage	Digital Code
+9.9997 V	0xFFFF
+5.0 V	0xC000
+2.5 V	0xA000
0 V	0x8000
-2.5 V	0x6000
-5.0 V	0x4000
-10.0 V	0x0000

Table 6-5 : Voltage coding for the VREF, VOFF Reference Voltages

$$VOFF_{data} = \frac{(VOFF_{value} + 10V)}{20V * 2^{16}}$$

$$VREF_{data} = \frac{(VREF_{value} + 10V)}{20V * 2^{16}}$$

There is one 32bit Register for each of the 32 TPCE646 DAC output channels. However, only the registers for DAC channels that are configured for an individual output voltage range need to be programmed!

Bit	Symbol	Description	Access	Reset Value
31:16	VREF	16-bit Data Value for VREF which specifies the half voltage swing of the reference voltage for the AD5547 DAC channel.	R/W	0x8000
15:0	VOFF	16-bit Data Value for VOFF which represents the negative reference voltage of the AD5547 DAC channel.	R/W	0x8000

Table 6-6 : Reference Voltage Register (32x)

See register map in *SPI Configuration BMC Register Space* for the register offset to DAC channel mapping.

6.2.6 Extended Control and Status Register – 0xA0

Bit	Symbol	Description	Access	Reset Value
31	CLKGEN_ INTR	Clock Generator Interrupt Request Shows the interrupt request line status of the onboard clock generator. *Active-high polarity*	R	0
30	-	Reserved	R	0
29:28	DBG_PRSNT	Debug (JTAG) Plug Detected When using a standard AMD JTAG programmer, these bits indicate whether a cable is connected or not. [1] := 11.8 Additional PJTAG Header [0] := User MPSoC JTAG Header	R	0
27:20	FUNC_SW	Function Switch Shows the board functional switch setting. [7] := - [6] := - [5] := - [4] := SW_I2C_SEL [3] := - [2] := SW_CNF_MEM[1] [1] := SW_CNF_MEM[0] [0] := SW_PCE_MUX	R	0
19:16	BRD_OPT	Board Option **Internal use only**	R	0
15:5	-	Reserved	R	0
4	EXT_RST	Extended Reset High-active writing causes an BMC re-initialization cycle. *Does not affect the power-controller and registers.*	R/W1S	0
3:1	-	Reserved	R	0
0	I2C_BRDG_ MODE_EN	I2C Bridge Mode Enable Controls the I2C bus coupler (bus isolator) of the UAD and BMC I2c bus segments 0: decoupled (default value) 1: coupled	R/W	0

Table 6-7 : Extended Control and Status Register

6.2.7 Power Supply Control and Status Register – 0xA8

This register controls power related functionalites and shows power supply status event information, not the current status of single supplies.

Actual status is provided in register Power Supply Extended Status Register.

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	W1/R	0
27	VCOM	Associated with Vcom Power Good *See VCCint description*	W1/R	0
26	+5.0V	Associated with +5V Power Good *See VCCint desription*	W1/R	0
25	VEE	Associated with VEE Power Good *See VCCint desription*	W1/R	0
24	PL_DDR	Associated with PL_DDR Power Good *See VCCint description*	W1/R	0
23	PS_DDR	Associated with PS_DDR Power Good *See VCCint description*	W1/R	0
22	GTR_AVTT_PS	Associated with GTR_AVTT_PS Power Good *See VCCint desription*	W1/R	0
21	MISC_PL	Associated with MISC_PL Power Good *See VCCint desription*	W1/R	0
20	MISC_PS	Associated with MISC_PS Power Good *See VCCint desription*	W1/R	0
19	GTY	Associated with GTY Power Good *See VCCint desription*	W1/R	0
18	GTH	Associated with GTH Power Good *See VCCint desription*	W1/R	0
17	GTY_AUX	Associated with GTY_AUX Power Good *See VCCint desription*	W1/R	0
16	GTH_AUX	Associated with GTH_AUX Power Good *See VCCint desription*	W1/R	0
15	GTY_AVCC	Associated with GTY_AVcc Power Good *See VCCint desription*	W1/R	0
14	GTH_AVCC	Associated with GTH_AVcc Power Good *See VCCint desription*	W1/R	0
13	BMC	Associated with BMC Power Good *See VCCint desription*	W1/R	0
12	VCCINT	VCCint Power Good Event Set when VCCint transistion from not power good to power good is detected. ‘0’ := no transistion ‘1’ := transistion *W1 to clear bit*	W1/R	0
11:1	-	Reserved	R	

0	PS_CNTRL_ FTO_EN	Power Controller Failure Turn-Off Enable In case that the Global Power Good is reached but violated during operation, the safety turn-off can be enabled. (Stage [5]) ‘0’ := Disabled ‘1’ := Enabled *Power Cycle is required to get back into functional operation*	R/W	0

Table 6-8 : Power Supply Control and Status Register

6.2.8 Power Supply Extended Status Register – 0xAC

This register provides extended power supply information, including current power good information.

Bit	Symbol	Description	Access	Reset Value
31	-	Reserved	R	
30	GTR_AVCC_PS	GTR AVCC PS Power Good Status	R	0
29	EN_GTR_AVCC_PS	GTR AVCC PS Power Enable/Activation Status	R	0
28	VCOM	VCOM Power Good Status	R	0
27	EN_VCOM	VCOM Power Enable/Activation Status	R	0
26	+5.0V	5V Power Good Status	R	0
25	EN_+5.0V	5V Power Enable/Activation Status	R	0
24	VEE	VEE Power Good Status	R	0
23	EN_VEE	VEE Power Enable/Activation Status	R	0
22	PL_VDD	PL VDD Power Good Status	R	0
21	EN_PL_VDD	PL VDD Power Enable/Activation Status	R	0
20	PL_DDR	PL DDR Power Good Status	R	0
19	EN_PL_DDR	PL DDR Power Enable/Activation Status	R	0
18	PS_DDR	PS DDR Power Good Status	R	0
17	EN_PS_DDR	PS DDR Power Enable/Activation Status	R	0
16	GTR_AVTT_PS	GTR AVTT PS Power Good Status	R	0
15	EN_GTR_AVTT_PS	GTR AVTT PS Power Enable/Activation Status	R	0
14	MISC_PL	Multi-Control PL Power Good Status	R	0
13	EN_MISC_PL	Multi-Control PL Power Enable/Activation Status	R	0
12	MISC_PS	Multi-Control PL Power Good Status	R	0
11	EN_MISC_PS	Multi-Control PL Power Enable/Activation Status	R	0
10	GTY	GTY Power Good Status	R	0
9	GTY_AUX	GTY AUX Power Good Status	R	0
8	EN_GTY	GTY Power Enable/Activation Status	R	0
7	GTY_AVCC	GTY AVCC Power Good Status	R	0
6	GTH	GTH Power Good Status	R	0
5	GTH_AUX	GTH AUX Power Good Status	R	0
4	EN_GTH	GTH Power Enable/Activation Status	R	0
3	GTH_AVCC	GTH AVCC Power Good Status	R	0
2	+2.5V	2.5V Power Good Status	R	0
1	BMC	BMC Power Good Status	R	0
0	VCCINT	VCCINT Power Good Status	R	0

Table 6-9 : Power Supply Extended Status Register

6.2.9 Fan Control and Status Register – 0xB0

Register for fan controlling and monitoring.

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	R	
15:13	-	Reserved	R	
12	FAN_ERR	Fan Error Used to signal a fan error when detected by internal monitoring.	R	0
11:9	-	Reserved	R	
8	FAN_ERR_MASK	Fan Error Mask Error Mask and clears (by disabling and reactivation) a detected fan error. 0b0 = not masked 0b1 = masked	R/W	0
7:5	-	Reserved	R	
4	FAN_DET_EN	Fan Detection Enable Allow controlling, enable or disable, the internal fan detection. 0b0 = off 0b1 = on	R/W	1
3:2	FAN_SPEED_ MAN_SEL	Fan Speed Manual Selection Determines the fan speed in Manual Fan Mode. 0b00 = Disabled 0b01 = Reserved 0b10 = User Adjusted (UA) Speed 0b11 = High Speed ***Disabling the FAN might cause thermal issues or hardware damages***.	R/W	0b10
1:0	FAN_OPMODE	Fan Operation Mode 0b00 = Reset (Off) 0b01 = Manual Mode others = Reserved ***Disabling the FAN might cause thermal issues or hardware damages***.	R/W	0b01

Table 6-10 : Fan Control and Status Register

6.2.10 Fan Detection Period Register – 0xB4

Used for defining a FAN turn-on detection time-out value.

Bit	Symbol	Description	Access	Reset Value
31:0	FAN_DET_PER	Detection Period Value (5s) ***Factory determined. Do not change Reset Value*** $5s * 53.2MHz = 0x0FA067F$	R/W	0x0FDA067F

Table 6-11 : Fan Detection Period Register

6.2.11 Fan Detection Revolution Limit Register – 0xB8

Used for defining a FAN turn-on detection RPM minimum value.

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	R	
19:0	FAN_DET_REVOL_LIM	Minimum Revolution Count Compare Value ***Factory determined. Do not change Reset Value***	R/W	0x00FFFFFF

Table 6-12 : Fan Detection Revolution Limit Register

6.2.12 Fan Pulse Width Modulation User Adjusted Period Register – 0xBC

Register for defining an user-specific PWM fan speed.

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	-	
19:0	FAN_PWM_UA_PER	FAN PWM Period Selects the User Adjusted PWM Period. *Default value sets fan to 50%.* *0% ---------- 50% ---------- 100%* *0x00000000 0x00000427 0x0000084F*	R/W	0x00000427

Table 6-13 : Pulse Width Modulation User Adjusted Period Register

6.2.13 Fan Error Revolution Limit Register – 0xC0

Used for defining a FAN operational detection RPM minimum value.

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	R	
19:0	FAN_OPM_REVOL_LIM	Minimum Revolution Count Compare Value ***Factory determined. Do not change Reset Value***	R/W	0x00FFFFFF

Table 6-14 : Fan Error Revolution Limit Period Register

6.2.14 Fan Revolution Register – 0xC4

Register for extended fan monitoring.

Bit	Symbol	Description	Access	Reset Value
31:0	FAN_CUR_RPM_ECM	Fan Current Speed The value represents the most-recent measured time between two FAN speed pulses. Count resolution is 2us. $\mathbf{RPM} = \frac{\mathbf{60}}{\mathbf{FAN\_CUR\_RPM\_ECM} * \mathbf{2\mu s} * \mathbf{PoleCount}}$ *PoleCount is defined to be 4.*	R	-

Table 6-15 : Fan Revolution Register

6.2.15 User Application Device Control and Status Register – 0xD0

Each individual bit reflects the current state of the corresponding configuration pin of the Zynq™ UltraScale+™ MPSoC. The bit values indicate the real-time logic level present on these pins, allowing the system to monitor and evaluate the device's configuration status.

Bit	Symbol	Description	Access	Reset Value
31:12	-	Reserved	R	-
11	PS_ERR_STAT	Status output that indicates whether an error occurred during the boot/configuration process	R	-
10	PS_ERR_OUT	Serious errors from the processing system to external logic or the PL	R	-
9	PS_DONE	Processing system configuration successfully completed	R	-
8	PS_INIT_B	Indicates the initialization status	R	-
7	PS_PROG_B	Active low input that resets the PS configuration or initiates a reboot/reconfiguration process	R	-
6	PS_SRST_B	System reset input that completely resets the processing system	R	-
5	-		R	-
4	PS_POR_B	Power-on reset input; keeps the PS in reset until the supply voltages are stable	R	-
3:0	PS_MODE	Boot mode pins that determine which source the processing system boots from (JTAG, QSPI, SD) 0b0000 = PS JTAG (default) 0b0010 = Quad-SPI (32b) 0b0011 = SD0 (2.0)	R	-

Table 6-16 : UAD Register

6.2.16 TPCE646 Board Temperature Sensor Register - 0xF0

Register for temperature controlling and board temperature monitoring.

Bit	Symbol	Description	Access	Reset Value
31:25	-	Reserved	R	-
24	BRD_TMP_ALERT	TMP-Alert (Status-Readback) TMP-Alert (Status-Feedback) This bit shows the TMP441 alarm status of the TPCE646 and becomes active if the temperature exceeds limits. Lower Limit = -40°C Upper Limit = +85°C	R	0
23	TMP441_BRD_UPDATE	TMP Data Update Strobe Indicates active communication between the temperature sensor and the BMC.	R/W1C	0
22	-	Reserved	R	-
21	TMP441_AUTO _TRD_EN	TMP441 Automatic Temperature Read Enable Controls the periodic board temperature read feature. Refresh time = 1s ‘0’ = disabled ‘1’ = enabled *Setting is applied on all onboard temperature sensors (board and I/O area)*	R/W	1
20	BRD_TMP_SENS_REG	Manual-trigger Request When Automatic mode is disabled, this triggers a manual temperature reading of both the board and I/O area.	R/S	0
19:16	-	Reserved	R	-
15:8	TMP441_BRD_TEMP	TMP441 Board Temperature Data Measured data of the on-board temperature sensor The read value of the temperature sensor is stored sign-extended as a 8bit two's complement. To actually calculate the temperature from the two's complement data value, use the following formula: Temperature (°C) = TEMP	R	-
7:0	-	Reserved	R	-

Table 6-17 : TPCE646 Board Temperature Sensor Register

6.2.17 TPCE646 I/O Area Temperature Sensor Register - 0xF4

Register for IO area temperature monitoring.

Bit	Symbol	Description	Access	Reset Value
31:25	-	Reserved	R	-
24	IO_TMP_ALERT	TMP-Alert (Status-Feedback) This bit shows the TMP441 alarm status of the TPCE646 I/O area and becomes active if the temperature exceeds limits. Lower Limit = -40°C Upper Limit = +85°C	R	0
23	TMP441_IO_UPDATE	TMP Data Update Strobe Indicates active communication between the temperature sensor and the BMC.	R/W1C	0
22:16	-	Reserved	R	-
15:8	TMP441_IO_TEMP	TMP441 I/O Temperature Data Measured data of the I/O area temperature sensor The read value of the temperature sensor is stored sign-extended as an 8 bit two's complement. To actually calculate the temperature from the two's complement data value, use the following formula: Temperature (°C) = TEMP	R	-
7:0	-	Reserved	R	-

Table 6-18 : TPCE646 I/O Area Temperature Sensor Register

6.2.18 TPCE646 Serial Number Register - 0xF8

Bit	Symbol	Description	Access	Reset Value
31:0	S_NUMBER	The value is the unique serial number of each TPCE646 module Example: 0x0091_50DD => SNo.: 9523421	R	-

Table 6-19 : TPCE646 Serial Number Register

6.2.19 BCC Firmware ID - 0xFC

Bit	Symbol	Description	Access	Reset Value
31:0	CODE_VER	The value shows the BCC Firmware ID.	R	-

Table 6-20 : BCC Firmware ID

7 Interrupts

7.1 Interrupt Sources

7.1.1 User MPSoC

The User MPSoC interrupt sources depend on the active user application and are not part of this manual.

7.2 Interrupt Handling

7.2.1 User MPSoC

The interrupt handling depends on the user application and is not part of this manual.

8 Functional Description

8.1 User MPSoC (Zynq™ UltraScale+™)

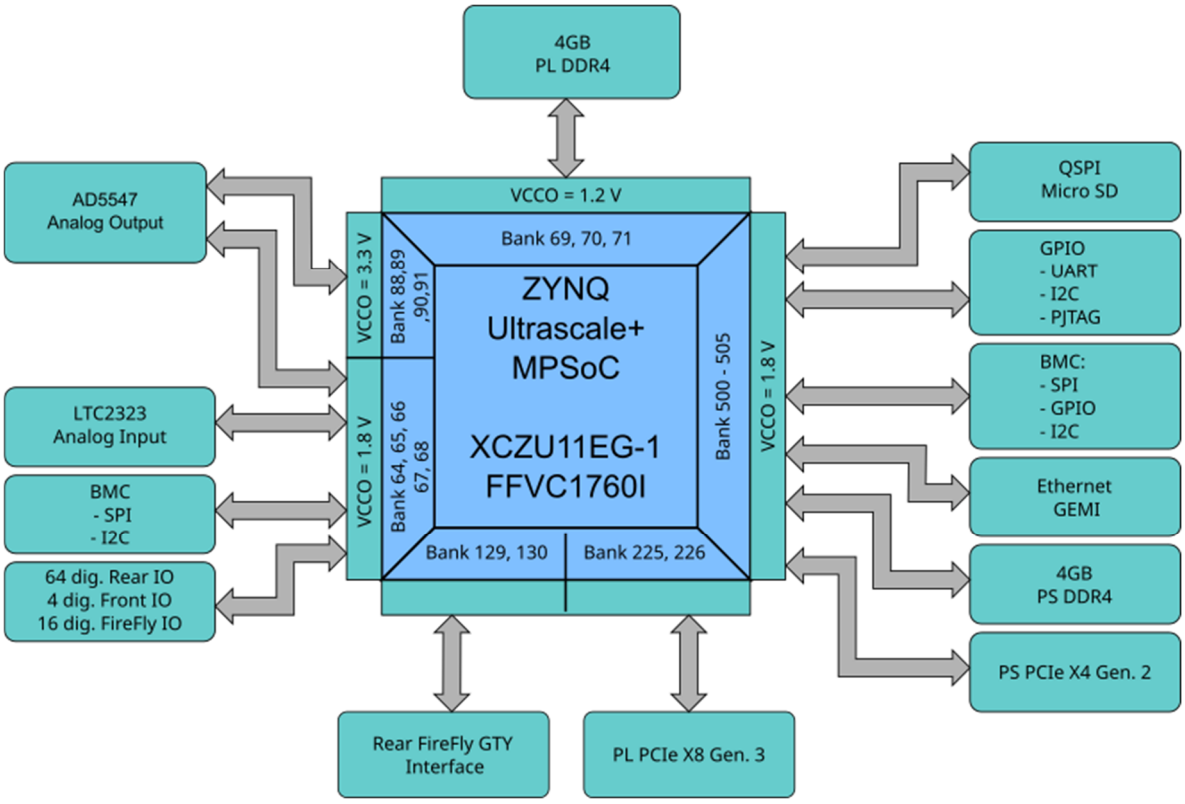


Figure 8-1 : User MPSoC Block Diagram

The User MPSoC is equipped with 12 PL I/O banks, 6 PS MIO banks, 8 GTH and 4 GTY Transceiver banks.

Bank	VCCO	VREF	Signals	Note
Bank 88	3.3 V	none	Parallel DAC Interface	
Bank 89	3.3 V	none		
Bank 90	3.3 V	none		
Bank 91	3.3 V	none		
Bank 64	1.8 V	none	Digital Rear I/O Interface Optional UART Handshake Signals FireFly Sideband Signals	
Bank 65	1.8 V	none		
Bank 66	1.8 V	none	Digital FireFly Interface Digital Front I/O	
Bank 67	1.8 V	none	ADC Interface	
Bank 68	1.8 V	none	DAC ADR Lines USER LEDs	

Bank 69	1.2 V	0.6 V	64 bit DDR4 Memory Interface 4GB	
Bank 70	1.2 V	0.6 V		
Bank 71	1.2 V	0.6 V		
Bank 500	1.8 V	none	QSPI MicroSD	
Bank 501	1.8 V	none	GPIO to BMC Ethernet Phy. (GEM1)	
Bank 502	1.8 V	none	UART QSPI to BMC PJTAG	
Bank 503	1.8 V	none	Configuration JTAG SYSMON – internal ADC	
Bank 504	1.2 V	none	64 bit DDR4 Memory Interface 4GB	
Bank 505	PCIe X4 Interface Gen.2 via PCIe Multiplexer to TPCE646 PCIe Connector			
Bank 128, 131	Not used on TPCE646			
Bank 129	Connected to High Speed GTY Interface			
Bank 130	Connected to High Speed GTY Interface			
Bank 225, 226	PCIe X8 Gen.3 Interface via PCIe Multiplexer to TPCE646 PCIe Connector			
Bank 224, 227	Not used on TPCE646			
Bank 228, 229, 230, 231	Not used on TPCE646			

Table 8-1 : User MPSoC Bank Usage

For a detailed overview of all user MPSoC I/O pins and the respective constraints to be set for each pin, TEWS Board Reference Design constraint file "tpce646_xczu11_xxx_ffvc1760.xdc" should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

8.2 User MPSoC GTH and GTR Interface

The PCIe interface of the TPCE646 edge connector is routed to the user MPSoC through a 1:2 multiplexer. This multiplexer provides two selectable PCIe paths: one to the MPSoC Programmable Logic (PL) and one to the MPSoC Processing System (PS).

The PCIe connection to the PL is implemented as an x8 Gen3 interface, while the PCIe connection to the PS is implemented as an x4 Gen2 interface.

The active PCIe path (PL or PS) is selected via a DIP switch on the TPCE646. This selection must be configured prior to powering on the TPCE646, as runtime switching is not supported.

Note: The MPSoC requires a defined configuration time after power-up before the selected PCIe interface becomes operational. Depending on the system design and the selected boot mode, this initialization phase may lead to delays that can violate the PCIe link training or setup timing requirements of the host system. It is therefore essential to ensure that the system's power-up and reset sequencing accommodates the MPSoC configuration time to prevent PCIe link establishment issues.

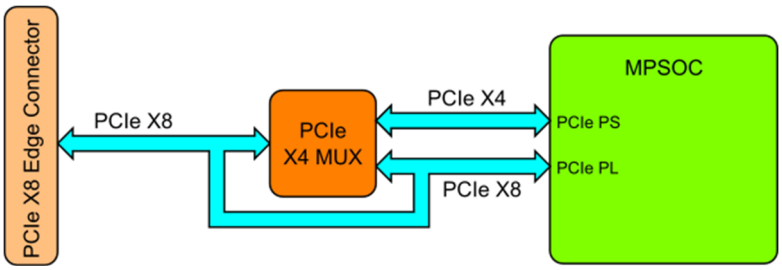


Figure 8-2 : PCIe Multiplexer Interface

Only one interface can be used at a time. Either PCIe X8 to the PL or PCIe X4 to the PS.

GTH	TPCE646 Signal	User MPSoC Pins	Bank
MGTHRXx0	PER00-	AJ1	226
	PER00+	AJ2	
MGTHRXx1	PER01-	AK3	
	PER01+	AK4	
MGTHRXx2	PER02-	AL1	
	PER02+	AL2	
MGTHRXx3	PER03-	AM3	
	PER03+	AM4	
MGTHTXx0	PET00-	AH7	226
	PET00+	AH8	
MGTHTXx1	PET01-	AJ5	
	PET01+	AJ6	
MGTHTXx2	PET02-	AK7	
	PET02+	AK8	
MGTHTXx3	PET03-	AL5	

	PET03+	AL6	
MGTHRXx4	PER04-	AN1	225
	PER04+	AN2	
MGTHRXx5	PER05-	AP3	
	PER05+	AP4	
MGTHRXx6	PER06-	AR1	
	PER06+	AR2	
MGTHRXx7	PER07-	AT3	
	PER07+	AT4	
MGTHTXx4	PET04-	AM7	225
	PET04+	AM8	
MGTHTXx5	PET05-	AN5	
	PET05+	AN6	
MGTHTXx6	PET06-	AP7	
	PET06+	AP8	
MGTHTXx7	PET07-	AR5	
	PET07+	AR6	

Table 8-2 : User MPSoC GTH (PL PCIe)

GTH	TPCE646 Signal	User MPSoC Pins	Bank
PS_MGTHRXx0	PS_PER00-	AG42	505
	PS_PER00+	AG41	
PS_MGTHRXx1	PS_PER01-	AE42	
	PS_PER01+	AE41	
PS_MGTHRXx2	PS_PER02-	AC42	
	PS_PER02+	AC41	
PS_MGTHRXx3	PS_PER03-	AA42	
	PS_PER03+	AA41	
PS_MGTHTXx0	PS_PET00-	AH40	505
	PS_PET00+	AH39	
PS_MGTHTXx1	PS_PET01-	AF40	
	PS_PET01+	AF39	
PS_MGTHTXx2	PS_PET02-	AD40	
	PS_PET02+	AD39	
PS_MGTHTXx3	PS_PET03-	AB40	
	PS_PET03+	AB39	

Table 8-3 : User MPSoC GTR (P PCIe)

8.3 User MPSoC GTY Interface

Two Multi Gigabit Transceiver banks (with 4 GTY transceivers each) of the User MPSoC are completely connected to two Samtec Firefly Micro Flyover connector interfaces.

The data rate to be achieved for each of the 8 data channels is 25Gbps.

Two Multi-Gigabit Transceiver (MGT) banks of the user MPSoC, each containing four GTY transceivers, are fully routed to two Samtec Firefly Micro Flyover connector interfaces. In total, eight GTY channels are available, each supporting a maximum data rate of 25 Gbps.

These high-speed transceiver interfaces provide a flexible and robust physical layer for high-bandwidth serial communication. The Firefly connectors support copper Samtec Firefly modules, enabling adaptation to a wide range of system requirements such as link distance, signal integrity, and environmental constraints.

The GTY-based MGT interfaces can be utilized for various high-speed communication applications.

When implementing inter-board communication via the Firefly interfaces, the achievable data rate depends on the specific cable assembly and the subsequent interconnect path and may therefore vary from the maximum specified rate.

Additionally, eight single-ended GPIO lanes of the user MPSoC are routed to each Firefly connector. The resulting 16 digital I/O lines available on the two rear I/O Firefly connectors are interfaced through a voltage-level translator with automatic direction detection. The characteristics of these I/O lines are as follows:

- 2.5 V I/O level
- Automatic direction detection
- Data rate up to 140 Mbps (depending on load capacitance)
- Propagation delay: 3.8 ns (typ.) / 5.2 ns (max.)
- Channel-to-channel skew: 0.15 ns
- No LVDS support

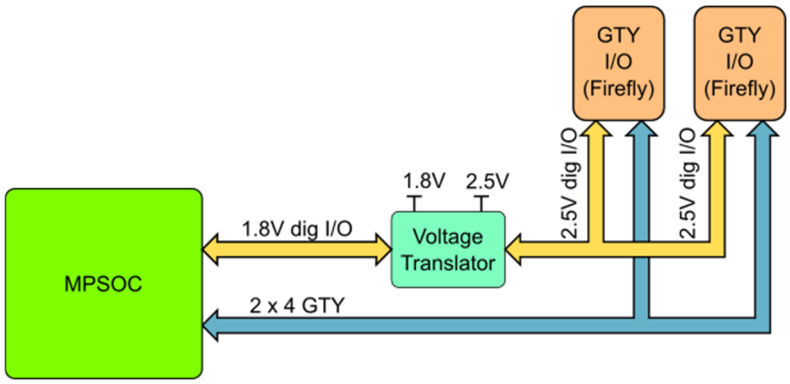


Figure 8-3 : Rear GTY and digital I/O Interface

GTY	TPCE646 Signal	User MPSoC Pins	Connected to
MGTYRXx0_129	MGTRX0-	R42	GTY Rear I/O Firefly Connector X9
	MGTRX0+	R41	
MGTYRXx1_129	MGTRX1-	P40	
	MGTRX1+	P39	
MGTYRXx2_129	MGTRX2-	N42	
	MGTRX2+	N41	
MGTYRXx3_129	MGTRX3-	M40	
	MGTRX3+	M39	
MGTYTXx0_129	MGTTX0-	T35	GTY Rear I/O Firefly Connector X9
	MGTTX0+	T34	
MGTYTXx1_129	MGTTX1-	R37	
	MGTTX1+	R36	
MGTYTXx2_129	MGTTX2-	P35	
	MGTTX2+	P34	
MGTYTXx3_129	MGTTX3-	N37	
	MGTTX3+	N36	
MGTYRXx0_130	MGTRX4-	L42	GTY Rear I/O Firefly Connector X11
	MGTRX4+	L41	
MGTYRXx1_130	MGTRX5-	K40	
	MGTRX5+	K39	
MGTYRXx2_130	MGTRX6-	J42	
	MGTRX6+	J41	
MGTYRXx3_130	MGTRX7-	H40	
	MGTRX7+	H39	
MGTYTXx0_130	MGTTX4-	M35	GTY Rear I/O Firefly Connector X11
	MGTTX4+	M34	
MGTYTXx1_130	MGTTX5-	L37	
	MGTTX5 +	L36	
MGTYTXx2_130	MGTTX6 -	K35	
	MGTTX6 +	K34	
MGTYTXx3_130	MGTTX7 -	J37	
	MGTTX7 +	J36	

Table 8-4 : User MPSoC GTY Connections

Signal	Bank	Pin	Description	Clock Capable
DIG_IO0	66	AV17	Up to 140Mbps Interface to X9 User MPSoC I/O Standard = LVCMOS18 X9 IO Level = 2.5 V	Yes
DIG_IO1		AV16		Yes
DIG_IO2		AU18		-
DIG_IO3		AV18		-
DIG_IO4		AR18		-
DIG_IO5		AT18		-
DIG_IO6		AR17		-
DIG_IO7		AT17		-
DIG_IO8		AT15	Up to 140Mbps Interface to X11 User MPSoC I/O Standard = LVCMOS18 X11 IO Level = 2.5 V	Yes
DIG_IO9		AU15		Yes
DIG_IO10		AT16		-
DIG_IO11		AU16		-
DIG_IO12		AJ18		-
DIG_IO13		AK18		-
DIG_IO14		AL18		-
DIG_IO15		AM18		-

Table 8-5 : User MPSoC GTY Connections

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, TEWS Board Reference Design constraint file "tpce646_xczu11_xxx_ffvc1760.xdc" should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

8.4 Boot and Configuration User MPSoC

The system boot-up process of the user MPSoC is controlled and executed by the **Platform Management Unit (PMU)**. This process is organized into three main stages, which ensure proper initialization of the Processing System (PS) and, optionally, the Programmable Logic (PL):

1. **Pre-configuration stage**
    - This stage begins immediately after the **Power-On Reset (POR)**.
    - The PMU performs basic hardware initialization, including clock setup, power sequencing verification, and essential low-level system checks.
    - No user code is executed at this stage; it is purely hardware and PMU-driven.
2. **Configuration stage**
    - The PMU loads the **First-Stage Boot Loader (FSBL)** into the PS.
    - The FSBL is responsible for initializing the PS subsystems, performing memory tests, and setting up essential interfaces required for subsequent boot stages.
    - If the PL is to be configured, the FSBL also prepares the PL configuration process at this stage.
3. **Post-configuration stage**
    - The FSBL is executed on the PS.
    - Typically, this includes the configuration of the PL (if used), initialization of peripherals, and preparation of the system for execution of the second-stage boot loader or the main application.
    - During PL configuration, the **AMD Tandem Configuration Feature** should be enabled to ensure full PCI Express specification compliance, regardless of the complexity of the PL design. This requires proper setup already during the PCIe IP core generation (see Xilinx PG213 for details).

Boot Mode of the TPCE646

- By default, the TPCE646 uses **QSPI 32 bit boot mode** for loading the boot image.
- Other supported boot modes can be selected via hardware boot switches or configuration, but the QSPI mode ensures standard, reliable startup for the TPCE646 system.

On delivery the QSPI configuration Platform Flashes contain the TEWS TPCE646 Reference Design for the Zynq™ UltraScale+™ device. In this case at Power-up, the TPCE646 Zynq™ UltraScale+™ configures via QSPI Interface by "Master Quad-SPI (32b)" mode.

However, JTAG or the microSD card can also be set as the configuration source via the DIP switch configuration.

8.4.1 Configuration via JTAG

The TPCE646 provides the following JTAG capable devices:

- User MPSoC
- Lattice MachXO3 (LCMXO3-9400E)

There are 3 independent JTAG chains on the TPCE646.

The two Molex 2mm AMD programmer compatible connectors lead directly to the PS JTAG and the configurable PJTAG of the User MPSoC.

The third chain leads from the PCIe Edge Connector to the BMC and is only used for the TEWS factory configuration.

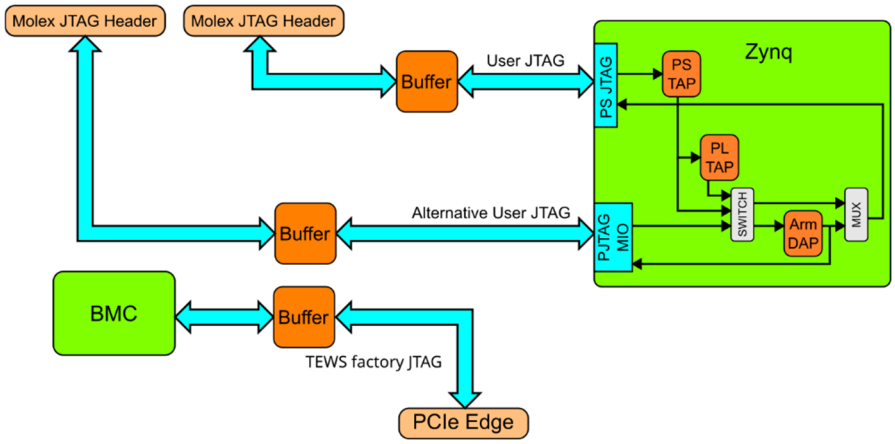


Figure 8-4 : TPCE646 JTAG-Chain

8.4.1.1 User PS-JTAG Chain

For direct User MPSoC configuration, User MPSoC read back or in-system diagnostics with Vivado™ Logic Analyzer, one of the Molex Debug Connector can be used to access the JTAG-chain. Also, an indirect SPI – PROM programming is possible via the User JTAG Chain. This Connector provides a direct connection to a AMD Programmer compatible 2 mm shrouded header.

The Molex JTAG connector has default priority. If a cable is connected here, the BCC switches this interface active. However, each of the sources can be selected via the User MPSoC JTAG Control and Status Register - 0x80 in BCC.

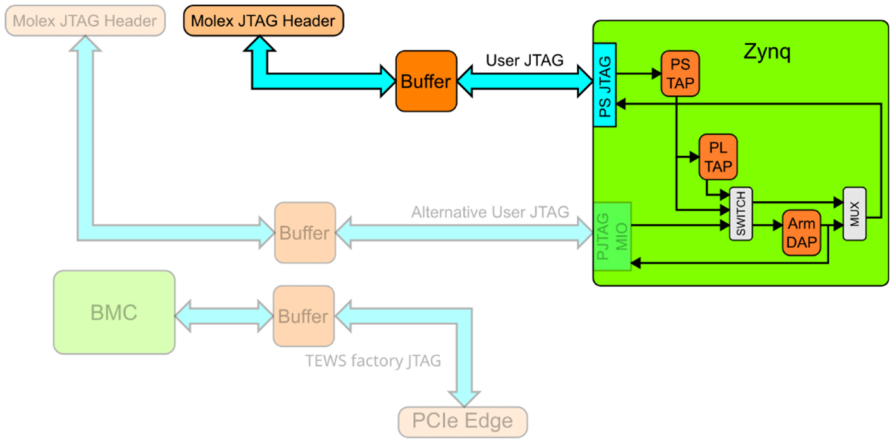


Figure 8-5 : User MPSoC PS-JTAG

8.4.1.2 User PJTAG Chain

A second possible JTAG connection for debug purposes or for communication with the User MPSoC is routed to a second AMD Programmer compatible 2 mm shrouded header.

The interface must be configured via the contents of the User MPSoC before regular use. This configuration is not part of the TEWS configuration.

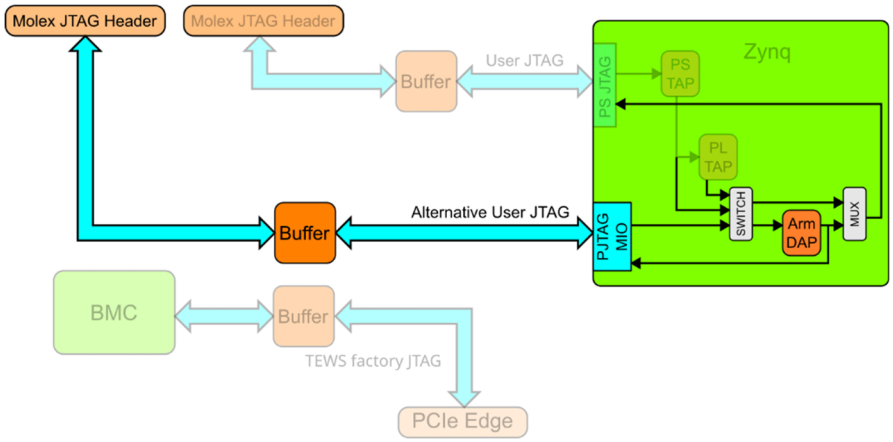


Figure 8-6 : User MPSoC P-JTAG

For more information on using the User MPSoC JTAG connection, please also refer to the AMD documentation.

8.4.1.3 TEWS Factory JTAG Chain

The TEWS Factory JTAG Chain is accessible from the PCIe Edge Connector.

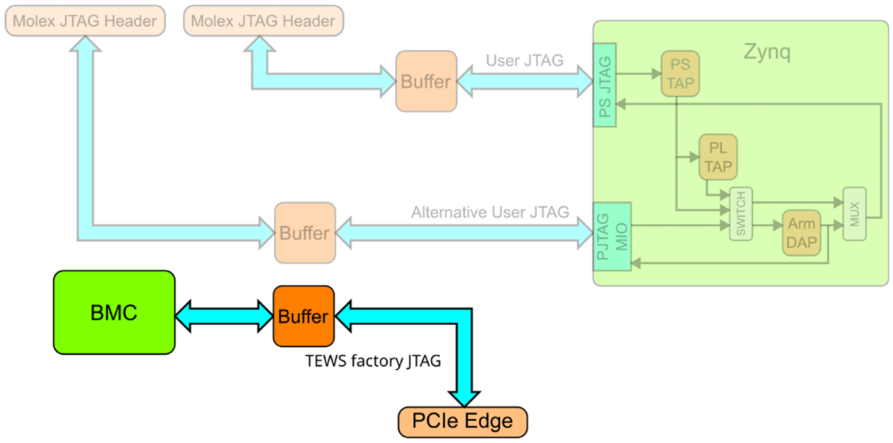


Figure 8-7 : TEWS Factory JTAG-Chain

8.5 BMC (Board Management Controller) FPGA

The Board Management FPGA handles the programming of the Si5338 clock generator, enables and monitors the User MPSoC Power Supply, board temperature, power up configuration of the User MPSoC and the default programming of the reference voltages for the DAC output voltage range.

Changing or erasing the BCF (Board Configuration Firmware) content leads to an inoperable TPCE646.

8.5.1 SPI Interface between BMC and User MPSoC

The BMC is connected to SPI1 of the MPSoC Processor System using a unidirectional x1 SPI interface. Although the interface is associated with MIO[58:63], only the required pins are used.

Of the three available chip selects, only CS#0 is active; the others are reserved. The interface uses active-low chip select, samples write data on rising edges, and updates read data on falling edges.

An X1 SPI interface is provided for in-system reprogramming from the user MPSoC, and the BMC register interface operates as an SPI slave.

The BMC Register interface is designed as a slave register interface and the register set can be found in the ***BMC Register Description*** chapter.

On the User MPSoC, this interface is to be executed as an SPI master.

User MPSoC PS Signal	Bank	TPCE646 Signal	Pin	Description
PS_MIO58	502	SPI_SCK	AC29	Serial Clock
PS_MIO62		SPI_MISO	AD31	Master In Slave Out
PS_MIO63		SPI_MOSI	AD30	Master Out Slave In
PS_MIO61		SPI_SS_OUT0	AC32	SS (Slave Select)
PS_MIO60		SPI_SS_OUT1	AD29	actual not used
PS_MIO59		SPI_SS_OUT2	AC31	actual not used

Table 8-6: User MPSoC SPI Interface to BMC

Note that SPI Interface Clock frequency is limited to maximum of 2 MHz. SPI configuration must not violate this restriction.

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file “tpce646_xczu11_xxx_ffvc1760.xdc” should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

The SPI Interface uses a nine byte request format as follows to perform read and write transfers.

Byte	*Bit*	*Information*
0:2	*23*	*Instruction, Access Classifier* *0b1 := Read* *0b0 := Write*
	22:20	Instruction, Base Address Range 0b001 := Register Space others := Reserved
	19:16	Instruction, Byte Enable 0bnnnn := set as required (active high)
	15:0	Instruction, Byte Address 0xnnnn := set as required *Consider BMC Address Space Depth*
3	-	unused (reserved for future use) *Internal Note: used to perform read access with 8 clock timeouts*
4	-	unused (reserved for future use)
5	31:24	Write Data, Read Data Byte [3], MSB
6	23:16	Byte [2]
7	15:08	Byte [1]
8	07:00	Byte [0], LSB *Internal Note: used to perform write access after 32 bit*
		Internal Note: Idle state is selected after CS de-assertion

Internally the register interface is 32 bit wide with separate byte lanes, incl. byte enables. This native width must always be considered.

Back-to-back transfers are not supported. There must be an idle time with chip select de-asserted between every access.

Violating the request format might result in unintended behavior.
Read accesses might be considered successfully while the data is actually not read and write accesses might not be performed.

Further information about the User MPSoC SPI Interface can be found in the AMD documentation UG1137, UG1085 and UG1087.

8.5.2 Optional I2C Interface between BMC and User MPSoC

Currently, this interface is only intended as reserved or for further future functions.

User MPSoC PS Signal	Bank	TPCE646 Signal	Pin	Description
PS_MIO26	501	USER_SCL	L27	Serial Clock Output A negative edge clock data out.
PS_MIO27		USER_SDA	L29	Bisectional Serial Data
IO_L1P	66	USER_SCL	AY17	Serial Clock Output A negative edge clock data out.
IO_L1N		USER_SDA	BA17	Bisectional Serial Data

Table 8-7: User MPSoC I2C Interface to BMC

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file "tpce646_xczu11_xxx_ffvc1760.xdc" should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

Additional slave devices are connected to this I2C bus. These are the I2C PROM with the ADC and DAC correction data, the SI5338 (Skyworks Solutions) clock generator and the programmable XO (SI514 - Skyworks Solutions).

A detailed description of this I2C bus can be found in the chapter ***User MPSoC I2C Bus***.

8.6 Clocking

8.6.1 User MPSoC Clock Sources

As a central clock generator of the TPCE646 the Si5338 clock generator is used. It provides all necessary clocks for the User MPSoC and the BMC.

The following table lists the available clock sources on the TPCE646 User MPSoC.

User MPSoC Clock Signal Name	User MPSoC Pin	Source	Description
PL_REFCL±	AH12 / AH11	PI6CB18200 2-Output PCIe clock buffer	100 MHz differential PCIe reference clock input
PS_REFCL±	AG37 / AG38		100 MHz differential PCIe reference clock input
USER_CLK±	AU14 / AV14	SI5338 low-jitter clock generator	105 MHz Clock Input This clock is designated for ADC/DAC interface clock source.
CLK_MGT±	W32 / W33	SI5338 low-jitter clock generator	125.25 MHz
MCB_CLK±	E32 / D32	SI5338 low-jitter clock generator	125.046892585 MHz clock input with external termination
REF_CLK±	C30 / C31	SI5338 low-jitter clock generator	200.00 MHz clock input with external termination
Si514_CLK±	R32 / R33	Si514	Any-Frequency I2C programmable XO Default: 156.25 MHz
PS_PADI	AE28	clock crystal	32.768 kHz crystal for real-time clock (RTC)
PS_PADO	AE2		
PS_REF_CLK	AC27	quarz oscilator	50 MHz User MPSoC PS reference clock input

Table 8-8 : Available User MPSoC clocks

Further IO pins of the front and rear I/O interfaces are routed to clockable pins of the User MPSoC. See the individual chapters on the different I/O interfaces for more information.

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file “tpce646_xczu11_xxx_ffvc1760.xdc” should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.BRD Project.

8.7 8 Channel Serial ADC Interface

8.7.1 Overview

The 8 analog inputs of the TPCE646 are implemented with 4 LTC2323-16 ADC devices. Each of these SAR-ADCs has two ADC channels. Thus, a total of 8 ADC channels are available on the TPCE646.

A coarse overview over the analog input section of the TPCE646 is shown by the following figure:

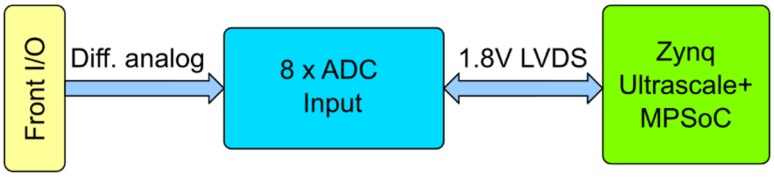


Figure 8-8 : Analog Input Section

The key-features of the LTC2323-16 are:

- Dual Channel - SAR-ADC
- 16 bit resolution
- **5Msps Sample Rate for each Channel**
- **81dB SNR (typ) at f_{in}= 2MHz**
- **-85db THD (typ) at f_{in}= 2MHz**
- LVDS SPI-Compatible Serial Interface to User MPSoC

In order to adapt the LTC2323-16 to a ±10 V input voltage maximum on each input-pin (±20 V differential voltage range), two input operational amplifiers for input impedance conversion and gain adaption are needed in addition to the actual ADC.

The following figure shows the structure and principle of the two ADC inputs. All channels are connected via an impedance converter and a level adjustment to the LTC2323-16 dual channel ADC.

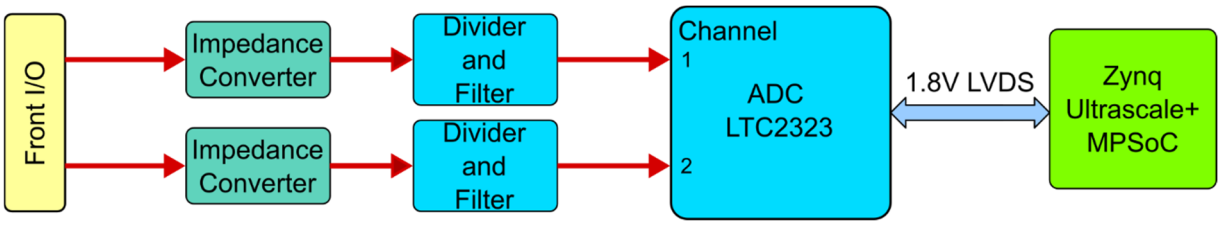


Figure 8-9 : Analog Input Block Diagram

8.7.2 ADC digital Output Coding

Differential common mode voltage is compensated by the analog input stage. In addition, the differential input voltage is reduced by an analogue divider which is built with a differential operational amplifier. The feedback resistors of this operational amplifier determine the divider value. The two resistance values 4.7kΩ and 931Ω build the divider of 5.0483. With the ADC LTC2323-16's maximum analogue differential input voltage range of ±4.096V a theoretical maximum of ±20.678 V differential input voltage range is given for a TPCE646 analog input channel.

Due to the ADC's true differential inputs, the ADC output coding significantly differs compared to a single-ended input.

Analogue to a single-ended input, where the range setting directly describes the ground related input voltage range, the ADC range setting describes the range of ground related voltages that can be tied to the ADC differential inputs. This results in an extended input voltage range, since the ADC measures the voltage between the differential inputs VIN- and VIN+.

An Example: The TPCE646 (differential input) voltage range is ±20.678 V, so the allowed (single-ended, ground related) voltage on each ADC input pin is ±10.339 V. When we examine the two largest differential voltages, we get following results:

VIN- (to GND)	VIN+ (to GND)	ADC Input (differential)
-10.339 V	+10.339 V	+20.678 V
+10.339 V	-10.339 V	-20.678 V

Table 8-9: ADC Max Differential Voltages

The example shows that the range of differential ADC input values is -20.678 V to +20.678 V, which results to a full-scale range of 41.356 V for the ±20.678 V ADC Input Range.

The TPCE646 data coding is two's complement.

8.7.2.1 ADC Data Coding ±20.678 V Voltage Range

Description	TPCE646	Digital Code
Full Scale Range	41.356 V	-
Least Significant bit	631 µV	-
Full Scale (pos.)	20.678 V	0x7FFF
Midscale + 1LSB	631 µV	0x0001
Midscale	0.0 V	0x0000
Midscale – 1LSB	-631 µV	0xFFFF
Full Scale (neg.)	-20.678 V	0x8000

Table 8-10: ADC Data Coding

8.7.3 User MPSoC Pinning

Each ADC is connected to the User MPSoC via a dedicated serial clocked Interface. Each ADC device has one input clock, one output clock and one conversion signal. For the eight ADC channel there are four differential double data rate LVDS output lines. In addition, two ADC channels are provided via each data line in multiplex mode.

Signal	Bank	Pin	Description
SCK_00+	67	BB9	Differential Clock Output for ADC Channel 0 / 1
SCK_00-		BB8	
SCKOUT_00+		AT13	Differential Clock Input for ADC Channel 0 / 1
SCKOUT_00-		AT12	
SDO1_00+		AW9	Differential Data from ADC Channel 0
SDO1_00-		AY9	
SDO2_00+		AW8	Differential Data from ADC Channel 1
SDO2_00-		AY8	
CNV_N_00		AY10	Convert Signal for ADC Channel 0 / 1

Signal	Bank	Pin	Description
SCK_01+	67	AM11	Differential Clock Output for ADC Channel 2 /3
SCK_01-		AN11	
SCKOUT_01+		AR13	Differential Clock Input for ADC Channel 2 / 3
SCKOUT_01-		AR12	
SDO1_01+		AR15	Differential Data from ADC Channel 2
SDO1_01-		AR14	
SDO2_01+		AN12	Differential Data from ADC Channel 3
SDO2_01-		AP12	
CNV_N_01		AP15	Convert Signal for ADC Channel 2 / 3

Signal	Bank	Pin	Description
SCK_02+	67	BB5	Differential Clock Output for ADC Channel 4 / 5
SCK_02-		BB4	
SCKOUT_02+		AT11	Differential Clock Input for ADC Channel 4 / 5
SCKOUT_02-		AT10	
SDO1_02+		BA8	Differential Data from ADC Channel 4
SDO1_02-		BA7	
SDO2_02+		BA6	Differential Data from ADC Channel 5
SDO2_02-		BB6	
CNV_N_02		AV12	Convert Signal for ADC Channel 4 / 5

Signal	Bank	Pin	Description
SCK_03+	67	AV9	Differential Clock Output for ADC Channel 6 / 7
SCK_03-		AV8	
SCKOUT_03+		AP10	Differential Clock Input for ADC Channel 6 / 7
SCKOUT_03-		AR10	
SDO1_03+		AU11	Differential Data from ADC Channel 6
SDO1_03-		AV11	
SDO2_03+		AW11	Differential Data from ADC Channel 7
SDO2_03-		AW10	
CNV_N_03		AU10	Convert Signal for ADC Channel 6 / 7

Table 8-11: ADC Interface Connections

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, TEWS Board Reference Design constraint file "tpce646_xczu11_xxx_ffvc1760.xdc" should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

To use the clocked serial interface between the User MPSoC and one of the two LTC2320-16 ADC devices please use the LTC2320-16 data sheet which describes the communication process.

8.7.4 Programming Hints LTC2323-16

The LTC2323-16 digital interface is a simple clocked SPI based interface.

This differential interface uses differential LVDS signals for serial data transfer. All LVDS signals need a termination on the receiver side of the connection. For the SCK± an external resistor is implemented on the TPMC646. The User MPSoC inputs CLKOUT±, SDO1± and SDO2± of each ADC channel need an internal termination. The corresponding constraints for the pin assignment, the I/O standard, termination and slew rate are specified in the TEWS Board Reference Design constraint file.

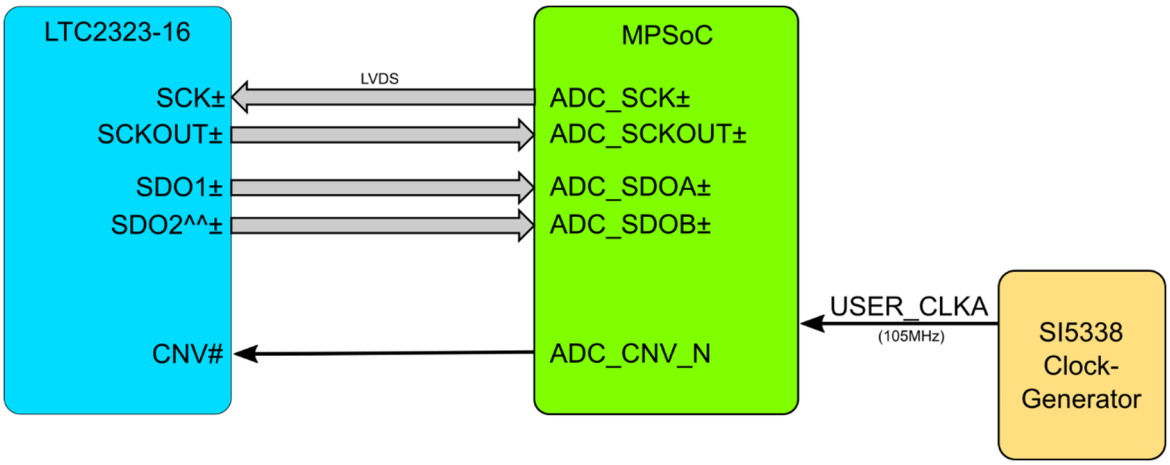


Figure 8-10 : Digital ADC to User MPSoC Interface

A conversion is triggered by a negative edge on the CNV# line. The acquisition is done during the positive phase of the CNV# signal. Following the User MPSoC drives the SCK clock, which then initiates the data transfer from the ADC to the User MPSoC. The ADC then transmits the serial data SDO1 / SDO2 synchronous to CLKOUT. The data sequence is MSB first and the LSB at least.

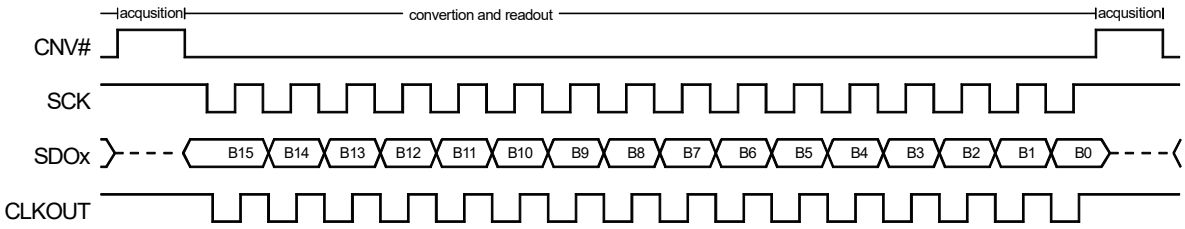


Figure 8-11 : Timing Diagram LTC2323-16

Note, that the one-cycle conversion latency has the result that the previous sample word is transmitted first. That means, at the beginning of a burst sampling period the first conversion result will be invalid.

For a detailed description of the LTC2323-16 interface and the LTC2323-16 function please use the data sheet which describes the whole communication process and all special characteristics of the ADC.

8.8 32 Channel Parallel DAC Interface

8.8.1 Overview

The 32 analog DAC outputs of the TPCE646 are realized with 16 AD5547 16 bit Dual-Current DAC devices. Each of these DACs has two DAC channels. Thus, a total of 32 DAC channels are available on the TPCE646. Because of the current output DACs, it is necessary to use operational amplifier for each DAC output channel to generate an output voltage in the range of up to ±10V.

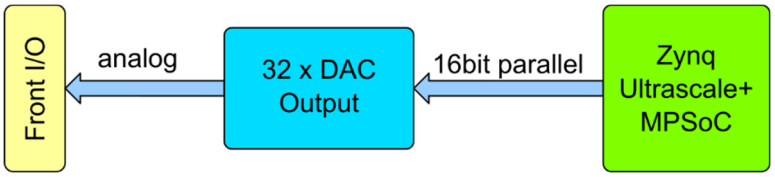


Figure 8-12 : Analog Output Section

For programming, four 16 bit wide bus interfaces are implemented. Four DAC devices (8 DAC Channels) share one 16 bit data bus from the User MPSoC. To allow setting each output individually, each DAC device has its own control interface.

The following figure shows the structure and principle of two DAC outputs. Both are connected via an independent operational amplifier to the TPCE646 Front I/O Connector.

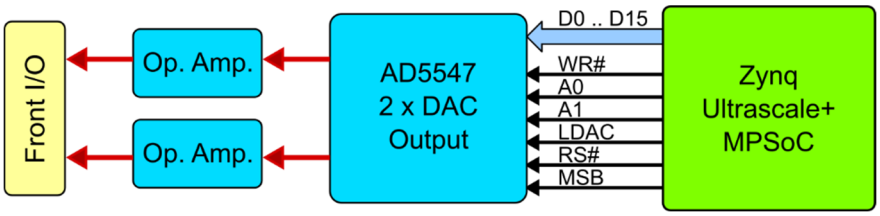


Figure 8-13 : Analog Output Section

The key-features of the TPCE646 DAC Interface are:

- 16 bit Resolution
- Built-in 4-quadrant resistors in combination with an operational amplifier to allow ±10 V outputs
- Outputs Drive ±10mA per channel
- Capacitive Load Driving = 1000pF

8.8.2 Output Voltage Range

The output voltage ranges of the TPCE646 DAC outputs are set via BMC Registers - *DAC Control / Status Register* and *DAC Output Voltage Range Registers*.

There are three predefined output voltage ranges ±10 V, ±5 V, ±2,5 V and a fourth mode in which the high and low voltage range can be set individually.

For the first three predefined fix voltage ranges, the correction data is determined during the TEWS factory test. Determined correction values are stored in an I2C EEPROM. There are no correction values for the individually adjustable voltage range mode.

Due to tolerances of the reference voltage generation, basic tolerances of the DAC components and temperature dependence, it may happen that the extreme limits for the output voltage cannot be reached.

8.8.3 User MPSoC Pinning

First DAC configuration interface is for controlling the DAC channel 1 up to 8.

Signal	Bank	Pin	Description
DAC_D0	94	F5	First DAC Data Bus to DAC Device 1 - 4 with DAC Channel 1 - 8
DAC_D1		F4	
DAC_D2		E5	
DAC_D3		E3	
DAC_D4		E4	
DAC_D5		E2	
DAC_D6		E1	
DAC_D7		D1	
DAC_D8		D4	
DAC_D9		D3	
DAC_D10		D2	
DAC_D11		C1	
DAC_D12		C6	
DAC_D13		C5	
DAC_D14		C4	
DAC_D15		C3	
DAC_ADR0	68	P15	DAC Address Line to select the DAC channel A or B from one DAC Device.
DAC_'WR00_01'	94	B2	A low active WR transfers data to DAC input register. One write signal for each DAC device respectively for two DAC channel.
DAC_'WR02_03'		B1	
DAC_'WR04_05'		B3	
DAC_'WR06_07'		A3	
DAC_LDAC00_01		B6	Load the DAC output register with contents of the input register. One write signal for each DAC device respectively for two DAC channel.
DAC_LDAC02_03		B5	
DAC_LDAC04_05		A5	
DAC_LDAC06_07		A4	

Second DAC configuration interface is for controlling the DAC channel 9 up to16.

Signal	Bank	Pin	Description
DAC_D16	93	F8	First DAC Data Bus to DAC Device 5 - 8 with DAC Channel 9 - 16
DAC_D17		F6	
DAC_D18		G7	
DAC_D19		G6	
DAC_D20		H8	
DAC_D21		H9	
DAC_D22		F7	
DAC_D23		C8	
DAC_D24		J8	
DAC_D25		D7	
DAC_D26		D8	
DAC_D27		G8	
DAC_D28		E7	
DAC_D29		J9	
DAC_D30		E9	
DAC_D31		F9	
DAC_ADR1	68	F14	DAC Address Line to select the DAC channel A or B from one DAC Device.
DAC_'WR08_09'	93	E6	A low active WR transfers data to DAC input register. One write signal for each DAC device respectively for two DAC channel.
DAC_'WR10_11'		D6	
DAC_'WR12_13'		B7	
DAC_'WR14_15'		A7	
DAC_LDAC08_09		B8	Load the DAC output register with contents of the input register. One write signal for each DAC device respectively for two DAC channel.
DAC_LDAC10_11		A8	
DAC_LDAC12_13		D9	
DAC_LDAC14_15		C9	

Third DAC configuration interface is for controlling the DAC channel 16 up to 23.

Signal	Bank	Pin	Description
DAC_D32	91	H11	First DAC Data Bus to DAC Device 9 - 12 with DAC Channel 17 - 24
DAC_D33		H10	
DAC_D34		F10	
DAC_D35		J11	
DAC_D36		D12	
DAC_D37		E10	
DAC_D38		E11	
DAC_D39		G13	
DAC_D40		G10	
DAC_D41		F12	
DAC_D42		F13	
DAC_D43		G12	
DAC_D44		H13	
DAC_D45		H14	
DAC_D46		E12	
DAC_D47		G11	
DAC_ADR2	68	N15	DAC Address Line to select the DAC channel A or B from one DAC Device.
DAC_'WR16_17'	91	D11	A low active WR transfers data to DAC input register. One write signal for each DAC device respectively for two DAC channel.
DAC_'WR18_19'		C11	
DAC_'WR20_21'		C10	
DAC_'WR22_23'		B10	
DAC_LDAC16_17		B12	Load the DAC output register with contents of the input register. One write signal for each DAC device respectively for two DAC channel.
DAC_LDAC18_19		B11	
DAC_LDAC20_21		A10	
DAC_LDAC22_23		A9	

Fourth DAC configuration interface is for controlling the DAC channel 25 up to 32.

Signal	Bank	Pin	Description
DAC_D48	90	P12	First DAC Data Bus to DAC Device 13 - 16 with DAC Channel 25 - 32
DAC_D49		N11	
DAC_D50		K12	
DAC_D51		P13	
DAC_D52		L14	
DAC_D53		R14	
DAC_D54		P14	
DAC_D55		N12	
DAC_D56		N13	
DAC_D57		N14	
DAC_D58		N10	
DAC_D59		M12	
DAC_D60		L12	
DAC_D61		L13	
DAC_D62		M13	
DAC_D63		M11	
DAC_ADR3	68	R15	DAC Address Line to select the DAC channel A or B from one DAC Device.
DAC_'WR24_25'	90	M10	A low active WR transfers data to DAC input register. One write signal for each DAC device respectively for two DAC channel.
DAC_'WR26_27'		L10	
DAC_'WR28_29'		K11	
DAC_'WR30_31'		K10	
DAC_LDAC24_25		K14	Load the DAC output register with contents of the input register. One write signal for each DAC device respectively for two DAC channel.
DAC_LDAC26_27		J14	
DAC_LDAC28_29		J13	
DAC_LDAC30_31		J12	

The following signals are used for all 16 DAC channels.

Signal	Bank	Pin	Description
DAC_RS#	68	A12	Active low resets all 16 input and output DAC registers. Value depends on DAC_MSB line.
DAC_MSB		D13	**MSB Power-On Reset State.** DAC_MSB = 0 corresponds to zero-scale reset; DAC_MSB = 1 corresponds to midscale reset

Table 8-12: TPCE646 parallel DAC Interface

Please note that the four DAC_ADR lines, DAC_RS#, and DAC_MSB signals are routed through a 1.8 V to 3.3 V level-shifting buffer, which introduces a propagation delay of approximately 1.8 ns to 8.3 ns. This delay must be considered when defining the DAC interface timing in the user MPSoC.

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file "tpce646_xczu11_xxx_ffvc1760.xdc" should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

For a detailed description of the AD5547 parallel interface and the AD5547 function please use the data sheet which describes the whole data transfer, data register and output process and all special characteristics of the DAC.

8.8.4 Programming Hints for AD5547

TPCE646 DAC Channel write to DAC Input Register Decoding.

ADR0	'WR00_01'	'WR02_03'	'WR04_05'	'WR06_07'	DAC Channel
0	0	1	1	1	Channel 0
1	0	1	1	1	Channel 1
0	1	0	1	1	Channel 2
1	1	0	1	1	Channel 3
0	1	1	0	1	Channel 4
1	1	1	0	1	Channel 5
0	1	1	1	0	Channel 6
1	1	1	1	0	Channel 7

ADR1	'WR08_09'	'WR10_11'	'WR12_13'	'WR14_15'	DAC Channel
0	0	1	1	1	Channel 8
1	0	1	1	1	Channel 9
0	1	0	1	1	Channel 10
1	1	0	1	1	Channel 11
0	1	1	0	1	Channel 12
1	1	1	0	1	Channel 13
0	1	1	1	0	Channel 14
1	1	1	1	0	Channel 15

ADR2	'WR16_17'	'WR18_19'	'WR20_21'	'WR22_23'	DAC Channel
0	0	1	1	1	Channel 16
1	0	1	1	1	Channel 17
0	1	0	1	1	Channel 18
1	1	0	1	1	Channel 19
0	1	1	0	1	Channel 20
1	1	1	0	1	Channel 21
0	1	1	1	0	Channel 22
1	1	1	1	0	Channel 23

ADR3	'WR24_25'	'WR26_27'	'WR28_29'	'WR30_31'	DAC Channel
0	0	1	1	1	Channel 24
1	0	1	1	1	Channel 25
0	1	0	1	1	Channel 26
1	1	0	1	1	Channel 27
0	1	1	0	1	Channel 28
1	1	1	0	1	Channel 29
0	1	1	1	0	Channel 30
1	1	1	1	0	Channel 31

TPCE646 DAC Channel LOAD_DAC Register Decoding.

ADR0	'LDAC00_01'	'LDAC02_03'	'LDAC04_05'	'LDAC06_07'	DAC Channel
0	1	0	0	0	Channel 1
1	1	0	0	0	Channel 2
0	0	1	0	0	Channel 3
1	0	1	0	0	Channel 4
0	0	0	1	0	Channel 5
1	0	0	1	0	Channel 6
0	0	0	0	1	Channel 7
1	0	0	0	1	Channel 8

ADR1	'LDAC08_09'	'LDAC10_11'	'LDAC12_13'	'LDAC14_15'	DAC Channel
0	1	0	0	0	Channel 8
1	1	0	0	0	Channel 9
0	0	1	0	0	Channel 10
1	0	1	0	0	Channel 11
0	0	0	1	0	Channel 12
1	0	0	1	0	Channel 13
0	0	0	0	1	Channel 14
1	0	0	0	1	Channel 15

ADR2	'LDAC16_17'	'LDAC18_19'	'LDAC20_21'	'LDAC22_23'	DAC Channel
0	1	0	0	0	Channel 16
1	1	0	0	0	Channel 17
0	0	1	0	0	Channel 18
1	0	1	0	0	Channel 19
0	0	0	1	0	Channel 20
1	0	0	1	0	Channel 21
0	0	0	0	1	Channel 22
1	0	0	0	1	Channel 23

ADR3	'LDAC24_25'	'LDAC26_27'	'LDAC28_29'	'LDAC30_31'	DAC Channel
0	1	0	0	0	Channel 24
1	1	0	0	0	Channel 25
0	0	1	0	0	Channel 26
1	0	1	0	0	Channel 27
0	0	0	1	0	Channel 28
1	0	0	1	0	Channel 29
0	0	0	0	1	Channel 30
1	0	0	0	1	Channel 31

8.9 LVDS Front I/O Lines

The TPCE646 provides four LVDS lanes on the front I/O connector. These are 4 channels with M-LVDS buffers and a data rate of up to 50Mbps.

The connection between the MPSoC and the M-LVDS buffer is implemented through a transparent 1.8 V to 3.3 V voltage translator. It must be taken into account that this translator introduces a design-related propagation delay of approximately 1.3 ns to 8.4 ns, depending on the direction of signal flow and the connected load.

Each LVDS lane has its own 100 Ω termination resistor. It is important to ensure that a maximum of 2 termination resistors are present in an LVDS network.

On the User MPSoC each Front I/O LVDS channel consists of four signals.

D : Driver – Data Output
R : Receiver – Data Input
DE : Driver enable
RE : Receiver enable

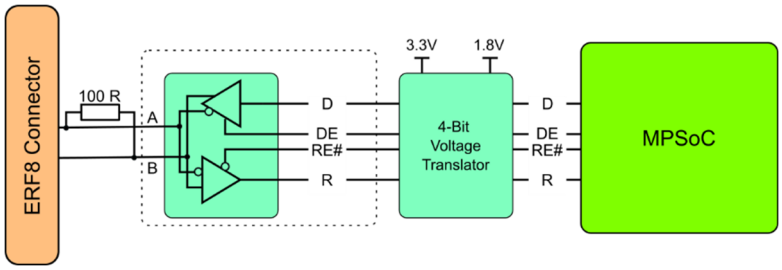


Figure 8-14 : One M-LVDS Lane

Signal Name	Bank	Pin Number	Direction	Description
IO_D0	66	AL17	OUT	Driver Output
IO_D1		AP17	OUT	
IO_D2		AY14	OUT	
IO_D3		AY13	OUT	
IO_DE0		AN16	OUT	Driver Enable pin High = Enable Low = Disable
IO_DE1		AU13	OUT	
IO_DE2		AY12	OUT	
IO_DE3		BB10	OUT	
IO_R0		AY15	IN	Receiver Input
IO_R1		AW15	IN	
IO_R2		BB15	IN	
IO_R3		BB11	IN	
IO_'RE'0		AW14	OUT	Receiver Enable pin High = Disable Low = Enable
IO_'RE'1		AV13	OUT	
IO_'RE'2		BB14	OUT	
IO_'RE'3		BA12	OUT	

Table 8-13 : LVDS Front I/O Lines

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file "tpce646_xczu11_xxx_ffvc1760.xdc" should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

8.10 Memory

The TPCE646 is equipped with two 4 GB, 64 bit wide DDR4 SDRAM and two 512 Mbit non-volatile SPI-Flash. The SPI-Flash can also be used as the User MPSoC configuration memory.

There are 4GB DDR4 interfaces connected to the PL and the PS part of the User MPSoC.

8.10.1 PL DDR4 SDRAM

The TPCE646 provides four (96-ball) DDR4 memory devices. The memory is accessible through a Memory Interface Controller Block IP in bank 69, 70 and 71of the User MPSoC.

Signal	MPSoC Pin Number	Termination
PL_A0	C36	39 Ω VTT
PL_A1	B35	39 Ω VTT
PL_A2	B36	39 Ω VTT
PL_A3	A35	39 Ω VTT
PL_A4	A37	39 Ω VTT
PL_A5	B33	39 Ω VTT
PL_A6	B41	39 Ω VTT
PL_A7	C33	39 Ω VTT
PL_A8	B42	39 Ω VTT
PL_A9	D34	39 Ω VTT
PL_A10	B37	39 Ω VTT
PL_A11	C42	39 Ω VTT
PL_A12	C34	39 Ω VTT
PL_A13	B32	39 Ω VTT
PL_A14	A38	39 Ω VTT
PL_A15	D33	39 Ω VTT
PL_A16	A34	39 Ω VTT
PL_'ACT'	B30	39 Ω VTT
PL_'ALERT'	A30	49.9 Ω 1.2 V
PL_BA0	B40	39 Ω VTT
PL_BA1	A33	39 Ω VTT
PL_BG0	C37	39 Ω VTT
PL_CK_-	A40	33 Ω 1.2V
PL_CK_+	A39	33 Ω 1.2 V

Signal	MPSoC Pin Number	Termination
PL_CKE	D29	39 Ω VTT
PL_'CS'	E29	39 Ω VTT
PL_'DM_DBI_0'	P18	ODT
PL_'DM_DBI_1'	K19	ODT
PL_'DM_DBI_2'	G22	ODT
PL_'DM_DBI_3'	D19	ODT
PL_'DM_DBI_4'	P26	ODT
PL_'DM_DBI_5'	K27	ODT
PL_'DM_DBI_6'	G26	ODT
PL_'DM_DBI_7'	C28	ODT
PL_DQ0	M18	ODT
PL_DQ1	L18	ODT
PL_DQ2	M20	ODT
PL_DQ3	L19	ODT
PL_DQ4	P21	ODT
PL_DQ5	N21	ODT
PL_DQ6	M22	ODT
PL_DQ7	M21	ODT
PL_DQ8	L20	ODT
PL_DQ9	K20	ODT
PL_DQ10	K21	ODT
PL_DQ11	J21	ODT
PL_DQ12	H20	ODT
PL_DQ13	H19	ODT
PL_DQ14	H21	ODT
PL_DQ15	G20	ODT
PL_DQ16	F23	ODT
PL_DQ17	F22	ODT
PL_DQ18	F19	ODT
PL_DQ19	E19	ODT
PL_DQ20	E21	ODT
PL_DQ21	D21	ODT
PL_DQ22	E22	ODT
PL_DQ23	D22	ODT
PL_DQ24	C20	ODT
PL_DQ25	B20	ODT
PL_DQ26	A20	ODT
PL_DQ27	A19	ODT
PL_DQ28	B22	ODT

Signal	MPSoC Pin Number	Termination
PL_DQ29	A22	ODT
PL_DQ30	B23	ODT
PL_DQ31	A23	ODT
PL_DQ32	M25	ODT
PL_DQ33	L25	ODT
PL_DQ34	N24	ODT
PL_DQ35	N25	ODT
PL_DQ36	P23	ODT
PL_DQ37	N23	ODT
PL_DQ38	M23	ODT
PL_DQ39	L23	ODT
PL_DQ40	K26	ODT
PL_DQ41	J26	ODT
PL_DQ42	J23	ODT
PL_DQ43	J24	ODT
PL_DQ44	H25	ODT
PL_DQ45	H26	ODT
PL_DQ46	H24	ODT
PL_DQ47	G25	ODT
PL_DQ48	F25	ODT
PL_DQ49	E25	ODT
PL_DQ50	F27	ODT
PL_DQ51	F28	ODT
PL_DQ52	D27	ODT
PL_DQ53	D28	ODT
PL_DQ54	F24	ODT
PL_DQ55	E24	ODT
PL_DQ56	A27	ODT
PL_DQ57	A28	ODT
PL_DQ58	C26	ODT
PL_DQ59	B27	ODT
PL_DQ60	C24	ODT
PL_DQ61	C25	ODT
PL_DQ62	A24	ODT
PL_DQ63	A25	ODT
PL_DQS_0-	N19	ODT
PL_DQS_0+	N20	ODT
PL_DQS_1-	J22	ODT
PL_DQS_1+	K22	ODT

Signal	MPSoC Pin Number	Termination
PL_DQS_2-	E20	ODT
PL_DQS_2+	F20	ODT
PL_DQS_3-	B21	ODT
PL_DQS_3+	C21	ODT
PL_DQS_4-	K24	ODT
PL_DQS_4+	L24	ODT
PL_DQS_5-	G23	ODT
PL_DQS_5+	H23	ODT
PL_DQS_6-	E27	ODT
PL_DQS_6+	E26	ODT
PL_DQS_7-	B26	ODT
PL_DQS_7+	B25	ODT
PL_ODT	C29	39 Ω VTT
PL_PAR	C35	39 Ω VTT
PL_'RESET'	A29	4k7 PullDown

Table 8-14 : PL DDR4 SDRAM Interface

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file “tpce646_xczu11_xxx_ffvc1760.xdc” should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

For details regarding the DDR4 SDRAM interface, please refer to AMD Memory Interface Generator Documentation. AMD PG150: *UltraScale Architecture-Based FPGAs Memory IPv1.4*.

8.10.2 PS DDR4 SDRAM

The TPCE646 provides four (96-ball) DDR4 memory devices. The memory is accessible through the User MPSoC PS Memory Interface on bank 505.

Signal	MPSoC Pin Number	Termination
PS_A0	BA38	39 Ω VTT
PS_A1	BB36	39 Ω VTT
PS_A2	BA35	39 Ω VTT
PS_A3	BB35	39 Ω VTT
PS_A4	BB38	39 Ω VTT
PS_A5	AY35	39 Ω VTT
PS_A6	AP37	39 Ω VTT
PS_A7	AT36	39 Ω VTT
PS_A8	AR35	39 Ω VTT
PS_A9	AT35	39 Ω VTT
PS_A10	AU35	39 Ω VTT
PS_A11	AU36	39 Ω VTT
PS_A12	AW36	39 Ω VTT
PS_A13	AW37	39 Ω VTT
PS_A14	AW35	39 Ω VTT
PS_A15	AW34	39 Ω VTT
PS_A16	AR34	39 Ω VTT
PS_'ACT'	AR37	39 Ω VTT
PS_'ALERT'	AM36	49.9 Ω 1.2 V
PS_BA0	AN37	39 Ω VTT
PS_BA1	AN36	39 Ω VTT
PS_BG0	AP36	39 Ω VTT
PS_CK_-	BA37	33 Ω 1.2V
PS_CK_+	BA36	33 Ω 1.2 V
PS_CKE	AY38	39 Ω VTT
PS_'CS'	AY37	Not connected
PS_'DM_DBI_0'	AY29	ODT
PS_'DM_DBI_1'	AY34	ODT
PS_'DM_DBI_2'	AR29	ODT
PS_'DM_DBI_3'	AR33	ODT
PS_'DM_DBI_4'	AR39	ODT
PS_'DM_DBI_5'	AL36	ODT
PS_'DM_DBI_6'	AU39	ODT
PS_'DM_DBI_7'	AL42	ODT
PS_DQ0	AV29	ODT

Signal	MPSoC Pin Number	Termination
PS_DQ1	AW30	ODT
PS_DQ2	AW29	ODT
PS_DQ3	AW31	ODT
PS_DQ4	BB31	ODT
PS_DQ5	BB30	ODT
PS_DQ6	BB29	ODT
PS_DQ7	BA31	ODT
PS_DQ8	BB33	ODT
PS_DQ9	BA32	ODT
PS_DQ10	BA33	ODT
PS_DQ11	BB34	ODT
PS_DQ12	AV31	ODT
PS_DQ13	AW32	ODT
PS_DQ14	AV32	ODT
PS_DQ15	AV33	ODT
PS_DQ16	AN29	ODT
PS_DQ17	AP29	ODT
PS_DQ18	AP30	ODT
PS_DQ19	AP31	ODT
PS_DQ20	AT31	ODT
PS_DQ21	AU30	ODT
PS_DQ22	AU31	ODT
PS_DQ23	AU29	ODT
PS_DQ24	AV34	ODT
PS_DQ25	AU33	ODT
PS_DQ26	AT33	ODT
PS_DQ27	AU34	ODT
PS_DQ28	AN33	ODT
PS_DQ29	AP32	ODT
PS_DQ30	AN32	ODT
PS_DQ31	AN31	ODT
PS_DQ32	AN41	ODT
PS_DQ33	AN42	ODT
PS_DQ34	AP42	ODT
PS_DQ35	AP41	ODT
PS_DQ36	AN39	ODT
PS_DQ37	AR38	ODT
PS_DQ38	AP39	ODT
PS_DQ39	AN38	ODT

Signal	MPSoC Pin Number	Termination
PS_DQ40	AL37	ODT
PS_DQ41	AL38	ODT
PS_DQ42	AK38	ODT
PS_DQ43	AK39	ODT
PS_DQ44	AJ36	ODT
PS_DQ45	AL35	ODT
PS_DQ46	AJ35	ODT
PS_DQ47	AK35	ODT
PS_DQ48	AR42	ODT
PS_DQ49	AT41	ODT
PS_DQ50	AT42	ODT
PS_DQ51	AT40	ODT
PS_DQ52	AV42	ODT
PS_DQ53	AV41	ODT
PS_DQ54	AV39	ODT
PS_DQ55	AV38	ODT
PS_DQ56	AM39	ODT
PS_DQ57	AM38	ODT
PS_DQ58	AM40	ODT
PS_DQ59	AM41	ODT
PS_DQ60	AJ42	ODT
PS_DQ61	AK42	ODT
PS_DQ62	AK40	ODT
PS_DQ63	AK41	ODT
PS_DQS_0-	BA30	ODT
PS_DQS_0+	AY30	ODT
PS_DQS_1-	AY33	ODT
PS_DQS_1+	AY32	ODT
PS_DQS_2-	AT30	ODT
PS_DQS_2+	AR30	ODT
PS_DQS_3-	AT32	ODT
PS_DQS_3+	AR32	ODT
PS_DQS_4-	AR40	ODT
PS_DQS_4+	AP40	ODT
PS_DQS_5-	AK37	ODT
PS_DQS_5+	AJ37	ODT
PS_DQS_6-	AU41	ODT
PS_DQS_6+	AU40	ODT
PS_DQS_7-	AL41	ODT

Signal	MPSoC Pin Number	Termination
PS_DQS_7+	AL40	100 Ω
PS_ODT	BB39	39 Ω VTT
PS_PAR	AM35	39 Ω VTT
PS_DDR_ZQ	AN34	Not connected

Table 8-15 : PS DDR4 SDRAM Interface

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file "tpce646_xczu11_xxx_ffvc1760.xdc" should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

For details regarding the DDR4 SDRAM interface, please refer to AMD Memory Interface Generator Documentation. AMD PG150: *UltraScale Architecture-Based FPGAs Memory IPv1.4*.

8.10.3 SPI-Flash

The TPCE646 features two Micron MT25QU512 512 Mbit serial Flash memories. These Flash memories are used as the default configuration source for the User MPSoC configuration. After configuration, they remain accessible from the User MPSoC, allowing them to be used for code or user data storage.

The two SPI Flash memories are connected to the User MPSoC configuration interface via a (x4) SPI interface. Together, they form a dual parallel QSPI (QSPI32) configuration interface, which corresponds to the default configuration mode. If a different configuration mode is desired, it can be selected via a DIP switch (see chapter 4.14.1Hardware Power Up Configuration).

User MPSoC PS Signal	Bank	TPCE646 Signal	Pin	Description
PS_MIO0	500	PS_MIO0_SCLK	AM33	Serial Clock
PS_MIO5		PS_MIO5_SS	AL32	Slave Select
PS_MIO3		PS_MIO3_IO3	AM30	MISO[3] – D03
PS_MIO2		PS_MIO2_IO2	AM31	MISO[2] – D02
PS_MIO1		PS_MIO1_IO1	AM29	Serial Data output (DIN) / MISO[1]
PS_MIO4		PS_MIO4_IO0	AL33	Serial Data input (MOSI) / MISO[0]
PS_MIO12		PS_MIO12	AJ34	Upper Serial Clock
PS_MIO7		PS_MIO7	AL30	Upper Slave Select
PS_MIO11		PS_MIO11	AK32	Upper MISO[3] – D03
PS_MIO10		PS_MIO10	AK30	Upper MISO[2] – D02
PS_MIO9		PS_MIO9	AK34	Upper Serial Data output (DIN) / MISO[1]
PS_MIO8		PS_MIO8	AK33	Upper Serial Data input (MOSI) / MISO[0]

Table 8-16 : User MPSoC QSPI32 Flash Interface

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file “tpce646_xczu11_xxx_ffvc1760.xdc” should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

8.10.4 I2C - EEPROM

The TPCE646 provides a STMicroelectronics M24128 (128 Kbit) I2C-Compatible (2-wire) Serial EEPROM.

This EEPROM is used as ADC and DAC correction data memory. In addition, for each correction data set ADC Input and DAC Output the corresponding voltage range of ADC inputs and DAC outputs is also stored.

During factory test the analog input and output channel gain error and offset error are determined. For each device, 16 bit correction values are stored to the I2C EEPROM. These correction values have been determined with TEWS test environment. If system specific correction values are needed, the determination of the correction values of the entire system can be done by the user and the I2C EEPROM could be used as a possible memory to store the custom correction values.

Both the PL (Programmable Logic) and the PS (Processing System) parts of the User MPSoC have a redundant interface, connected to this I2C bus.

As usual for the I2C interface the two pins must be realized as open drain buffers. Additionally, it must always be ensured that only one of the two User MPSoC parts is active/master at a time.

MPSoC PS Signal	Bank	TPCE646 Signal	Pin	Description
PS_MIO26	501	USER_SCL	L27	PS Serial clock
PS_MIO27		USER_SDA	L29	PS Serial data
IO_L1P	66	USER_SCL	AY17	PL Serial clock
IO_L1N		USER_SDA	BA17	PL Serial data

Table 8-17: MPSoC I2C EEPROM Connections

For using the serial I2C interface between the User MPSoC and the I2C EEPROM please see the STMicroelectronics M24128 data sheet which describes the serial communication process.

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file “tpce646_xczu11_xxx_ffvc1760.xdc” should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

8.10.4.1 ADC and DAC Correctable Errors

There are two errors affecting the accuracy of the ADC and DAC that can be corrected using the factory determined correction values. The correction values are obtained during factory test and are stored in an on-board I2C EEPROM as 2-complement 16 bit values in the range from -32768 to +32767. To achieve a higher accuracy, they are scaled to ¼ LSB.

DAC Offset Error:

For the DAC, this is the data value that is required to produce a zero-voltage output signal. This error is corrected by subtracting the offset from the DAC data value.

ADC Offset Error:

The offset error is the data value when converting with the input connected to its own ground in single-ended mode, or with shorted inputs in differential mode. This error is corrected by subtracting the known error from the reading.

DAC Gain Error:

The gain error is the difference between the ideal gain and the actual gain of the DAC. It is corrected by multiplying the DAC data value with a correction factor.

ADC Gain Error:

The gain error is the difference between the ideal gain and the actual gain of the programmable gain amplifier and the ADC. This error is corrected by multiplying the reading with a correction factor.

8.10.4.2 ADC Correction Values

The 8 ADC channels are realized with two octal LTC2323-16 ADC devices.

For each ADC channel and input voltage ranges a 16 bit Offset correction and a 16 bit gain correction value is stored.

I2C EEPROM Address	Description	Size (bit)
	ADC Range 0	
0x000	ADC Channel 0, $Offset_{Corr}$ High Byte	8
0x001	ADC Channel 0, $Offset_{Corr}$ Low Byte	8
0x002	ADC Corretion 0, $Gain_{Corr}$ High Byte	8
0x003	ADC Corretion 0, $Gain_{Corr}$ Low Byte	8
0x004	ADC Channel 1, $Offset_{Corr}$ High Byte	8
0x005	ADC Channel 1, $Offset_{Corr}$ Low Byte	8
0x006	ADC Corretion 1, $Gain_{Corr}$ High Byte	8
0x007	ADC Corretion 1, $Gain_{Corr}$ Low Byte	8
. . .		
0x01C	ADC Channel 7, $Offset_{Corr}$ High Byte	8
0x01D	ADC Channel 7, $Offset_{Corr}$ Low Byte	8
0x01E	ADC Corretion 7, $Gain_{Corr}$ High Byte	8
0x01F	ADC Corretion 7, $Gain_{Corr}$ Low Byte	8
0x020 .. 0x03E	Reserved	256

Table 8-18: ADC Correction Values

8.10.4.3 DAC Correction Values

The 32 DAC channels are realized with sixteen dual AD5547 DAC devices.

For each DAC channel three correction value sets are stored. One set for each DAC Output Voltage Range Selection (±10V range (default value), ±5V range and ±2.5V range).
Each correction value set consists of a 16 bit value for Offset correction and Gain correction for each channel.

I2C EEPROM Address	Description	Size (bit)
DAC Range 0 (±10V)		
0x040	DAC Range 0 Channel 0 $Offset_{corr}$ High Byte	8
0x041	DAC Range 0 Channel 0 $Offset_{corr}$ Low Byte	8
0x042	DAC Range 0 Channel 0 $Gain_{corr}$ High Byte	8
0x043	DAC Range 0 Channel 0 $Gain_{corr}$ Low Byte	8
0x044	DAC Range 0 Channel 1 $Offset_{corr}$ High Byte	8
0x045	DAC Range 0 Channel 1 $Offset_{co}$ Low Byte	8
0x046	DAC Range 0 Channel 1 $Gain_{corr}$ High Byte	8
0x047	DAC Range 0 Channel 1 $Gain_{corr}$ Low Byte	8
…		
0x0BC	DAC Range 0 Channel 31 $Offset_{corr}$ High Byte	8
0x0BE	DAC Range 0 Channel 3 $Offset_{corr}$ Low Byte	8
0x0BE	DAC Range 0 Channel 31 $Gain_{corr}$ High Byte	8
0x0BF	DAC Range 0 Channel 31 $Gain_{corr}$ Low Byte	8
DAC Range 1 (±5V)		
0x0C0	DAC Range 1 Channel 0 $Offset_{corr}$ High Byte	8
0x0C1	DAC Range 1 Channel 0 $Offset_{corr}$ Low Byte	8
0x0C2	DAC Range 1 Channel 0 $Gain_{corr}$ High Byte	8
0x0C3	DAC Range 1 Channel 0 $Gain_{corr}$ Low Byte	8
0x0C4	DAC Range 1 Channel 1 $Offset_{corr}$ High Byte	8
0x0C5	DAC Range 1 Channel 1 $Offset_{corr}$ Low Byte	8
0x0C6	DAC Range 1 Channel 1 $Gain_{corr}$ High Byte	8
0x0C7	DAC Range 1 Channel 1 $Gain_{corr}$ Low Byte	8
…		
0x13C	DAC Range 1 Channel 31 $Offset_{corr}$ High Byte	8
0x13D	DAC Range 1 Channel 31 $Offset_{corr}$ Low Byte	8
0x13E	DAC Range 1 Channel 31 $Gain_{corr}$ High Byte	8
0x13F	DAC Range 1 Channel 31 $Gain_{corr}$ Low Byte	8
DAC Range 2 (±2.5V)		
0x140	DAC Range 2 Channel 0 $Offset_{corr}$ High Byte	8
0x141	DAC Range 2 Channel 0 $Offset_{corr}$ Low Byte	8
0x142	DAC Range 2 Channel 0 $Gain_{corr}$ High Byte	8
0x143	DAC Range 2 Channel 0 $Gain_{corr}$ Low Byte	8
0x144	DAC Range 2 Channel 1 $Offset_{corr}$ High Byte	8

0x145	DAC Range 2 Channel 1 $Offset_{corr}$ Low Byte	8
0x146	DAC Range 2 Channel 1 $Gain_{corr}$ High Byte	8
0x147	DAC Range 2 Channel 1 $Gain_{corr}$ Low Byte	8
…		
0x1BC	DAC Range 2 Channel 31 $Offset_{corr}$ High Byte	8
0x1BD	DAC Range 2 Channel 31 $Offset_{corr}$ Low Byte	8
0x1BE	DAC Range 2 Channel 31 $Offset_{corr}$ High Byte	8
0x1BF	DAC Range 2 Channel 31 $Offset_{corr}$ Low Byte	8

Table 8-19: DAC Correction Data Values

8.10.4.4 ADC Data Correction Formula

Please use the total 16 bit data register value for the ADC correction formula.

The basic formula for correcting any ADC reading for the TPCE646 (bipolar input voltage range) is:

$$Value = Reading \cdot \left(1 - \frac{Gain_{corr}}{131072}\right) - \frac{Offset_{corr}}{4}$$

Value is the corrected result.

Reading is the data read from the ADC Data Register.

$Gain_{corr}$ and $Offset_{corr}$ are the ADC correction factors from the Correction Data ROM stored for each programmable gain factor.

The correction values are stored as two's complement 16 bit values in the range -32768 to 32767. For higher accuracy they are scaled to ¼ LSB.

Floating point arithmetic or scaled integer arithmetic is necessary to avoid rounding errors while computing above formula.

8.10.4.5 DAC Data Correction Formula

The basic formula for correcting any DAC value is:

$$Data = Value \cdot \left(1 - \frac{Gain_{corr}}{131072}\right) - \frac{Offset_{corr}}{4}$$

Value is the desired DAC value.

Data is the corrected DAC value that must be send to the DAC.

$Gain_{corr}$ and $Offset_{corr}$ are the DAC correction values from the Correction Data ROM. They are stored separately for each of the 8 DAC channels.

The correction values are stored as two's complement byte wide values in the range from –32768 to +32767. For higher accuracy they are scaled to ¼ LSB.

Floating point arithmetic or scaled integer arithmetic must be used to avoid rounding errors in computing above formula.

8.10.4.6 DAC and ADC voltage ranges

The voltage range for each DAC output and ADC input is composed of two bytes, one high byte and one low byte. Together they provide the 16 bit voltage range in mV.

I2C EEPROM Address	Description	Size (bit)
DAC Range 0		
0x1C0	DAC Output Range 0, Channel 0 High Byte	8
0x1C1	DAC Output Range 0, Channel 0 Low Byte	8
0x1C2	DAC Output Range 0, Channel 1 High Byte	8
0x1C3	DAC Output Range 0, Channel 1 Low Byte	8
0x1C4	DAC Output Range 0, Channel 2 High Byte	8
0x1C5	DAC Output Range 0, Channel 2 Low Byte	8
…		
0x1FE	DAC Output Range 0, Channel 31 High Byte	8
0x1FF	DAC Output Range 0, Channel 31 Low Byte	8
DAC Range 1		
0x200	DAC Output Range 1, Channel 0 High Byte	8
0x201	DAC Output Range 1, Channel 0 Low Byte	8
0x202	DAC Output Range 1, Channel 1 High Byte	8
0x203	DAC Output Range 1, Channel 1 Low Byte	8
0x204	DAC Output Range 1, Channel 2 High Byte	8
0x205	DAC Output Range 1, Channel 2 Low Byte	8
…		
0x23E	DAC Output Range 1, Channel 31 High Byte	8
0x23F	DAC Output Range 1, Channel 31 Low Byte	8
DAC Range 2		
0x240	DAC Output Range 2, Channel 0 High Byte	8
0x241	DAC Output Range 2, Channel 0 Low Byte	8
0x242	DAC Output Range 2, Channel 1 High Byte	8
0x243	DAC Output Range 2, Channel 1 Low Byte	8
0x244	DAC Output Range 2, Channel 2 High Byte	8
0x245	DAC Output Range 2, Channel 2 Low Byte	8
0x27E	DAC Output Range 2, Channel 7 High Byte	8
0x27F	DAC Output Range 2, Channel 7 Low Byte	8
ADC Range 0		
0x280	ACD Input Voltage Range 0, Channel 0 High Byte	8
0x281	ACD Input Voltage Range 0, Channel 0 Low Byte	8
0x282	ACD Input Voltage Range 0, Channel 1 High Byte	8
0x283	ACD Input Voltage Range 0, Channel 1 Low Byte	8
0x284	ACD Input Voltage Range 0, Channel 2 High Byte	8

0x285	ACD Input Voltage Range 0, Channel 2 Low Byte	8
…		
0x28E	ACD Input Voltage Range 0, Channel 7 High Byte	8
0x28F	ACD Input Voltage Range 0, Channel 7 Low Byte	8
0x290 .. 0x7EF	Reserved	1376

Table 8-20: ADC and DAC voltage ranges

8.10.4.7 TPCE646 MAC Address Information

The MAC address is required for the optional User MPSoC Ethernet interface can be found in this memory section.

I2C EEPROM Address	Description	Size (bit)
0x7F0	MAC Address Information Area Example: **00:01:06:00:C2:1D**	48

Table 8-21: Version of EEPROM data structure

8.10.4.8 Version of EEPROM data structure

In the first versions of TPCE646 only the correction data were stored. A version register is used to identify whether the voltage ranges are also present.

I2C EEPROM Address	Description	Size (bit)
0x7FF	EEPROM data structure Version 0x00: Only the ADC and DAC correction data are available. 0x01: ADC and DAC correction data and voltage range data are available.	8

Table 8-22: Version of EEPROM data structure

8.11 Rear I/O Interface

The rear I/O pins of the TPCE646 are directly routed to the User MPSoC, with their functionality determined by the User MPSoC configuration. Sixteen rear I/O signals (eight differential pairs) are clock-capable on the User MPSoC. Additionally, two individual User MPSoC signals are provided as an I2C bus via the Samtec rear I/O connector, both supporting a maximum voltage level of 1.8V.

The User MPSoC VCCO voltage for rear I/O is set to 1.8V, allowing only 1.8V I/O standards such as LVCMOS18 and LVDS to be used with the TPCE646 rear I/O interface.

Signal Name	Pin Number	Direction	IO Standard for BRD	Clock Capable
REAR_IO0-	AK19	IN/OUT	LVDS	-
REAR_IO0+	AK20	IN/OUT	LVDS	-
REAR_IO1-	AJ20	IN/OUT	LVDS	-
REAR_IO1+	AJ21	IN/OUT	LVDS	-
REAR_IO2-	AT21	IN/OUT	LVDS	yes
REAR_IO2+	AT22	IN/OUT	LVDS	yes
REAR_IO3-	AU19	IN/OUT	LVDS	yes
REAR_IO3+	AT20	IN/OUT	LVDS	yes
REAR_IO4-	AN19	IN/OUT	LVDS	-
REAR_IO4+	AM19	IN/OUT	LVDS	-
REAR_IO5-	AM20	IN/OUT	LVDS	-
REAR_IO5+	AM21	IN/OUT	LVDS	-
REAR_IO6-	AK22	IN/OUT	LVDS	-
REAR_IO6+	AJ22	IN/OUT	LVDS	-
REAR_IO7-	AL21	IN/OUT	LVDS	-
REAR_IO7+	AL22	IN/OUT	LVDS	-
REAR_IO8-	AR19	IN/OUT	LVDS	-
REAR_IO8+	AP19	IN/OUT	LVDS	-
REAR_IO9-	AR20	IN/OUT	LVDS	-
REAR_IO9+	AP20	IN/OUT	LVDS	-
REAR_IO10-	AV21	IN/OUT	LVDS	yes
REAR_IO10+	AU21	IN/OUT	LVDS	yes
REAR_IO11-	AV19	IN/OUT	LVDS	yes
REAR_IO11+	AU20	IN/OUT	LVDS	yes
REAR_IO12-	AP22	IN/OUT	LVDS	-
REAR_IO12+	AN22	IN/OUT	LVDS	-
REAR_IO13-	AN23	IN/OUT	LVDS	-
REAR_IO13+	AM23	IN/OUT	LVDS	-
REAR_IO14-	AP21	IN/OUT	LVDS	-
REAR_IO14+	AN21	IN/OUT	LVDS	-
REAR_IO15-	AW19	IN/OUT	LVDS	-
REAR_IO15+	AW20	IN/OUT	LVDS	-

REAR_IO16-	AL23	IN/OUT	LVDS	-
REAR_IO16+	AK23	IN/OUT	LVDS	-
REAR_IO17-	AN26	IN/OUT	LVDS	-
REAR_IO17+	AM26	IN/OUT	LVDS	-
REAR_IO18-	AT26	IN/OUT	LVDS	yes
REAR_IO18+	AT25	IN/OUT	LVDS	yes
REAR_IO19-	AU26	IN/OUT	LVDS	yes
REAR_IO19+	AU25	IN/OUT	LVDS	yes
REAR_IO20-	AP25	IN/OUT	LVDS	-
REAR_IO20+	AP24	IN/OUT	LVDS	-
REAR_IO21-	AT23	IN/OUT	LVDS	-
REAR_IO21+	AR23	IN/OUT	LVDS	-
REAR_IO22-	AP27	IN/OUT	LVDS	-
REAR_IO22+	AN27	IN/OUT	LVDS	-
REAR_IO23-	AN28	IN/OUT	LVDS	-
REAR_IO23+	AM28	IN/OUT	LVDS	-
REAR_IO24-	AV23	IN/OUT	LVDS	-
REAR_IO24+	AU23	IN/OUT	LVDS	-
REAR_IO25-	AW22	IN/OUT	LVDS	-
REAR_IO25+	AV22	IN/OUT	LVDS	-
REAR_IO26-	AT27	IN/OUT	LVDS	yes
REAR_IO26+	AR27	IN/OUT	LVDS	yes
REAR_IO27-	AR25	IN/OUT	LVDS	yes
REAR_IO27+	AR24	IN/OUT	LVDS	yes
REAR_IO28-	BA20	IN/OUT	LVDS	-
REAR_IO28+	AY20	IN/OUT	LVDS	-
REAR_IO29-	AY24	IN/OUT	LVDS	-
REAR_IO29+	AW24	IN/OUT	LVDS	-
REAR_IO30-	AW26	IN/OUT	LVDS	-
REAR_IO30+	AV26	IN/OUT	LVDS	-
REAR_IO31-	AV28	IN/OUT	LVDS	-
REAR_IO31+	AU28	IN/OUT	LVDS	-
REAR_SCL	AP26	OUT	LVCMOS18	-
REAR_SDA	AW25	IN/OUT	LVCMOS18	-

Table 8-23 : Digital Rear I/O Interface

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, TEWS Board Reference Design constraint file “tpce646_xczu11_xxx_ffvc1760.xdc” should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

8.12 User MPSoC I2C Bus

Various functions and settings on the TPCE646 are configured and controlled by the BMC via an I2C bus. After the power up phase, this bus is also available to the User MPSoC. With the default configuration, only the Correction Data EEPROM can be accessed. If access to the two other I2C buses of the TPCE646 is to be enabled, the board configuration must be changed via DIP switch S2 (see chapter **Hardware Power Up Configuration**).

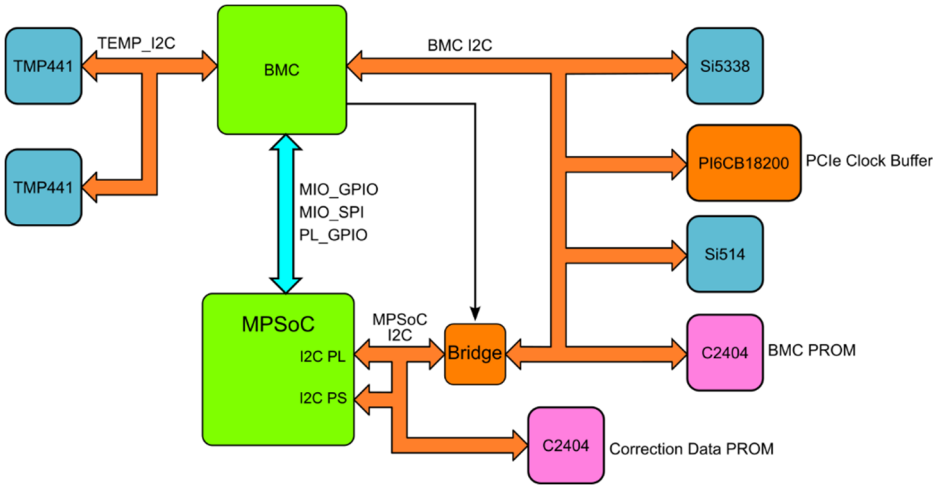


Figure 8-15 : User MPSoC I2C to BMC I2C Bridge

For pin assignment, see section 8.10.4

In I2C communication, each device on the bus has a unique I2C address. This address is used by the master device to communicate with a specific slave device. The address is typically 7-bit wide. The addresses on the TPCE646 are fix.

I2C Device	Device Type	I2C Device Address (7 bit)	Description
Correction Data PROM	M24128	0b1010 001	For a detailed explanation of accesses and functionality, refer to the corresponding datasheet of the component.
BMC PROM	M24128	0b1010 000	
Clock Generator	SI5338	0b1110 000	
Any-Frequency I2C programmable XO	SI514	0b0101 010	
Temperatur Sensor	TMP441	0b0011 100	
Temperatur Sensor I/O	TMP441	0b0011 101	
PCIe Clock Buffer	PI6CB18200	0b1101 101	

Table 8-24: MPSoC I2C Bus

Do not change the SI5338 Output driver properties like “Format and Voltage”

Channel 0 must be 1.8 V LVDS

Channel 1 must be 1.8 V LVDS

Channel 2 must be 1.8 V LVDS

Channel 4 must be 1.8 V LVDS

Do not change Si5338 Core VDD or I2C Bus Voltage

Core VDD = 3.3 V

I2C Bus Voltage = 2.5 V or 3.3 V

8.13 MPSoC UART

A USB to UART interface is provided as a possible debug interface between the user User MPSoC and a debug system.

The UART interface is realized via a FTDI FT2232H Serial dual UART IC . This component is a USB 2.0 Slave to UART Converter. A micro-USB connector is used as USB connector.

The second UART channel is connected to the Board Management Controller (BMC). This interface is factory reserved and not implemented in the current BMC firmware.

- Data Rate: 480Mb/s
- Channel: 2
- USB-Signals: USB_D+, USB_D-
- UART Signals from ZYNC: TXD, RXD, CTS# and RTS#
- UART Signals from BCC: TXD, RXD, CTS# and RTS#

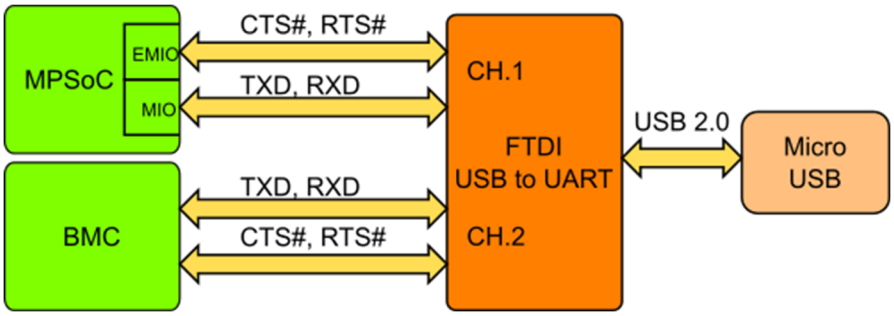


Figure 8-16 : TPCE646 UART to USB Interface

User MPSoC PS / PL Signal	Bank	TPCE646 Signal	Pin	Description
PS_MIO56	502	PS_TXD	AA30	TXD (Transmit Data Output)
PS_MIO57		PS_RXD	AB30	RXD (Receive Data Input)
IO_L10N	64	PS_CTS	AY18	CTS (Clear to Send Input)
IO_L10P		PS_RTS#	AY19	RTS (Request to Send Output)

Table 8-25 : MPSoC UART Pins

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file "tpce646_xczu11_xxx_ffvc1760.xdc" should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

8.14 Si5338 Clock Generator

An SI5338 Clock Generator is used on the TPCE646. It provides all necessary clocks for the User MPSoC.

After power up, the BMC sets up the SI5338 Clock Generator with default settings. These settings are based on peripheral requirements and ensure optimal operation of ADC, DAC, DDR4 memory and GTY interfaces.

- Channel 1: 125 MHz (GTY)
- Channel 2: 200 MHz
- Channel 3: 105 MHz (ADC)
- Channel 4: 125.046892585 MHz (DDR4)

After the initial configuration of the clock generator, it is possible to change the default settings from the User MPSoC by reprogramming the SI5338 device. For this purpose, the SI5338 I2C configuration bus will be accessible from either the programmable logic or processing system.

8.15 Rear I/O RJ45 Ethernet Interface

The TPCE646 provides a rear I/O RJ45 10/100/1000 Mbps Ethernet interface based on a Texas Instruments Ethernet PHY (DP83867IS). It offers the desired 1.8V RGMII interface to the User MPSoC.

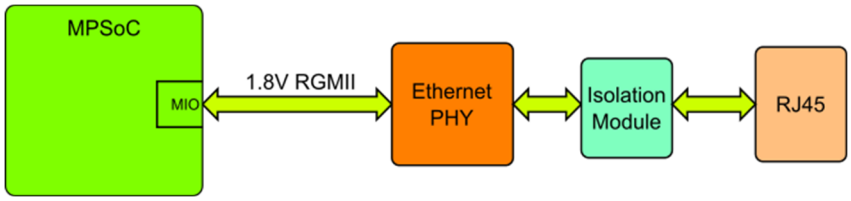


Figure 8-17 : Rear I/O RJ45 Ethernet Interface

- 10/100/1000 Mbps Ethernet IEEE802.3
- RGMII 1.8V Tolerant
- Temperature: -40°C to +85°C
- Standard RJ45 Pin assignment

User MPSoC PS / PL Signal	Bank	TPCE646 Signal	Pin	Description
PS_MIO44	501	RGMII_RX_CLK	R29	For a detail description of the AMD MPSoC RGMII Interface and the Texas Instruments Ethernet PHY (DP83867IS) read the corresponding datasheets.
PS_MIO49		RGMII_RX_CTL	U29	
PS_MIO45		RGMII_RXD0	T29	
PS_MIO46		RGMII_RXD1	U28	
PS_MIO47		RGMII_RXD2	T28	
PS_MIO48		RGMII_RXD3	V30	
PS_MIO38		RGMII_TX_CLK_R	R27	
PS_MIO43		RGMII_TX_CTL_R	R30	
PS_MIO39		RGMII_TXD0_R	P29	

PS_MIO40		RGMII_TXD1_R	P28	
PS_MIO41		RGMII_TXD2_R	P30	
PS_MIO42		RGMII_TXD3_R	T30	
PS_MIO50		GEM1_MDC_R	V29	
PS_MIO51		GEM1_MIO_out_R	W30	

Table 8-26 : MPSoC RGMII Interface Pins

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file "tpce646_xczu11_xxx_ffvc1760.xdc" should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

8.16 MicroSD Card Slot

A microSD card slot is provided as an alternative User MPSoC configuration device.

The selection via which interface (QSPI or SD-Card) the MPSoC is to be configured is made via a DIP switch. The selection must be made before the TPCE646 is powered on.

User MPSoC PS / PL Signal	Bank	TPCE646 Signal	Pin	Description
PS_MIO13	500	PS_MIO13_DATA0_R	AD34	A detailed description of the interface can be found in the AMD Zynq™ UltraScale+™ Device Technical Reference Manual (UG1085).
PS_MIO14		PS_MIO14_DATA1_R	AJ32	
PS_MIO15		PS_MIO15_DATA2_R	AD35	
PS_MIO16		PS_MIO16_DATA3_R	AJ31	
PS_MIO21		PS_MIO21_CMD_R	AF35	
PS_MIO22		PS_MIO22_CLK_R	AH32	
PS_MIO23		PS_MIO23_POW_R	AG35	
PS_MIO24		PS_MIO24_'CD'	AH33	

Table 8-27 : MPSoC RGMII Interface Pins

XILINX / AMD recommends using microSD cards ≤ 32 GB (up to SDHC) with a FAT16 or FAT32 file system. Compatibility with SDXC cards formatted in FAT32 is not guaranteed.

For further information regarding which files are required on the microSD card for configuration, please refer to AMD documentation such as the *"Zynq UltraScale+ MPSoC Software Developer Guide"* (UG1137) or the *"Bootgen User Guide"* (UG1283).

For a detailed overview of all User MPSoC I/O pins and the respective constraints to be set for each pin, the TEWS Board Reference Design constraint file "tpce646_xczu11_xxx_ffvc1760.xdc" should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

8.17 Thermal Management

Forced air cooling is recommended during operation. Without forced air cooling, damage to the device can occur.

To avoid permanent damage of the User MPSoC, the temperature of the Zynq™ UltraScale+™ should be monitored.

All components on the TPCE646 are rated for the industrial temperature range of -40°C to +85°C. The module has several hot spots (input operational amplifier, ADC devices, power supplies) but the main hot-spot is the User MPSoC. The heat sink is directly mounted to the Zynq™ UltraScale+™ die. For maximum heat transfer the heat sink is embodied so large that it covers a lot of the module.

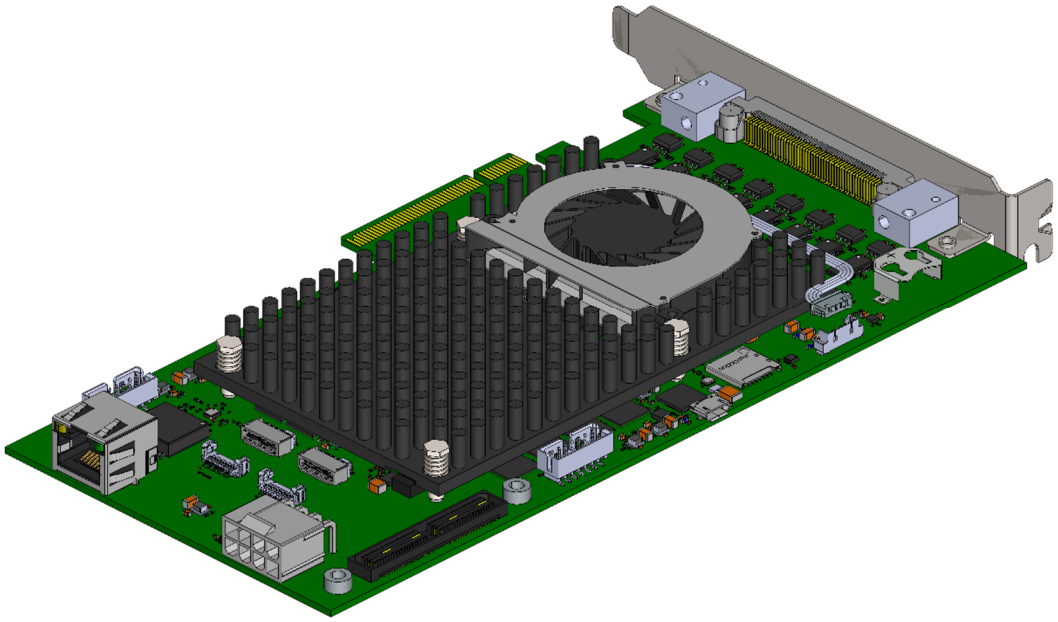


Figure 8-18: TPCE646 with Heatsink

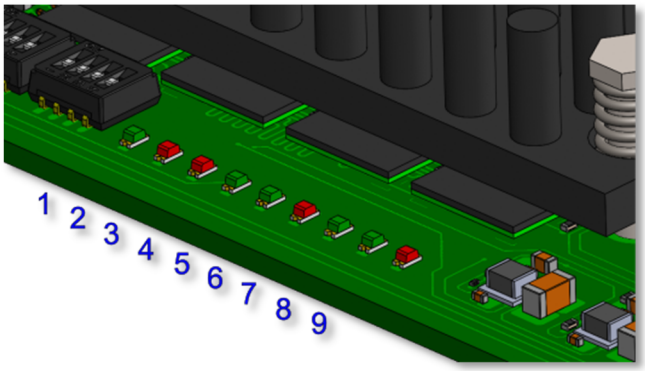
The actual achievable ambient operating temperature range is highly dependent on the MPSoC design, the load of the modules I/O circuitry and the applied cooling method.

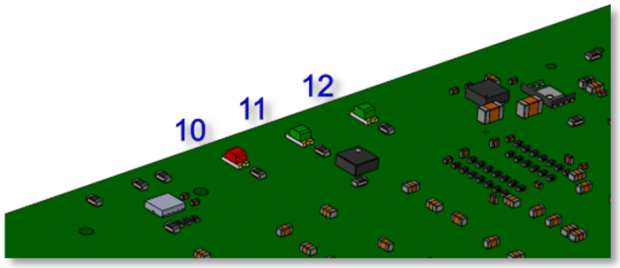
The active fan is set to a fixed fan speed by default. However, this can be adjusted to the conditions via the BMC fan control. The ventilation of the entire system must also be taken into account. If the TPCE646 is installed next to another PCIe card in the system that also generates a lot of heat, this must be considered. A system airflow must carry the waste heat out of the system.

Use the AMD Power Estimator (XPE) or Power Analyzer to determine whether additional cooling requirements such as forced air cooling apply. It is also strongly recommended to use the internal temperature monitoring of the Zynq™ UltraScale+™. Corresponding descriptions can be found in the AMD documentation.

8.18 On-Board Indicators

The TPCE646 provides a couple of board-status LEDs as shown below. These include Power-Good and User MPSoC configuration status indications as well as two general purpose LEDs.





No.	LED	Color	State		Description
1	Power Good	Green	on	On-Board Power Supplies are all ok	Power Good Signal for all on-board power supplies.
2		Red	on	On-Board Power Supplies are not ok	
3	MPSoC INIT	Red	on	INIT state is active	User MPSoC INIT# - Pin LED Indicates configuration status
			off	Device is not configured	
4	MPSoC DONE	Green	off	PL Part of MPSoC is not configured	User MPSoC DONE-Pin LED Indicates successful PL & PS MPSoC configuration
			on	MPSoC is completely configured	
5	BMC STA 1	Green	on	General State is IDLE	BMC Firmware Status A combination of a hard power-on reset, power-good signals from all power supplies, and the SPI configuration between the BMC and the Zynq™MPSoC.
			off	General State is not IDLE	
6	BMC FAIL	Red	on	Global Power Fail	Currently only the display shows a power fail. Further functions possible.
			off	Currently no problem	
7	BMC STA 0	Green	on	Setup Done	BMC internal Status indicator for SI5338 Clock Generator Setup
			off	Setup in Progress or not possible	
8	BMC Power Good	Green	on	BMC Main Power Supplies are all ok	BMC Power Good Signal for first Power state on-board power supplies.
9		Red	on	BMC Main Power Supplies are not ok	
10	TEMP ALERT	Red	on	Temperature has exceeded the limit value	This alarm combines temperature alerts from the board, I/O areas, and the four DAC reference devices. The limits for the alarm are Lower Limit = -40°C Upper Limit = +85°C
			off	Temperature is below the limit value	

11	GPIO LED 0	Green	-	-	Configuration MPSoC depends ant
12	GPIO LED 1	Green	-	-	

Table 8-28: Board-Status and User LEDs

8.18.1 User MPSoC LED Pinning

General purpose I/O connected to the User MPSoC.

Signal	Bank	VCCO	Pin	Description
USER_LED0	68	1.8 V	A15	2x green on-board LEDs
USER_LED1			B16	

Table 8-29: TPCE646 User On-Board Indicators

For a detailed overview of all User MPSoC I/O pins and the respective constrains to be set for each pin, the TEWS Board Reference Design constraint file “tpce646_xczu11_xxx_ffvc1760.xdc” should be used.

An omission of the respective specifications for buffer driver strength, slew rate, I/O standard, and on-chip termination can lead to significant issues with timing and signal integrity.

8.19 Power Supply

The TPCE646 provides an additional power connector besides the power contacts at the PCIe edge connector. This 150W-ATX power connector is compatible to the PCIe specification and designed as 2x4 auxiliary power connector.

This power connector also allows the TPCE646 to be operated as a standalone solution. For operation, only the 150W ATX power is required. All other interface connections are optional.

Without a plugged and powered 2x4 auxiliary power connector the TPCE646 is not switched on and cannot be used.

9 Design Help

9.1 Board Reference Design

User applications for the TPCE646 may be developed by using the TPCE646 User MPSoC Board Reference Design.

TEWS offers this Board Reference Design as a well-documented basic example. It includes a xdc constrain file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TPCE646. It implements a PCIe endpoint with interrupt support, register mapping, DDR4 memory access and basic I/O functions. It comes as an AMD Vivado™ 2024.1 project with source code and as a ready-to-download bit stream. This example design can be used as a starting point for own projects.

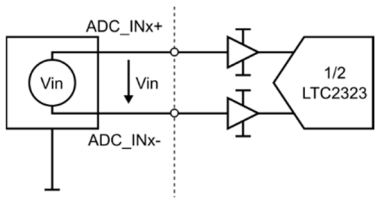
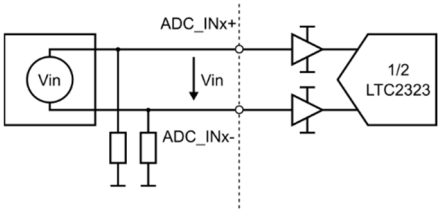
The TPCE646 User MPSoC Application design can be developed using the design software Vivado™ Design Suite. Licenses for design tools are required.

For TPCE646 User MPSoC Board Reference Design also see the included BRD User Manual.

10 I/O Interfaces

10.1.1 Front I/O - Analog Input Level

All analog inputs are connected via an impedance converter and a second operation amplifier for level adjustment and filtering to the differential ADC inputs. This also serves as a protection of the ADC from excessive analog input levels.

Diff. Source with Ground Reference	Diff. Source without Ground Reference
	
Maximum VIN = ±20.678 V	Maximum VIN = ±20.678 V

The TPCE646 has differential analog inputs. When talking about the input voltage range of a differential input, one has to differentiate between the differential input voltage between the two pins, and the input voltage relative to ground for each pin.

With an input voltage range of ±10.339 V (ground related) for each pin of the differential input, we get the ±20.678V differential input voltage range:

Voltage	Description	TPCE646
V_{diff_max}	Maximum differential input voltage (range)	±20.678 V
V_{cm_max}	Maximum common mode input voltage (range)	0V
V_{in_max}	Operating voltage range of the input pins	±10.339 V
V_{in_abs}	Absolute maximum voltage range of the input	Power Off: ±5.0V Power On: ±18.5V

Table 10-1 : Differential Input Voltage Ranges

The range of a differential input is -20.678 V to +20.678 V, which results to a full-scale range of 41.356 V for the ±10.339 V (per pin, relative to ground) Input voltage range.

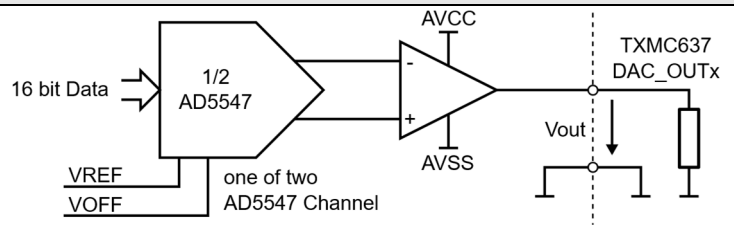
10.1.2 Front I/O – Analog Output Level

All analog outputs of the AD5547 DAC are routed through operational amplifiers to front I/O connector.

Outputs Drive Current	**±10 mA**
Capacitive Load	1000 pF

Table 10-2 : DAC Electrical Interface

Single-ended DAC Output



Maximum Vout = ±10.0 V

Figure 10-1 : DAC Output Interface

The output voltage range of each DAC channel can be set via VREF and VOFF.

See also the chapter about the configuration of the DAC output voltage in the BCC Register Description.

10.1.3 Rear I/O Interface

All 64 single-ended / 32 differential digital rear I/O Pins of the TPCE646 are directly routed from the User MPSoC to the 64 pin X13 (Samtec QSE-040) rear I/O connector. The I/O functions of these User MPSoC pins are directly dependent on the configuration of the User MPSoC.

The User MPSoC VCCO voltage is set to 1.8 V, so only the 1.8 V I/O standards LVCMOS18 and LVDS are possible when using the TPCE646 rear I/O interface.

10.1.4 LVDS Front I/O Interface

The 4-channel M-LVDS front I/O interface consists of four independent SN65MLVD204B M-LVDS transceivers, each forming one bidirectional differential pair. Every channel provides one differential line, routed as a controlled-impedance PCB pair.

Each provides a 100 Ω termination on TPCE646. All four devices are supplied with 3.3 V and are connect directly to the X1 front connector.

11 I/O Description

11.1 Overview

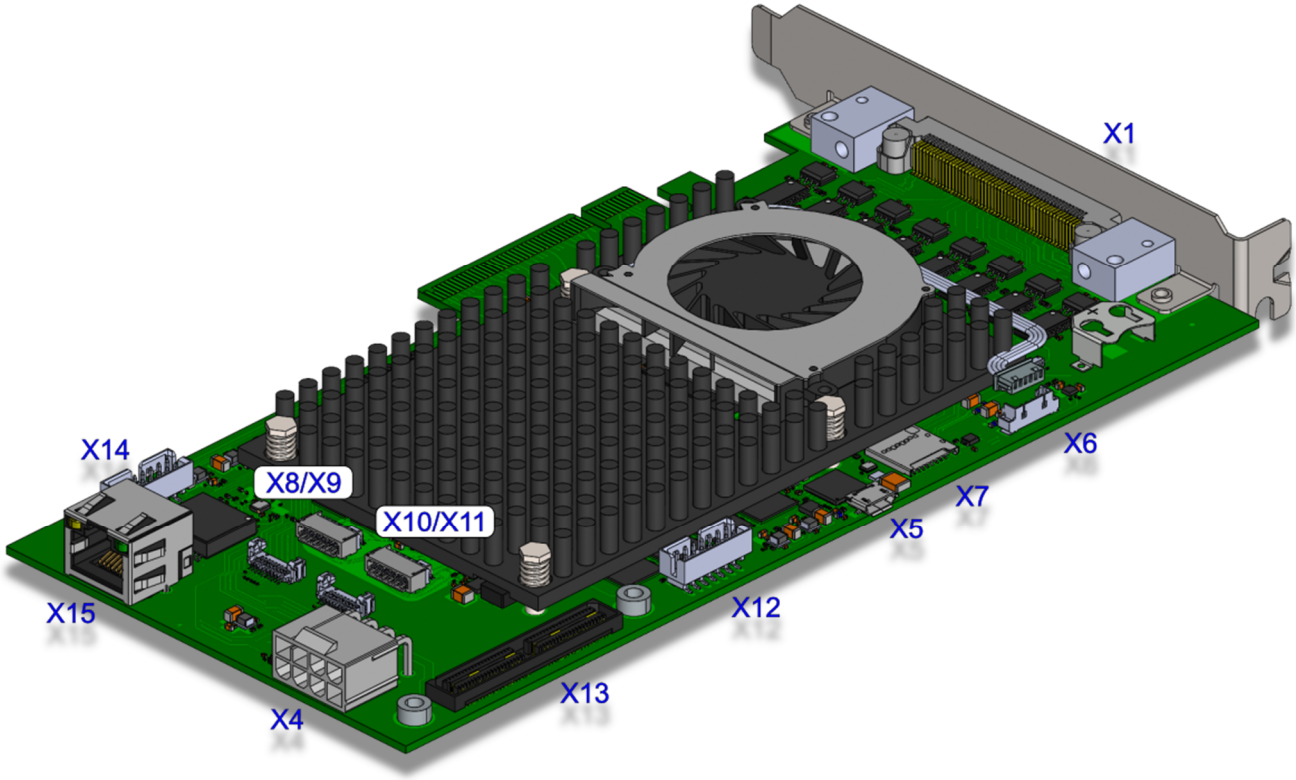


Figure 11-1 : I/O Connector Overview

11.2 Front I/O Connector (X1)

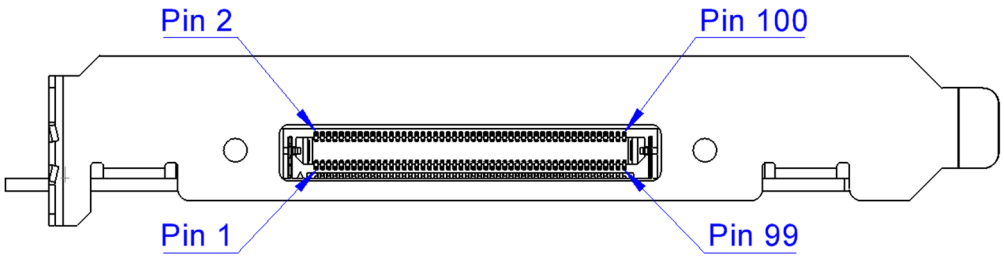


Figure 11-2 : Front Panel I/O Connector Numbering

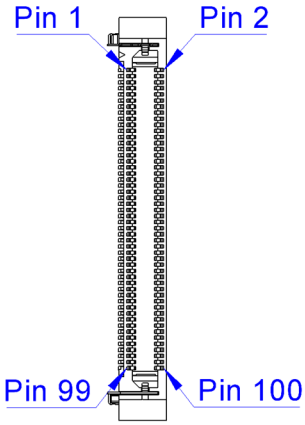
11.2.1 Connector Type

Pin-Count	100
Connector Type	Rugged Edge Rate Strip, 0.8mm Pitch Connector
Source & Order Info	ERF8-050-01-L-D-RA-L-TR Samtec

Table 11-1: Front Panel I/O Connector

11.2.2 Pin Assignment

Pin	I/O	Connector View	Pin	I/O
1	ADC_IN0+		2	ADC_IN1+
3	ADC_IN0-		4	ADC_IN1-
5	GND		6	GND
7	ADC_IN2+		8	ADC_IN3+
9	ADC_IN2-		10	ADC_IN3-
11	GND		12	GND
13	ADC_IN4+		14	ADC_IN5+
15	ADC_IN4-		16	ADC_IN5-
17	GND		18	GND
19	ADC_IN6+		20	ADC_IN7+
21	ADC_IN6-		22	ADC_IN8-
23	GND		24	GND
25	DAC_OUT0		26	DAC_OUT1
27	GND		28	GND
29	GND		30	GND
31	DAC_OUT2		32	DAC_OUT3
33	GND		34	GND
35	GND		36	GND
37	DAC_OUT4		38	DAC_OUT5
39	GND		40	GND
41	GND		42	GND
43	DAC_OUT6		44	DAC_OUT7
45	GND		46	GND
47	DAC_OUT8		48	DAC_OUT9
49	GND		50	GND
51	DAC_OUT10		52	DAC_OUT11
53	GND		54	GND
55	DAC_OUT12		56	DAC_OUT13
57	GND		58	GND
59	DAC_OUT14		60	DAC_OUT15



Pin	I/O	Connector View	Pin	I/O
61	GND		62	GND
63	DAC_OUT16		64	DAC_OUT17
65	DAC_OUT18		66	DAC_OUT19
67	DAC_OUT20		68	DAC_OUT21
69	DAC_OUT22		70	DAC_OUT23
71	GND		72	GND
73	DAC_OUT24		74	DAC_OUT25
75	DAC_OUT26		76	DAC_OUT27
77	DAC_OUT28		78	DAC_OUT29
79	DAC_OUT30		80	DAC_OUT31
81	GND		82	GND
83	NC		84	NC
85	NC		86	NC
87	NC		88	NC
89	NC		90	NC
91	GND		92	GND
93	IO_F_0+		94	IO_F_1+
95	IO_F_0-		96	IO_F_1-
97	IO_F_2+		98	IO_F_3+
99	IO_F_2-		100	IO_F_3-

Table 11-2: Front Panel I/O Connector Pin Assignment

11.3 Digital Rear I/O Connector (X13)

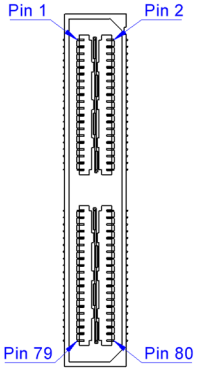
11.3.1 Connector Type

Pin-Count	80
Connector Type	Samtec High-Speed Ground Plane Header, 0.80mm Pitch
Source & Order Info	Samtec **QSE-040-01-L-D-A**

Table 11-3: Digital Rear I/O Connector

11.3.2 Pin Assignment

Pin	differential I/O	single ended I/O		Pin	differential I/O	single ended I/O
1	I2C SCL			2	I2C SDA	
3	IO_R_30-	IO_R_31		4	IO_R_31-	IO_R_63
5	IO_R_30+	IO_R_30		6	IO_R_31+	IO_R_62
7	IO_R_28-	IO_R_29		8	IO_R_29-	IO_R_61
9	IO_R_28+	IO_R_28		10	IO_R_29+	IO_R_60
11	GND	GND		12	GND	GND
13	IO_R_26-	IO_R_27		14	IO_R_27-	IO_R_59
15	IO_R_26+	IO_R_26		16	IO_R_27+	IO_R_58
17	IO_R_24-	IO_R_25		18	IO_R_25-	IO_R_57
19	IO_R_24+	IO_R_24		20	IO_R_25+	IO_R_56
21	GND	GND		22	GND	GND
23	IO_R_22-	IO_R_23		24	IO_R_23-	IO_R_55
25	IO_R_22+	IO_R_22		26	IO_R_23+	IO_R_54
27	IO_R_20-	IO_R_21		28	IO_R_21-	IO_R_53
29	IO_R_20+	IO_R_20		30	IO_R_21+	IO_R_52
31	GND	GND		32	GND	GND
33	IO_R_18-	IO_R_19		34	IO_R_19-	IO_R_51
35	IO_R_18+	IO_R_18		36	IO_R_19+	IO_R_50
37	IO_R_16-	IO_R_17		38	IO_R_17-	IO_R_49
39	IO_R_16+	IO_R_16		40	IO_R_17+	IO_R_48
41	GND	GND		42	GND	GND
43	IO_R_14-	IO_R_15		44	IO_R_15-	IO_R_47
45	IO_R_14+	IO_R_14		46	IO_R_15+	IO_R_46
47	IO_R_12-	IO_R_13		48	IO_R_13-	IO_R_45
49	IO_R_12+	IO_R_12		50	IO_R_13+	IO_R_44
51	GND	GND		52	GND	GND
53	IO_R_10-	IO_R_11		54	IO_R_11-	IO_R_43
55	IO_R_10+	IO_R_10		56	IO_R_11+	IO_R_42
57	IO_R_8-	IO_R_9		58	IO_R_9-	IO_R_41
59	IO_R_8+	IO_R_8		60	IO_R_9+	IO_R_40
61	GND	GND		62	GND	GND
63	IO_R_6-	IO_R_7		64	IO_R_7-	IO_R_39
65	IO_R_6+	IO_R_6		66	IO_R_7+	IO_R_38



Pin	differential I/O	single ended I/O		Pin	differential I/O	single ended I/O
67	IO_R_4-	IO_R_5		68	IO_R_5-	IO_R_37
69	IO_R_4+	IO_R_4		70	IO_R_5+	IO_R_36
71	GND	GND		72	GND	GND
73	IO_R_2-	IO_R_3		74	IO_R_3-	IO_R_35
75	IO_R_2+	IO_R_2		76	IO_R_3+	IO_R_34
77	IO_R_0-	IO_R_1		78	IO_R_1-	IO_R_33
79	IO_R_0+	IO_R_0		80	IO_R_1+	IO_R_32

Table 11-4: Digital Rear I/O Connector Pin Assignment

11.3.3 Alignment and Position

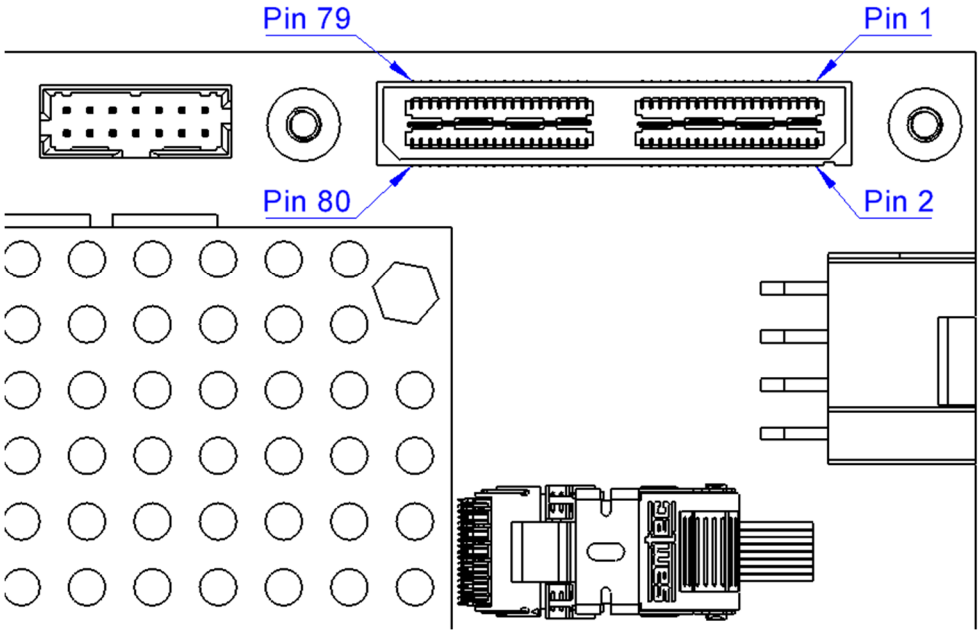


Figure 11-3 : Alignment and Position Digital Rear I/O Connector

11.4 GTY Rear I/O Connector

Each of both GTY Rear I/O Connectors is a Samtec Firefly Micro Flyover Connector which consists of two parts. One part is the connector for the high-speed signals (UEC5) and the second part (UCC8) is for power and control signals.

11.4.1 Connector Type UEC5 (X9)

Pin-Count	38
Connector Type	Firefly Micro Flyover Connector
Source & Order Info	Samtec – UEC5-019-1-H-D-RA-2-A

Table 11-5: Firefly UCE5 Rear I/O Connector

11.4.2 Pin Assignment UEC5 (X9)

Pin	UEC5 - A	UEC5 - B
1	GND	GND
2	Tx0-	Tx1-
3	TX0+	Tx1+
4	GND	GND
5	Tx2-	Tx3-
6	Tx2+	Tx3+
7	GND	GND
8	DIG_IO_0	DIG_IO_2
9	DIG_IO_1	DIG_IO_3
10	GND	GND
11	DIG_IO_4	DIG_IO_6
12	DIG_IO_5	DIG_IO_7
13	GND	GND
14	Rx3+	Rx2+
15	Rx3-	Rx2-
16	GND	GND
17	Rx1+	Rx0+
18	Rx1-	Rx0-
19	GND	GND

Table 11-6: Firefly UCE5 Rear I/O Connector Pin Assignment

11.4.3 Connector Type UCC8 (X8)

Pin-Count	10
Connector Type	Firefly Micro Flyover Connector
Source & Order Info	Samtec – UCC8-010-1-H-S-2-A

Table 11-7: Firefly UCC8 Rear I/O Connector

11.4.4 Pin Assignment UCC8 (X8)

Pin	UCC8
1	+3.3V
2	GND
3	PRESENTL_A
4	SELECTL_A
5	INTL_A
6	RESETL_A
7	SDA_A
8	SCL_A
9	n.c.
10	+3.3V

Table 11-8: Firefly UCC8 Rear I/O Connector Pin Assignment

11.4.5 Connector Type UEC5 (X11)

Pin-Count	38
Connector Type	Firefly Micro Flyover Connector
Source & Order Info	Samtec – UEC5-019-1-H-D-RA-2-A

Table 11-9: Firefly UCE5 Rear I/O Connector

11.4.6 Pin Assignment UEC5 (X11)

Pin	UEC5 - A	UEC5 - B
1	GND	GND
2	Tx4-	Tx5-
3	TX4+	Tx5+
4	GND	GND
5	Tx6-	Tx7-
6	Tx6+	Tx7+
7	GND	GND
8	DIG_IO_8	DIG_IO_10
9	DIG_IO_9	DIG_IO_11
10	GND	GND
11	DIG_IO_12	DIG_IO_14
12	DIG_IO_13	DIG_IO_15
13	GND	GND
14	Rx7+	Rx6+
15	Rx7-	Rx6-
16	GND	GND
17	Rx5+	Rx4+
18	Rx5-	Rx4-
19	GND	GND

Table 11-10: Firefly UCE5 Rear I/O Connector Pin Assignment

11.4.7 Connector Type UCC8 (X10)

Pin-Count	10
Connector Type	Firefly Micro Flyover Connector
Source & Order Info	Samtec – UCC8-010-1-H-S-2-A

Table 11-11: Firefly UCC8 Rear I/O Connector

11.4.8 Pin Assignment UCC8 (X10)

Pin	UCC8
1	+3.3V
2	GND
3	PRESENTL_B
4	SELECTL_B
5	INTL_B
6	RESETL_B
7	SDA_B
8	SCL_B
9	n.c.
10	+3.3V

Table 11-12: Firefly UCC8 Rear I/O Connector Pin Assignment

11.5 Micro-USB Connector (X5)

The Micro-USB Header from UART to USB Interface of the PS User MPSoC corresponds in the mechanic and the pin assignment to the USB 2.0 standard.

11.5.1 Connector Type

Pin-Count	5
Connector Type	MICRO USB 2.0 SMT TYPE B
Source & Order Info	Mürth Elektronik or compatible

Table 11-13: Micro-USB Connector

11.5.2 Pin Assignment

Pin	Signal	Description
1	Power	VBUS +5.0 V
2	D-	USB 2.0, differential pair
3	D+	
4	ID	NC
5	GND	GND

Table 11-14: Micro-USB Connector Pin Assignment

11.6 Ethernet RJ45 Connector Header (X15)

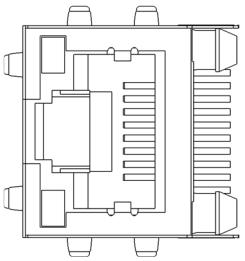
The pinout of the TPCE646 RJ45 Ethernet connector complies with the standard for 10/100/1000 Mbps Ethernet connections:

11.6.1 Connector Type

Pin-Count	8
Connector Type	Shielded Modular Jack Assembly
Source & Order Info	Würth Connectors 615 008 137 421

Table 11-15: Ethernet RJ45 Connector

11.6.2 Pin Assignment



Pin	Signal (1000Base-T)	Signal (100Base-TX/10Base-T)
1	TX0/RX0+	TX+
2	TX0/RX0-	TX-
3	TX1/RX1+	RX+
4	TX2/RX2+	not used
5	TX2/RX2-	not used
6	TX1/RX1-	RX-
7	TX3/RX3+	not used
8	TX3/RX3-	not used

Table 11-16: Ethernet RJ45 Connector pin Assignment

11.7 User MPSoC JTAG Header (X12)

This header is directly connected to the PS port of User MPSoC.

The pinout of this header is designed in conjunction with the standard pinning of the AMD programming adapters. This allows the direct use of AMD cables and AMD software-tools.

11.7.1 Connector Type

Pin-Count	14
Connector Type	2.00 mm Pitch Milli-Grid™ Header
Source & Order Info	Molex 87832-1420 or compatible

Table 11-17: User MPSoC JTAG Header

11.7.2 Pin Assignment

Pin	Signal	Description
1	NC	Not Connected
2	V_{REF}	JTAG Reference Voltage (3.3V)
3	GND	Ground
4	TMS	Test Mode Select Input
5	GND	Ground
6	TCK	Test Clock
7	GND	Ground
8	TDO	Test Data Output (Output from TPCE646)
9	GND	Ground
10	TDI	Test Data Input (Input to TPCE646)
11	GND	Ground
12	NC	not connected on the TPCE646
13	PGND	Used on TPCE646 for AMD Header present detection
14	NC	HALT_INIT_WP signal. Optional. Not connected on the TPCE646

Table 11-18: User MPSoC JTAG Header Pin Assignment

11.8 Additional PJTAG Header (X14)

This header is directly connected to configurable PS MIO pins of User MPSoC.

The pinout of this header is designed in conjunction with the standard pinning of the AMD programming adapters. This allows the direct us of AMD cables and AMD software-tools.

11.8.1 Connector Type

Pin-Count	14
Connector Type	2.00 mm Pitch Milli-Grid™ Header
Source & Order Info	Molex 87832-1420 or compatible

Table 11-19: Additional PJTAG Header

11.8.2 Pin Assignment

Pin	Signal	Description
1	NC	Not Connected
2	V_{REF}	JTAG Reference Voltage (3.3V)
3	GND	Ground
4	PTMS	Test Mode Select Input
5	GND	Ground
6	PTCK	Test Clock
7	GND	Ground
8	PTDO	Test Data Output (Output from TPCE646)
9	GND	Ground
10	PTDI	Test Data Input (Input to TPCE646)
11	GND	Ground
12	NC	not connected on the TPCE646
13	PGND	Used on TPCE646 for AMD Header present detection
14	NC	HALT_INIT_WP signal. Optional. Not connected on the TPCE646

Table 11-20: Additional PJTAG Header Pin Assignment

11.9 150W Auxiliary Power Connector (X4)

11.9.1 Connector Type

Pin-Count	8
Connector Type	Mini-Fit Jr. Header, Dual Row, Right-Angle
Source & Order Info	Molex 455860006 or compatible

Table 11-21: 150W Auxiliary Power

11.9.2 Pin Assignment

Pin	Signal	Description
1	+12 V	+12 V Auxiliary Power
2	+12 V	
3	+12 V	
4	Sense1	Sense pin for 150W auxiliary power identification
5	GND	System Ground
6	Sense0	Sense pin for 75W auxiliary power identification
7	GND	System Ground
8	GND	

Table 11-22: 150W Auxiliary Power Pin Assignment