The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC117

6 Channel SSI, Incremental Encoder, Counter Interface

Version 2.0

User Manual

Issue 2.0.1

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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

TPMC117-10R

6 Channel SSI, Incremental Encoder, Counter Interface, RS422 or TTL I/O, Timer, HD68

TPMC117-20R

6 Channel SSI, Incremental Encoder, Counter Interface, RS422 or TTL I/O, Timer, P14 I/O, blank front panel

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‘Active Low’ is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
-	Preliminary Issue	December 2005
1.0	First Issue	September 2006
1.0.1	New notation for HW Engineering Documentation Releases	February 2009
1.0.2	Added: “7.2 Clock Output Wiring”	June 2010
1.0.3	Added -20 Variant	July 2012
1.0.4	General Revision	August 2014
1.0.5	Added “Fault Detection” SSI Status Bit	January 2017
2.0.0	Changed to TPMC117 V2.0 Encoder: - Added “slow” / ”fast” clock prescaler setting Interval Timer: - Extended Interval Timer from 16 to 32 bit - Added time based clock divider Interrupts: - Added “Interrupt Acknowledge Configuration” Debouncing - Added “Advanced Debouncing” for SSI / Encoder and Digial Inputs Additional Registers: - Added Board Health Register - Added Scratchpad Register - Added Firmware Version Register Revised the technical information for the 24 V digital I/Os Revised the description for the termination resistor configuration The Clock outputs are now referenced to the isolated ground GND_I	March 2020
2.0.1	Fixed typos & layout issues	November 2022

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1 Product Description

The TPMC117 is a standard single-width 32 bit PMC module and offers six independent channels. Each of these channels can operate as a standard SSI interface controller, in a SSI 'Listen only' Mode, as an incremental encoder or general purpose counter.

The standard SSI interface controller outputs a clock burst to the absolute encoder and receives the returned positional data. The SSI interface controller operates with a programmable clock rate from 1 µs to 15 µs and programmable data word length from 1 bit to 32 bit.

In 'Listen only' Mode the channel listens to an existing SSI interface to observe its data transfer. It takes both the SSI clock and data as inputs. In 'Listen only' Mode the channel also has a programmable data word length from 1 bit to 32 bit; the SSI clock rate of the observed SSI interface can be in the range of 1 µs to 15 µs.

In both modes the data word can be encoded in Binary- or in Gray code and with odd, even or no parity.

The 32 bit incremental encoder counter is a preloadable up- and down counter. The counter is programmable for single, double and quadruple analysis of the encoder signals. In conjunction with the isolated 24 V digital inputs it provides the possibility of automatic preload of the counter whenever the motion system passes a reference position.

The 32 bit general purpose preloadable up- and down counter can be fed with an internal clock or with external signals.

Both counter modes offer a 32 bit preload register, a 32 bit compare register and various count modes.

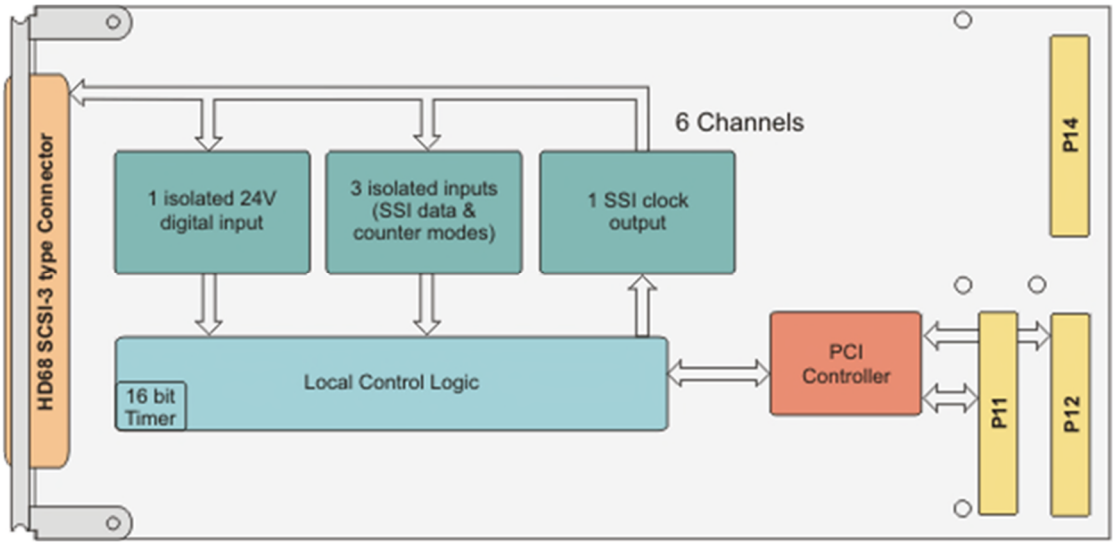


Figure 1-1: Block Diagram

A 'Multiple Channel Read' function latches the actual values of all enabled channels whose values can then be read without interfering with normal function. In addition the TPMC117 provides a 32 bit down-counter with preload register which can be used as reference timer for closed loop applications or as trigger for the Multiple Channel Read function.

All data inputs are isolated. The level of the input signals can be RS422 or TTL. The input signals pass a digital filter for noise suppression before they are further used. The level of the SSI clock output signals is RS422.

Each of the six motion control channels of the TPMC117 offers one isolated IEC 61131-2 compliant 24 V digital input. The input circuit ensures a defined switching point and polarization protection against confusing the pole. The input has an electronic debounce circuit. All six 24 V digital inputs can generate an interrupt, triggered on rising or falling edge. Depending on the selected mode the input can be used as general purpose input or reference input.

All TPMC117-10R signals are accessible through an HD68 SCSI-3 type front I/O connector. The TPMC117-20R offers P14 back I/O and a blank front panel.

The TPMC117 can operate with 3.3 V and 5.0 V PCI I/O signaling voltage.

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 3.0 compliant 33 MHz / 32 bit PCI 3.3 V and 5 V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	Artix-7 FPGA with PCI core	
SSI / Encoder I/O Interface		
Number of Channels	6 isolated channels with 3 input lines and 1 output line per channel	
Input Levels	RS422 differential or TTL single-ended	
Output Level	RS422 differential	
ESD Protection	±15 kV - Human Body Model	
Maximum Input Frequency	5 MHz	
Isolated 24 V Digital Inputs		
Number of Inputs	6 digital inputs: reference input or general purpose input depending on mode	
Input Voltage	24 V DC typical, 60 V DC maximum	
Input Current	2.5 mA @ 24 V input voltage	
Input Switching Level	10.5 V typical, 8.5 V minimum, 11.5 V maximum (conforms to IEC 61131-2 Type 3)	
ESD Protection	±2 kV - Human Body Model	
Additional Features		
Interval Timer	Programmable with timing intervals up to 2^{32} s	
I/O Connector	TPMC117-10R: HD68 SCSI-3 type connector (e.g. AMP# 787082) TPMC117-20R: P14 Back I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	280 mA typical @ +5V DC (no load) 380 mA typical @ +5V DC (SSI mode @ 1 MHz, with RS422 load)	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	209 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	78 g	

Table 2-1: Technical Specification

3 Address Map

3.1 PCI Configuration Space

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				Initial Values (Hex Values)
	31 24	23 16	15 8	7 0	
0x00	Device ID		Vendor ID		0075 1498
0x04	Status		Command		0280 0000
0x08	Class Code			Revision ID	118000 00
0x0C	not supported	Header Type	PCI Latency Timer	not supported	00 00 00 00
0x10	Base Address Register 0 (BAR0) – Legacy Support				FFFFFF80
0x14	Base Address Register 1 (BAR1) – Legacy Support				FFFFFF81
0x18	Base Address Register 2 (BAR2)				FFFFFF00
0x1C	not supported				00000000
0x20	not supported				00000000
0x24	not supported				00000000
0x28	PCI CardBus Information Structure Pointer				00000000
0x2C	Subsystem ID		Subsystem Vendor ID		s.b. 1498
0x30	not supported				00000000
0x34	Reserved			New Cap. Ptr.	000000 00
0x38	Reserved				00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	00 00 01 00
0x40-0xFF	Reserved				00000000

Table 3-1: PCI Configuration Space Header

Device-ID:	0x0075	TPMC117
Vendor-ID:	0x1498	TEWS TECHNOLOGIES
Subsystem-ID:	0x000A	-10R
	0x0014	-20R
Subsystem Vendor-ID:	0x1498	TEWS TECHNOLOGIES

3.2 PCI Memory Space

The PCI IP core maps the internal registers into an address space within the PCI memory space, using the Base Address Register (BAR2). For backward compatibility two additional BARs have been implemented.

The following table shows the PCI BAR configuration. The BAR configuration is the same for all product variants.

Base Address Register (BAR)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	MEM	128	32	Little	Legacy, unused
1	IO	128	32	Little	Legacy, unused
2	MEM	256	32	Big	Register Space

Table 3-2: Memory Address Spaces

The BARs marked as “Legay, unused” exist to maintain compatibility with older versions of the TPMC117. Reads from these spaces return zero, writes are ignored.

3.3 Register Space

The Register Space is accessible via the PCI Base Address Register 2 (BAR2). Adresses marked as “Reserved” should be written as “0”.

Offset	Description	Size (Bit)
SSI / Encoder Registers		
0x00	Control Register 0	32
0x04	Data Register 0	32
0x08	Status Register 0	32
0x0C	Counter Preload Register 0	32
0x10	Counter Compare Register 0	32
0x14	Counter Command Register 0	32
0x18	Control Register 1	32
0x1C	Data Register 1	32
0x20	Status Register 1	32
0x24	Counter Preload Register 1	32
0x28	Counter Compare Register 1	32
0x2C	Counter Command Register 1	32
0x30	Control Register 2	32
0x34	Data Register 2	32
0x38	Status Register 2	32
0x3C	Counter Preload Register 2	32
0x40	Counter Compare Register 2	32

Offset	Description	Size (Bit)
0x44	Counter Command Register 2	32
0x48	Control Register 3	32
0x4C	Data Register 3	32
0x50	Status Register 3	32
0x54	Counter Preload Register 3	32
0x58	Counter Compare Register 3	32
0x5C	Counter Command Register 3	32
0x60	Control Register 4	32
0x64	Data Register 4	32
0x68	Status Register 4	32
0x6C	Counter Preload Register 4	32
0x70	Counter Compare Register 4	32
0x74	Counter Command Register 4	32
0x78	Control Register 5	32
0x7C	Data Register 5	32
0x80	Status Register 5	32
0x84	Counter Preload Register 5	32
0x88	Counter Compare Register 5	32
0x8C	Counter Command Register 5	32
General Registers		
0x90	Digital Input Register	32
0x94	Interval Timer Control Register	32
0x98	Interval Timer Preload Register	32
0x9C	Interval Timer Data Register	32
0xA0	Global Control Register	32
0xA4	Interrupt Enable Register	32
0xA8	Interrupt Status Register	32
0xAC	Test Register	32
0xB0	Advanced SSI/Encoder Debouncing	32
0xB4	Advanced Digital Input Debouncing	32
0xB8 … 0xF0	Reserved	-
0xF4	Board Health Register	32
0xF8	Scratchpad Register	32
0xFC	Firmware Version Register	32

Table 3-3: Local Register Address Space

4 Register Description

4.1 Control Register

The Control Register is divided into two parts: bits[15:0] are dedicated for SSI control; bits [31:16] are dedicated for Counter control.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:30</td><td>-</td><td>Reserved, always reads as ‘0’</td><td>-</td><td>0</td></tr>
<tr><td>29</td><td>FAST</td><td>Determines if the Internal Clock Prescaler uses a “slow” or a “fast” clock:
‘0’ = use “slow” clock
‘1’ = use “fast” clock</td><td>R/W</td><td>0</td></tr>
<tr><td>28:26</td><td>POL [2:0]</td><td>A,B,I Polarity
The Input Polarity Control can be used to adapt the input to the input source polarity.
<table>
<tr><th>Bit</th><th>Input</th><th>Polarity</th></tr>
<tr><td>26</td><td>A</td><td>0 = high active, 1 = low active</td></tr>
<tr><td>27</td><td>B</td><td>0 = high active, 1 = low active</td></tr>
<tr><td>28</td><td>I</td><td>0 = high active, 1 = low active</td></tr>
</table></td><td>R/W</td><td>000</td></tr>
<tr><td>25:23</td><td>ICM [2:0]</td><td>Index Control Mode
The Index Control Mode determines how the counter interprets events on the I-input.
Reference modes are only valid when Input Mode = Quadrature Count
<table>
<tr><th>ICM</th><th>Mode</th></tr>
<tr><td colspan="2">None Reference Mode</td></tr>
<tr><td>000</td><td>Ignore I-input</td></tr>
<tr><td>001</td><td>Load on I</td></tr>
<tr><td>010</td><td>Latch on I</td></tr>
<tr><td>011</td><td>Gate on I</td></tr>
<tr><td>100</td><td>Reset on I</td></tr>
<tr><td colspan="2">Reference Modes</td></tr>
<tr><td>101</td><td>Reference mode</td></tr>
<tr><td>110</td><td>Auto reference mode</td></tr>
<tr><td>111</td><td>Index mode</td></tr>
</table>
See chapter ’5.3.3 Index Control Modes’ for details.</td><td>R/W</td><td>000</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>22:21</td><td>SCM [1:0]</td><td>Special Count Mode
<table>
<tr><th>SCM</th><th>Mode</th></tr>
<tr><td>00</td><td>No special mode active / cycling counter</td></tr>
<tr><td>01</td><td>Divide-by-N</td></tr>
<tr><td>10</td><td>Single Cycle</td></tr>
</table>
See chapter ’5.3.2 Special Count Modes’ for details.</td><td>R/W</td><td>00</td></tr>
<tr><td>20:19</td><td>CLKDIV [1:0]</td><td>Internal Clock Prescaler
Depending on FAST the Internal Clock Prescaler uses a “slow” ar a “fast” clock.

When using a “slow” clock:
<table>
<tr><th>CLKDIV</th><th>Clock frequency</th></tr>
<tr><td>00</td><td>32 MHz</td></tr>
<tr><td>01</td><td>16 MHz</td></tr>
<tr><td>10</td><td>8 MHz</td></tr>
<tr><td>11</td><td>4 MHz</td></tr>
</table>
When using a “fast” clock:
<table>
<tr><th>CLKDIV</th><th>Clock frequency</th></tr>
<tr><td>00</td><td>160 MHz</td></tr>
<tr><td>01</td><td>80 MHz</td></tr>
<tr><td>10</td><td>40 MHz</td></tr>
<tr><td>11</td><td>20 MHz</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
<tr><td>18:16</td><td>INPUT [2:0]</td><td>Counter Input Mode
The Input Mode determines the input source and how the counter interprets these input signals. The Quadrature mode can be used with a 1x, 2x or 4x resolution multiplier.
<table>
<tr><th>INPUT</th><th>Input Mode</th><th>Input Source</th></tr>
<tr><td>000</td><td>Counter disabled</td><td>-</td></tr>
<tr><td>001</td><td>Timer Mode Up</td><td>Internal Clock Prescaler</td></tr>
<tr><td>010</td><td>Timer Mode Down</td><td>Internal Clock Prescaler</td></tr>
<tr><td>011</td><td>Direction Count</td><td>Input A & Input B</td></tr>
<tr><td>100</td><td>Up/Down Count</td><td>Input A & Input B</td></tr>
<tr><td>101</td><td>Quadrature Count 1x</td><td>Input A & Input B</td></tr>
<tr><td>110</td><td>Quadrature Count 2x</td><td>Input A & Input B</td></tr>
<tr><td>111</td><td>Quadrature Count 4x</td><td>Input A & Input B</td></tr>
</table>
See chapter ’5.3.1 Input Modes’ for details.</td><td>R/W</td><td>000</td></tr>
</table>

Bit	Symbol	Description	Access	Reset Value
15	BREAK	Break on Read Error (Listen only) 1 = The channel stops to listen on read errors 0 = Read errors are ignored and the channel resumes to listen	R/W	0
14	MODE	1 = SSI 'Listen only' Mode 0 = Standard SSI Interface Controller	R/W	0
13	BC5	Number of Data Bits Bits are used to program the number of bits of the serial absolute encoder. It can be read and written by software. The data bits must be programmed in the range from 1 to 32. BC5…BC0 = 0x01 to 0x20 means 1 to 32 bit. BC5…BC0 = 0x00 not valid BC5…BC0 = 0x21 to 0x3F not valid	R/W	0
12	BC4			
11	BC3			
10	BC2			
9	BC1			
8	BC0			
7	CODE	SSI Data word coding 1 = Gray Code The data word is converted into binary code 0 = Binary Code	R/W	0
6	ZB	Parity Bit with Zero Bit, controls the clock cycles 1 = two additional clock cycles 0 = one additional clock cycle are provided to get the parity bit	R/W	0
5	EO	Controls the parity detection 1 = odd parity 0 = even parity This bit is ignored if bit 4 is set to '0'.	R/W	0
4	PAR	Encoder with parity - If encoder provides a parity bit: 1 = detect parity errors 0 = do not detect parity errors / no parity bit	R/W	0
3	CR3	Clock Rate for encoder serial clock speed The clock can be programmed in steps of 1 µs in the range of 1 to 15. A value of 0 for the clock rate will stop the operation of the SSI interface. The 'Listen only' Mode will ignore the Clock Rate setting; in this mode the Clock Rate will be detected automatically.	R/W	0
2	CR2			
1	CR1			
0	CR0			

Table 4-1: Control Register

Note that a value of 0x00 or a value from 0x21 to 0x3F for BC5...BC0 is not valid and will stop the operation of the SSI Interface.

4.2 Data Register

Bit	Symbol	Description	Access	Reset Value
31:0	-	Data Register	R/S	0

Table 4-2: Data Register

When the channel is disabled, the Data Register returns 0x00000000 on read accesses.

4.2.1 Data Register in SSI Mode

The serial data of the absolute encoder is shifted into the Data Register.

In Standard SSI Interface mode a write access to the Data Register initiates a data transfer from the absolute encoder independently of the other channels.

In 'Listen only' SSI Interface mode a read access to the Data Register sets the Busy bit to '1' and the channel is listening again.

The data register may not contain valid data, if the serial data transfer is in progress (the corresponding Busy bit is read as '1').

4.2.2 Data Register in Counter Mode

The Data Register contains the actual counter value.

While a Multiple Channel Read is in progress, this register may contain latched data. In 'Latch on I' control mode this register contains latched data after a control mode event. See chapter 'Data Register Lock' for details.

4.3 Status Register

The Status Register is divided into two parts: bits[15:0] are dedicated for SSI status; bits[31:16] are dedicated for Counter status.

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved, always reads as '0'	-	0
23	SGL	Single Cycle active In Single Cycle counting mode this bit is set to '1' when the counter is active. It is reset to '0', when the counter has counted down to zero.	R	0
22	OVFL	Data Register Latch Overflow When a Latch Mode event occurs while the Data Register Lock is still active, the data in the Data Register will be retained and this bit will be set to indicate that data was lost. This bit must be reset by writing a '1' to this bit.	R/C	0

Bit	Symbol	Description	Access	Reset Value
21	DRL	Data Register Latch This bit is set to '1', when the Data Register is locked due to a 'Latch on I' or a Multiple Channel Read. This bit is cleared after a read access to the Data Register or by writing a '1' to this bit.	R/C	0
20	DIR	Count Direction This bit indicates the counting direction of the counter. '1' indicates up, '0' indicates down. In the 'Up/Down Count' mode this bit indicates the direction at the last count. In the 'Direction Count' mode this bit corresponds to the I-input.	R	0
19	SGN	Sign The Sign bit is set to '1' when the counter overflows, and is set to '0' when the counter underflows. After reset or power-up this bit should be considered as "don't care" until the first Carry or Borrow occurred.	R	0
18	MAT	Match This bit is set to '1' when the counter value matches the value of the Counter Compare Register. This bit must be reset by writing a ‘1’ to this bit.	R/C	0
17	CRY	Carry This bit is set to '1' when the counter changes from 0xFFFFFFFF to 0x00000000. This bit must be reset by writing a ‘1’ to this bit.	R/C	0
16	BOR	Borrow This bit is set to '1' when the counter changes from 0x00000000 to 0xFFFFFFFF. This bit must be reset by writing a ‘1’ to this bit.	R/C	0
15:4	-	Reserved, always reads as ‘0’	-	0
3	FAULT	This bit indicates data line faults and loss of communication which can indicate a defective sensor. It is updated after each data transmission. 1 = Data line fault detected 0 = No data line fault detected	R	0
2	RER	Read Error 1 = Data is invalid because of an error during the last transmission 0 = Data OK This bit is only valid for channels in ‘Listen only’ mode. For channels in Standard SSI Interface Controller mode this bit will always read ‘0’ Reasons for a read error are: - The number of data bits set in the control register does not match the actual size of the received transmission. - Only a partial transmission was received (this could happen when the mode is switched and a transmission is in progress on the observed SSI-interface).	R	0

Bit	Symbol	Description	Access	Reset Value
1	PRY	Parity Error 1 = Parity Error at the last data transmission 0 = No Parity Error at the last data transmission During a transmission the parity error bit is not valid. The parity error status is updated only if the parity enable bit of the corresponding channel is set to ‘1’. Otherwise the parity status is read as ‘0’.	R	0
0	BSY	Busy Bit 0 = Data Ready (set after every completed transmission, even if a parity or a read error was issued) In Standard SSI Interface Controller mode Busy Bit = ‘1’ indicates a transmission in progress. In ‘Listen only’ Mode the Busy Bit is set to ‘1’ when a transmission is in progress. It is set to '0' when transmission was received and stays '0' until the data word was read.	R	0

Table 4-3: SSI Status Register

4.4 Counter Preload Register

Bit	Symbol	Description	Access	Reset Value
31:0	-	Counter Preload Register The value of this register can be loaded into the counter by: - Setting bit 1 (LCNT) of the Counter Command Register - An impulse on the I-input when the 'Load on I'-mode is active - Automatically in the 'Divide-by-N'-mode every time the counter creates a borrow or a carry - Reference modes	R/W	0

Table 4-4: Counter Preload Register

4.5 Counter Compare Register

Bit	Symbol	Description	Access	Reset Value
31:0	-	Counter Compare Register Every time the counter matches the Counter Compare Register value, bit 18 (MAT) of the Status Register is set to '1' and, if enabled, an interrupt is generated.	R/W	-1

Table 4-5: Counter Compare Register

4.6 Counter Command Register

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved, always reads as ‘0’	-	0
1	LCNT	Load Counter Write ‘1’ to load the counter with the value of the Counter Preload Register.	W	0
0	RCNT	Reset Counter Write ‘1’ to reset the counter.	W	0

Table 4-6: Counter Command Register

Commands are performed by writing a '1' to the according bit.

4.7 Digital Input Register

Bit	Symbol	Description	Access	Reset Value
31:12	-	Reserved, always reads as ‘0’	-	0
11	DIIC5	Digital Input Interrupt Control Selects interrupt on rising or falling edge for corresponding 24 V digital input. 1 = selects interrupt for rising edge 0 = selects interrupt for falling edge	R/W	0
10	DIIC4			
9	DIIC3			
8	DIIC2			
7	DIIC1			
6	DIIC0			
5	DI5	These bits reflect the actual state of the digital 24 V inputs. In “Reference Mode” and “Auto Reference Mode” the digital 24 V inputs are used as reference inputs. In all other modes the digital 24 V inputs can be used as general purpose inputs.	R	-
4	DI4			
3	DI3			
2	DI2			
1	DI1			
0	DI0			

Table 4-7: Digital Input Register

4.8 Interval Timer Control Register

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:3</td><td>-</td><td>Reserved, always reads as ‘0’</td><td>-</td><td>0</td></tr>
<tr><td>3</td><td>ISET</td><td>Determines if the Interval Timer Clock Divider uses a prescaled clock or fixed time bases:
‘0’ = use prescaled clock
‘1’ = use time base</td><td>R/W</td><td>0</td></tr>
<tr><td>2:1</td><td>ITDIV</td><td>Interval Timer Clock Divider
Depending on ITSET the Interval Timer uses a prescaled clock or a fixed time base.
When using a prescaled clock:
<table>
<tr><th colspan="2">Value</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>8 MHz</td></tr>
<tr><td>0</td><td>1</td><td>4 MHz</td></tr>
<tr><td>1</td><td>0</td><td>2 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1 MHz</td></tr>
</table>
When using a time base:
<table>
<tr><th colspan="2">Value</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>100 ns</td></tr>
<tr><td>0</td><td>1</td><td>1 µs</td></tr>
<tr><td>1</td><td>0</td><td>1 ms</td></tr>
<tr><td>1</td><td>1</td><td>1 s</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
<tr><td>0</td><td>ITEN</td><td>Interval Timer Enable
'0' disables the Interval Timer
'1' enables the Interval Timer</td><td>R/W</td><td>0</td></tr>
</table>

Table 4-8: Interval Timer Control Register

4.9 Interval Timer Preload Register

Bit	Symbol	Description	Access	Reset Value
31:0	ITPRE	Interval Timer Preload Register	R/W	0

Table 4-9: Interval Timer Preload Register

4.10 Interval Timer Data Register

Bit	Symbol	Description	Access	Reset Value
31:0	ITDR	Interval Timer Data Register This register contains the actual Interval Timer Value.	R	0

Table 4-10: Interval Timer Data Register

4.11 Global Control Register

Bit	Symbol	Description	Access	Reset Value
31:27	-	Reserved, always reads as '0'	-	0
26	MCRTR	Multiple Channel Read Trigger By writing '1' to this bit, a Multiple Channel Read is triggered. This is only valid for channels which are already enabled for a Multiple Channel Read. Do not set the SLx bits and the MCRTR bit on the same write access!	W	0
25	MCRST	Multiple Channel Read Status This bit indicates pending Multiple Channel Read data. When a SSI channel is enabled for Multiple Channel Read, it takes time for the conversion to complete. This bit indicates that the conversions of all enabled channels are complete. 1 = Multiple Channel Read Data is valid (for all enabled channels) 0 = The Data Registers of all enabled channels have been read out. To reset a multiple channel read sequence, write '1' to this bit	R/C	0
24	ITRG	Interval Timer as trigger for Multiple Channel Read 1: Enable Interval Timer as trigger for multiple channel read 0: Disable Interval Timer as trigger for multiple channel read	R/W	0
23	SL5	Enable Multiple Channel Read for the corresponding channel 1 = enables multi channel read 0 = disables multi channel read See chapter '5.4 Multiple Channel Read' for details.	R/W	0
22	SL4			
21	SL3			
20	SL2			
19	SL1			
18	SL0			

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>17</td><td>PRL5</td><td rowspan="6">Manual Counter Preload
Writing a ‘1’ issues a preload of the corresponding counter with the value of the Counter Preload Register. This preload method is only possible for channels in a ‘None Reference Mode’.
Before using this preload method, the corresponding Counter Preload Registers must be loaded with valid data</td><td rowspan="6">W</td><td rowspan="6">0</td></tr>
<tr><td>16</td><td>PRL4</td></tr>
<tr><td>15</td><td>PRL3</td></tr>
<tr><td>14</td><td>PRL2</td></tr>
<tr><td>13</td><td>PRL1</td></tr>
<tr><td>12</td><td>PRL0</td></tr>
<tr><td>11:10</td><td>IC5 [1:0]</td><td rowspan="6">Interface Control
<table><tr><th>IC</th><th>Mode</th></tr><tr><td>00</td><td>Channel disabled</td></tr><tr><td>01</td><td>SSI Mode</td></tr><tr><td>10</td><td>Counter Mode</td></tr><tr><td>11</td><td>Channel disabled</td></tr></table>(the selection between normal SSI mode and ‘SSI listen only’ mode is done the Channel Control Register)</td><td rowspan="6">R/W</td><td rowspan="6">0</td></tr>
<tr><td>9:8</td><td>IC4 [1:0]</td></tr>
<tr><td>7:6</td><td>IC3 [1:0]</td></tr>
<tr><td>5:4</td><td>IC2 [1:0]</td></tr>
<tr><td>3:2</td><td>IC1 [1:0]</td></tr>
<tr><td>1:0</td><td>IC0 [1:0]</td></tr>
</table>

Table 4-11: Global Control Register

4.12 Interrupt Enable Register

For pending interrupts and interrupt acknowledge see the Interrupt Status Register

Bit	Symbol	Description	Access	Reset Value
31	IRQ ACK CONF	Interrupt Acknowledge Configuration 0 = Interrupts are acknowledged by writing '1' to the appropriate bit in the Interrupt Status Register 1 = Interrupts are cleared when the Interrupt Status Register is read	R/W	0
30:25	-	Reserved, always reads as '0'	-	0
24	TIEN	Interval Timer Interrupt	R/W	0
23	DIEN5	Enable 24 V digital input Interrupt 1 = Digital Input Interrupt enabled 0 = Digital Input Interrupt disabled An interrupt will be generated on an (rising or falling) edge of the digital input.		
22	DIEN4			
21	DIEN3			
20	DIEN2			
19	DIEN1			
18	DIEN0			
17	CIEN5	Enable Control Mode Interrupt 1 = Control Mode Interrupt enabled 0 = Control Mode Interrupt disabled An interrupt will be generated on a control mode event.	R/W	0
16	CIEN4			
15	CIEN3			
14	CIEN2			
13	CIEN1			
12	CIEN0			
11	MIEN5	Enable Match Interrupt 1 = Counter Match Interrupt enabled 0 = Counter Match Interrupt disabled An interrupt will be generated when the counter value matches the Counter Compare Register.	R/W	0
10	MIEN4			
9	MIEN3			
8	MIEN2			
7	MIEN1			
6	MIEN0			
5	SIEN5	Enable SSI Interrupt 1 = SSI Data Valid Interrupt enabled 0 = SSI Data Valid Interrupt disabled An interrupt will be generated when a SSI transmission completes and the Busy status bit is set to '0'.	R/W	0
4	SIEN4			
3	SIEN3			
2	SIEN2			
1	SIEN1			
0	SIEN0			

Table 4-12: Interrupt Enable Register

4.13 Interrupt Status Register

The interrupt status is updated only if the interrupt enable bit of the corresponding channel is set to ‘1’. Otherwise the interrupt status is read as ‘0’.

Bit	Symbol	Description	Access	Reset Value
31:25	-	Reserved, always reads as ‘0’	-	0
24	TISTA	Pending Interval Timer Interrupts (Read), Interrupt acknowledge (Write) On a read-access this bit indicates a pending Interval Timer interrupt. A '1' indicates a pending interrupt. The interrupt is acknowledged by writing a '1' to this bit.	R/C	0
23	DISTA5	Pending Digital Input Interrupts (Read), Interrupt acknowledge (Write) On a read-access these bits indicate the channels with pending digital input interrupts. A '1' indicates a pending interrupt. The interrupts are acknowledged by writing a '1' to the according bit.	R/C	0
22	DISTA4			
21	DISTA3			
20	DISTA2			
19	DISTA1			
18	DISTA0			
17	CISTA5	Pending Control Mode Interrupts (Read), Interrupt acknowledge (Write) On a read-access these bits indicate the channels with pending control mode interrupts. A '1' indicates a pending interrupt. The interrupts are acknowledged by writing a '1' to the according bit.	R/C	0
16	CISTA4			
15	CISTA3			
14	CISTA2			
13	CISTA1			
12	CISTA0			
11	MISTA5	Pending Match Interrupts (Read), Interrupt acknowledge (Write) On a read-access these bits indicate the channels with pending match interrupts. A '1' indicates a pending interrupt. The interrupts are acknowledged by writing a '1' to the according bit.	R/C	0
10	MISTA4			
9	MISTA3			
8	MISTA2			
7	MISTA1			
6	MISTA0			
5	SISTA5	Pending SSI Interrupts (Read), Interrupt acknowledge (Write) On a read-access these bits indicate the channels with pending SSI interrupts. A '1' indicates a pending interrupt. The interrupts are acknowledged by writing a '1' to the according bit.	R/C	0
4	SISTA4			
3	SISTA3			
2	SISTA2			
1	SISTA1			
0	SISTA0			

Table 4-13: Interrupt Status Register

4.14 Test Register

This register allows quick testing of the RS422/TTL in- and outputs. To check the digital input levels read the Digital Input Register.

Bit	Symbol	Description	Access	Reset Value
31:25	-	Reserved, always reads as '0'	-	0
24	TSTEN	Enable Test Output 1 = Test Output enabled 0 = Test Output disabled	R/W	0
23	CLK5	SSI Clock outputs. When TSTEN is '1' these bits will control the SSI clock outputs.	R/W	0
22	CLK4			
21	CLK3			
20	CLK2			
19	CLK1			
18	CLK0			
17	I5	Channel 6 Inputs	R	0
16	B5			
15	A5			
14	I4	Channel 4 Inputs	R	0
13	B4			
12	A4			
11	I3	Channel 3 Inputs	R	0
10	B3			
9	A3			
8	I2	Channel 2 Inputs	R	0
7	B2			
6	A2			
5	I1	Channel 1 Inputs	R	0
4	B1			
3	A1			
2	I0	Channel 0 Inputs	R	0
1	B0			
0	A0			

Table 4-14: Test Register

4.15 Advanced Debouncing Register (Digital)

Same as “Advanced Debouncing Register (Encoder)”, see below.

4.16 Advanced Debouncing Register (Encoder)

To avoid false counts caused by noisy input signals, the encoder and digital inputs are digitally filtered. This filter is typical 3-stage debounce circuit. By default it runs with a 32 MHz sampling clock, resulting in input signals shorter ~100 ns being suppressed. To address input sources such as mechanical switches with longer bouncing times, the debouncing can be configured here.

There are separate Advanced Debouncing Registers for the encoder and digital inputs. Advanced Debouncing can be enabled separately for each encoder and digital input channel.

Bit	Symbol	Description	Access	Reset Value
31:30	-	Reserved, always reads as ‘0’	-	00
29	ADE5	Advanced Debouncing Enable 0 = Default Debouncing 1 = Enable Advanced Debouncing with the settings below	R/W	0
28	ADE4		R/W	0
27	ADE3		R/W	0
26	ADE2		R/W	0
25	ADE1		R/W	0
24	ADE0		R/W	0
23:18	-	Reserved, always reads as ‘0’	-	0
17:16	ADV DEB BASE	Time base used for the input filter 00 = use 31,25 ns time base 01 = use 100 ns time base 10 = use 1 µs time base 11 = use 1 ms time base	R/W	00
15:0	ADV DEB TIME	These bits set the filter time together with the time base set by ADV DEB BASE. Filter time is ~ADV DEB TIME * ADV DEB BASE * 3-stages A value of zero effectively turns the debouncer off.	R/W	0

Table 4-15: Advanced Debouncing Register

4.17 Board Health Register

Bit	Symbol	Description	Access	Reset Value
31:25	-	Reserved, always reads as '0'	-	0
24:16	XADC	XADC sensor alarm bits	R	0
15:0	TEMP XADC	Result of the XADC on-chip temperature sensor measurement in degrees centigrade in steps of 1/256 °C. This is a signed value. A new readout is available every ~100 µs	R	0

Table 4-16: Board Health Register

4.18 Scratchpad Register

Bit	Symbol	Description	Access	Reset Value
31:0	SCRATCH	Scratchpad Register Can be used to test read and write operations	R/W	0

Table 4-17: Scratchpad Register

4.19 Firmware Identification Register

Bit	Symbol	Description	Access	Reset Value
31:24	FW_MAJ	Firmware Major Version	R	2
23:16	FW_MIN	Firmware Minor Version	R	0
15:8	FW_REV	Firmware Revision	R	0
7:0	FW_BLD	Firmware Build Count	R	0

Table 4-18: Firmware Identification Register

5 Functional Description

Each channel can either work as a SSI interface or as an encoder / general purpose counter. The choice between both modes is made in the Global Control Register on a per channel base. In addition to this main functionality the TPMC117 offers one isolated 24 V digital input per channel plus an interval timer.

5.1 SSI Short Description

The Synchronous Serial Interface (SSI) is based on two differential signal lines, CLOCK and DATA. The CLOCK line is an input, the DATA line is an output of the absolute encoder.

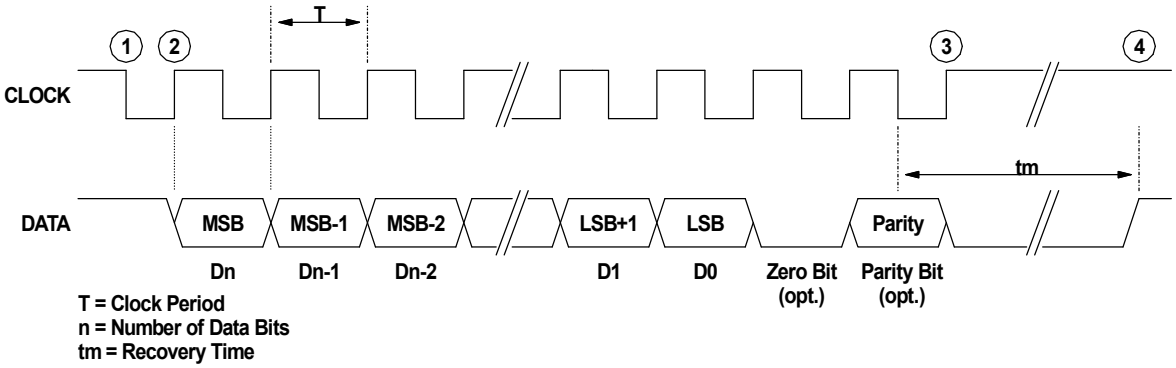


Figure 5-1: SSI Timing Example

When not transmitting, the clock and data lines are high. To read out the positional data of an absolute encoder, the controller transmits a pulse train on the CLOCK line. The first falling edge of CLOCK ① latches the positional data of the absolute encoder. At the first rising edge of CLOCK ② the absolute encoder presents the most significant bit on the DATA line. On each subsequent rising edge in the CLOCK pulse train the next bit in order is transmitted to the controller.

In addition to the data bits the absolute encoder can transmit a parity bit for error detection. As an option a zero bit can be placed between the data and the parity bit.

After all bits are transmitted ③, the absolute encoder holds the data line low for 10-30µs (recovery time tm). After that the absolute encoder is ready for a new transmission ④. A new transmission must not started before ④.

The maximum achievable baud rate depends on the cable length. Cables are assumed to be twisted pair and screened.

Cable length (m)	Baud rate (kHz)
< 50	< 400
< 100	< 300
< 200	< 200
< 400	< 100

5.2 SSI Mode

5.2.1 Standard SSI Interface Controller Mode

In this mode a TPMC117 channel operates as a standard SSI interface controller. The SSI clock is an output and data signal is an input to the TPMC117.

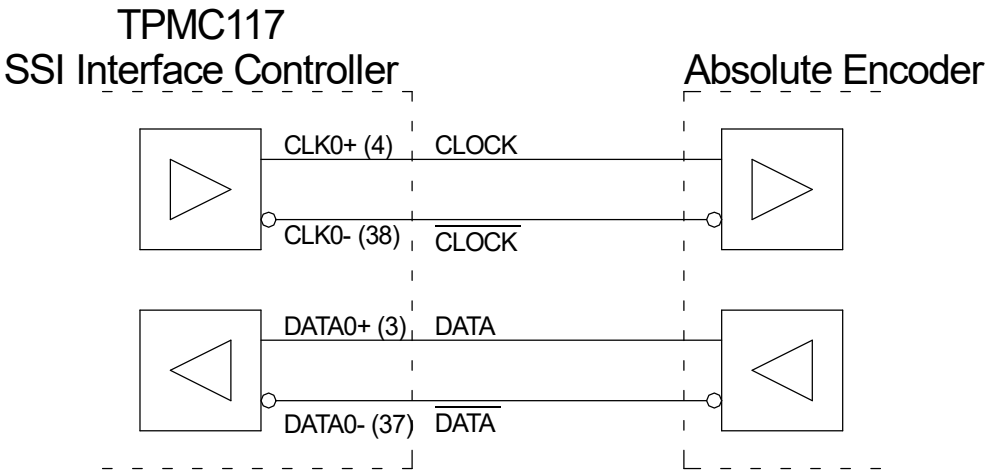


Figure 5-2: Wiring Example: Channel 0, SSI Interface Controller Mode

This mode is enabled when the Interface Control in the Global Control Register is set to “01” and the MODE bit in the Control Register is set to ‘0’:

Register	Symbol	Setting
Global Control Register	ICx	“01”
Control Register X	MODE	‘0’

Table 5-1: SSI Standard Mode Selection

In the Control Register the SSI interface must be set up, conforming to the settings required of the connected absolute encoder:

Register	Symbol	Setting
Control Register X	BC	Number of data bits
	CODE	Binary/Gray Code
	ZB	Additional Zero Bit
	EO	Even/Odd Parity
	PAR	Parity detection
	CR	Clock Rate

Table 5-2: SSI Setup

A data transfer is initiated by a write to the Data Register. The SSI interface controller then generates a clock burst, on which the absolute encoder returns its positional data. The SSI Controller receives this data, processes it (parity check, gray- to binary code conversion) and indicates the end of the data transfer with the deassertion of the Busy bit. If enabled, an interrupt is asserted and the positional data can be read in the Data Register.

In this mode the “Read Error” status bit is always read as ‘0’.

5.2.2 SSI ‘Listen only’ Mode

In ‘Listen only’ Mode a TPMC117 channel listens to an existing SSI interface to observe the data transfer. Both the SSI clock and data signals are inputs to the TPMC117.

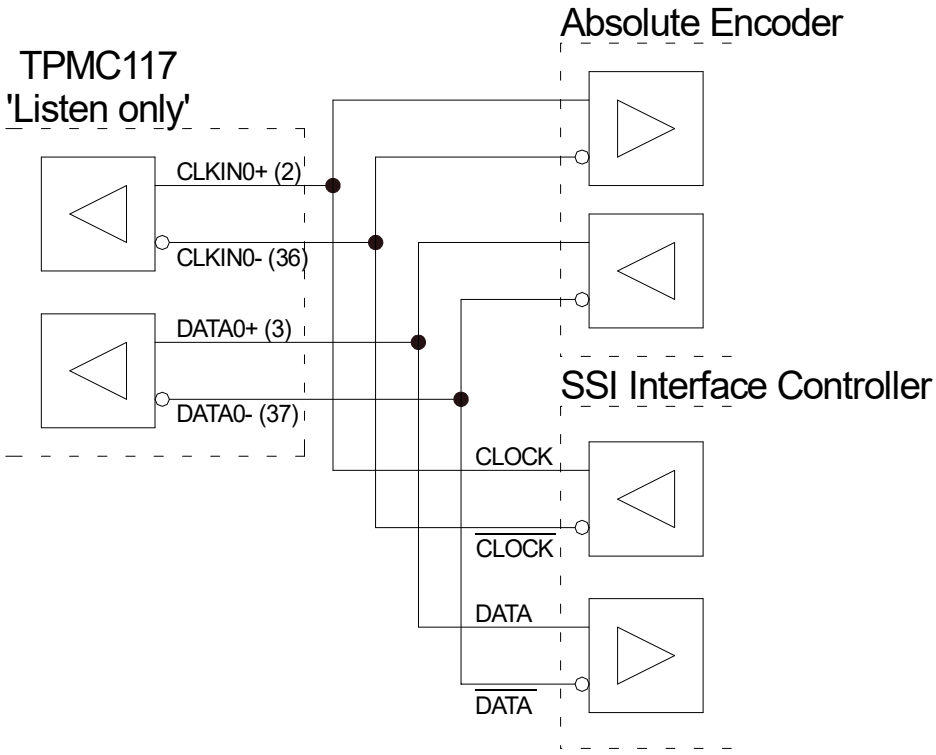


Figure 5-3: Wiring Example: Channel 0, ‘Listen only’ Mode

This mode is enabled when the Interface Control in the Global Control Register is set to “01” and the MODE bit in the Control Register is set to ‘1’.

Register	Bit	Setting
Global Control Register	ICx	“01”
Control Register X	MODE	‘1’

Table 5-3: SSI ‘Listen only’ Mode Selection

In the Control Register the SSI interface must be set up, conforming to the settings required of the observed SSI interface:

Register	Symbol	Setting
Control Register X	BC	Number of data bits
	CODE	Binary/Gray Code
	ZB	Additional Zero Bit
	EO	Even/Odd Parity
	PAR	Parity detection
	CR	-

Table 5-4: SSI ‘Listen only’ Setup

The clock rate setting in the Control Register is ‘don’t care’; the clock rate of the observed SSI interface will be detected automatically.

After the Control Register is set up, the channel listens (indicated by Busy = ‘1’).

A data transfer is initiated by the observed SSI interface. The positional data will be received and processed (parity check, gray- to binary code conversion) and the end of the data transfer is indicated with the deassertion of the Busy bit. If enabled, an interrupt is asserted and the positional data can be read in the Data Register.

Reading the Data Register will set the Busy bit to ‘1’ and the channel is listening again.

Note that in this mode the clock rate setting in the Control Register is ignored; the Clock Rate will be detected automatically. Writes to the Data Register are also ignored for channels in this mode.

In case of a partial transmission a read error will be issued in the Status Register. To detect read errors, the width of the first SSI clock pulse is measured to detect the clock rate. This clock rate is multiplied by 4 and used as the initial value for a watchdog timer. Every new received bit resets the watchdog timer, until either the programmed data word length is reached (successful read) or a timeout occurs (read error). In case of a timeout the Read Error bit is set to ‘1’. Depending on the BREAK setting in the Control Register the channel ignores a read error and continues listening or it stops to listen.

Reasons for a read error are:

- The number of data bits set in the control register does not match the actual size of the received transmission.
- Only a partial transmission was monitored (this could happen when the mode is switched and a transmission is in progress on the observed SSI interface).

In the case that a SSI communication is in progress when the mode is switched to ‘Listen only’, a read error will be issued for the first reading.

5.2.3 SSI Mode behavior differences

	Standard SSI Interface Mode	**‘Listen only’ Mode**
Control Register	Control Register SSI bits fully used Bit 14 (MODE) is set to ‘0’	Clock rate setting in Control Register is ‘don’t care’ Bit 14 (MODE) is set to ‘1’
Status Register	Busy bit = ‘1’ during transmission	Busy bit = ‘1’ during transmission or after the data word was read (channel is listening again)
Read Error Bit	Read Error bit is always ‘0’	Read Error bit is set to ‘1’ on a erroneous transmission
Connections	Connect external SSI data outputs to TPMC117 ‘DATA’ inputs. Connect external SSI Clock inputs to TPMC117 ‘CLK OUT’ outputs.	Connect external SSI data to TPMC117 ‘DATA’ inputs. Connect external SSI clock to TPMC117 ‘CLK IN’ inputs.
Data Transfer Start	Data transfer is initiated by a write to the Data Register or a Multiple Channel Read	Data transfer is initiated by external SSI interface controller

Table 5-5: Mode behavior differences

5.3 Counter Mode

The TPMC117 counter offers 4 input modes, 2 special count modes and 8 index control modes.

5.3.1 Input Modes

The input mode determines how the counter interprets the A and B input lines:

Input Mode	A Input	B Input	I Input
Timer	not used	not used	Available for Input Control Modes
Direction Count	Count	Count direction (up/down)	
Up/Down Count	Count UP	Count DOWN	
Quadrature Count	Quadrature A	Quadrature B	

Table 5-6: Input Modes

Changing the input mode does not affect the counter reading. If no input mode is selected, the counter is disabled.

5.3.1.1 Timer Mode

In Timer mode the counter uses an internal clock as input. Depending on the FAST-setting in the Control Register, the internal clock is prescaled as follows:

FAST	CLKDIV	Clock frequency
1	00	160 MHz
1	01	80 MHz
1	10	40 MHz
1	11	20 MHz
0	00	32 MHz
0	01	16 MHz
0	10	8 MHz
0	11	4 MHz

Table 5-7: Timer Mode Clock Prescaler

5.3.1.2 Direction Count

The counter acts as up/down counter. Counting pulses are generated when a transition from low to high of the A-input is detected. The B-input determines the count direction.

B-input	Count Direction
0	Down
1	Up

Table 5-8: Count Directions

5.3.1.3 Up/Down Count

The counter acts as up-/down counter. Counting pulses are generated when a transition from low to high of either the A- or the B-input is detected. The A-input counts up, the B-input counts down. Simultaneous transitions on the A- and B-input do not generate a counting pulse.

5.3.1.4 Quadrature Count

The counter acts as quadrature counter. A-input is quadrature input A, B-input is quadrature input B. The quadrature inputs can be interpreted as 1x, 2x or 4x counting. 1x lets the counter count once for each full cycle of the quadrature inputs, 2x lets the counter count once for each half cycle of the quadrature inputs and 4x lets the counter count once for each quarter cycle of the quadrature inputs. The count direction (increase or decrease) is determined by the relative phase of the A- and B-signals.

The maximum input frequency is 2 MHz. In 4x mode the counter counts with max. 8 MHz.

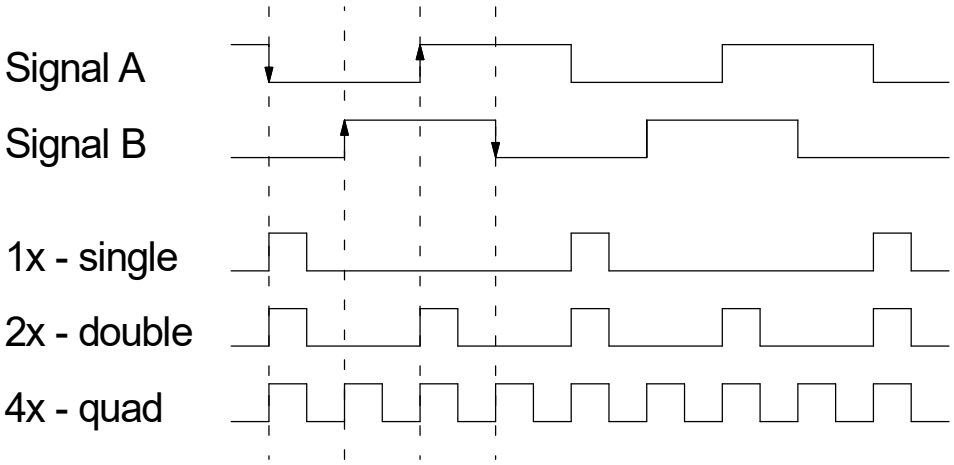


Figure 5-4: Quadrature Signals

5.3.2 Special Count Modes

In normal operation, the counter is a cycling counter. Two additional special count modes are available. The Count Modes are available for every Input Mode.

5.3.2.1 Divide-by-N

The counter is enabled in the Control Register and will run until it is disabled. The counter is loaded with the content of the preload register every time the counter creates a borrow or a carry.

5.3.2.2 Single Cycle

The counter is enabled in the Control Register and will start on following events:

- A manual preload or reset in the Counter Command Register
- A manual counter preload in the Global Control Register
- A control mode event in ‘Load on I’ or ‘Reset on I’ mode.

The counter will stop when it creates a borrow or a carry.

5.3.3 Index Control Modes

The Index Control Mode determines how events on the I-input are interpreted. With the exception of the ‘Gate on I’ mode, all modes react on a level change on the I-input. Due to the digital input filtering, a change in the input level is only detected, when the input line is stable for at least 100ns. The following table gives an overview of the index control mode events.

Index Control Mode	Polarity	
	high active (POL = 0)	low active (POL = 1)
No I-Control	-	-
Load on I	Rising edge	Falling edge
Latch on I	Rising edge	Falling edge
Gate on I	High level	Low Level
Reset on I	Rising edge	Falling edge
Reference Mode	Rising edge	Falling edge
Auto Reference Mode	Rising edge	Falling edge
Index Mode	Rising edge	Falling edge

Table 5-9: Index Control Mode events

The control modes ‘Reference Mode’, ‘Auto Reference Mode’ and ‘Index Mode’ are only valid when the input mode is quadrature count. They control the counter with the encoder index input in cooperation with a reference switch connected to the isolated 24 V digital input.

An interrupt can be generated on a control mode event. This is only available for the Load-, Latch-, Gate- and Reset on I modes.

Index Control Mode	Interrupt generation
No Control Mode	No interrupt
Load Mode Latch Mode Reset Mode	Control mode event
Gate Mode	Gate closed

Table 5-10: Index control mode interrupt generation

5.3.3.1 No I-Control

In this mode the I-input is ignored.

5.3.3.2 Load on I

An event on the I-input loads the counter with the content of the Counter Preload Register. If the 'Single Cycle' mode is active, the event on the I-input will start the counter. The counter can also be preloaded by writing '1' to the 'Load Counter' (LCNT) bit in the Counter Command Register.

This control mode can be used to establish a known reference position in a mechanical system.

5.3.3.3 Latch on I

An event on the I-input loads and locks the Data Register with the actual counter value (see chapter 'Data Register Lock' for details. It will remain latched until the Data Register is read or the latch is released with the CDLT bit in the Status Register.

When a 'Latch on I' event occurs while the Data Register Lock is still active, the data in the Data Register will be retained and the Data Register Lock Overflow (OVFL) will be set to indicate that data was lost.

This control mode can be used to capture a position in a mechanical system.

5.3.3.4 Gate on I

The signal level on the I-input enables or disables counting. Remember that in this mode the I-input is level sensitive.

I-Input	Counter
0	Disabled
1	Enabled

Table 5-11: Gate Mode

In this mode an interrupt is generated (if enabled) when the gate is being closed (I-Input transition from '1' to '0').

When a signal with constant frequency is connected to the A- and B-inputs, this control mode can be used for impulse width measurements.

5.3.3.5 Reset on I

An event on the I-input resets (clears) the counter. If the 'Single Cycle' mode is active, the event on the I-input starts the counter.

The counter can also be reset by writing '1' to the 'Reset Counter' (RCNT) bit in the Counter Command Register.

This control mode can be used to establish a known home or reference position in a mechanical system.

5.3.3.6 Reference Mode

This mode controls the counter with the (isolated 24 V digital) reference input and the encoder index signal. A specified reference input signal and a following index impulse produce a counter preload. The host software must set the motion direction during such a reference access to backwards.

The following figure shows the two normal preload accesses. An encoder motion area with eight index pulses and the corresponding reference input is described as an example. Two different 'start positions' (1a and 1b) are shown:

Position 1a

Direction is forward and the reference input is active. The host software must move into the area where the reference input is inactive. Now the direction must be changed. The next index pulse after entering the area with reference input active triggers the preload function for the counter.

Position 1b

Direction is backwards and the reference input is inactive. The host software must move further backwards, and after entering the area with reference input active the next index pulse triggers the preload function for the counter.

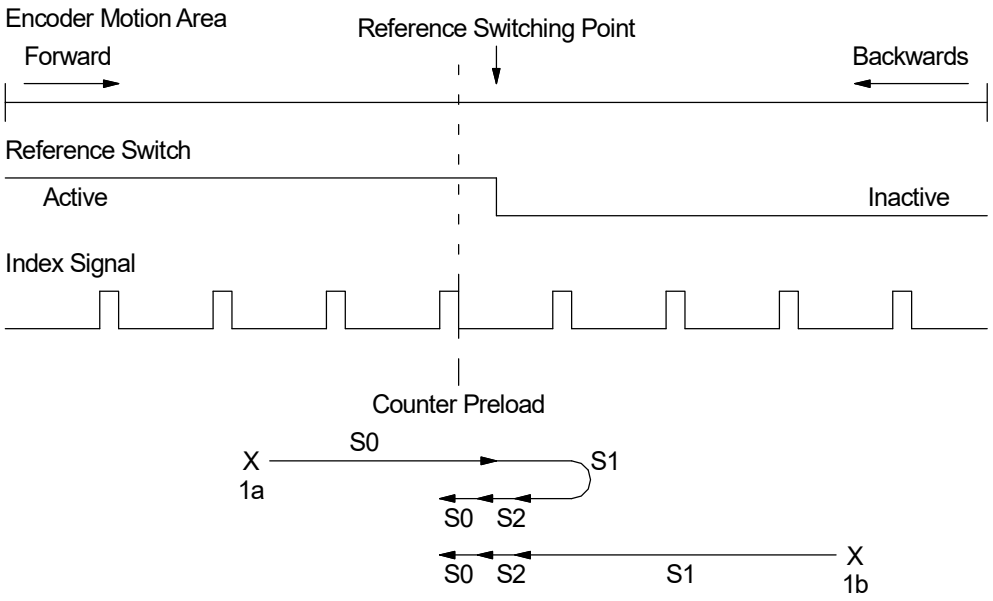


Figure 5-5: Reference mode preload example

A correct execution of the reference function can be monitored in the Control Register. After successful execution the mode is reset from Reference Mode to No I-Control Mode.

5.3.3.7 Auto Reference Mode

This mode is the automation of the Reference Mode. Every time the reference switching point and a following index pulse are crossed during backward direction, a new preload is generated. In “Auto Reference Mode” there is no change of the Index Control Mode in the Control Register!

5.3.3.8 Index Mode

In this mode the reference input is not used. Only the index impulse produces a counter preload. After setting this mode the next occurrence of the index signal independent from direction will preload the counter. A correct execution of this preload function can be monitored in the Control Register. After successful execution the mode is reset from Index Mode to No I-Control Mode.

5.3.4 Data Register Lock

The Data Register is loaded and locked with the actual counter value on following conditions:

- Latch in I Mode
- Multiple channel read

The Data Register is locked until following conditions are met:

- A read-access to the Data Register
- A write '1' to the RCNT bit in the Counter Command Register

Until the lock is released, the Data Register will not load again. The status of the Data Register lock can be monitored in the Status Register (DRL). When the lock is released, the Data Register retains its value until it is loaded again.

When a Multiple channel read is issued or a Latch Mode event occurs while a Data Register is locked, the Data Register content will be retained and the Data Register Lock Overflow (OVFL) will be set to indicate that data was lost.

5.4 Multiple Channel Read

The Multiple Channel Read option is enabled in the Global Control Register. A Multiple Channel Read is triggered by writing ‘1’ to the MCRTR-bit. Alternatively the interval timer can be used to trigger a multiple channel read. For Counter mode the Multiple Channel Read latches the enabled counter channels. For SSI mode the Multiple Channel Read starts a conversion for the enabled SSI channels.

The data of counter channels is instantly available. SSI channels need time for the conversion to complete. To indicate that all data is available, the MCRST bit in the Global Control Register will be set to ‘1’. This bit will stay ‘1’ until the Data Registers of all enabled channels were read. Then it changes back to ‘0’. To reset a Multiple Channel Read sequence beforehand, write ‘1’ to the MCRST bit.

	SSI	Counter	SSI & Counter
Data availability	When all channel conversions are complete	Instantly	SSI: When all channel conversions are completed Counter: Instantly
Data availability indication	MCRST = ‘1’	MCRST = ‘1’	MCRST = ‘1’ Counter data may already be read before MCRST = ‘1’

Table 5-12: Multiple Channel Read data availability

Example:

Channels 1-3 are configured for SSI mode, channels 4-6 are configured for counter mode. Channels 1, 4 and 6 are enabled for Multiple Channel Read. A write to the MCRTR bit starts the Multiple Channel Read. Channel 1 starts a conversion and the data of channels 4 and 6 are latched. The data of the enabled counter channels is instantly available and can be read at once. The SSI data is not available until MCRST is set to ‘1’. When all enabled channels were read, MCRST is reset to ‘0’.

There is no designated interrupt to indicate the completion of a Multiple Channel Read. Alternatively an interrupt can be set up for the SSI channel that takes the longest time to complete a conversion. If

only counter channels are read, an interrupt is not necessary because the counter data is instantly available.

5.5 Interval Timer

The interval timer is a 32 bit preloadable counter with a programmable clock rate. On activation the counter loads from the Interval Timer Preload Register und starts counting down. When the counter reaches zero, it generates an interrupt (if enabled), is automatically preloaded again and continues counting. The ITSET setting in the Interval Timer Control Register determines if the Interval Timer uses a prescaled clock or a time base.

Calculate the interval times using the prescaled clock with the following formula:

Interval Time = Value of Interval Timer Preload Register * Clock Period

ITDIV	Clock Frequency	Clock Period
00	8 MHz	125 ns
01	4 MHz	250 ns
10	2 MHz	500 ns
11	1 MHz	1 µs

Table 5-13: Interval Timer Clock Periods

Calculate the interval times using the time base with the following formula:

Interval Time = Value of Interval Timer Preload Register * Time Base

ITDIV	Time Base
00	100 ns
01	1 µs
10	1 ms
11	1 s

Table 5-14: Interval Timer Time Bases

The interval timer can be used as a reference timer in closed loop applications or as a trigger for a multiple channel read.

5.6 Isolated 24 V Digital Inputs

The TPMC117 offers one isolated digital 24 V input per channel. The inputs are electronically debounced. Each digital 24 V input can generate an interrupt, triggered on rising or falling edge. Depending on the selected counter reference mode the input can be used as a general purpose input or as a reference input.

5.7 SSI/Counter Input Filtering

To avoid false counts caused by noisy input signals, the encoder and digital inputs are digitally filtered. This filter is typical 3-stage debounce circuit. By default it runs with a 32 MHz sampling clock, resulting in input signals shorter ~100 ns being suppressed. To address input sources such as mechanical switches with longer bouncing times, an advanced debouncing can be enabled in the Adavanced Doubounceing Registers, where the time base for the 3-stage debounce circuit can be configured.

There are separate Advanced Debouncing Registers for the encoder and digital inputs. Advanced Debpouncing can be enabled separately for each encoder and digital input channel.

6 Hardware Interface

6.1 Encoder/Counter Input Wiring

The following schematic shows the principle input wiring for one encoder signal. There is a SPDT slide switches for each input signal that allows to select the input configuration. It can either be set to differential RS422 input mode with 120Ω termination, or to single-ended/TTL input configuration with a bias voltage for the unused A- input.

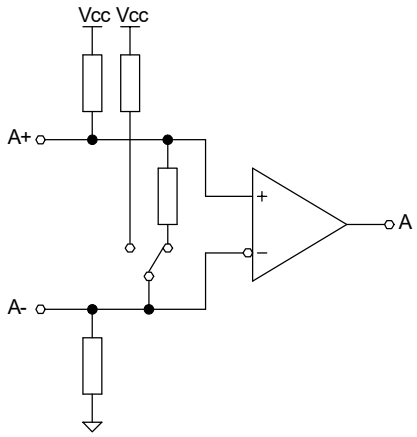


Figure 6-1: Input Wiring

6.1.1 Termination Resistor Slide Switches

The following picture highlights in red the positions of the slide switches. The slide switches a placed in groups of three, each group belonging to one of the six input channels. The channel association is from CH0 in the lower left clockwise to CH5 in the upper right.

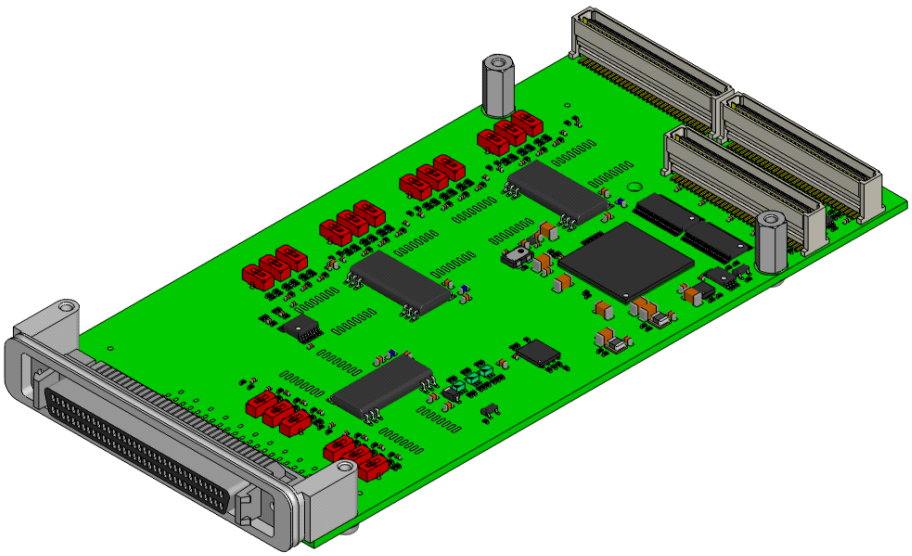


Figure 6-2: Termination Resistor Slide Switches

Each channel has three dedicated slides switches for its input signals.

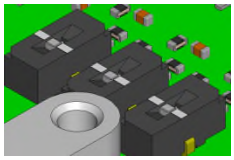
Switch	Signal
	← ENC_I / DATA
	← ENC_B / CLK_IN
	← ENC_A / -

Table 6-1: Silde Switch Signal Assignment

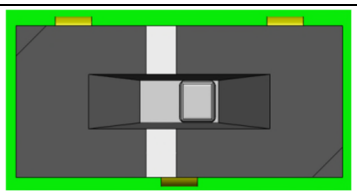
SPDT slide switch top view		
Switch Setting	ON (white marking)	OFF
Termination	Enabled	Disabled
Input Mode	Differential / RS422	Single-ended/TTL

Table 6-2: Slide Switch Settings

The Factory setting of the slide switch is OFF, hence the input configuration is single-ended/TTL.

6.1.2 Single-Ended / TTL

The following schematic shows the principle input wiring for one single-ended/TTL encoder signal. For single-ended/TTL input, leave the inverting input (A-) open and connect the TTL signal to the noninverting input (A+).

The120Ω termination resistor must be switched off when using single-ended/TTL input signals!

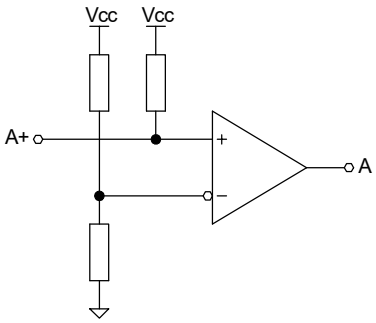


Figure 6-3: Single-ended Input Wiring

The switching point lies at approx. 1.5 V, with a hysteresis of about 0.4 mV.

6.1.3 Differential / RS422

The following schematic shows the principle input wiring for one differential/RS422 encoder signal. RS422 input signals should be terminated. The encoder input is fail-safe based, so that unused inputs can be left open.

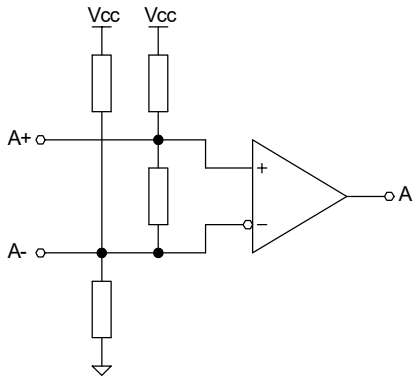


Figure 6-4: Differential Input Wiring

It is recommended to terminate differential/RS422 input signals.

6.2 Clock Output Wiring

Just like the encoder inputs, the TPMC117's clock outputs are isolated. The TPMC117's clock drivers are referenced to the isolated ground GND_I.[1]

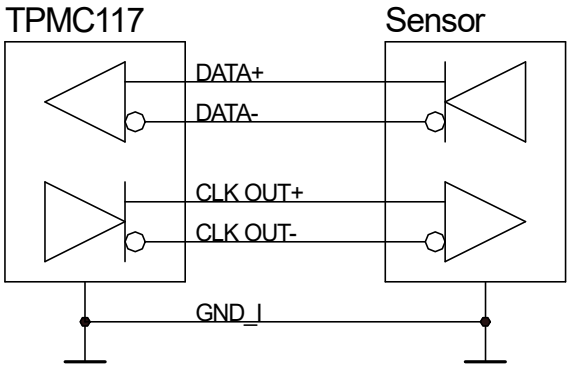


Figure 6-5: TPMC117 Clock Output Wiring

[1] Older Versions of the TPMC117 (V1.x) adhered to the original SSI specification that featured galvanic insulation with optocouplers, so that the clock inputs in the sensor did not need a ground reference. But nowadays the sensor's clock inputs are often built with conventional RS422 receivers, which require a ground reference. Since the TPMC117's clock drivers were referenced to circuit ground, which was not available on the connector, an external connection from the system ground to the sensor ground was required. The current TPMC117 versions no longer require this external ground connection.

6.3 Isolated 24 V Digital Input Characteristics

The TPMC117 offers one galvanically isolated digital 24 V input per channel. A high performance input circuit ensures a defined switching point and polarization protection against confusing the pole. The input characteristics of the inputs are compliant to IEC 61131-2 Type 3.

Parameter	Unit	Typical
Input voltage	V	24
Input current	mA	2.5 (at 24 V input voltage)
Switching level	V	10.5 (min. 8.5, max. 11.5)

Table 6-3: Digital Input Characteristics

7 Pin Assignment – I/O Connector

7.1 Front Panel I/O Connector

The TPMC117 front panel I/O connector is a HD68 SCSI-3 type female connector (e.g. AMP# 787082)

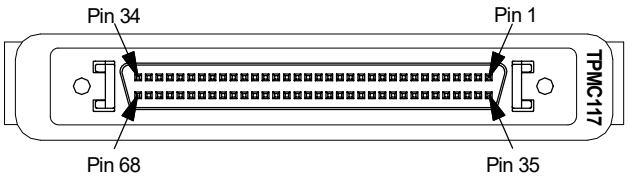


Figure 7-1: Front Panel I/O Connector

7.1.1 Front Panel I/O Pinout

Pin	SSI Signal	Counter Signal
1	-	ENC_A0+
2	CLK IN0+	ENC_B0+
3	DATA0+	ENC_I0+
4	CLK OUT0+	-
5	GND_I	
6	-	ENC_A1+
7	CLK IN1+	ENC_B1+
8	DATA1+	ENC_I1+
9	CLK OUT1+	-
10	-	ENC_A2+
11	CLK IN2+	ENC_B2+
12	DATA2+	ENC_I2+
13	CLK OUT2+	-
14	GND_I	
15	-	ENC_A3+
16	CLK IN3+	ENC_B3+
17	DATA3+	ENC_I3+
18	CLK OUT3+	-
19	-	ENC_A4+
20	CLK IN4+	ENC_B4+
21	DATA4+	ENC_I4+
22	CLK OUT4+	-
23	GND_I	
24	-	ENC_A5+
25	CLK IN5+	ENC_B5+
26	DATA5+	ENC_I5+
27	CLK OUT5+	-
28	-	
29	24 V Digital Input 0	
30	24 V Digital Input 1	
31	24 V Digital Input 2	
32	24 V Digital Input 3	
33	24 V Digital Input 4	
34	24 V Digital Input 5	

Pin	SSI Signal	Counter Signal
35	-	ENC_A0-
36	CLK IN0-	ENC_B0-
37	DATA0-	ENC_I0-
38	CLK OUT0-	-
39	GND_I	
40	-	ENC_A1-
41	CLK IN1-	ENC_B1-
42	DATA1-	ENC_I1-
43	CLK OUT1-	-
44	-	ENC_A2-
45	CLK IN2-	ENC_B2-
46	DATA2-	ENC_I2-
47	CLK OUT2 -	-
48	GND_I	
49	-	ENC_A3-
50	CLK IN3-	ENC_B3-
51	DATA3-	ENC_I3-
52	CLK OUT3-	-
53	-	ENC_A4-
54	CLK IN4-	ENC_B4-
55	DATA4-	ENC_I4-
56	CLK OUT4-	-
57	GND_I	
58	-	ENC_A5-
59	CLK IN5-	ENC_B5-
60	DATA5-	ENC_I5-
61	CLK OUT5-	-
62	-	
63	24 V Digital Input 0 GND	
64	24 V Digital Input 1 GND	
65	24 V Digital Input 2 GND	
66	24 V Digital Input 3 GND	
67	24 V Digital Input 4 GND	
68	24 V Digital Input 5 GND	

Table 7-1: Pin Assignment Front I/O Connector

7.2 P14 Back I/O Connector

The TPMC117 P14 Back I/O connector is Standard 64 pin Mezzanine Connector.

7.2.1 P14 Back I/O Pinout

Pin	SSI Signal	Counter Signal
1	-	ENC_A0+
3	CLK IN0+	ENC_B0+
5	DATA0+	ENC_I0+
7	CLK OUT0+	-
9	-	ENC_A1+
11	CLK IN1+	ENC_B1+
13	DATA1+	ENC_I1+
15	CLK OUT1+	-
17	-	ENC_A2+
19	CLK IN2+	ENC_B2+
21	DATA2+	ENC_I2+
23	CLK OUT2+	-
25	-	ENC_A3+
27	CLK IN3+	ENC_B3+
29	DATA3+	ENC_I3+
31	CLK OUT3+	-
33	-	ENC_A4+
35	CLK IN4+	ENC_B4+
37	DATA4+	ENC_I4+
39	CLK OUT4+	-
41	-	ENC_A5+
43	CLK IN5+	ENC_B5+
45	DATA5+	ENC_I5+
47	CLK OUT5+	-
49	GND_I	
51	GND_I	
53	24 V Digital Input 0	
55	24 V Digital Input 1	
57	24 V Digital Input 2	
59	24 V Digital Input 3	
61	24 V Digital Input 4	
63	24 V Digital Input 5	

Pin	SSI Signal	Counter Signal
2	-	ENC_A0-
4	CLK IN0-	ENC_B0-
6	DATA0-	ENC_I0-
8	CLK OUT0-	-
10	-	ENC_A1-
12	CLK IN1-	ENC_B1-
14	DATA1-	ENC_I1-
16	CLK OUT1-	-
18	-	ENC_A2-
20	CLK IN2-	ENC_B2-
22	DATA2-	ENC_I2-
24	CLK OUT2 -	-
26	-	ENC_A3-
28	CLK IN3-	ENC_B3-
30	DATA3-	ENC_I3-
32	CLK OUT3-	-
34	-	ENC_A4-
36	CLK IN4-	ENC_B4-
38	DATA4-	ENC_I4-
40	CLK OUT4-	-
42	-	ENC_A5-
44	CLK IN5-	ENC_B5-
46	DATA5-	ENC_I5-
48	CLK OUT5-	-
50	GND_I	
52	GND_I	
54	24 V Digital Input 0 GND	
56	24 V Digital Input 1 GND	
58	24 V Digital Input 2 GND	
60	24 V Digital Input 3 GND	
62	24 V Digital Input 4 GND	
64	24 V Digital Input 5 GND	

Table 7-2: Pin Assignment Back I/O Connector