The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC118

6 Channel Motion Control

Version 1.0

User Manual

Issue 1.0.7

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TPMC118-10

6 Channel Motion Control

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	March 2000
1.1	Changed Index Mode	July 2000
1.2	Correction Target Configuration EEPROM	February 2001
1.3	General Revision	March 2003
1.4	New address TEWS LLC	September 2006
1.5	Revision Figure “Detailed Motion Control Channel”	September 2006
1.6	General Revision	May 2008
1.0.7	New notation of User Manual Issue	June 2012

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1 Product Description

The standard single-width 32 bit PMC module TPMC118 is designed for motion control applications offering six independent channels. Each channel consists of a TTL / RS422 compatible encoder interface, one digital 24V input and one +/-10V analog output.

The position feedback for each of the six channels is provided by an encoder interface and a 32 bit up/down counter with preload and latch register. The input level of the encoder signals can be TTL or RS422. All six encoder interfaces are isolated from the local controller unit by high speed optocouplers. An on board DC/DC converter supplies the isolated part. The encoder signals pass a digital filter for noise suppression before they are fed to the counters and reference logic. The counters are programmable for single, double and quadruple analysis of the encoder signals. The maximum frequency of the encoder inputs is 2 MHz.

An 'auto reference mode' provides the possibility of automatic preload of the encoder counter during normal operation, whenever the motion system passes the reference position.

Each of the six motion control channels of the TPMC118 offers one digital 24V input which is galvanically isolated by optocoupler. A high performance input circuit ensures a defined switching point and polarization protection against confusing the pole. The input has an electronic debounce circuit. Each of the six digital 24V inputs can generate an interrupt, triggered on rising or falling edge. Depending on the selected mode the input can be used as general purpose input or reference input.

The +/-10V analog output of each channel is realized by a 16 bit digital to analog converter (DAC). An operational amplifier is used to drive high capacitive loads and to protect the DAC's.

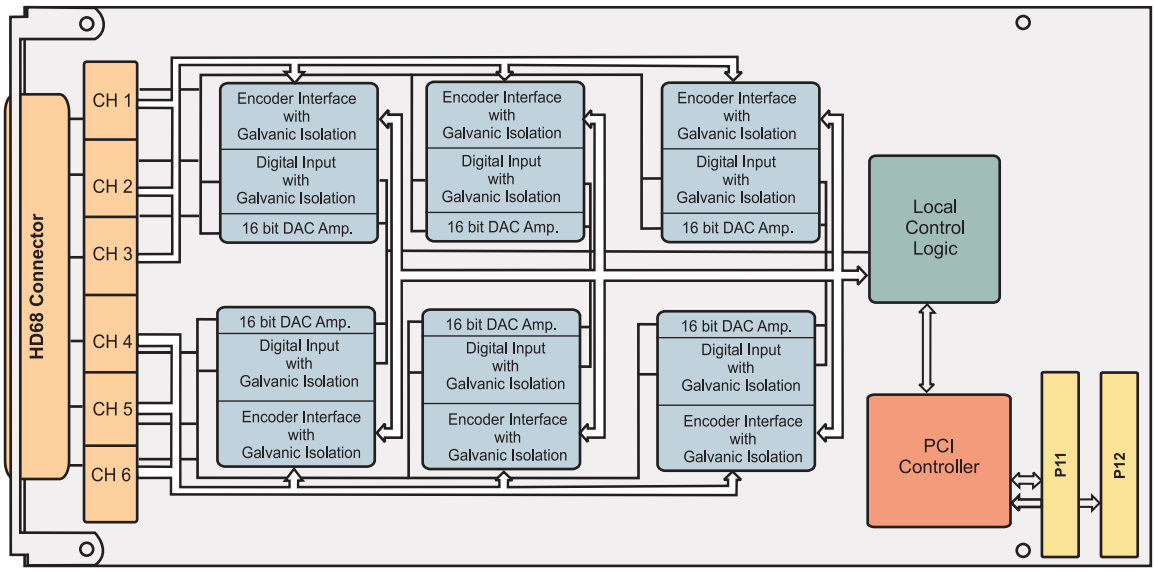

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size	
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9050-1 (PLX Technology)	
Module Specific Data		
Number of Encoder Inputs	6 channels with A, A#, B, B#, I, I#	
Encoder Counter	32 bit up/down counter with preload and output register	
Interface	Isolated RS422 or TTL level	
Encoder Input Frequency	Up to 2 MHz	
Isolation	Optocoupler for galvanic isolation, on board DC/DC converter to supply isolated part of encoder interface	
Number of Digital Inputs	6 digital inputs: reference input or general purpose input depending on mode	
Input Voltage	24V DC typical	
Input Current	4.2mA @24V input voltage	
Input Switching Level	12V typical, 7.5V minimum, 14V maximum	
Number of Analog Outputs	6 analog outputs: 16 bit DAC's followed by OpAmp.	
Analog Output Voltage	+/-10V	
Analog Output Current	+/-6mA maximum	
DAC Access Time	350ns minimum between two PCI accesses to Analog Output Register	
DAC Settling Time	Typical 8µs for voltage steps from negative full scale to full scale	
I/O Interface		
I/O Connector	HD68 SCSI-3 type connector	
Physical Data		
Power Requirements	60mA typical @+3.3V DC 250mA typical @ +5V DC 5mA typical @+12V DC 10mA typical @-12V DC	
Temperature Range	Operating Storage	0 °C to +70 °C -40°C to +125°C
MTBF	404000 h	
Humidity	5 – 95 % non-condensing	
Weight	78 g	

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9050 local spaces.

PCI9050 Local Space	PCI9050 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0 (0x10)	MEM	128	32	LITTLE	Local Configuration Registers
1	1(0x14)	I/O	128	32	LITTLE	Local Configuration Registers
2	2 (0x18)	MEM	64	32	BIG (upper lane)	Local Address Space 0
3	3 (0x1C)	-	-	-	-	Local Address Space 1
4	4 (0x20)	-	-	-	-	Local Address Space 2
5	5 (0x24)	-	-	-	-	Local Address Space 3
6	6 (0x30)	-	-	-	-	Local Expansion ROM Space

Table 3-1 : PCI9030 Local Space Configuration

3.2 Local Register Space 1

PCI Base Address: PCI9050 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).

Offset to PCI Base Address 2	Register Name	Access	Size (Bit)
0x0000	Global Control / Status Register	R/W	32
0x0004	Encoder Control / Status Register	R/W	32
0x0008	Interrupt Control / Status Register	R/W	32
0x000C	Input Register	R	32
0x0010	Encoder Counter Preload / Data Register 1	R/W	32
0x0014	Encoder Counter Preload / Data Register 2	R/W	32
0x0018	Encoder Counter Preload / Data Register 3	R/W	32
0x001C	Encoder Counter Preload / Data Register 4	R/W	32
0x0020	Encoder Counter Preload / Data Register 5	R/W	32
0x0024	Encoder Counter Preload / Data Register 6	R/W	32
0x0028	Analog Output Register 1	R/W	32
0x002C	Analog Output Register 2	R/W	32
0x0030	Analog Output Register 3	R/W	32
0x0034	Analog Output Register 4	R/W	32
0x0038	Analog Output Register 5	R/W	32
0x003C	Analog Output Register 6	R/W	32

Table 3-2 : Local Register Space 1

After power-on or reset all read/write registers are cleared to ‘0’.

3.2.1 Local Register Read/Write

The local register design is developed for a long word (32 bit) read/write access. A byte or word access could fail. After power-on or reset all read/write registers are cleared to ‘0’.

3.2.2 Global Control / Status Register

The Global Control / Status Register is a read/write register.

Bit	Symbol	Description	Access	Reset Value
31:7		Not used and undefined during reads		
6		Master Interrupt Enable bit 1 = enables interrupts for the six digital 24V inputs 0 = disables interrupts The digital 24V inputs generate interrupts at pin INTA# of the PMC bus.	R/W	
5:0		Preload of the corresponding encoder counter possible only in "NONE Reference Mode" (encoder interface 1 to 6) 1 = preload access 0 = no preload After preload access is executed all these bits are cleared automatically and signal a successful preload. Before using the preload method, the corresponding Encoder Counter Register must be loaded with valid data.	R/W	

Table 3-3 : Global Control / Status Register

Additional to this Global Interrupt Enable the interrupt INTA' must be enabled in the Interrupt Control / Status Register (INTCSR; 0x4C) of the PCI Controller PCI9050-1. Default after power-on and reset: INTA# is enabled.

3.2.3 Encoder Control / Status Register

The Encoder Control / Status Register is a 32 bit wide read/write register.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31</td><td></td><td>Not used and undefined during reads</td><td></td><td></td></tr>
<tr><td>30</td><td></td><td>Simultaneous Load Status
1 = is set after a simultaneous load access
0 = is set after the last read access to one of the enabled and latched Encoder Counter Data Registers.</td><td>R/W</td><td></td></tr>
<tr><td>29:28</td><td>Channel 6</td><td rowspan="7">Reference Control Mode (2 bit for each channel)
<table><tr><th colspan="2">Value</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>None reference mode</td></tr><tr><td>0</td><td>1</td><td>Reference mode</td></tr><tr><td>1</td><td>0</td><td>Auto reference mode</td></tr><tr><td>1</td><td>1</td><td>Index mode</td></tr></table>More information see below.</td><td rowspan="7">R/W</td><td rowspan="7"></td></tr>
<tr><td>27:26</td><td>Channel 5</td></tr>
<tr><td>25:24</td><td>Channel 4</td></tr>
<tr><td>23:22</td><td>Channel 3</td></tr>
<tr><td>21:20</td><td>Channel 2</td></tr>
<tr><td>19:18</td><td>Channel 1</td></tr>
<tr><td>17:16</td><td>Channel 6</td><td rowspan="4">Encoder Counter Clock Generation bits are used for each encoder interface 1…6 (2 bit for each channel)
<table><tr><th colspan="2">Value</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>Disable Counter</td></tr><tr><td>0</td><td>1</td><td>1x – single</td></tr></table></td><td rowspan="4">R/W</td><td rowspan="4"></td></tr>
<tr><td>15:14</td><td>Channel 5</td></tr>
<tr><td>13.12</td><td>Channel 4</td></tr>
<tr><td>11:10</td><td>Channel 3</td></tr>
</table>

<table>
<tr><td>9:8</td><td>Channel 2</td><td rowspan="2">
<table>
<tr><td>1</td><td>0</td><td>2 x – double</td></tr>
<tr><td>1</td><td>1</td><td>3 x - quadruple</td></tr>
</table>
More information see below.
</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td>7:6</td><td>Channel 1</td></tr>
<tr><td>5</td><td>Encoder Counter 6</td><td rowspan="6">Enable simultaneous load for the corresponding encoder counter for each channel 1..6
1 = enables simultaneous load
0 = disables corresponding encoder counter
Counter values of all enabled channels are latched during a read access to one of the enabled Encoder Counter Data Registers. After such a ‘Latch Access’ the other enabled and latched Encoder Counter Data Registers can be read one after another. A new simultaneous load is only possible after reading the Encoder Counter Data Register of all enabled channels.</td><td rowspan="6">R/W</td><td rowspan="6"></td></tr>
<tr><td>4</td><td>Encoder Counter 5</td></tr>
<tr><td>3</td><td>Encoder Counter 4</td></tr>
<tr><td>2</td><td>Encoder Counter 3</td></tr>
<tr><td>1</td><td>Encoder Counter 2</td></tr>
<tr><td>0</td><td>Encoder Counter 1</td></tr>
</table>

Table 3-4 : Encoder Control / Status Register

3.2.3.1 Encoder counter

The encoder counter can be programmed to interpret the encoder inputs as 1x, 2x or 4x as described below: The maximum encoder input frequency is 2 MHz. In 4x mode the encoder counter counts with max. 8 MHz.

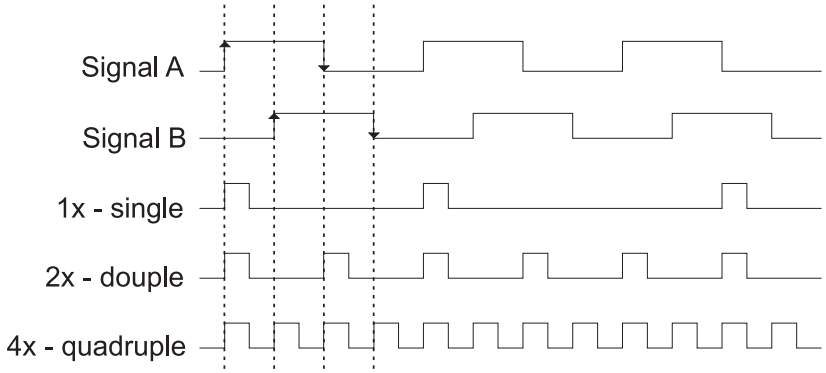

Figure 3-1 : Encoder inputs

3.2.3.2 Reference Mode Control

3.2.3.2.1 None Reference Mode

In this mode there is no automatic preload of the encoder counter possible. To make an encoder counter preload in this mode, a write access to the Global Control / Status Register (bit 0 to 5) is necessary.

3.2.3.2.2 Reference Mode

This mode controls the encoder counter with the corresponding digital 24V input (used as reference input) and the encoder index signal. A specified reference input signal and a following index impulse produce a counter preload. The host software must set the motion direction during such a reference access to backwards.

The following figure shows the two normal preload accesses. An encoder motion area with eleven index pulses and the corresponding reference input is described as an example.

Two different ‘start positions’ (1a and 1b) are shown.

Position 1a

Direction is forward and the reference input is active. The host software must move into the area where the reference input is inactive. Now the direction must be changed. The next index pulse after entering the area with reference input active triggers the preload function for the encoder counter.

Position 1b

Direction is backwards and the reference input is inactive. The host software must move further backwards, and after entering the area with reference input active the next index pulse triggers the preload function for the encoder counter.

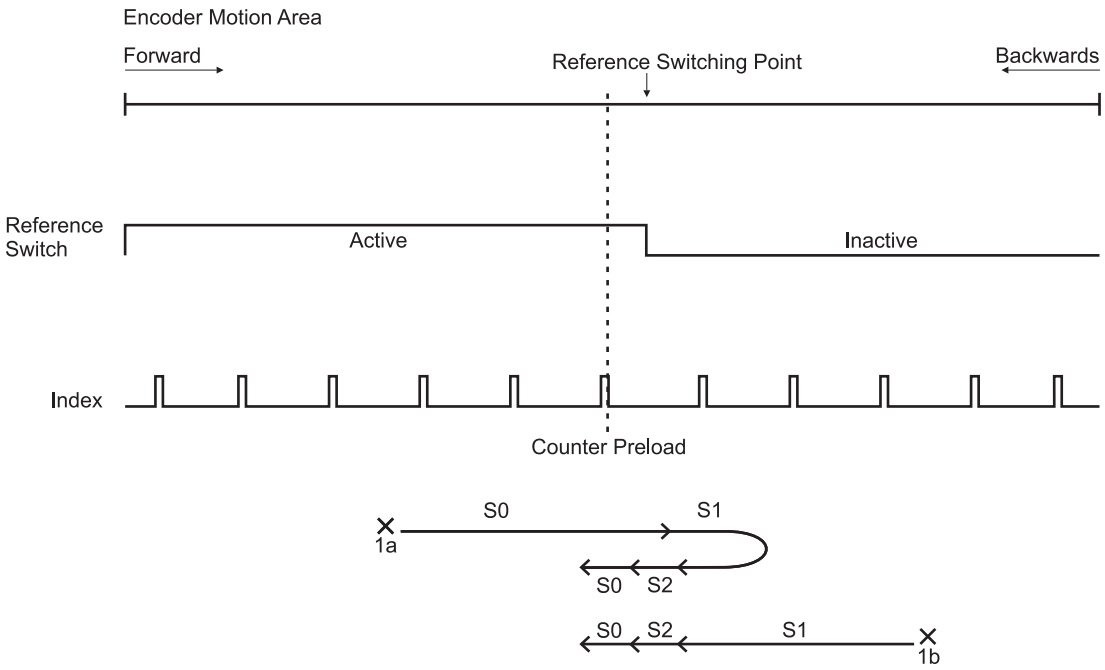

Figure 3-2 : Encoder preload example

A correct execution of the reference function can be monitored in the Encoder Control / Status Register. After successful execution the mode of this encoder is set from bit combination ‘01’ (Reference Mode) to ‘00’ (None Reference Mode).

3.2.3.2.3 Auto Reference Mode

This mode is the automation of the Reference Mode. That means every time if the reference switching point and a following index pulse are crossed during backward direction, a new preload is generated. In “Auto Reference Mode” there is no change of the mode in the Encoder Control / Status Register!

3.2.3.2.4 Index Mode

In this mode the digital 24V input is not used. Only the index impulse produces a counter preload. After setting this mode the next occurrence of the index signal independent from direction the counter will preload. A correct execution of this preload function can be monitored in the Encoder Control / Status Register. After successful execution the mode of this encoder is set from bit combination ‘11’ (Index) to ‘00’ (None Reference Mode).

3.2.4 Interrupt Control / Status Register

The Interrupt Control / Status Register is a 32 bit wide read/write register.

Bit	Symbol	Description	Access	Reset Value
31:18		Not used and undefined during reads		
17	Input 6	Interrupt Control bit is used to select interrupt on rising or falling edge for corresponding 24V input. 1 = enables interrupt for rising edge 0 = enables interrupt for falling edge	R/W	
16	Input 5			
15	Input 4			
14	Input 3			
13	Input 2			
12	Input 1			
11	Input 6	Interrupt Status bit reflects the interrupt input status of the corresponding 24V inputs. 1 = interrupt request is pending 0 = no interrupt request is pending An interrupt request for a specific digital 24V input is cleared by writing '1' to the according bit.	R/W	
10	Input 5			
9	Input 4			
8	Input 3			
7	Input 2			
6	Input 1			
5	Input 6	Interrupt Enable bit for corresponding 24V input 1 = enables interrupts 0 = disables interrupts	R/W	
4	Input 5			
3	Input 4			
2	Input 3			
1	Input 2			
0	Input 1			

Table 3-5 : Interrupt Control / Status Register

The following table shows a short overview about enable interrupts and the active trigger edge:

Digital 24V Input	Bit	Interrupt		Bit	Active Edge	
		Disable	Enable		Falling	rising
IN1	0	0	1	12	0	1
IN2	1	0	1	13	0	1
IN3	2	0	1	14	0	1
IN4	3	0	1	15	0	1
IN5	4	0	1	16	0	1
IN6	5	0	1	17	0	1

Table 3-6 : Input Interrupt Configuration

3.2.5 Data Input Register

The Data Input Register is a 32 bit wide read only register. The Data Input Register is always active and reflects the actual state of the digital 24V inputs at all time.

Bit	Symbol	Description	Access	Reset Value
31:6		Not used and undefined during reads		
5	Channel 6	In "**None Reference Mode**" and "**Index Mode**" the digital 24V inputs can be used as general purpose inputs. In "**Reference Mode**" and "**Auto Reference Mode**" the digital 24V inputs are used as reference inputs.	R	
4	Channel 5			
3	Channel 4			
2	Channel 3			
1	Channel 2			
0	Channel 1			

Table 3-7 : Data Input Register

3.2.6 Encoder Counter Preload / Data Registers (Channel 1…6)

The Encoder Counter Preload / Data Register are 32 bit wide read/write registers.

Bit	Symbol	Description	Access	Reset Value
31:0		32 bit register for each counter Write into Encoder Counter PRELOAD Register Read from Encoder Counter DATA Register	R/W	

Table 3-8 : Encoder Counter Preload / Data Registers

In write access the digital preload value is loaded into the Encoder Counter Preload Register. The Encoder Counter Preload Register is used in all modes for reference preload.

In the read access the actual counter value is latched into the Encoder Counter Data Register.

If the simultaneous load feature is used for the Encoder Counter Data Registers one read access latches all counter values for the enabled counter at the same time. Then the Encoder Counter Data Registers can be read one after the other. A new simultaneous load access is only possible after finish reading all latched Encoder Counter Data Registers.

3.2.7 Analog Output Registers (Channel 1…6)

The Analog Output Registers are 32 bit wide read/write registers. One 32 bit register for each DAC output (DAC_OUT1 … DAC_OUT6). The analog output device is a 16 bit DAC.

Bit	Symbol	Description	Access	Reset Value
31:16		Not used and undefined during reads		
15:0		Digital value for analog output voltage Writing a digital value sets the analog output voltage. In read access the register reflects the digital value of the analog output voltage. Bit 0 = LSB, bit 15 = MSB of the digital value. One LSB stands for 0.31mV.	R/W	

Table 3-9 : Analog Output Registers

The following table shows some special digital values with the corresponding analog output voltage:

DAC Data Coding		
Data	**Analog Output Voltage**	
0x7FFF	Full Scale – 1LSB	9.9997V
0x4000	¾ Scale	5V
0x0001	Mdiscale + 1 LSB	0.0003V
0x0000	Midscale	0V
0xFFFF	Midscale – 1 LSB	-0.0003V
0xC000	¼ Scale	-5V
0x8000	Negative Full Scale	-10V

Table 3-10: Samples of Analog Output Voltage

After power-on or reset the value of all output registers are cleared to '0'. The analog output voltage is set to Midscale 0V DC.

The settling time for voltage steps from negative to positive full scale or obversely is typically 8µs and maximum 10µs.

The interval between two PCI accesses to the Analog Output Register should not be shorter than 350ns.

4 PCI9050 Target Chip

4.1 PCI Configuration Registers (CFG)

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	0076 1498
0x04	Status				Command				Y	0280 0000
0x08	Class Code						Revision ID		N	FF0000 XX
0x0C	BIST		Header Type		PCI Latency Timer		Cache Line Size		Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers								Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers								Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0								Y	FFFFFFC0
0x1C	PCI Base Address 3 for Local Address Space 1								Y	00000000
0x20	PCI Base Address 4 for Local Address Space 2								Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3								Y	00000000
0x28	PCI CardBus Information Structure Pointer								N	00000000
0x2C	Subsystem ID				Subsystem Vendor ID				N	000A 1498
0x30	PCI Base Address for Local Expansion ROM								Y	00000000
0x34	Reserved						New Cap. Ptr.		N	000000 00
0x38	Reserved								N	00000000
0x3C	Max_Lat		Min_Gnt		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00

Table 4-1 : PCI9050 Header TPMC118-10

4.1.1 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9050 PCI Base Address Initialization:

- Write 0xFFFF_FFFF to the PCI9050 PCI Base Address Register
- Read back the PCI9050 PCI Base Address Register
- For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space:

  Bit 0 = '0' requires PCI Memory Space mapping

  Bit 0 = '1' requires PCI I/O Space mapping

  For the PCI Expansion ROM Base Address Register, check bit 0 for usage:

  Bit 0 = '0': Expansion ROM not used

  Bit 0 = '1': Expansion ROM used
- Or PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to ‘1’, the PCI 9050 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).

- Determine the base address and write the base address to the PCI9050 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9050 PCI Base Address Register.

  After programming the PCI9050 PCI Base Address Registers, the software must enable the PCI9050 for PCI I/O and/or PCI Memory Space access in the PCI9050 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9050, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9050, set bit 1 to '1'.

For more information please refer to the PCI90-50-1 data sheet which is part of the TMPC118-ED Engineering Documentation.

4.2 Local Configuration Register (LCR)

After reset, the PCI9050 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9050 Local Configuration Registers is :

PCI9050 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9050 PCI Configuration Register Space) or

PCI9050 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9050 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9050 Local Configuration Registers.

PCI (Offset from Local Base Address)	Register	Value
0x00	Local Address Space 0 Range	0x0FFFFFC0
0x04	Local Address Space 1 Range	0x00000000
0x08	Local Address Space 2 Range	0x00000000
0x0C	Local Address Space 3 Range	0x00000000
0x10	Local Exp. ROM Range	0x00000000
0x14	Local Re-map Register Space 0	0x00000001
0x18	Local Re-map Register Space 1	0x00000000
0x1C	Local Re-map Register Space 2	0x00000000
0x20	Local Re-map Register Space 3	0x00000000
0x24	Local Re-map Register ROM	0x00000000
0x28	Local Address Space 0 Descriptor	0x1B17900
0x2C	Local Address Space 1 Descriptor	0x00000000
0x30	Local Address Space 2 Descriptor	0x00000000
0x34	Local Address Space 3 Descriptor	0x00000000
0x38	Local Exp. ROM Descriptor	0x00000000
0x3C	Chip Select 0 Base Address	0x00000021
0x40	Chip Select 1 Base Address	0x00000000
0x44	Chip Select 2 Base Address	0x00000000
0x48	Chip Select 3 Base Address	0x00000000
0x4C	Interrupt Control/Status	0x00000043
0x50	Miscellaneous Control Register	0x00780000

Table 4-2 : PCI9050 Local Configuration Registers

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9050 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x0F : PCI9050 PCI Configuration Register Values
- Address 0x10 to 0x64 : PCI9050 Local Configuration Register Values
- Address 0x65 to 0x7C : Not used
- Address 0x7E + 0x7F : TPMC variant

See the PCI9050 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x0076	0x1498	0x1180	0x0000	0x000A	0x1498	0x0000	0x0100
0x10	0x0FFF	0xFFC0	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x20	0x0000	0x0000	0x0000	0x0001	0x0000	0x0000	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x01B1	0x7900	0x0000	0x0000
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0021
0x50	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0043
0x60	0x0078	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x70	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0x000A

Table 4-3 : Configuration EEPROM TPMC118-10

4.4 Local Software Reset

The PCI9050 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9050 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9050 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9050 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9050 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9050 PCI and Local Configuration Registers are not reset. The PCI9050 PCI Interface is not reset.

The PCI-9050 LRESET# pin is connected to the TPMC118 on board logic's master reset.

4.5 PCI Interrupt Control/Status

For disabling / enabling PCI interrupts set bit 6 of the PCI9050 Interrupt Control/Status Register (INTCSR, 0x4C) to '0' / '1'. Do not change any other bits of this register.

5 Configuration Hints

5.1 Local Space Endian Mode

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Table 5-1: Local Bus Little/Big Endian

Standard use of the TPMC118:

Local Address Space 0	32 bit Bus in Big Endian Mode
Local Address Space 1	not used
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

For further information please refer to the PCI9050 manual which is also part of the TPMC118-ED Engineering Documentation.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

Short cut Offset	Name	
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 0 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 0 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 0 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

6 Installation

6.1 Detailed Motion Control Channel

Each of the six motion control channels of the TPM118 is built up as shown below:

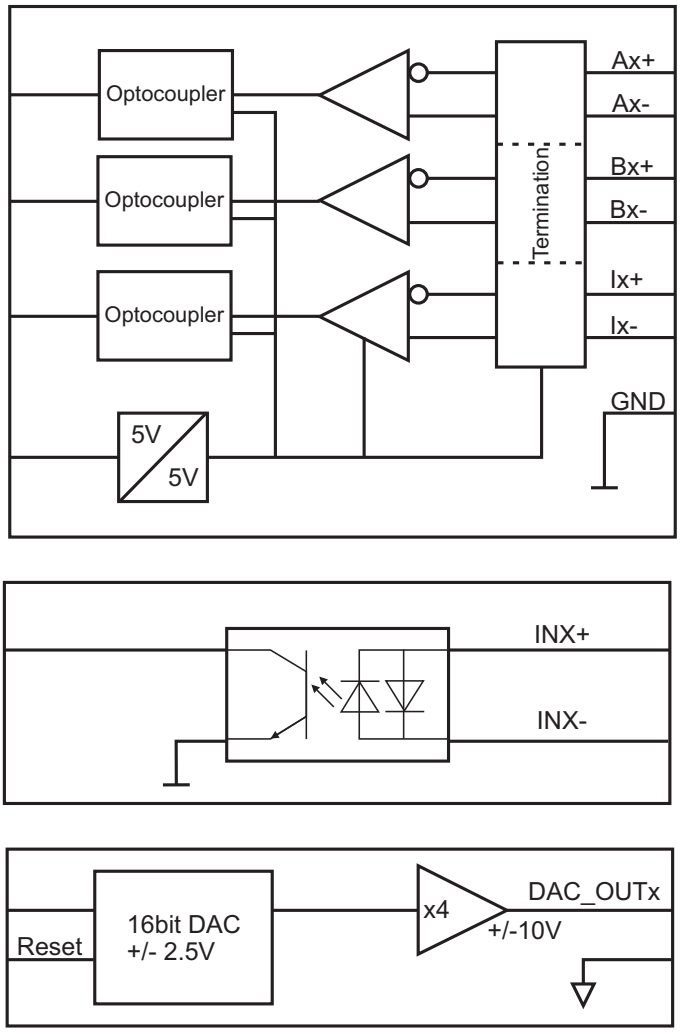

Figure 6-1 : Detailed Motion Control Channel

The motion control channel consists of:

- Encoder input with 3 differential RS422 / TTL signals
- 1 digital 24V reference input with galvanic isolation used as general purpose input or reference input
- 1 analog output, 16 bit, +/-10V DC.

6.2 Encoder Wiring

The following figure shows the principle encoder input wiring for one channel and one encoder signal. In the example the encoder signal A1 is shown.

The RS422 / TTL input signal is terminated and connected to a differential RS422 driver. The optocoupler builds a galvanically isolation. To allow the maximum input frequency of 2 MHz high speed optocouplers are used for the encoder inputs.

The termination voltage and the supply voltage for the driver are supplied by an on board DC/DC converter.

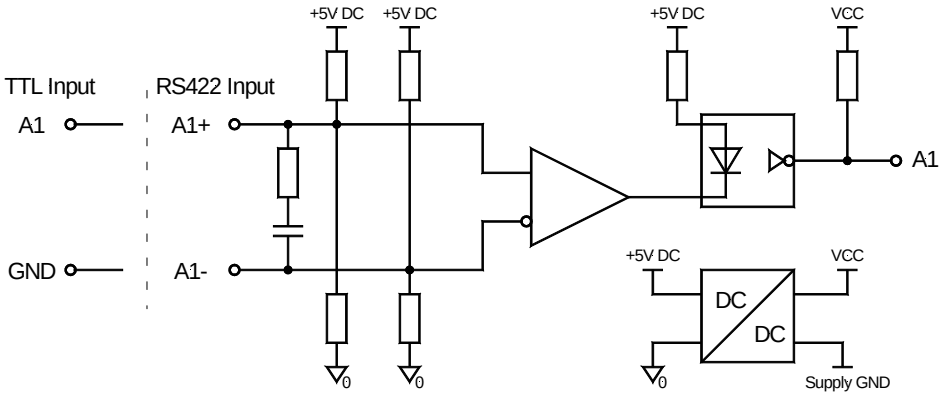

Figure 6-2 : Encoder Input Wiring

6.3 Input Wiring

The digital 24V inputs are also isolated to the local controller by optocoupler. The input circuit ensures a defined switching point and polarization protection against confusing the pole. The switching levels are defined as 7.5V minimum, 14V maximum and 12V typical.

This Input Data Register reflects the state of all digital 24V inputs at any time independent of the mode resp. use as reference input or general purpose input.

The following figure shows the input wiring of one digital 24V input.

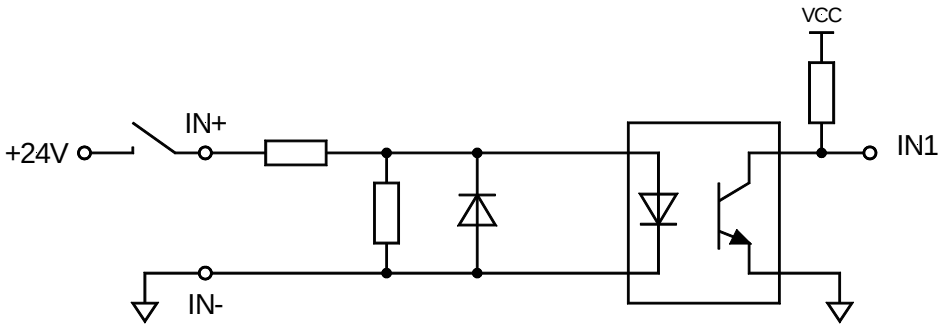

Figure 6-3 : Input Wiring

6.4 Output Wiring

The DAC is used to generate the +/-10V analog output voltage. The operational amplifier is able to drive high capacitance loads and protects the DAC.

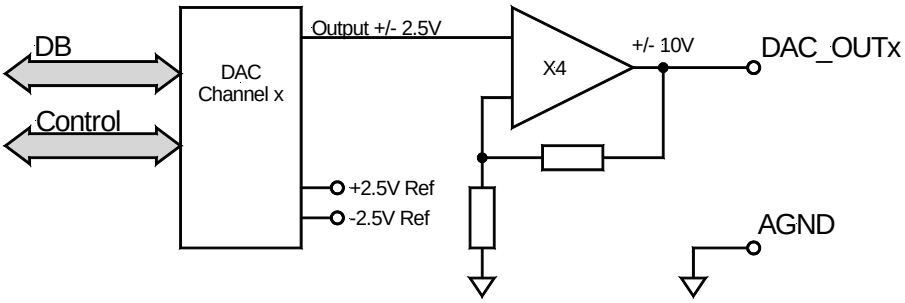

Figure 6-4 : Output Wiring

7 Pin Assignment – I/O Connector

7.1 X1 Front Panel I/O Connector

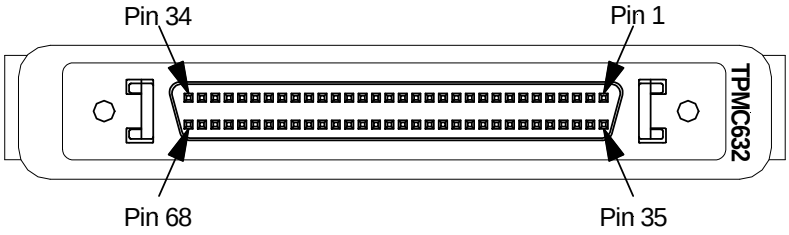

Figure 7-1 : Front Panel I/O Connector Numbering

7.1.1 Connector Type

Pin-Count	68
Connector Type	HD68 SCSI-3 type female connector
Source & Order Info	AMP 787082-7 or compatible

7.1.2 Pin Assignment

Pin	Signal RS422	Signal TTL
1	A1+	A1
2	B1+	B1
3	I1+	I1
4	A2+	A2
5	B2+	B2
6	I2+	I2
7	GND	
8	A3+	A3
9	B3+	B3
10	I3+	I3
11	A4+	A4
12	B4+	B4
13	I4+	I4
14	GND	
15	A5+	A5
16	B5+	B5
17	I5+	I5
18	A6+	A6
19	B6+	B6
20	I6+	I6

Pin	Signal RS422	Signal TTL
35	A1-	GND
36	B1-	GND
37	I1-	GND
38	A2-	GND
39	B2-	GND
40	I2-	GND
41	GND	
42	A3-	GND
43	B3-	GND
44	I3-	GND
45	A4-	GND
46	B4-	GND
47	I4-	GND
48	GND	
49	A5-	GND
50	B5-	GND
51	I5-	GND
52	A6-	GND
53	B6-	GND
54	I6-	GND

Pin	Signal RS422	Signal TTL
21	GND	
22	IN1 +	
23	IN2 +	
24	IN3 +	
25	IN4 +	
26	IN5 +	
27	IN6 +	
28	NC	
29	DAC_OUT1	
30	DAC_OUT2	
31	DAC_OUT3	
32	DAC_OUT4	
33	DAC_OUT5	
34	DAC_OUT6	

Pin	Signal RS422	Signal TTL
55	GND	
56	IN1 -	
57	IN2 -	
58	IN3 -	
59	IN4 -	
60	IN5 -	
61	IN6 -	
62	NC	
63	AGND	
64	AGND	
65	AGND	
66	AGND	
67	AGND	
68	AGND	

Table 7-1 : Pin Assignment I/O Connector