The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC160

Automotive Sensor Simulator

Version 1.1

User Manual

Issue 1.1.0

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TPMC160-10R

Automotive Sensor Simulator

(RoHS compliant)

Issue	Description	Date
0.9.0	Preliminary issue	June 2021
1.0.0	Initial issue	August 2021
1.0.1	- The PSI5 Microcut Rejection Time detection and the associated interrupts have been removed. The detection was not deterministic. - The description for the PSI5 SYNC Data Registers has been extended. - The Protocol Setup Examples were revised.	October 2021
1.0.2	- Description of the Board health register has been improved - The description of the interrupt status registers was added - Corrected I/O Connector description	July 2022
1.0.3	- Clarified the “Cycle Register” behavior when it gets new values. - Description of the PWM Protocol Register has been enhanced.	July 2024
1.0.4	Added “7.1.4 Typical Test and Application Circuit”	August 2024
1.1.0	- Corrected ADC Data Register Reserved Bits Index - Added the new “Extended Cycle” and “Extended TP” functionality to the “5.3.1 Register Map” - Added the register descriptions of the “5.3.10 Extended Timer Registers” - Updated Firmware Identification Register	September 2025

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1 Product Description

The TPMC160 is a standard single-width 32 bit PMC module and supports a 33 MHz / 32-bit universal (5 V / 3.3 V) PCI interface.

The TPMC160 offers eight isolated automotive sensor simulator channels, which can act as a PSI5 or as wheel speed sensor. The sensor simulation supports a current sink with three adjustable levels. It also features PSI5 Sync and Reset pulse detection. The sensor simulation channels are isolated against the system and against each other.

PSI5 support includes PSI5-P, -U and -D bus topologies and both 125 kbps and 189 kbps transmission rates. Asynchronous and Variable Time Triggered Synchronous Operation Modes are supported.

Wheel speed sensor support covers two- and three current levels sensors, sensors with additional status information and the “AK-protocol”.

All TPMC160 signals are accessible through a HD50 SCSI-2 type front I/O connector.

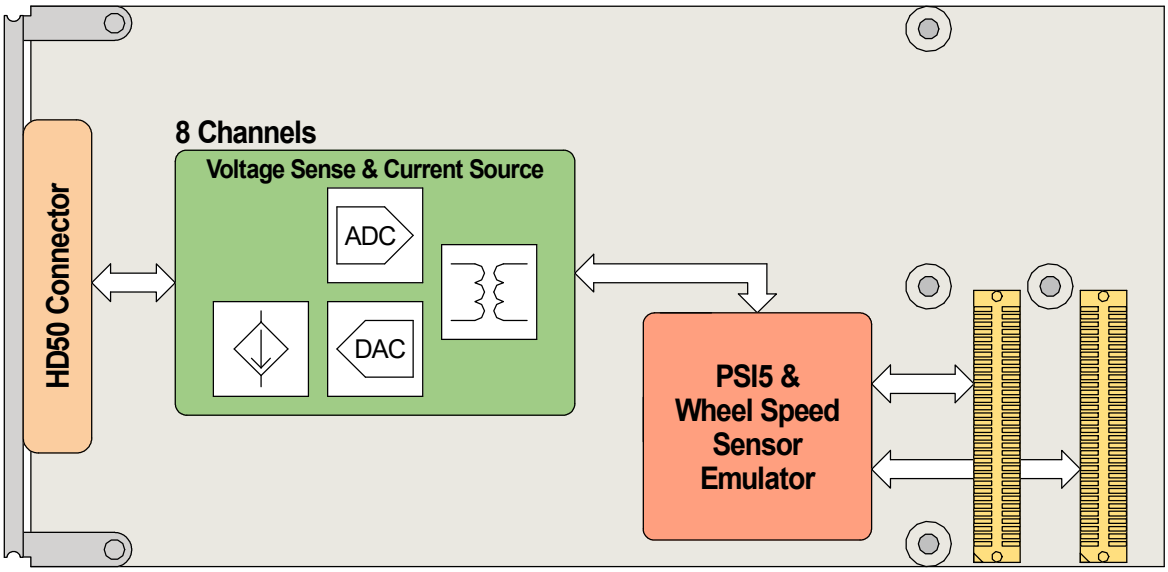


Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size (149 mm x 74 mm)
Electrical Interface	PCI Rev. 3.0 compliant 33 MHz / 32 bit PCI 3.3 V and 5 V PCI Signaling Voltage

On Board Devices	
PCI Target Chip	Artix-7 FPGA with PCI core

I/O Interface	
Number of Channels	8
I/O Standards	PSI5 Wheel Speed Sensor
Sensor Supply	4-24 V
I/O Connector	HD50 SCSI-2 type connector (e.g. AMP# 787395-5)

Physical Data		
Power Requirements	450 mA typical @ +5 V	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	369 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	77 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

3.2 Power Dissipation

This PMC module requires adequate forced air cooling!

3.3 Ground for Isolated I/O

I/O Connector's isolated ground signals must be connected to external ground.

4 Terms and Definitions

4.1 Register Bit Access Types

Register Bit Access Type		Description
R	Read	The bit is readable by software
R/W	Read/Write	The bit is readable and writeable by software
R/C	Read/Clear	The bit is readable by software The bit is set by firmware Software may clear the bit by writing a '1'
R/S	Read/Set	The bit is readable by software Software may set this bit to '1' The bit is cleared by firmware

When reading reserved register bits, the read value is undefined.

For future software compatibility: For register write access reserved bits shall be written '0'.

4.2 Style Conventions

Hexadecimal characters are specified with prefix 0x (i.e. 0x029E).

For signals on hardware products, "Active Low" is represented by the signal name with an added # (i.e. IP_RESET#).

5 PCI Interface

5.1 Identifiers

Vendor-ID	0x1498 (TEWS Technologies)
Device-ID	0x00A0 (TPMC160)
Class Code	0x118000 (Other data acquisition/signal processing controllers)
Subsystem Vendor-ID	0x1498 (TEWS Technologies)
Subsystem Device-ID	0x000A (TPMC160-10R)

Table 5-1 : PCI Identifiers

5.2 PCI Base Address Register Configuration

PCI Base Address Register (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	4096	32	Little	Register Space

Table 5-2 : PCI Base Address Registers

5.3 Register Space

5.3.1 Register Map

PCI Base Address Register 0 Offset	Description	Size (Bit)
Common Protocol Registers		
0x000	Channel Control Register	32
0x004 - 0x020	Current Level Registers	32
0x024 - 0x030	ADC Data Registers	32
0x034 - 0x04C	Reserved	32
Custom Protocol Registers		
0x050 - 0x06C	CP Cycle Registers	32
0x070	CP FIFO Status Register	32
0x074 - 0x090	CP FIFO Data Registers	32
0x094 - 0x0AC	Reserved	32
Square Wave Protocol Registers		
0x0B0 - 0x0CC	SWP Cycle Registers	32
0x0D0 - 0x11C	Reserved	32
PWM Protocol Registers		
0x120 - 0x13C	PWM Cycle Registers	32
0x140 - 0x15C	Reserved	32

PCI Base Address Register 0 Offset	Description	Size (Bit)
AK / VDA Protocol Registers		
0x160 - 0x17C	AK Cycle Registers	32
0x180 - 0x19C	AK Control Registers	32
0x1A0 - 0x21C	Reserved	32
PSI5 Mode Registers		
0x220 - 0x23C	PSI5 Cycle Registers	32
0x240	PSI5 Interrupt Status Register	32
0x244 - 0x260	PSI5 Status Registers	32
0x264 - 0x280	PSI5 Detection Registers	32
0x284 - 0x2A0	PSI5 Control Registers	32
0x2A4 - 0x2E0	Reserved	32
0x2E4 - 0x300	PSI5 Default Data Frame Registers	32
0x304 - 0x320	PSI5 Transmit Data Frame FIFO Registers	32
0x324	PSI5 FIFO Status Register	32
0x328 - 0x32C	Reserved	32
0x330 - 0x34C	PSI5 SYNC Data Registers	32
0x350 - 0x36C	Reserved	32
Cycle Counter Registers		
0x370	Cycle Counter Control Register	32
0x374 - 0x380	Cycle Counter Match Registers	32
0x384 - 0x390	Cycle Counter Value Registers	32
0x400 - 0x41C	Reserved	32
Interrupt Registers		
0x420	Interrupt Enable Register	32
0x424	PSI5 Status IRQ Trigger Register	32
0x428	Interrupt Status Register	32
0x42C - 0x4FC	Reserved	32
Extended Timer Registers		
0x500 - 0x51C	Extended Cycle Register	32
0x520 - 0x53C	Extended TP Register	32
0x540 - 0xFF0	Reserved	32
Board Status Registers		
0xFF4	Board Health Register	32
0xFF8	Scratchpad Register	32
0xFFC	Firmware Identification Register	32

Table 5-3 : Register Space

5.3.2 Common Protocol Registers

These registers are not protocol specific, and are used by all protocols.

5.3.2.1 Channel Control Register: 0x000

Bit	Symbol	Description	Access	Reset Value
31:29	MODE7	Protocol selection for Channel 7	R/W	0x0
27:24	MODE6	Protocol selection for Channel 6	R/W	0x0
23:20	MODE5	Protocol selection for Channel 5	R/W	0x0
19:16	MODE4	Protocol selection for Channel 4	R/W	0x0
15:12	MODE3	Protocol selection for Channel 3	R/W	0x0
11:8	MODE2	Protocol selection for Channel 2	R/W	0x0
7:4	MODE1	Protocol selection for Channel 1	R/W	0x0
3:0	MODE0	Protocol selection for Channel 0	R/W	0x0

Table 5-4 : Control Register

For each of the eight channels the protocol is freely selectable. Protocol options:

MODE	Description
0x0	Channel disabled
0x1	Custom protocol / Manual current setting
0x2	Square Wave Protocol
0x3	PWM Protocol
0x4	AK Protocol / VDA Protocol
0x5	PSI5 Protocol
Others	Reserved

5.3.2.2 Current Level Registers 0x004 – 0x020

Bit	Symbol	Description	Access	Reset Value
31:30	-	Reserved’	-	-
29:20	HIGH[x]	HIGH Current Level Setting for Channel [x] HIGH = Desired Current (µA) / 73.85 µA	R/W	0
19:10	MID[x]	MID Current Level Setting for Channel [x] MID = Desired Current (µA) / 73.85 µA	R/W	0
9:0	LOW[x]	LOW Current Level Setting for Channel [x] LOW = Desired Current (µA) / 73.85 µA	R/W	0

Table 5-5 : Current Level Registers

For each channel a current level register is provided, in which three adjustable values, LOW, MID, and HIGH can be defined.

The Custom protocol and the AK protocol use all three current levels. The other protocols just use the HIGH and LOW current level.

Typical values for these protocols are:

Protocol	HIGH	MID	LOW
Square Wave Protocol	14 mA	unused	7 mA
PWM Protocol	14 mA	unused	7 mA
AK Protocol / VD Protocol	28 mA	14 mA	7 mA
PSI5 Protocol	26 mA	unused	19 mA

Register	Bar Offset
Current Level Register Channel 0	0x004
Current Level Register Channel 1	0x008
Current Level Register Channel 2	0x00C
Current Level Register Channel 3	0x010
Current Level Register Channel 4	0x014
Current Level Register Channel 5	0x018
Current Level Register Channel 6	0x01C
Current Level Register Channel 7	0x020

5.3.2.3 ADC Data Register Ch0-1 0x024

Bit	Symbol	Description	Access	Reset Value
31:26	-	Reserved	-	-
25:16	ADC1	Last sampled ADC value of Channel 1 Voltage = ADC1 * 26.16 mV	R	0
15:10	-	Reserved	-	-
9:0	ADC0	Last sampled ADC value of Channel 0 Voltage = ADC0 * 26.16 mV	R	0

Table 5-6 : ADC Data Register Ch0-1

A new value is provided every 1.6 µs.

5.3.2.4 ADC Data Register Ch2-3 0x028

Bit	Symbol	Description	Access	Reset Value
31:26	-	Reserved	-	-
25:16	ADC3	Last sampled ADC value of Channel 3 Voltage = ADC3 * 26.16 mV	R	0
15:10	-	Reserved	-	-
9:0	ADC2	Last sampled ADC value of Channel 2 Voltage = ADC2 * 26.16 mV	R	0

Table 5-7 : ADC Data Register Ch2-3

A new value is provided every 1.6 µs.

5.3.2.5 ADC Data Register Ch4-5 0x02C

Bit	Symbol	Description	Access	Reset Value
31:26	-	Reserved	-	-
25:16	ADC5	Last sampled ADC value of Channel 5 Voltage = ADC5 * 26.16 mV	R	0
15:10	-	Reserved	-	-
9:0	ADC4	Last sampled ADC value of Channel 4 Voltage = ADC4 * 26.16 mV	R	0

Table 5-8 : ADC Data Register Ch4-5

A new value is provided every 1.6 µs.

5.3.2.6 ADC Data Register Ch6-7 0x030

Bit	Symbol	Description	Access	Reset Value
31:26	-	Reserved	-	-
25:16	ADC7	Last sampled ADC value of Channel 7 Voltage = ADC7 * 26.16 mV	R	0
15:10	-	Reserved	-	-
9:0	ADC6	Last sampled ADC value of Channel 6 Voltage = ADC6 * 26.16 mV	R	0

Table 5-9 : ADC Data Register Ch6-7

A new value is provided every 1.6 µs.

5.3.3 Custom Protocol Registers

The TPMC160 supports custom protocols by allowing the manual setting of the current level. This can be done either directly through the CP[x] DEFAULT bits, or as a sequence through the CP FIFO.

After starting a sequence, each current level is provided one after the other for a duration of CP[x] TP. As soon as the Manual Sequence FIFO is empty the corresponding output is set to the value defined by the CP[x] DEFAULT bits. After filling the FIFO again, the next sequence can be started.

5.3.3.1 CP Cycle Registers 0x050 – 0x06C

Bit	Symbol	Description	Access	Reset Value
31:30	CP[x] DEFAULT	Default Current Level of Channel [x] Determines which current level, defined in the Channel's "Current Level Register", shall be used as default output current: 0x0 = Off 0x1 = LOW 0x2 = MID 0x3 = HIGH	R/W	0
29:28	CP[x] TP BASE	Channel [x]: Time base used for the Custom Protocol bit width. 0x0 = 50 ns time base 0x1 = 0.1 µs time base 0x2 = 1 µs time base 0x3 = 1 ms time base A new value becomes active as soon as the current pulse is completed.	R/W	0
27:16	CP[x] TP	Channel [x]: Custom protocol bit width. Bit width of a single bit in the corresponding protocol. The time base depends on the CP[x] TP BASE. A new value becomes active as soon as the currently transmitted pulse is completed.	R/W	0
15	CP[x] TRIG	Channel [x]: Manual Trigger for the Custom Protocol Starts the transfer of the full content of the sequence stored in the Custom Protocol FIFO. Only valid if CP[x] MODE is set to 0 and no sequence is currently transferred. The bit is cleared automatically.	R/S	0
14	CP[X] MODE	Channel [x]: Custom Protocol Trigger Selection 0 = Manual Mode, Triggered by CP[x] TRIG 1 = Sequencer Mode Triggered via the CP[x] CYCLE timer.	R/W	0
13:12	CP[x] CYCLE BASE	Channel [x]: Time base used for the Custom Protocol Cycle Time 0x0 = 50 ns time base 0x1 = 0.1 µs time base 0x2 = 1 µs time base 0x3 = 1 ms time base A new value becomes active as soon as the current cycle is completed.	R/W	0

Bit	Symbol	Description	Access	Reset Value
11:0	CP[x] CYCLE	Channel [x]: Custom Protocol Cycle Time The time base depends on CP[x] CYCLE BASE. The value has to be longer than the sequence stored in the CP FIFO. A new value becomes active as soon as the current cycle is completed.	R/W	0

Table 5-10 : CP Cycle Registers

A long timer value of the pulse width or cycle time can be reset by disabling the protocol via the Channel Control Register.

Register	Bar Offset
CP Cycle Register Channel 0	0x050
CP Cycle Register Channel 1	0x054
CP Cycle Register Channel 2	0x058
CP Cycle Register Channel 3	0x05C
CP Cycle Register Channel 4	0x060
CP Cycle Register Channel 5	0x064
CP Cycle Register Channel 6	0x068
CP Cycle Register Channel 7	0x06C

5.3.3.2 CP FIFO Status Register 0x070

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
15	CP FIFO7 RST	reset of the channel 7 Custom Protocol FIFO Writing a '1' flushes the FIFO	R/C	0
14	CP FIFO6 RST	reset of the channel 6 Custom Protocol FIFO Writing a '1' flushes the FIFO	R/C	0
13	CP FIFO5 RST	reset of the channel 5 Custom Protocol FIFO Writing a '1' flushes the FIFO	R/C	0
12	CP FIFO4 RST	Reset of the channel 4 Custom Protocol FIFO Writing a '1' flushes the FIFO	R/C	0
11	CP FIFO3 RST	Reset of the channel 3 Custom Protocol FIFO Writing a '1' flushes the FIFO	R/C	0
10	CP FIFO2 RST	Reset of the channel 2 Custom Protocol FIFO Writing a '1' flushes the FIFO	R/C	0
9	CP FIFO1 RST	Reset of the channel 1 Custom Protocol FIFO Writing a '1' flushes the FIFO	R/C	0
8	CP FIFO0 RST	Reset of the channel 0 Custom Protocol FIFO Writing a '1' flushes the FIFO	R/C	0
7	CP FIFO7 FULL	FIFO full flag of the Custom Protocol FIFO of channel 7	R	0
6	CP FIFO6 FULL	FIFO full flag of the Custom Protocol FIFO of channel 6	R	0
5	CP FIFO5 FULL	FIFO full flag of the Custom Protocol FIFO of channel 5	R	0
4	CP FIFO4 FULL	FIFO full flag of the Custom Protocol FIFO of channel 4	R	0
3	CP FIFO3 FULL	FIFO full flag of the Custom Protocol FIFO of channel 3	R	0
2	CP FIFO2 FULL	FIFO full flag of the Custom Protocol FIFO of channel 2	R	0
1	CP FIFO1 FULL	FIFO full flag of the Custom Protocol FIFO of channel 1	R	0
0	CP FIFO0 FULL	FIFO full flag of the Custom Protocol FIFO of channel 0	R	0

Table 5-11 : CP FIFO Status Register

5.3.3.3 CP FIFO Data Registers 0x074 – 0x090

Bit	Symbol	Description	Access	Reset Value
31:30	CP[x]_15	Current Level setting 15 of channel [x] Same as CP[x] DEFAULT: 00 = Off 01 = LOW 10 = MID 11 = HIGH	W	0
29:28	CP[x]_14	Current Level setting 14 of channel [x]	W	0
27:26	CP[x]_13	Current Level setting 13 of channel [x]	W	0
25:24	CP[x]_12	Current Level setting 12 of channel [x]	W	0
23:22	CP[x]_11	Current Level setting 11 of channel [x]	W	0
21:20	CP[x]_10	Current Level setting 10 of channel [x]	W	0
19:18	CP[x]_9	Current Level setting 9 of channel [x]	W	0
17:16	CP[x]_8	Current Level setting 8 of channel [x]	W	0
15:14	CP[x]_7	Current Level setting 7 of channel [x]	W	0
13:12	CP[x]_6	Current Level setting 6 of channel [x]	W	0
11:10	CP[x]_5	Current Level setting 5 of channel [x]	W	0
9:8	CP[x]_4	Current Level setting 4 of channel [x]	W	0
7:6	CP[x]_3	Current Level setting 3 of channel [x]	W	0
5:4	CP[x]_2	Current Level setting 2 of channel [x]	W	0
3:2	CP[x]_1	Current Level setting 1 of channel [x]	W	0
1:0	CP[x]_0	Current Level setting 0 of channel [x]	W	0

Table 5-12 : CP FIFO Data Registers

Writing to the CP FIFO Data Register fills a FIFO that can hold up to 16 x 16 (=256) current level settings. If a channel is triggered in the custom protocol, the current FIFO contents are transmitted. Fill unneeded current level settings within the CP FIFO Data Registers with the CP[x] DEFAULT or with the OFF value (as appropriate for the implemented protocol).

Register	Bar Offset
CP FIFO Data Register Channel 0	0x074
CP FIFO Data Register Channel 1	0x078
CP FIFO Data Register Channel 2	0x07C
CP FIFO Data Register Channel 3	0x080
CP FIFO Data Register Channel 4	0x084
CP FIFO Data Register Channel 5	0x088
CP FIFO Data Register Channel 6	0x08C
CP FIFO Data Register Channel 7	0x090

5.3.4 Square Wave Protocol Registers

The Square Wave Protocol (SWP) supports mainly the simulation of Standard 2-level (7/14 mA) sensors which work after the “Speed Protocol” or “Duty Cycle” principle.

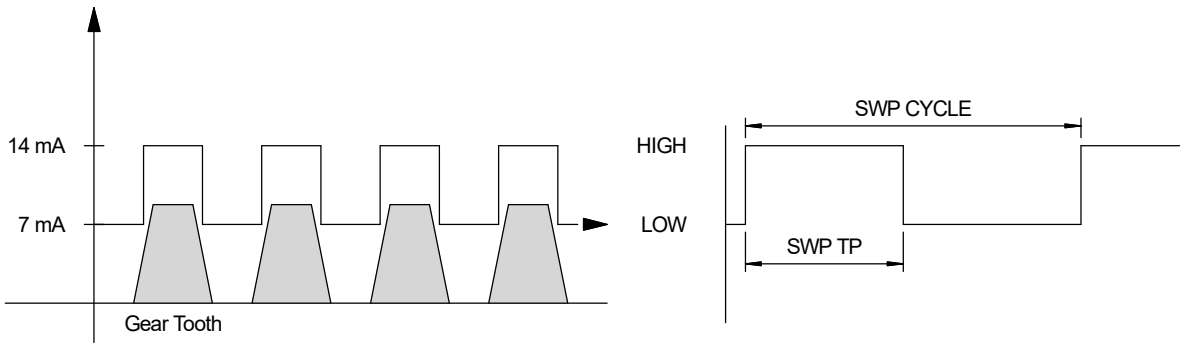


Figure 5-1 : Square Wave Protocol

The Square Wave Protocol uses the HIGH and the LOW Current Level of the Current Level Register.

5.3.4.1 SWP Cycle Registers 0x0B0 – 0x0CC

Bit	Symbol	Description	Access	Reset Value
31:30	-	Reserved	-	-
29:28	SWP[x] TP BASE	Channel [x]: Time base used for the SWP high time SWP[x] TP. 0x0 = 50 ns time base 0x1 = 0.1 µs time base 0x2 = 1 µs time base 0x3 = 1 ms time base A new value becomes active as soon as the currently transmitted pulse is completed.	R/W	0
27:16	SWP[x] TP	Channel [x]: SWP high time SWP TP. The time base depends on the SWP[x] TP Base . A new value becomes active as soon as the currently transmitted pulse is completed.	R/W	0
15:14	-	Reserved	-	-
13:12	SWP[x] CYCLE BASE	Channel [x]: Time base used for the SWP Cycle Time SWP[x] CYCLE 0x0 = 50 ns time base 0x1 = 0.1 µs time base 0x2 = 1 µs time base 0x3 = 1 ms time base A new value becomes active as soon as the current cycle is completed.	R/W	0

Bit	Symbol	Description	Access	Reset Value
11:0	SWP[x] CYCLE	Channel [x]: SWP Cycle Time The time base depends on the SWP[x] CYCLE BASE. A new value becomes active as soon as the current cycle is completed.	R/W	0

Table 5-13 : SWP Cycle Registers

A long timer value of the pulse width or cycle time can be reset by disabling the protocol via the Channel Control Register.

Register	Bar Offset
SWP Cycle Register Channel 0	0x0B0
SWP Cycle Register Channel 1	0x0B4
SWP Cycle Register Channel 2	0x0B8
SWP Cycle Register Channel 3	0x0BC
SWP Cycle Register Channel 4	0x0C0
SWP Cycle Register Channel 5	0x0C4
SWP Cycle Register Channel 6	0x0C8
SWP Cycle Register Channel 7	0x0CC

5.3.5 PWM Protocol Registers

PWM Wheel Speed Sensors transmit additional information by varying the length of the speed pulses.

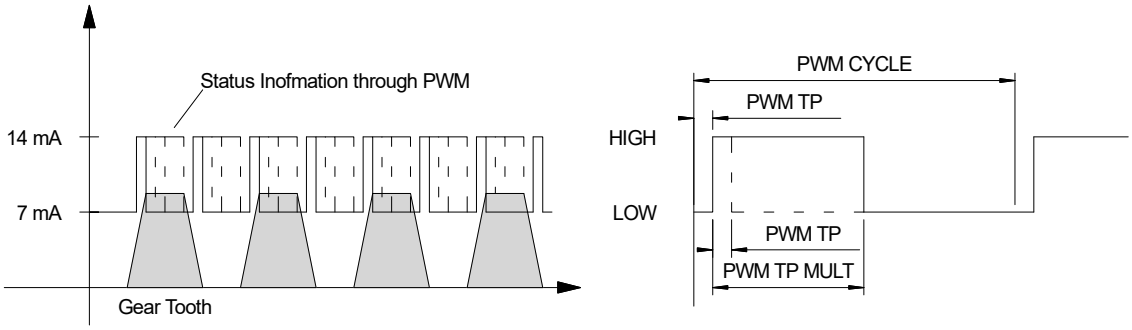


Figure 5-2 : PWM Wave Protocol

PWM encoding is based on the TP setting. All pulse widths are derived from this value. The two current levels of the PWM Protocol are defined as LOW and HIGH in the Current Level Registers.

The usual value for PWM TP is at around 50 µs.

Each sequence starts with a PWM TP wide LOW Level, followed by a HIGH Level of duration PWM TP * PWM TP MULT. After the cycle time has elapsed, the sequence starts again with the PWM TP wide LOW level.

If the cycle time is too short (less then PWM TP * (PWM TP MULT + 1)) the sequence interrupted and restarted.

5.3.5.1 PWM Cycle Registers 0x120 – 0x13C

Bit	Symbol	Description	Access	Reset Value
31:20	PWM[x] TP	Channel [x]: PWM Protocol bit width TP in 0.1 µs, used for the PWM bit width calculation. The time base is always 0.1 µs. A new value becomes active as soon as the currently transmitted pulse is completed.	R\W	0
19:14	PWM[x] TP MULT	Channel [x]: TP length multiplier 0x0 = no high time 0x1 = 1 * PWM[x] TP high time … 0x3F = 63 * PWM[x] TP high time A new value becomes active as soon as the currently transmitted pulse is completed.	R\W	0

Bit	Symbol	Description	Access	Reset Value
13:12	PWM[x] CYCLE BASE	Channel [x]: Time base used for the PWM Protocol Cycle Time 0x0 = 50 ns time base 0x1 = 0.1 µs time base 0x2 = 1 µs time base 0x3 = 1 ms time base A new value becomes active as soon as the current cycle is completed.	R\W	0
11:0	PWM[x] CYCLE	Channel [x]: PWM Protocol Cycle Time The time base depends on the PWM[x] CYCLE BASE A new value becomes active as soon as the current cycle is completed.	R\W	0

Table 5-14 : PWM Cycle Registers

A long timer value of the pulse width or cycle time can be reset by disabling the protocol via the Channel Control Register.

Register	Bar Offset
PWM Cycle Register Channel 0	0x120
PWM Cycle Register Channel 1	0x124
PWM Cycle Register Channel 2	0x128
PWM Cycle Register Channel 3	0x12C
PWM Cycle Register Channel 4	0x130
PWM Cycle Register Channel 5	0x134
PWM Cycle Register Channel 6	0x138
PWM Cycle Register Channel 7	0x13C

5.3.6 AK-Protocol / VDA Registers

Wheel Speed Sensors with “AK-Protocol” or “VDA” use three current levels and transmit up to 9 status bits after the speed pulse.

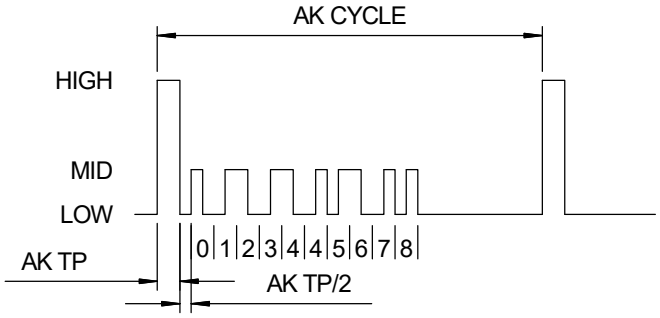


Figure 5-3 : AK-Protocol

The AK encoding starts with a “speed pulse” with HIGH or MID current level, followed by a short gap, and then followed by the Manchester encoded protocol bits with MID current levels.

5.3.6.1 AK Cycle Registers 0x160 – 0x17C

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:16	AK[x] TP	Channel [x]: AK protocol bit width TP in in 0.1 µs. The time base is always 0.1 µs. A new value becomes active as soon as the currently transmitted pulse is completed.	R\W	0
15:14	-	Reserved	-	-
13:12	AK[x] CYCLE BASE	Channel [x]: Time base used for the AK Protocol Cycle Time. 0x0 = 50 ns time base 0x1 = 0.1 µs time base 0x2 = 1 µs time base 0x3 = 1 ms time base A new value becomes active as soon as the current cycle is completed.	R\W	0
11:0	AK[x] CYCLE	Channel [x]: AK Protocol Cycle Time The time base depends on the AK[x] CYCLE BASE A new value becomes active as soon as the current cycle is completed.	R\W	0

Table 5-15 : AK Cycle Registers

A long timer value of the pulse width or cycle time can be reset by disabling the protocol via the Channel Control Register.

Register	Bar Offset
AK Cycle Register Channel 0	0x160
AK Cycle Register Channel 1	0x164
AK Cycle Register Channel 2	0x168
AK Cycle Register Channel 3	0x16C
AK Cycle Register Channel 4	0x170
AK Cycle Register Channel 5	0x174
AK Cycle Register Channel 6	0x178
AK Cycle Register Channel 7	0x17C

5.3.6.2 AK Control Registers 0x180 – 0x19C

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	-	-
15:12	AK[x] BIT NUMBER	Channel [x]: Number of bits to transmit. (Excluding speed pulse) 0x0 = No bits are transmitted … 0x9 = Nine bits are transmitted >0x9 = reserved	R/W	0
11:10	-	Reserved	-	-
9	AK[x] ASP	Channel [x]: Artificial Speed Pulse 0 = Normal Speed Pulse (High Current) 1 = Artificial Speed Pulse (Mid Current)	R/W	0
8	AK[x] B8	Channel [x]: AK protocol: Bit position 8	R/W	0
7	AK[x] B7	Channel [x]: AK protocol: Bit position 7	R/W	0
6	AK[x] B6	Channel [x]: AK protocol: Bit position 6	R/W	0
5	AK[x] B5	Channel [x]: AK protocol: Bit position 5	R/W	0
4	AK[x] B4	Channel [x]: AK protocol: Bit position 4	R/W	0
3	AK[x] B3	Channel [x]: AK protocol: Bit position 3	R/W	0
2	AK[x] B2	Channel [x]: AK protocol: Bit position 2	R/W	0
1	AK[x] B1	Channel [x]: AK protocol: Bit position 1	R/W	0
0	AK[x] B0	Channel [x]: AK protocol: Bit position 0	R/W	0

Table 5-16 : AK Control Registers

Register	Bar Offset
AK Control Register Channel 0	0x180
AK Control Register Channel 1	0x184
AK Control Register Channel 2	0x188
AK Control Register Channel 3	0x18C
AK Control Register Channel 4	0x190
AK Control Register Channel 5	0x194
AK Control Register Channel 6	0x198
AK Control Register Channel 7	0x19C

5.3.7 PSI5 Protocol Registers

The PSI5 Protocol uses the LOW and HIGH Current Levels of the Current Level Registers.

5.3.7.1 PSI5 Cycle Registers 0x220 – 0x23C

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:16	PSI5[x] TP	Channel [x]: PSI5 Protocol bit width TP in in 0.1 µs. The time base is always 0.1 µs. This is basically the PSI5 nominal time for a single bit T_{BIT} A new value becomes active as soon as the currently transmitted pulse is completed.	R\W	0
15:12	-	Reserved	-	-
11:0	PSI5[x] CYCLE	Channel [x]: PSI5 Protocol Cycle Time in µs. The time base is always 1 µs. This is basically the PSI5 sync period T_{SYNC} A new value becomes active as soon as the current cycle is completed.	R\W	0

Table 5-17 : PSI5 Cycle Registers

The period duration of a bit PSI5[x] TP is defined for each channel individually. Typical values for a PSI5 sensor are 8.0 µs for the 125 kbp/s mode and 5.3 µs for the 189 kbp/s mode.

A long timer value of the pulse width or cycle time can be reset by disabling the protocol via the Channel Control Register.

Register	Bar Offset
PSI5 Cycle Register Channel 0	0x220
PSI5 Cycle Register Channel 1	0x224
PSI5 Cycle Register Channel 2	0x228
PSI5 Cycle Register Channel 3	0x22C
PSI5 Cycle Register Channel 4	0x230
PSI5 Cycle Register Channel 5	0x234
PSI5 Cycle Register Channel 6	0x238
PSI5 Cycle Register Channel 7	0x23C

5.3.7.2 PSI5 Interrupt Status Registers 0x240

For an interrupt status bit to be set, the interrupt must be enabled before the interrupt event.

Bit	Symbol	Description	Access	Reset Value
31	PSI5[7] OFLOW	Channel [x]: PSI5[x] SYNC bit overflow. After a PSI5[x] SYNC MATCH interrupt is generated, new SYNC pulses are stored in a swap register until the PSI5 SYNC Data Registers was read. If the swap register overflows before PSI5 SYNC Data Registers was read and SYNC pulses are lost, corresponding PSI5[x] OFLOW bit is set to '1'. This bits are cleared by reading this register.	R/C	0
30	PSI5[6] OFLOW		R/C	0
29	PSI5[5] OFLOW		R/C	0
28	PSI5[4] OFLOW		R/C	0
27	PSI5[3] OFLOW		R/C	0
26	PSI5[2] OFLOW		R/C	0
25	PSI5[1] OFLOW		R/C	0
24	PSI5[0] OFLOW		R/C	0
23	PSI5 [7] SPUR	Channel [x]: PSI5 Spurious Sync signal Spurious sync signal detected The SYNC Threshold Voltage was reached outside of the T_{TRIG} window or an invalid SYNC Pulse was detected during the TRIG window. This bits are cleared by reading this register.	R/C	0
22	PSI5 [6] SPUR		R/C	0
21	PSI5 [5] SPUR		R/C	0
20	PSI5 [4] SPUR		R/C	0
19	PSI5 [3] SPUR		R/C	0
18	PSI5 [2] SPUR		R/C	0
17	PSI5 [1] SPUR		R/C	0
16	PSI5 [0] SPUR		R/C	0

Bit	Symbol	Description	Access	Reset Value
15	PSI5 [7] RESET	Channel [x]: PSI5[x] RESET TTH status The ADC reading was below the value set in PSI5[x] RESET THRESHOLD for longer than the time set in PSI5[x] RESET TTH. This bits are cleared by reading this register.	R/C	0
14	PSI5 [6] RESET		R/C	0
13	PSI5 [5] RESET		R/C	0
12	PSI5 [4] RESET		R/C	0
11	PSI5 [3] RESET		R/C	0
10	PSI5 [2] RESET		R/C	0
9	PSI5 [1] RESET		R/C	0
8	PSI5 [0] RESET		R/C	0
7:0	Reserved	Reserved	-	-

Table 5-18 : PSI5 Interrupt Status Registers

5.3.7.3 PSI5 Status Registers 0x244 – 0x260

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:18</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>17:12</td><td>PSI5[x] SYNC CNT</td><td>Channel [x]: This value shows the current unread bits in the PSI5 SYNC Register (0 to 32). This status is reset to 0 when the PSI5 SYNC Register was read.
When this value reaches the PSI5[x] SYNC MATCH value, an interrupt can be generated.</td><td>R</td><td>0</td></tr>
<tr><td>11:10</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>9:4</td><td>PSI5[x] FIFO CNT</td><td>Channel [x]: This value shows the current PSI5 FIFO fill level in DWORDs (0 - 33)</td><td>R</td><td>0</td></tr>
<tr><td>3:0</td><td>PSI5[x] SYNC ERROR TYPE</td><td>Channel [x]: SYNC Pulse Error Status
The last unexpected sync signal was a:
<table><tr><th>Value</th><th>Mode</th></tr><tr><td>0000</td><td>No unexpected sync pulse detected yet</td></tr><tr><td>0001</td><td>Absence of the sync pulse at the expected time window</td></tr><tr><td>0010</td><td>Too short for a short pulse</td></tr><tr><td>0011</td><td>Too long for a short pulse
too short for a long pulse</td></tr><tr><td>0100</td><td>Too long for a long pulse</td></tr><tr><td>0101</td><td>Long pulse instead of expected short pulse detected</td></tr></table>
Only synchronization pulses within the allowed time window are recognized.

This bits are cleared by writing 0xF to this bits</td><td>R/C</td><td>0</td></tr>
</table>

Table 5-19 : PSI5 Status Registers

Register	Bar Offset
PSI5 Status Register Channel 0	0x244
PSI5 Status Register Channel 1	0x248
PSI5 Status Register Channel 2	0x24C
PSI5 Status Register Channel 3	0x250
PSI5 Status Register Channel 4	0x254
PSI5 Status Register Channel 5	0x258
PSI5 Status Register Channel 6	0x25C
PSI5 Status Register Channel 7	0x260

5.3.7.4 PSI5 Detection Registers 0x264 – 0x280

Bit	Symbol	Description	Access	Reset Value
31	-	Reserved	-	-
30:26	PSI5[x] SYNC MATCH VALUE	Channel [x]: Maximum of stored SYNC Bits - 1 When PSI5[x] SYNC CNT matches this value, an interrupt can be generated. 0x0 = Match Value is 1 0x1F = Match value is 32	R/W	0
25:16	PSI5[x] SYNC THRESHOLD	Channel [x]: Sync signal sustain voltage This is the value that is used to detect PSI5 SYNC pulses. (absolute voltage) Value = Desired Voltage (mV) / 26.16 mV	R/W	0
15:6	PSI5[x] RESET THRESHOLD	Channel [x]: Undervoltage reset threshold This is the value that is used to detect PSI5 undervoltage reset(absolute voltage) Value = Desired Voltage (mV) / 26.16 mV	R/W	0
5:0	PSI5[x] RESET TTH	Channel [x]: The voltage level of the PSI5 line has to stay below the PSI5[x] RESET THRESHOLD for the sensor for time tTh to initiate a reset; in 100 µs steps. Settable range is 0 - 6.39 ms	R/W	0

Table 5-20 : PSI5 Detection Registers

Register	Bar Offset
PSI5 Detection Register Channel 0	0x264
PSI5 Detection Register Channel 1	0x268
PSI5 Detection Register Channel 2	0x26C
PSI5 Detection Register Channel 3	0x270
PSI5 Detection Register Channel 4	0x274
PSI5 Detection Register Channel 5	0x278
PSI5 Detection Register Channel 6	0x27C
PSI5 Detection Register Channel 7	0x280

5.3.7.5 PSI5 Control Registers 0x284 – 0x2A0

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:28</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>27:16</td><td>PSI5[x] SLOT DELAY</td><td>Channel [x]: Delay between the start of an synchronization pulse and the Data Frame in µs. - t_{DELAY}
This can be used to determine in which Slot the sensor shall send its data.

Not used in asynchronous mode.</td><td>R/W</td><td>0</td></tr>
<tr><td>15:11</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>10</td><td>PSI5[x] PULSE MODE</td><td>Channel [x]: ECU to Sensor Communication method:
0 = Tooth Gap method
1 = Pulse Width method</td><td>R/W</td><td>0</td></tr>
<tr><td>9:8</td><td>PSI5[x] START BIT</td><td>Channel [x]: PSI5 start bits,
only valid when START BIT EN = 1
START BIT[0] = Start bit S1
START BIT[1] = Start bit S2</td><td>R/W</td><td>0</td></tr>
<tr><td>7</td><td>PSI5[x] START BIT EN</td><td>Channel [x]: Start bit enable.

0 = Start bits are disabled.
If the start bits are disabled, the user should add them manually to the frame.

1 = The Start bits PSI5[x] START BIT[1:0] are prefixed to each PSI5 data frame.</td><td>R/W</td><td>0</td></tr>
<tr><td>6:2</td><td>PSI5[x] BIT NUMBER</td><td>Channel [x]: Number of PSI5 Data Frame Bits – 1 (omitting the PSI5[x] START BIT)
0x0 = 1 bit is send
0x1F = 32 bits are send</td><td>R/W</td><td>0</td></tr>
<tr><td>1:0</td><td>PSI5[x] BUS MODE</td><td>Channel [x]: PSI5 Communication Mode

<table>
<tr><th>MODE</th><th>Mode</th></tr>
<tr><td>00</td><td>Asynchronous Mode</td></tr>
<tr><td>01</td><td>Synchronous Mode
without Daisy Chain</td></tr>
<tr><td>10</td><td>Synchronous Mode
with Daisy Chain</td></tr>
<tr><td>11</td><td>Variable Sync pulse mode
(PSI5[x]Pulse Mode has to be PWM)</td></tr>
</table>
</td><td>R/W</td><td>0</td></tr>
</table>

Table 5-21 : PSI5 Control Registers

Register	Bar Offset
PSI5 Control Register Channel 0	0x284
PSI5 Control Register Channel 1	0x288
PSI5 Control Register Channel 2	0x28C
PSI5 Control Register Channel 3	0x290
PSI5 Control Register Channel 4	0x294
PSI5 Control Register Channel 5	0x298
PSI5 Control Register Channel 6	0x29C
PSI5 Control Register Channel 7	0x2A0

5.3.7.6 PSI5 Default Data Frame Registers 0x2E4 – 0x300

Bit	Symbol	Description	Access	Reset Value
31:0	PSI5[x] FRAME	Channel [x]: Holds the payload that is transferred in a data frame from the sensor to the ECU. The payload must include the parity or CRC bits. The bits are transmitted in ascending order, starting with bit 0.	R/W	0

Table 5-22 : PSI5 Control Registers

The data frame register holds the payload that is transferred in a data frame from the sensor to the ECU. The Default Data Frame is only send when the PSI5 Data Frame FIFO is empty.

Start bits are inserted if selected in PSI5[x] START BIT. Parity or CRC bits must be included in the payload.

The number of bits actually transferred depends on PSI5[x] BIT NUMBER and the PSI5[x] START BIT EN values in the PSI5 Control Register.

Register	Bar Offset
PSI5 Default Data Frame Register Channel 0	0x2E4
PSI5 Default Data Frame Register Channel 1	0x2E8
PSI5 Default Data Frame Register Channel 2	0x2EC
PSI5 Default Data Frame Register Channel 3	0x2F0
PSI5 Default Data Frame Register Channel 4	0x2F4
PSI5 Default Data Frame Register Channel 5	0x2F8
PSI5 Default Data Frame Register Channel 6	0x2FC
PSI5 Default Data Frame Register Channel 7	0x300

5.3.7.7 PSI5 Data Frame FIFO Registers 0x304 – 0x320

Bit	Symbol	Description	Access	Reset Value
31:0	PSI5[x] FIFO	Channel [x]: PSI5 Transmit Data Frame FIFO input. Holds the payload that is transferred in a data frame from the sensor to the ECU. The payload must include the parity or CRC bits. The bits are transmitted in ascending order, starting with bit 0.	W	0

Table 5-23 : PSI5 Data Frame FIFO Registers

To support the Sensor to ECU communication, the TPMC160 offers the PSI5 Data Frame FIFO, which can be used instead of the “PSI5 Default Data Frame Register”. The FIFO holds up to 33 Data Frames, which is sufficient to hold Data Frames required for a complete serial data frame.

The PSI5 Data Frame FIFO will take precedence over the “PSI5 Default Data Frame Register” as soon it contains data. When the FIFO is empty, the protocol engine switches back to the “PSI5 Default Data Frame Register”.

Register	Bar Offset
PSI5 Data Frame FIFO Register Channel 0	0x304
PSI5 Data Frame FIFO Register Channel 1	0x308
PSI5 Data Frame FIFO Register Channel 2	0x30C
PSI5 Data Frame FIFO Register Channel 3	0x310
PSI5 Data Frame FIFO Register Channel 4	0x314
PSI5 Data Frame FIFO Register Channel 5	0x318
PSI5 Data Frame FIFO Register Channel 6	0x31C
PSI5 Data Frame FIFO Register Channel 7	0x320

5.3.7.8 PSI5 FIFO Status Register 0x324

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	-	-
15	PSI5 FIFO7 RST	FIFO reset of the channel 7 PSI5 Data Frame FIFO Writing a ‘1’ flushes the FIFO	R/C	0
14	PSI5 FIFO6 RST	FIFO reset of the channel 6 PSI5 Data Frame FIFO Writing a ‘1’ flushes the FIFO	R/C	0
13	PSI5 FIFO5 RST	FIFO reset of the channel 5 PSI5 Data Frame FIFO Writing a ‘1’ flushes the FIFO	R/C	0
12	PSI5 FIFO4 RST	FIFO reset of the channel 4 PSI5 Data Frame FIFO Writing a ‘1’ flushes the FIFO	R/C	0
11	PSI5 FIFO3 RST	FIFO reset of the channel 3 PSI5 Data Frame FIFO Writing a ‘1’ flushes the FIFO	R/C	0
10	PSI5 FIFO2 RST	FIFO reset of the channel 2 PSI5 Data Frame FIFO Writing a ‘1’ flushes the FIFO	R/C	0
9	PSI5 FIFO1 RST	FIFO reset of the channel 1 PSI5 Data Frame FIFO Writing a ‘1’ flushes the FIFO	R/C	0
8	PSI5 FIFO0 RST	FIFO reset of the channel 0 PSI5 Data Frame FIFO Writing a ‘1’ flushes the FIFO	R/C	0
7	PSI5 FIFO7 FULL	FIFO full flag of the channel 7 PSI5 Data Frame FIFO	R	0
6	PSI5 FIFO6 FULL	FIFO full flag of the channel 6 PSI5 Data Frame FIFO	R	0
5	PSI5 FIFO5 FULL	FIFO full flag of the channel 5 PSI5 Data Frame FIFO	R	0
4	PSI5 FIFO4 FULL	FIFO full flag of the channel 4 PSI5 Data Frame FIFO	R	0
3	PSI5 FIFO3 FULL	FIFO full flag of the channel 3 PSI5 Data Frame FIFO	R	0
2	PSI5 FIFO2 FULL	FIFO full flag of the channel 2 PSI5 Data Frame FIFO	R	0
1	PSI5 FIFO1 FULL	FIFO full flag of the channel 1 PSI5 Data Frame FIFO	R	0

Bit	Symbol	Description	Access	Reset Value
0	PSI5 FIFO0 FULL	FIFO full flag of the channel 0 PSI5 Data Frame FIFO	R	0

Table 5-24 : PSI5 FIFO Status Register

5.3.7.9 PSI5 SYNC Data Registers 0x330 – 0x34C

Bit	Symbol	Description	Access	Reset Value
31:0	PSI5[x] SYNC DATA	Channel [x]: Stores the received SYNC pulses that have not yet been read. The maximum number of sync pulses is set in PSI5[x] SYNC MATCH VALUE. This is a shifting register. The values of the sync pulses are shifted LSB sided into the register. Bit 0 contains the newest value. Tooth Gap method: / Pulse Width method 0 = absence of a sync pulse / 0 = short sync pulse 1 = short sync pulse / 1 = long sync pulse The actual fill status of this register is indicated in PSI5[x] SYNC CNT. When the match value is reached, newly received sync pulses are buffered in a swap register with the length of the PSI5[x] SYNC MATCH VALUE. After reading PSI5[x] SYNC DATA register the content is replaced by the content of the swap register. If an overflow occurs in the swap register, an interrupt can be triggered. The data of this register are no longer valid after the overflow. In this case it is cleared by one read access.	R/C	0

Table 5-25 : PSI5 SYNC Data Registers

Register	Bar Offset
PSI5 SYNC Data Register Channel 0	0x330
PSI5 SYNC Data Register Channel 1	0x334
PSI5 SYNC Data Register Channel 2	0x338
PSI5 SYNC Data Register Channel 3	0x33C
PSI5 SYNC Data Register Channel 4	0x340
PSI5 SYNC Data Register Channel 5	0x344
PSI5 SYNC Data Register Channel 6	0x348
PSI5 SYNC Data Register Channel 7	0x34C

5.3.8 Cycle Counter Registers

Each channel has its own Cycle Counter. When enabled, the counter increments its value after each Cycle of the selected protocol. The cycles for the protocols are defined as follows:

Custom Protocol:

Counts up when the corresponding protocol has been selected and a frame was sent.

Square Wave Protocol:

Counts up when the corresponding protocol is selected and the channel output (current) changes from LOW to HIGH.

PWM Protocol:

Counts up when the corresponding protocol has been selected and a PWM cycle was transmitted.

AK Protocol:

Counts up when the corresponding protocol has been selected and a the status bits were sent.

PSI5 Protocol:

Counts up when the corresponding protocol has been selected and a frame was sent.

5.3.8.1 Cycle Counter Control Register 0x370

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved	-	-
23	CNT7 RESET	Channel 7 Cycle Counter Reset Writing a '1' resets the Cycle Counter value	R/S	0
22	CNT6 RESET	Channel 6: Cycle Counter Reset Writing a '1' resets the Cycle Counter value	R/S	0
21	CNT5 RESET	Channel 5: Cycle Counter Reset Writing a '1' resets the Cycle Counter value	R/S	0
20	CNT4 RESET	Channel 4: Cycle Counter Reset Writing a '1' resets the Cycle Counter value	R/S	0
19	CNT3 RESET	Channel 3: Cycle Counter Reset Writing a '1' resets the Cycle Counter value	R/S	0
18	CNT2 RESET	Channel 2: Cycle Counter Reset Writing a '1' resets the Cycle Counter value	R/S	0
17	CNT1 RESET	Channel 1: Cycle Counter Reset Writing a '1' resets the Cycle Counter value	R/S	0
16	CNT0 RESET	Channel 0: Cycle Counter Reset Writing a '1' resets the Cycle Counter value	R/S	0

Bit	Symbol	Description	Access	Reset Value
15	CNT7 MATCH STATUS	Channel 7: Match Status 1 = The counters VALUE register was equal to the corresponding MATCH register. Cleared by writing a ‘1’	R/C	0
14	CNT6 MATCH STATUS	Channel 6: Match Status 1 = The counters VALUE register was equal to the corresponding MATCH register. Cleared by writing a ‘1’	R/C	0
13	CNT5 MATCH STATUS	Channel 5: Match Status 1 = The counters VALUE register was equal to the corresponding MATCH register. Cleared by writing a ‘1’	R/C	0
12	CNT4 MATCH STATUS	Channel 4: Match Status 1 = The counters VALUE register was equal to the corresponding MATCH register. Cleared by writing a ‘1’	R/C	0
11	CNT3 MATCH STATUS	Channel 3: Match Status 1 = The counters VALUE register was equal to the corresponding MATCH register. Cleared by writing a ‘1’	R/C	0
10	CNT2 MATCH STATUS	Channel 2: Match Status 1 = The counters VALUE register is equal to the corresponding MATCH register. Cleared by writing a ‘1’	R/C	0
9	CNT1 MATCH STATUS	Channel 1: Match Status 1 = The counters VALUE register was equal to the corresponding MATCH register. Cleared by writing a ‘1’	R/C	0
8	CNT0 MATCH STATUS	Channel 0: Match Status 1 = The counters VALUE register was equal to the corresponding MATCH register. Cleared by writing a ‘1’	R/C	0

Bit	Symbol	Description	Access	Reset Value
7	CNT7 EN	Channel 7: Cycle Counter Enable Register When set, the timer starts counting up beginning from 0.	R/W	0
6	CNT6 EN	Channel 6: Cycle Counter Enable Register When set, the timer starts counting up beginning from 0.	R/W	0
5	CNT5 EN	Channel 5: Cycle Counter Enable Register When set, the timer starts counting up beginning from 0.	R/W	0
4	CNT4 EN	Channel 4: Cycle Counter Enable Register When set, the timer starts counting up beginning from 0.	R/W	0
3	CNT3 EN	Channel 3: Cycle Counter Enable Register When set, the timer starts counting up beginning from 0.	R/W	0
2	CNT2 EN	Channel 2: Cycle Counter Enable Register When set, the timer starts counting up beginning from 0.	R/W	0
1	CNT1 EN	Channel 1: Cycle Counter Enable Register When set, the timer starts counting up beginning from 0.	R/W	0
0	CNT0 EN	Channel 0: Cycle Counter Enable Register When set, the timer starts counting up beginning from 0.	R/W	0

Table 5-26 : Cycle Counter Control Register

5.3.8.2 Cycle Counter Match Registers 0x374 – 0x380

The Match registers can be used to generate an interrupt, if the CNT[X] VALUE is equal to the corresponding CNT[x] MATCH and the Value of CNT[x] MATCH is unequal to '0'.

As soon as the cycle counter reaches the match value, it restarts from 0.

For new MATCH value to take effect, the corresponding counter has to be stopped and restarted.

5.3.8.2.1 Cycle Counter Match Register Ch0-1 0x374

Bit	Symbol	Description	Access	Reset Value
31:16	CNT1 MATCH	Channel 1: Match value for the corresponding Cycle Counter	R/W	0
15:0	CNT0 MATCH	Channel 0: Match value for the corresponding Cycle Counter	R/W	0

Table 5-27 : Cycle Counter Match Register Ch0-1

5.3.8.2.2 Cycle Counter Match Register Ch2-3 0x378

Bit	Symbol	Description	Access	Reset Value
31:16	CNT3 MATCH	Channel 3: Match value for the corresponding Cycle Counter	R/W	0
15:0	CNT2 MATCH	Channel 2: Match value for the corresponding Cycle Counter	R/W	0

Table 5-28 : Cycle Counter Match Register Ch2-3

5.3.8.2.3 Cycle Counter Match Register Ch4-5 0x37C

Bit	Symbol	Description	Access	Reset Value
31:16	CNT5 MATCH	Channel 5: Match value for the corresponding Cycle Counter	R/W	0
15:0	CNT4 MATCH	Channel 4: Match value for the corresponding Cycle Counter	R/W	0

Table 5-29 : Cycle Counter Match Register Ch4-5

5.3.8.2.4 Cycle Counter Match Register Ch6-7 0x380

Bit	Symbol	Description	Access	Reset Value
31:16	CNT7 MATCH	Channel 7: Match value for the corresponding Cycle Counter	R/W	0
15:0	CNT6 MATCH	Channel 6: Match value for the corresponding Cycle Counter	R/W	0

Table 5-30 : Cycle Counter Match Register Ch6-7

5.3.8.3 Cycle Counter Value Registers 0x384 – 0x390

5.3.8.3.1 Cycle Counter Value Register Ch0-1 0x384

Bit	Symbol	Description	Access	Reset Value
31:16	CNT1 VALUE	Channel 1: Actual value of the corresponding Cycle Counter	R	0
15:0	CNT0 VALUE	Channel 0: Actual value of the corresponding Cycle Counter	R	0

Table 5-31 : Cycle Counter Value Register Ch0-1

5.3.8.3.2 Cycle Counter Value Register Ch2-3 0x388

Bit	Symbol	Description	Access	Reset Value
31:16	CNT3 VALUE	Channel 3: Actual value of the corresponding Cycle Counter	R	0
15:0	CNT2 VALUE	Channel 2: Actual value of the corresponding Cycle Counter	R	0

Table 5-32 : Cycle Counter Value Register Ch2-3

5.3.8.3.3 Cycle Counter Value Register Ch4-5 0x38C

Bit	Symbol	Description	Access	Reset Value
31:16	CNT5 VALUE	Channel 5: Actual value of the corresponding Cycle Counter	R	0
15:0	CNT4 VALUE	Channel 4: Actual value of the corresponding Cycle Counter	R	0

Table 5-33 : Cycle Counter Value Register Ch4-5

5.3.8.3.4 Cycle Counter Value Register Ch6-7 0x390

Bit	Symbol	Description	Access	Reset Value
31:16	CNT7 VALUE	Channel 7: Actual value of the corresponding Cycle Counter	R	0
15:0	CNT6 VALUE	Channel 6: Actual value of the corresponding Cycle Counter	R	0

Table 5-34 : Cycle Counter Value Register Ch6-7

5.3.9 Interrupt Registers

5.3.9.1 Interrupt Enable Register 0x420

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved	-	-
23	CCM7 IE	Enable Cycle Counter Match IRQ 1 = Cycle Counter Match Interrupt enabled 0 = Cycle Counter Match Interrupt disabled An interrupt is generated when the CNT[x] MATCH STATUS changes from 0 to 1.	R/W	0
22	CCM6 IE		R/W	0
21	CCM5 IE		R/W	0
20	CCM4 IE		R/W	0
19	CCM3 IE		R/W	0
18	CCM2 IE		R/W	0
17	CCM1 IE		R/W	0
16	CCM0 IE		R/W	0
15	PSI7 IE	Enable PSI5 Status Interrupt IRQ 1 = PSI5 Status Interrupt enabled 0 = PSI5 Status Interrupt disabled The source for this interrupt is set in the PSI5 Status IRQ Trigger Register, below.	R/W	0
14	PSI6 IE		R/W	0
13	PSI5 IE		R/W	0
12	PSI4 IE		R/W	0
11	PSI3 IE		R/W	0
10	PSI2 IE		R/W	0
9	PSI1 IE		R/W	0
8	PSI0 IE		R/W	0
7	PSM7 IE	Enable PSI5 SYNC MATCH IRQ 1 = PSI5 SYNC MATCH interrupt enabled 0 = PSI5 SYNC MATCH interrupt disabled An interrupt will be generated when the PSI5[x] SYNC CNT value matches the corresponding PSI5[x] SYNC MATCH VALUE.	R/W	0
6	PSM6 IE		R/W	0
5	PSM5 IE		R/W	0
4	PSM4 IE		R/W	0
3	PSM3 IE		R/W	0
2	PSM2 IE		R/W	0
1	PSM1 IE		R/W	0
0	PSM0 IE		R/W	0

Table 5-35 : Interrupt Enable Register

5.3.9.2 PSI5 IRQ Trigger Enable Register 0x424

Trigger of the PSI5 status interrupt

Bit	Symbol	Description	Access	Reset Value
31	POF7 TRIG	Channel [x]: PSI5[x] OFLOW trigger 1 = PSI5[x] OFLOW triggers the PSI5 Status Interrupt IRQ 0 = PSI5[x] OFLOW trigger is disabled	R/W	0
30	POF6 TRIG		R/W	0
29	POF5 TRIG		R/W	0
28	POF4 TRIG		R/W	0
27	POF3 TRIG		R/W	0
26	POF2 TRIG		R/W	0
25	POF1 TRIG		R/W	0
24	POF0 TRIG		R/W	0
23	PSS7 TRIG	PSI5[x] SYNC SPUR trigger 1 = PSI5[x] SYNC SPUR triggers the PSI5 Status Interrupt IRQ 0 = PSI5[x] SYNC SPUR trigger is disabled	R/W	0
22	PSS6 TRIG		R/W	0
21	PSS5 TRIG		R/W	0
20	PSS4 TRIG		R/W	0
19	PSS3 TRIG		R/W	0
18	PSS2 TRIG		R/W	0
17	PSS1 TRIG		R/W	0
16	PSS0 TRIG		R/W	0
15	PR7 TRIG	PSI5[x] RESET trigger 1 = PSI5[x] RESET triggers the PSI5 Status Interrupt IRQ 0 = PSI5[x] RESET trigger is disabled	R/W	0
14	PR6 TRIG		R/W	0
13	PR5 TRIG		R/W	0
12	PR4 TRIG		R/W	0
11	PR3 TRIG		R/W	0
10	PR2 TRIG		R/W	0
9	PR1 TRIG		R/W	0
8	PR0 TRIG		R/W	0

Bit	Symbol	Description	Access	Reset Value
7:0	-	Reserved	-	-

Table 5-36 : PSI5 IRQ Trigger Enable Register

5.3.9.3 Interrupt Status Register 0x428

For an interrupt status bit to be set, the interrupt must be enabled before the interrupt event.

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved	-	-
23	CCR7 ST	Cycle Counter Reached IRQ Status This bits are cleared by reading this register	R/C	0
22	CCR6 ST		R/C	0
21	CCR5 ST		R/C	0
20	CCR4 ST		R/C	0
19	CCR3 ST		R/C	0
18	CCR2 ST		R/C	0
17	CCR1 ST		R/C	0
16	CCR0 ST		R/C	0
15	PSI7 ST	PSI5 Status Interrupt Status Cleared by reading the PSI5 Interrupt Status Register	R	0
14	PSI6 ST		R	0
13	PSI5 ST		R	0
12	PSI4 ST		R	0
11	PSI3 ST		R	0
10	PSI2 ST		R	0
9	PSI1 ST		R	0
8	PSI0 ST		R	0
7	PSM7 ST	PSI5 SYNC MATCH IRQ Status This bits are cleared by reading this register	R/C	0
6	PSM6 ST		R/C	0
5	PSM5 ST		R/C	0
4	PSM4 ST		R/C	0
3	PSM3 ST		R/C	0
2	PSM2 ST		R/C	0
1	PSM1 ST		R/C	0
0	PSM0 ST		R/C	0

Table 5-37 : Interrupt Status Register

5.3.10 Extended Timer Registers

The Extended Timer Registers enable the use of larger 31 Bit Cycle or TP values instead of the 12 Bit wide Values provided by the protocol registers. When setting the enable bit the extended the value of the protocol register is overwritten with the extended value.

5.3.10.1 Extended Cycle Registers 0x500 – 0x51C

Bit	Symbol	Description	Access	Reset Value
31	EX[x] CYCLE ENABLE	Enables the extended Cycle Register of Channel [x].	R/W	0
30:0	EX[x] CYCLE	Channel [x]: Extended Cycle Time. The time base depends on the *** [x] CYCLE BASE of the selected protocol (CP, SWP, PWM, AK, PSI5) A new value becomes active as soon as the currently transmitted pulse is completed.	R/W	0

Table 5-38 : Extended Cycle Registers

A long timer value of the pulse width or cycle time can be reset by disabling the protocol via the Channel Control Register.

Register	Bar Offset
Extended Cycle Register Channel 0	0x500
Extended Cycle Register Channel 1	0x504
Extended Cycle Register Channel 2	0x508
Extended Cycle Register Channel 3	0x50C
Extended Cycle Register Channel 4	0x510
Extended Cycle Register Channel 5	0x514
Extended Cycle Register Channel 6	0x518
Extended Cycle Register Channel 7	0x51C

5.3.10.2 Extended TP Registers 0x520 – 0x53C

Bit	Symbol	Description	Access	Reset Value
31	EX[x] TP ENABLE	Enables the extended TP Register of Channel [x].	R/W	0
30:0	EX[x] TP	Channel [x]: Extended TP Time. The time base depends on the *** [x] TP BASE of the selected protocol (CP, SWP, PWM, AK, PSI5) A new value becomes active as soon as the currently transmitted cycle is completed.	R/W	0

Table 5-39 : Extended TP Registers

A long timer value of the pulse width or cycle time can be reset by disabling the protocol via the Channel Control Register.

Register	Bar Offset
Extended TP Register Channel 0	0x520
Extended TP Register Channel 1	0x524
Extended TP Register Channel 2	0x528
Extended TP Register Channel 3	0x52C
Extended TP Register Channel 4	0x530
Extended TP Register Channel 5	0x534
Extended TP Register Channel 6	0x538
Extended TP Register Channel 7	0x53C

5.3.11 Board Status

5.3.11.1 Board Health Register 0xFF4

Bit	Symbol	Description	Access	Reset Value
31:23	-	Reserved	-	-
23:16	XADC	XADC sensor alarm bits An alarm bits indicates an out of limits supply voltage or an internal overtemperature	R	0
15:0	TEMP XADC	Result of the XADC on-chip temperature sensor measurement in degrees centigrade in steps of 1/256 °C. This is a signed value. A new readout is available every ~100 µs	R/W	0

Table 5-40 : Board Health Register

5.3.11.2 Scratchpad Register 0xFF8

Bit	Symbol	Description	Access	Reset Value
31:0	SCRATCH	Scratchpad Register Can be used to test read and write operations	R/W	0

Table 5-41 : Scratchpad Register

5.3.11.3 Firmware Identification Register 0xFFC

Used by the driver software to determine the firmware version.

Bit	Symbol	Description	Access	Reset Value
31:24	FW_MAJ	Firmware Major Version	R	0x01
23:16	FW_MIN	Firmware Minor Version	R	0x01
15:8	FW_REV	Firmware Revision	R	x
7:0	FW_BLD	Firmware Build Count	R	x

Table 5-42 : Firmware Identification Register

6 Protocol Setup Examples

6.1 Custom Protocol: Software procedure example

The software examples listed in this section show how to set up the different protocols. The interrupt handling was not considered for better understanding. Nevertheless the board is designed to be controlled by the interrupts, especially when reloading the FIFOS or receiving data and status messages.

6.1.1 Direct control by software

The default register of the custom protocol can be used to directly control the currents of the individual channels.

	Register	Value	Description
Setup:	Current Level register	HIGH, MID LOW	Set current levels
	CP Cycle register	CP DEFAULT	Select Default current
Start:	Channel Control Register	MODE	Set protocol for the channel
Operation:	CP Cycle register	CP DEFAULT	Change the Default current directly

```
Pseudo Code Example: Channel 0

// Channel 0: LOW = 0 mA, MID = 5 mA, HIGH = 10 mA
write_32bit (Current Level register channel 0, 0x0871_1000)

// Channel 0: Default Current is MID(5 mA)
write_32bit (CP Cycle Register Channel 0, 0x8000_0000)  // CP Mode has to be 0

// After setup, the custom protocol for channel 0 is activated to load it with 5
mA
write_32bit(Channel Control Register, 0x0000_0001)

// Channel 0: Default Current is set to HIGH(10 mA)
write_32bit (CP Cycle Register Channel 0, 0xC000_0000)  // CP Mode has to be 0
```

6.1.2 Custom Protocol in FIFO mode - Sequencer

The Sequencer mode allows to output the frame of an custom protocol equidistantly.

	Register	Value	Description
Setup:	Current Level Register	HIGH, MID LOW	Set the current levels
	CP Cycle Register	CP DEFAULT CP TP, CP TP Base CPCYCLE, CP CYCLE MODE CP MODE	Select the default current Set the bit width Set the cycle time Select the sequencer mode
	CP FIFO Data Register	CP	Load the FIFO with the Frame
Start:	Channel Control Register	MODE	Set protocol for the channel
Operation:	CP FIFO Data Register	CP	Reload the FIFO every Cycle with the new Data Frame

```
Pseudo Code Example: Channel 2

// Channel 2: LOW = 0 mA, MID = 5 mA, HIGH = 10 mA
write_32bit (Current Level register channel 2, 0x0871_1000)

// Channel 2: Default Current is LOW(0 mA); Bit width is 40 µs; Cycle time
// is 5 ms  CP Mode = Sequencer Mode
write_32bit (CP Cycle Register Channel 2, 0x2028_7005)

// Load the Frame into the FIFO. BIT 1 = HIGH; BIT 2 = MID; BIT 3 = HIGH,
// The remaining 13 bits are LOW
write_32bit(CP FIFO Data Register Channel 2, 0x5555_557B)

// After setup, the custom protocol for channel 2 is activated
write_32bit(Channel Control Register, 0x0000_0100)

// When a new frame is loaded into the FIFO, it is automatically output during
// the next cycle. In order to output frames equidistantly, the FIFO must be
// reloaded after each cycle.

// Load the Frame into the FIFO. BIT 1 = HIGH; BIT 2 = MID; BIT 3 = HIGH,
// The remaining 13 bits are LOW
write_32bit(CP FIFO Data Register Channel 2, 0x5555_557B)
```

6.1.3 Custom Protocol in FIFO mode - manual triggered

Manual mode allows the frame of a user-defined protocol to be triggered by software.

	Register	Value	Description
Setup:	Current Level Register	HIGH, MID LOW	Set the current levels
	CP Cycle Register	CP DEFAULT CP TP, CP TP Base CPCYCLE, CP CYCLE MODE CP MODE	Select the Default current Set the bit width Set the cycle time Select the manual trigger mode
	CP FIFO Data Register	CP	Load the FIFO with the Frame
Start:	Channel Control Register	MODE	Set protocol for the channel
	CP Cycle Register	CP Trig	Output the Frame stored in the FIFO
Operation:	CP FIFO Data Register	CP	Reload the FIFO
	CP Cycle Register	CP Trig	Output the Frame stored in the FIFO

```
Pseudo Code Example: Channel 2

// Channel 2: LOW = 0 mA, MID = 5 mA, HIGH = 10 mA
write_32bit (Current Level register channel 2, 0x0871_1000)

// Channel 2: Default Current is LOW(0 mA); Bit width is 40 µs;
// Cycle time is 5 ms
//            CP Mode = Manual Mode
write_32bit (CP Cycle Register Channel 2, 0x2028_3005)

// Load the Frame into the FIFO. BIT 1 = HIGH; BIT 2 = MID; BIT 3 = HIGH
// The remaining 13 bits are LOW
write_32bit(CP FIFO Data Register Channel 2, 0x5555_557B)

// After setup, the custom protocol for channel 2 is activated
write_32bit(Channel Control Register, 0x0000_0100)

// Channel 2: Set the bit CP Trig to "1" to start the output of the first frame.
//All other bits remain unchanged.
write_32bit (CP Cycle Register Channel 2, 0x2028_3005)

// Load the Frame into the FIFO. BIT 1 = HIGH; BIT 2 = MID; BIT 3 = HIGH,
// The remaining 13 bits are LOW
write_32bit(CP FIFO Data Register Channel 2, 0x5555_557B)

// Channel 2: Set the bit CP Trig to "1" to start the output of the
// second frame. All other bits remain unchanged.
write_32bit (CP Cycle Register Channel 2, 0x2028_3005)
```

6.2 Square Wave Protocol: Software procedure example

	Register	Value	Description
Setup:	Current Level Register	HIGH, MID LOW	Set the current levels
	SWP Cycle Register	SWP TP, SWP TP Base SWP CYCLE, SWP CYCLE MODE	Set the bit width Set the cycle time
Start:	Channel Control Register	MODE	Set protocol for the channel
Operation:	SWP Cycle Register	SWP TP, SWP TP Base SWP CYCLE, SWP CYCLE	Change the bit width and cycle time if needed

```
Pseudo Code Example: Channel 0

// Channel 0: Setup current load LOW = 0 mA, MID = don't care, HIGH = 10 mA
write_32bit (Current Level Register Channel 0, 0x0870_0000)

//Setup the Square Wave Protocol: Cycle time: 1 ms ; High Time = 100 µs
write_32bit (SWP Cycle Register Channel 0, 0x2064_3001)

// After setup, the Square Wave Protocol for channel 0 is activated
write_32bit(Channel Control Register, 0x0000_0002)

//Change the Square Wave Protocol timing: Cycle time: 2 ms ; High Time = 200 µs
write_32bit (SWP Cycle Register Channel 0, 0x20C8_3002)
```

6.3 PWM Protocol: Software procedure example

	Register	Value	Description
Setup:	Current Level Register	HIGH, MID LOW	Set the current levels
	PWM Cycle Register	PWM TP PWM TP MULT PWM CYCLE, PWM CYCLE BASE	Set the standard bit width TP Set the TP length multiplier Set the cycle time
Start:	Channel Control Register	MODE	Set protocol for the channel
Operation:	PWM Cycle Register	PWM CYCLE, PWM CYCLE PWM TP MULT	Change the cycle time or TP length multiplier if needed

```
Pseudo Code Example: Channel 0

// Channel 0: Setup current load LOW = 0 mA, MID = don't care, HIGH = 10 mA
write_32bit (Current Level Register Channel 0, 0x0870_0000)

// Setup the PWM Protocol: Cycle time: 1 ms ; standard TP length  = 10 µs,
// TP multiplier = 1
write_32bit (PWM Cycle Register Channel 0, 0x0640_7001)

// After setup, the PWM Protocol for channel 0 is activated
write_32bit(Channel Control Register, 0x0000_0003)

// The Pulse length is increased from 1 TP to 4 TPs:
// Cycle time: 1 ms ; standard TP length  = 10 µs, TP multiplier = 4
write_32bit (PWM Cycle Register Channel 0, 0x0641_3001)
```

6.4 AK Protocol: Software procedure example

	Register	Value	Description
Setup:	Current Level Register	HIGH, MID LOW	Set the current levels
	AK Cycle Register	AK TP AK CYCLE, AK CYCLE BASE	Set the bit width Set the cycle time
	AK Control Register	AK BIT NUMBER AK B# AK ASP	Set amount of bits to transfer Set bits to transfer Set the type of speed pulse
Start:	Channel Control Register	MODE	Set protocol for the channel

```
Pseudo Code Example: Channel 0

// Channel 0: Setup current load LOW = 0 mA, MID = don't care, HIGH = 10 mA
write_32bit (Current Level Register Channel 0, 0x0870_0000)

// Setup the AK Cycle Register: Cycle time: = 1 ms; Bit length = 10 µs
write_32bit (AK Cycle Register Channel 0, 0x0064_3001)

// Setup the AK Control Register: AK Protocol bits = 0x123;
// ASP = Normal Speed Pulse
// All nine bits are transmitted
write_32bit (AK Control Register Channel 0, 0x0000_9323)

// After setup, the AK Protocol for channel 0 is activated
write_32bit (Channel Control Register, 0x0000_0004)
```

6.5 PSI5 Protocol: Software procedure example

6.5.1 Asynchronous Mode

	Register	Value	Description
Setup:	Current Level Register	HIGH, MID LOW	Set the current levels
	PSI5 Cycle Register	PSI5 TP PSI5 CYCLE	Set the bit width Set the periodic output time of the frame
	PSI5 Detection Register	PSI5 RESET THRESHOLD PSI5 RESET TTH	Set the psi5 reset detection voltage Set the reset detection time
	PSI5 Control Register	PSI5 START BIT, PSI5 START BIT EN PSI5 BIT NUMBER PSI5[x] BUS MODE	Set whether start bits are to be sent and which Set number of bits to be sent Select the Asynchronous Mode
	PSI5 Default Date Frame Register	PSI5 Frame	Default frame to be send
	PSI5 Data Frame FIFO Register	PSI5 FIFO	Alternative to the PSI5 Default Frame
Start:	Channel Control Register	MODE	Set protocol for the channel

```
Pseudo Code Example: Channel 0

// Channel 0: Setup current load LOW = 0 mA, MID = don't care, HIGH = 10 mA
write_32bit (Current Level Register Channel 0, 0x0870_0000)

// Setup the PSI5 Cycle Register: Cycle time: = 500µs; Bit length = 10 µs
write_32bit (PSI5 Cycle Register Channel 0, 0x0064_01F4)

// In the PSI5 Detection Register it is defined that the reset is detected
// from a length of 5ms and a voltage of less than 3V.
write_32bit (PSI5 Detection Register Channel 0, 0x0000_1CF2)

// Setup of the PSI5 Control register
// The start bits are enabled and set to "11"; After the two start bits 26 bits
// of the frame will be transferred.
// PSI5 BUS MODE = Asynchronous Mode
write_32bit(PSI5 Control Register Channel 0, 0x0000_03E4)

// Here the frame is defined which is sent as soon as the
// PSI5 Data Frame FIFO is empty  default frame: 0x3654321
write_32bit (PSI5 Default Data Frame Register Channel 0, 0x0365_4321)

// If a defined sequence of frames needs to be sent, it must be loaded
// into the FIFO.
// first frame:         0x0111_1111
// second frame:        0x0222_2222
write_32bit (PSI5 Data Frame FIFO Register Channel 0, 0x0111_1111)
write_32bit (PSI5 Data Frame FIFO Register Channel 0, 0x0222_2222)

// After the setup the output is started in by activating the PSI5 protocol for
// the channel.
write_32bit (Channel Control Register, 0x0000_0005)
```

6.5.2 Synchronous Mode:

	Register	Value	Description
Setup:	Current Level Register	HIGH, MID LOW	Set the current levels
	PSI5 Cycle Register	PSI5 TP PSI5 CYCLE	Set the bit width Set the periodic output time of the frame
	PSI5 Detection Register	PSI5 SYNC THRESHOLD PSI5 RESET THRESHOLD PSI5 RESET TTH	Set the sync signal detection voltage Set the psi5 reset detection voltage Set the reset detection time
	PSI5 Control Register	PSI5 SLOT DELAY PSI5 PULSE MODE PSI5 START BIT, PSI5 START BIT EN PSI5 BIT NUMBER PSI5[x] BUS MODE	Select the PSI5 Slot Select Tooth Gap or Pulse Width method Set whether start bits are to be sent and which Set number of bits to be sent Select the Synchronous Mode
	PSI5 Default Date Frame Register	PSI5 Frame	Default frame to be send
	PSI5 Data Frame FIFO Register	PSI5 FIFO	Alternative to the PSI5 Default Frame
Start:	Channel Control Register	MODE	Set protocol for the channel

```
Pseudo Code Example: Channel 0

// Channel 0: Setup current load LOW = 0mA, MID = don't care, HIGH = 10mA
write_32bit (Current Level Register Channel 0, 0x0870_0000)

// Setup the PSI5 Cycle Register: Cycle time: = 500µs; Bit length = 10 µs
write_32bit (PSI5 Cycle Register Channel 0, 0x0064_01F4)

// In the PSI5 Detection Register it will be defined that the reset is detected
// from a length of 5ms and a voltage of less than 3V
// The Sync Threshold voltage is set so that sync pulses are detected from an
// absolute voltage of 5.5V.
write_32bit (PSI5 Detection Register Channel 0, 0x00D2_1CF2)

// Setup of the PSI5 Control register
// The start bits are enabled and set to "11"; After the two start bits 26 bits
// of the frame will be transferred. PSI5 BUS MODE = Synchronous Mode without
// Daisy Chain;   Slot Delay = 45 µs; Pulse Mode = Pulse Width method
write_32bit(PSI5 Control Register Channel 0, 0x002D_07E5)

// Here the frame is defined which is sent as soon as the
// PSI5 Data Frame FIFO is empty  default frame: 0x3654321
write_32bit (PSI5 Default Data Frame Register Channel 0, 0x0365_4321)

// If a defined sequence of frames needs to be sent, it must be loaded
// into the FIFO.  first frame:0x0111_1111     second frame:     0x0222_2222
write_32bit (PSI5 Data Frame FIFO Register Channel 0, 0x0111_1111)
write_32bit (PSI5 Data Frame FIFO Register Channel 0, 0x0222_2222)

// After the setup the output is started in by activating the PSI5 protocol for
// the channel.
write_32bit (Channel Control Register, 0x0000_0005)
```

6.5.3 Daisy Chain Operation

In daisy chain mode the sensors do not have a fixed time slot. Therefore, the start needs to be in PSI5[x] BUS MODE “Synchronous Mode **without** Daisy Chain”, so that the supply voltage is not passed to the following sensor. Wait for the ECU to assign the time slot and set up the PSI5[x] SLOT DELAY. Then Change the PSI5[x] BUS MODE to “Synchronous Mode **with** Daisy Chain”. The supply voltage is than passed on. Please refer to the PSI5 specification.

7 Functional Description

7.1 I/O Electrical Interface

The TPMC160 provides 8 channels of automotive sensor simulation, each with a programmable current sink that sinks current from the sensor's VDD to GND. Each channel also provides a switchable Daisy-Chain GND.

Symbol	Signal	Description
V_{DD}	4-24 V	Sensor Supply
V_{SS}	GND	Sensor Ground
V_{SS_DAISY}	(GND)	Daisy-Chain GND

Table 7-1 : Channel Signal Lines to FPGA

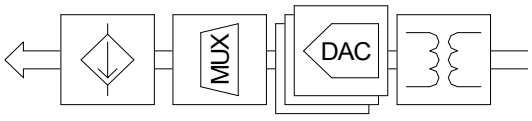
The TPMC160 supports both high-side and low-side sensing for wheel speed sensors.

Please note that the current load provides quite a substantial thermal load, concentrated on a small area. For example, a channel with VDD = 12 V and 40 mA sink current has to dissipate ~0,5 W. This can lead to quite substantial temperature rises, therefore active cooling of the TPMC160 is required.

Active cooling of the TPMC160 is required

7.1.1 Current Sink

Each Sensor simulation circuit provides a current sink, which sinks current from the sensor's VDD to VSS. It can be set to three different current levels. The Preset of the current levels are controlled with three DACs. During operation, the active current level is selected with a multiplexer that selects which DAC is connected to the current sink. The multiplexer can be controlled by the protocol engine or through a register setting to support custom protocols.



The maximum settable current is about 75 mA. This covers the PSI5 requirement of 65 mA, with additional headroom.

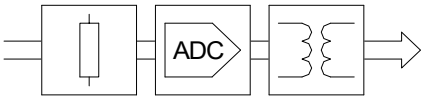
DAC Resolution	10 bit, single ended, unipolar
DAC LSB	73.85 µA
DAC Output Range	0 mA to 75.625 mA

Table 7-2 : Current Sink Characteristics

7.1.2 Voltage Monitor

The voltage monitor of each Sensor simulation circuit measures the voltage between the sensors VDD and VSS pins. It is mainly used for PSI5 SYNC pulse and reset detection, but can also be used for general supply monitoring.

The building blocks of the voltage monitor are a voltage scaling circuit followed by a buffer circuit that drives a 10 bit, 1 Msps ADC.



The maximum input voltage for the Voltage Monitor is 26,8 V, giving a full scale reading of the ADC.

ADC Resolution	10 bit, single ended, unipolar
ADC Sample Rate	1 Msps
ADC LSB	26.16 mV
ADC Input Range	0 V to 26.8 V
Input Impedance	570 kΩ

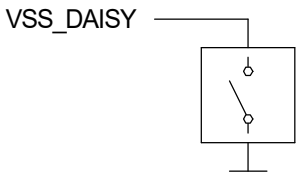
Table 7-3 : Voltage Monitor Characteristics

The ADC readout values are evaluated in the FPGA, and compared against settable values, to indicate the detection of a PSI5 Sync pulse or a PSI5 reset condition.

In principle, the ADC's input impedance leads to a leakage current that sums up with the DAC-controlled current flowing through the sink. The maximum leakage current, arising at 24V, amounts only 42 µA. This is less than 1 LSB of the DAC controlled current, and thus can be neglected.

7.1.3 Daisy-Chain GND

Each Sensor simulation circuit provides the additional Daisy-Chain GND. This is meant to be used for PSI5 Daisy Chain Bus Mode (PSI5-D), where the sensor provides an internal switch to connect the ground of the next sensor to the bus VSS (Sensor GND).



Leave this signal open when the sensor is not used in a daisy-chain topology, when used in a daisy-chain topology, connect it to the VSS of the next sensor.

7.1.4 Typical Test and Application Circuits

This figure shows a typical test and application circuit für Wheel Speed Sensors. V_{CC} would be an output of the ECU, or simply the battery voltage. R_L has usually a value in a range from 25 Ω to 100 Ω. C_L is optional and the value is application specific. The voltage over R_L (= V_{OUT}) can be used to determine the output current of the TPMC160.

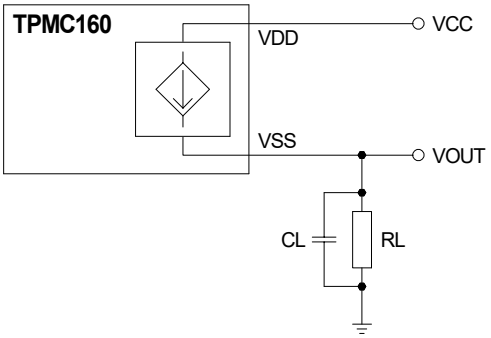


Figure 7-1 : Typical Test and Application Circuit: Wheel Speed

The figure shows a low-side sensing configuration. The TPMC160 supports both high-side and low-side sensing for wheel speed sensors.

For PSI5-D applications the TPMC160 provides a daisy chain GND that can be used to pass the supply to the next sensor in the daisy chain. Connect the V_{SS} of the following sensor to the V_{SS_DAISY} pin of the TPMC160. Please refer to the PSI5 specification for details about PSI5-D applications. For Wheel Speed applications the V_{SS_DAISY} pin can be ignored.

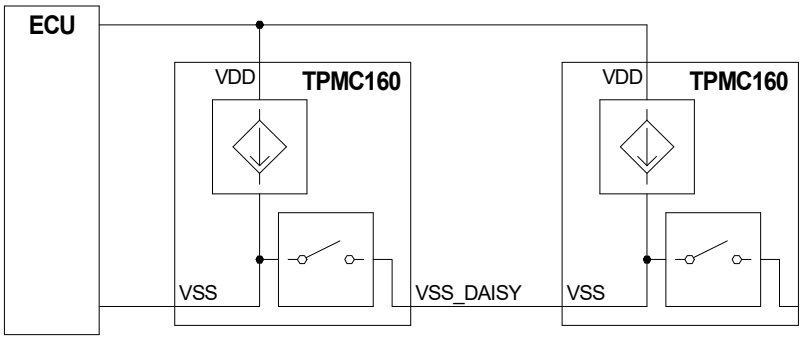


Figure 7-2 : Typical Test and Application Circuit: PSI5 Daisy Chain

7.2 Supported Protocols

7.2.1 Wheel Speed

The TPMC160 supports the simulation of the three main variants for Wheel Speed Sensors:

- Standard 2-level (7/14 mA) wheel speed sensors with “Speed Protocol” or “Duty Cycle”
- PWM encoded 2-level sensors, with support for airgap warning (LR), assembly position (EL) and direction of rotation (DR-R/L)
- Three level (7/14/28 mA) VDA or “AK-protocol” sensors

7.2.1.1 Square Wave “Speed Protocol” or “Duty Cycle”

For every detected tooth a 14 mA rotation signal is send. The pulse duration increases with lower rotation speed. This results in a 2-level encoding that is based on a duty cycle setting:

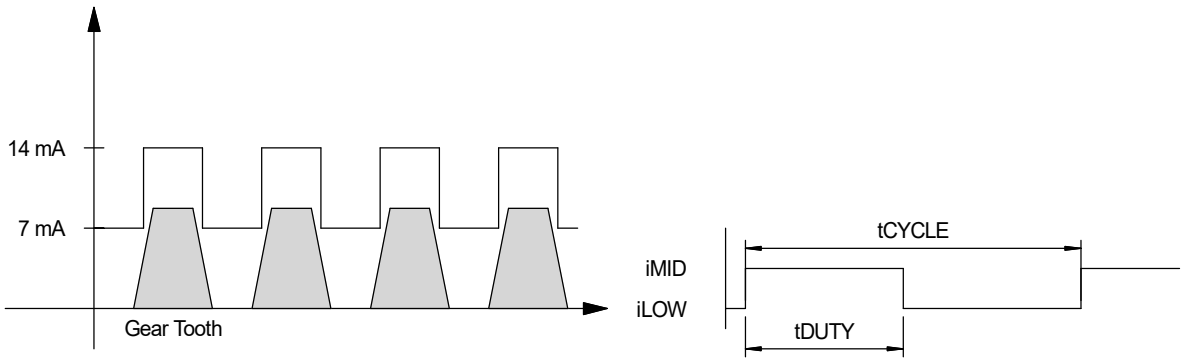


Figure 7-3 : Speed Protocol / Duty Cycle Diagram

7.2.1.2 “PWM”

PWM Wheel Speed Sensors transmit additional information by varying the length of the speed pulses. PWM encoding is based on the t_P setting. All pulse widths are derived from this value:

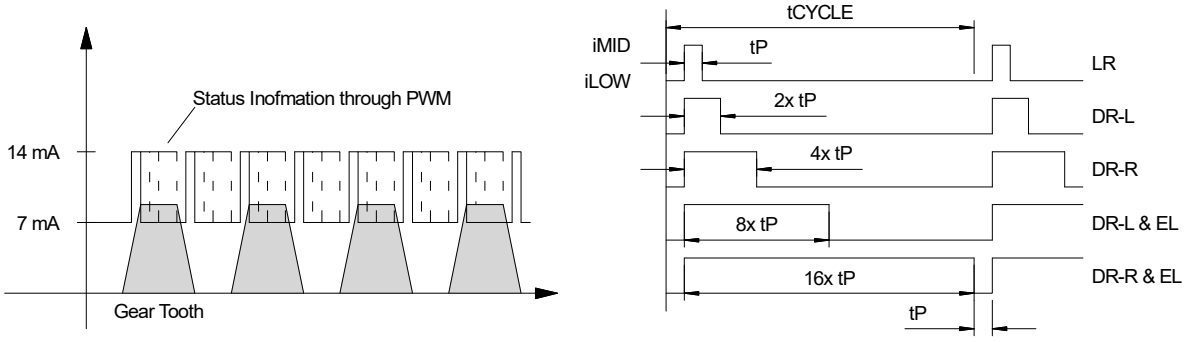


Figure 7-4 : PWM Diagram

A “zero speed” or “stand still” indication is usually done with pulses of 32 x t_P length and with an appropriate large gap (t_{CYCLE} = 0.5 – 2 ms).

When t_{CYCLE} is smaller than the status pulse width, the pulse is truncated. When t_{CYCLE} is elapsed, a low pulse with the length of t_P will be send, followed by the next high pulse.

7.2.1.3 “AK-Protocol” or “VDA”

Wheel Speed Sensors with “AK-Protocol” or “VDA” use three current levels and transmit a 9-bit status word after the speed pulse.

The VDA encoding starts with a “speed pulse” with HIGH current level, followed by a short gap, and then followed by the manchester encoded protocol bits with MID current levels.

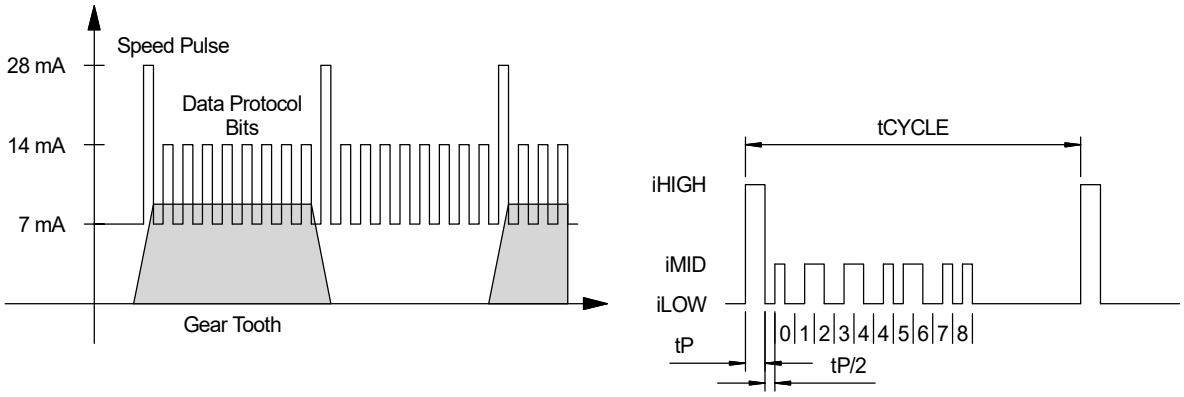


Figure 7-5 : AK-Protocol / VDA Diagram

7.2.1.4 Custom Protocol

The TPMC160 provides a “Custom Protocol” mode, which can be used to simulate sensors that are not covered by the above descriptions. It supports three current levels, and supports a t_P based FIFO that can hold up to 16 x 16 (=256) current level settings.

7.2.2 PSI5

In a usual PSI5 application the ECU sends "sync" pulses by modulating the sensor supply with a higher voltage, and the sensor answers with a current modulated manchester encoded data word:

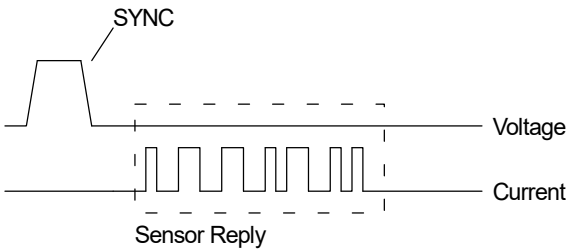


Figure 7-6 : PSI5 Diagram

The ECU can also use the sync pulses for an ECU to Sensor communication (using the "Tooth Gap" or "Pulse Width" method), to which the sensor can reply using an optional "Serial messaging channel" in the data word.

8 Pin Assignment – I/O Connector

8.1 Front Panel I/O Connector

Connector Type	HD 50 pos, female SCSI-2 type
Source & Order Info	AMP# 787395-5 (or compatible)

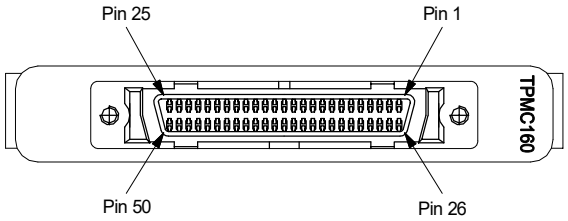


Figure 8-1 : Front Panel I/O Connector Pin Numbering

Pin	Name	Description	Channel
1	V_{DD}	Sensor Supply	Channel 0
2	V_{SS}	Sensor GND	
3	V_{SS_DAISY}	Daisy-Chain GND Leave open when the sensor is not used in a daisy-chain topology, when used in a daisy-chain topology, connect to the V_{SS} of the next sensor	
4	V_{DD}	Sensor Supply	Channel 1
5	V_{SS}	Sensor GND	
6	V_{SS_DAISY}	Daisy-Chain GND	
7	V_{DD}	Sensor Supply	Channel 2
8	V_{SS}	Sensor GND	
9	V_{SS_DAISY}	Daisy-Chain GND	
10	V_{DD}	Sensor Supply	Channel 3
11	V_{SS}	Sensor GND	
12	V_{SS_DAISY}	Daisy-Chain GND	
13	V_{DD}	Sensor Supply	Channel 4
14	V_{SS}	Sensor GND	
15	V_{SS_DAISY}	Daisy-Chain GND	
16	V_{DD}	Sensor Supply	Channel 5
17	V_{SS}	Sensor GND	
18	V_{SS_DAISY}	Daisy-Chain GND	
19	V_{DD}	Sensor Supply	Channel 6
20	V_{SS}	Sensor GND	
21	V_{SS_DAISY}	Daisy-Chain GND	

Pin	Name	Description	Channel
22	V_{DD}	Sensor Supply	Channel 7
23	V_{SS}	Sensor GND	
24	V_{SS_DAISY}	Daisy-Chain GND	
25-50	-	n.c.	-

Table 8-1 : Pin Assignment Front I/O Connector