The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC362

Conduction Cooled PMC

4 Channel High Speed

Synch/Asynch Serial Interface

Version 1.1

User Manual

Issue 1.7

September 2006

D76362800

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TPMC362-20

Conduction Cooled PMC

4 Channel High Speed Synch/Asynch Serial Interface

P14 Back I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	December 2003
1.1	Description of Build Option changed	May 2004
1.2	Added description of extended features/registers in TPMC362 V1.1	June 2004
1.3	Correction in Chapter “Build Option Register” (Reset Value)	September 2004
1.4	Changed naming of clock mode 4 to clock mode 9 and added description for clock mode 4 like the DSCC4 Clock Mode 4	December 2004
1.5	Power Requirements updated	December 2004
1.6	Changed description of reserved addresses	April 2005
1.7	New address TEWS LLC	September 2006

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1 Product Description

The TPMC362 is a standard single-width 32 bit Conduction Cooled PMC with four high speed serial data communication channels.

An Infineon PEF 20534 DMA Supported Serial communication controller (DSCC4) with integrated bus master PCI interface is used.

Several interrupt sources can generate interrupts on INTA for each channel. Interrupts can be enabled and disabled separately.

A 14.7456 MHz oscillator provides standard asynchronous baud rates. An additional 24 MHz oscillator is provided for other baud rates. A 10 MHz oscillator is used for the maximum synchronous baud rate of 10 Mbit/s.

Each channel can support many serial communication protocols such as HDLC, SDLC, PPP, asynchronous, monosynchronous, and bisynchronous.

Multiprotocol transceivers are used for the line interface. The physical interface can be selected by software individually for each channel as EIA-232, EIA-422, EIA-449, EIA-530, EIA-530A, V.35, V.36 or X.21.

The TPMC362 supports Receive Data (RxD +/-), Transmit Data (TxD +/-), Receive Clock (RxC +/-), Transmit Clock (TxC +/-), Ready-To-Send (RTS +/-), Clear-To-Send (CTS +/-), Carrier-Detect (CD +/-) and GND for each channel.

The DSCC4 contains a central receive and transmit FIFO of 128 long words (32 bit) each. Additionally each channel has a receive FIFO (17 long words deep) and a transmit FIFO (8 long words deep).

The TPMC362 provides rear panel I/O via P14.

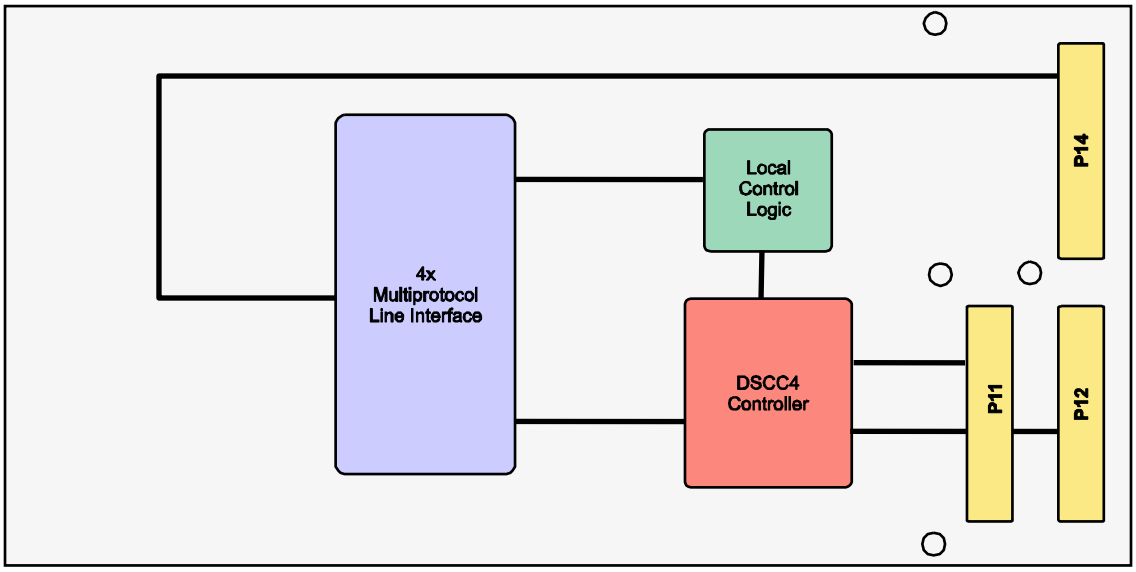

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	Conduction Cooled PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.1 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
Serial Controller with Integrated PCI Interface	PEF 20534 (Infineon)	
Serial Interface		
Number of Channels	4	
Physical Interface	LTC1544/LTC1546 (Linear Technology) Multiprotocol chip set, software-selectable, on-chip cable termination	
ESD Protection	4kV	
FIFO	Central receive and transmit FIFO of 128 long words (32 bit) each per channel: 17 long words receive FIFO and 8 long words transmit FIFO	
Maximum Data Rates	2 Mbit/s (asynchronous) 10 Mbit/s (synchronous)	
Interrupts	Using PCI INTA for all channels, on board Interrupt Status Register	
I/O Connector	PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	330 mA typical (no cable mode) @ +5V DC 770 mA typical (no load, V.35 mode) @ +5V DC	
Temperature Range	Operating Storage	-40 °C to +85 °C -65°C to +125°C
MTBF	337000 h	
Humidity	5 – 95 % non-condensing	
Weight	59 g	

Figure 2-1 : Technical Specification

3 Local Space Addressing

3.1 PEF 20534 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PEF 20534 local spaces.

PEF 20534 Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
1 (0x10)	MEM	2048	32	Little	DSCC4 On-Chip Register Address Space
2 (0x14)	MEM	64 K	8	Little	CPLD Register Address Space

Figure 3-1 : PEF 20534 Local Space Configuration

3.2 DSCC4 On-Chip Register Space Overview

PCI Base Address: PEF 20534 Base Address 1 (Offset 0x10 in PCI Configuration Space)

Offset to Base Address 1	Number of used DWORD registers	Description
0x0000	59 (0x0000…0x00EC)	Global Registers
0x0100	23 (0x0100…0x0158)	SCC0 Registers
0x0180	23 (0x0180…0x01D8)	SCC1 Registers
0x0200	23 (0x0200…0x0258)	SCC2 Registers
0x0280	23 (0x0280…0x02D8)	SCC3 Registers
0x0300	1 (0x0300)	LBI Control Register
0x0380	6 (0x0380…0x0394)	SCC Control Registers
0x0400	3 (0x0400…0x0408)	GPP Control Registers
0x0480	0	(unused)

Figure 3-2 : DSCC4 On-Chip Register Space Overview

For a detailed register description, please see DSCC4 data sheet at www.infineon.com.

3.3 CPLD Register Space

PCI Base Address: **PEF 20534 Base Address 2 (Offset 0x14 in PCI Configuration Space)**

Offset to Base Address 2	Register Name	Size (Bit)
0x00	MODE REGISTER 0	8
0x01	MODE REGISTER 1	8
0x02	TRANSMIT CLOCK SELECTION REGISTER	8
0x03	DTR3/DSR3 CONTROL REGISTER	8
0x04	RESET DSCC4 REGISTER	8
0x05	ID REGISTER	8
0x06	BUILD OPTION REGISTER	8
0x07...0x08	Reserved	8
0x09	OSCILLATOR SELECTION REGISTER	8
0x0A	CHANNEL 0 SPECIAL FUNCTION REGISTER A	8
0x0B	CHANNEL 0 SPECIAL FUNCTION REGISTER B	8
0x0C	CHANNEL 1 SPECIAL FUNCTION REGISTER A	8
0x0D	CHANNEL 1 SPECIAL FUNCTION REGISTER B	8
0x0E	CHANNEL 2 SPECIAL FUNCTION REGISTER A	8
0x0F	CHANNEL 2 SPECIAL FUNCTION REGISTER B	8
0x10	CHANNEL 3 SPECIAL FUNCTION REGISTER A	8
0x11	CHANNEL 3 SPECIAL FUNCTION REGISTER B	8
0x12 … 0x1F	Reserved	8

Figure 3-3 : CPLD Register Space

3.3.1 Mode Register 0 (0x00)

This register is left only for software compatibility reason with V1.0, please see 'Channel 0/1 Special Function Register A'

Bit	Symbol	Description	Access	Reset Value
7:5	MODE_CH1	Mode Channel 1	R/W	111
4	DCE_DTE1	DCE / DTE# Channel 1	R/W	1
3:1	MODE_CH0	Mode Channel 0	R/W	111
0	DCE_DTE0	DCE / DTE# Channel 0	R/W	1

Figure 3-4 : Mode Register 0

3.3.2 Mode Register 1 (0x01)

This register is left only for software compatibility reason with V1.0, please see 'Channel 2/3 Special Function Register A'

Bit	Symbol	Description	Access	Reset Value
7:5	MODE_CH3	Mode Selection Channel 3	R/W	111
4	DCE_DTE3	DCE / DTE# Channel 3	R/W	1
3:1	MODE_CH2	Mode Selection Channel 2	R/W	111
0	DCE_DTE2	DCE / DTE# Channel 2	R/W	1

Figure 3-5 : Mode Register 1

3.3.3 Transmit Clock Source Selection Register (0x02)

This register is left only for software compatibility reason with V1.0, please see 'Channel 0/1/2/3 Special Function Register A' (RxC_SRC0/1/2/3)

Bit	Symbol	Description	Access	Reset Value
7:6	TXC_SRC3	Clock Source TxC Channel 3	R/W	00
5:4	TXC_SRC2	Clock Source TxC Channel 2	R/W	00
3:2	TXC_SRC1	Clock Source TxC Channel 1	R/W	00
1:0	TXC_SRC0	Clock Source TxC Channel 0	R/W	00

Figure 3-6 : Clock Select Register

3.3.4 DTR3/DSR3 Control Register (0x03)

Bit	Symbol	Description	Access	Reset Value
7:2	-	Reserved (0 for reads)	R	0
1	DSR3	Data Set Ready Channel 3	R	-
0	DTR3	Data Terminal Ready Channel 3	R/W	0

Figure 3-7 : DTR3/DSR3 Register

As signals DTR3/DSR3 are not available at the P14 connector, accesses to this register have no further effect. This register only exists for compatibility reasons.

3.3.5 Reset DSCC4 Register (0x04)

Bit	Symbol	Description	Access	Reset Value
7:1	-	Reserved (0 for reads)	R	0
0	RSTSCC	Reset DSCC4 by writing '1'	R/W	0

Figure 3-8 : Reset DSCC4 Register

Setting bit RSTSCC will generate a reset pulse of about 200ns length on the "PCI RST#" pin of the DSCC4. This bit is self clearing.

Attention: When the DSCC4 is reset, all information in the *PCI Configuration Space* will be lost! It has to be saved before and restored after the reset of the device.

3.3.6 ID Register (0x05)

Bit	Symbol	Description	Access	Reset Value
7:0	ID	Revision ID	R	0x02

Figure 3-9 : ID Register

3.3.7 Build Option Register (0x06)

Bit	Symbol	Description	Access	Reset Value
7:4	-	Reserved (0 for reads)	R	0
3	BLD_OPT3	Build Option Input Pin 3	R	-
2	BLD_OPT2	Build Option Input Pin 2	R	-
1	BLD_OPT1	Build Option Input Pin 1	R	-
0	BLD_OPT0	Build Option Input Pin 0	R	-

Figure 3-10: Build Option Register

Address 0x07 and 0x08 are reserved.

The following registers are new in product version 1.1.

3.3.8 Oscillator Selection Register (0x09)

Bit	Symbol	Description	Access	Reset Value
7:1	-	Reserved (0 for reads)	R	0
0	OSC_SEL	0: Switch 14.7456 MHz to XTAL1/OSC (as in V1.0) 1: Switch 24 MHz to XTAL1/OSC	R/W	0

Figure 3-11: Oscillator Selection Register

This will select the oscillator switched to the global OSC input. This signal is supplied to the Baud Rate Generators (BRG) of all four channels. If a channel should get the others oscillator frequency for baud rate generation, this can be supplied via RxCLK input (see RXC_SRC setting of SFR A in the following chapter(s) and chapter "Clock Mode 8a/b").

The settings of 'transceiver mode' and 'clock selection' in registers addressed from 0x00 to 0x02 are now (in V1.1) alternatively organized per channel, together with the new features. For compatibility with V1.0, the old addressing is still possible.

3.3.9 Channel 0 Special Function Register A (0x0A)

Bit	Symbol	Description	Access	Reset Value
7	TXC_INV0	0: No inverting of TxC0; 1: TxC0 is inverted	R/W	0
6	RXC_INV0	0: No inverting of RxC0; 1: RxC0 is inverted	R/W	0
5:4	RXC_SRC0	Select RxCLK0 input source (see the table after next)	R/W	00
3:1	MODE_CH0	Mode Channel 0 (M2:M0, see next table)	R/W	111
0	DCE_DTE0	DCE / DTE# Channel 0	R/W	1

Figure 3-12: Channel 0 Special Function Register A

Transceiver Mode	M2	M1	M0	Driver/Receiver Mode
Not Used (Default V.11)	0	0	0	TxD,TxC,RxD,RxC,RTS,CTS,CD: **V.11**
EIA-530A	0	0	1	TxD,TxC,RxD,RxC,RTS,CTS,CD: **V.11**
EIA-530	0	1	0	TxD,TxC,RxD,RxC,RTS,CTS,CD: **V.11**
X.21	0	1	1	TxD,TxC,RxD,RxC,RTS,CTS,CD: **V.11**
V.35	1	0	0	TxD,TxC,RxD,RxC: **V.35** / RTS,CTS,CD: **V.28**
EIA-449/V.36	1	0	1	TxD,TxC,RxD,RxC,RTS,CTS,CD: **V.11**
V.28/EIA-232	1	1	0	TxD,TxC,RxD,RxC,RTS,CTS,CD: **V.28**
No Cable (high impedance)	1	1	1	TxD,TxC,RxD,RxC,RTS,CTS,CD: **Z**

Figure 3-13: Physical Interface Mode Selection

The default setting of the transceiver mode after reset is "111", that is the "No cable" mode, setting all drivers to high impedance.

The inverting of RxC and TxC can be used to change the active clock edge, when not corresponding correctly with the clock edge of external receiver/transmitter.

Apart from using RxCLK as input for an externally supplied receive clock on the RxC pin of the connector, RxCLK can also be source for the Baud Rate Generator (BRG) of a channel. Often the 14.7456 MHz oscillator is connected to the global XTAL1/OSC input for generating standard baud rates. To set data rates like e.g. 2 Mbit/s for one channel, an oscillator with 24 MHz is mounted. This alternative clock source can be switched to the RxCLKn inputs of the DSCC4 (choose "On board clock 24 MHz" in next figure). Setting the appropriate channel to Clock Mode 3b, RxCLK is connected to the internal baud rate generator (BRG) of this channel. See chapter "Clock mode 8a/b".

Input of RxC0	RXC_CTRL0
No Clock Source (RxCLK0 to GND)	00
External Clock (from RxC0)	01
On board Clock 24 MHz	10
On board Clock 14.7456 MHz	11

Figure 3-14: RxCLK input source selection

3.3.10 Channel 0 Special Function Register B (0x0B)

Bit	Symbol	Description	Access	Reset Value
7	-	Reserved	R	0
6	RTS_OUT0	Set value of RTS0_OUT (at Connector), when in 'Clock Mode 4' (see next line)	R/W	0
5	CM9_EN0	0: Normal Mode 1: Change Signal Routing to 'Clock Mode 9' (CM9): 10 MHz to TxCLK0, RTS0 to TxC_OUT0, external RxC0	R/W	0
4	CTS_VAL0	Set value of CTS0 Pin, when CTS_SRC0 is '1'	R/W	0
3	CTS_SRC0	Select CTS0 input source 0: CTS0 from external, 1: Set CTS0 value as CTS_VAL0	R/W	0
2	CD_OUT0	Set value of CD0_OUT line (at Connector); value of CD0 Pin (at DSCC4) is always low	R/W	0
1	CD_SRC0	Select CD0 input source 0: CD0 from external, 1: Pull CD0 Pin high	R/W	0
0	CD_DIR0	0: CD0 is input, 1: CD0 is output	R/W	0

Figure 3-15: Channel 0 Special Function Register B

CD_SRC0 is only significant when CD0 is set to input direction (CD_DIR0 = 0), CD_OUT0 is only significant when CD0 is output (CD_DIR0 = 1).

3.3.11 Channel 1 Special Function Register A (0x0C)

Bit	Symbol	Description	Access	Reset Value
7	TXC_INV1	0: No inverting of TxC1; 1: TxC1 is inverted	R/W	0
6	RXC_INV1	0: No inverting of RxC1; 1: RxC1 is inverted	R/W	0
5:4	RXC_SRC1	Select RxCLK1 input source	R/W	00
3:1	MODE_CH1	Mode Channel 1 (M2:M0, see next table)	R/W	111
0	DCE_DTE1	DCE / DTE# Channel 1	R/W	1

Figure 3-16: Channel 1 Special Function Register A

See description of 'Channel 0 Special Function Register A'.

3.3.12 Channel 1 Special Function Register B (0x0D)

Bit	Symbol	Description	Access	Reset Value
7	-	Reserved	R	0
6	RTS_OUT1	Set value of RTS1_OUT (at Connector), when in 'Clock Mode 4' (see next line)	R/W	0
5	CM9_EN1	0: Normal Mode 1: Change Signal Routing to 'Clock Mode 9' (CM9): 10 MHz to TxCLK1, RTS1 to TxC_OUT1, external RxC1	R/W	0
4	CTS_VAL1	Set value of CTS1 Pin, when CTS_IN_SRC1 is '1'	R/W	0
3	CTS_SRC1	Select CTS1 input source 0: CTS1 from external, 1: Set CTS1 value to CTS_VAL1	R/W	0
2	CD_OUT1	Set value of CD1_OUT line (at Connector), when Output; value of CTS1 Pin is always low	R/W	0
1	CD_SRC1	Select CD1 input source 0: CD1 from external, 1: Pull CD1 Pin high	R/W	0
0	CD_DIR1	0: CD1 is input, 1: CD1 is output	R/W	0

Figure 3-17: Channel 1 Special Function Register B

See description of 'Channel 0 Special Function Register B'.

3.3.13 Channel 2 Special Function Register A (0x0E)

Bit	Symbol	Description	Access	Reset Value
7	TXC_INV2	0: No inverting of TxC2; 1: TxC2 is inverted	R/W	0
6	RXC_INV2	0: No inverting of RxC2; 1: RxC2 is inverted	R/W	0
5:4	RXC_SRC2	Select RxCLK2 input source	R/W	00
3:1	MODE_CH2	Mode Channel 2 (M2:M0, see next table)	R/W	111
0	DCE_DTE2	DCE / DTE# Channel 2	R/W	1

Figure 3-18: Channel 2 Special Function Register A

See description of 'Channel 0 Special Function Register A'.

3.3.14 Channel 2 Special Function Register B (0x0F)

Bit	Symbol	Description	Access	Reset Value
7	-	Reserved	R	0
6	RTS_OUT2	Set value of RTS2_OUT (at Connector), when in 'Clock Mode 4' (see next line)	R/W	0
5	CM9_EN2	0: Normal Mode 1: Change Signal Routing to 'Clock Mode 9' (CM9): 10 MHz to TxCLK2, RTS2 to TxC_OUT2, external RxC2	R/W	0
4	CTS_VAL2	Set value of CTS2 Pin, when CTS_IN_SRC2 is '1'	R/W	0
3	CTS_SRC2	Select CTS2 input source 0: CTS2 from external, 1: Set CTS2 value to CTS_VAL2	R/W	0
2	CD_OUT2	Set value of CD2_OUT line (at Connector), when Output; value of CTS2 Pin is always low	R/W	0
1	CD_SRC2	Select CD2 input source 0: CD2 from external, 1: Pull CD2 Pin high	R/W	0
0	CD_DIR2	0: CD2 is input, 1: CD2 is output	R/W	0

Figure 3-19: Channel 2 Special Function Register B

See description of 'Channel 0 Special Function Register B'.

3.3.15 Channel 3 Special Function Register A (0x10)

Bit	Symbol	Description	Access	Reset Value
7	TXC_INV3	0: No inverting of TxC3; 1: TxC3 is inverted	R/W	0
6	RXC_INV3	0: No inverting of RxC3; 1: RxC3 is inverted	R/W	0
5:4	RXC_SRC3	Select RxCLK3 input source	R/W	00
3:1	MODE_CH3	Mode Channel 3 (M2:M0, see next table)	R/W	111
0	DCE_DTE3	DCE / DTE# Channel 3	R/W	1

Figure 3-20: Channel 3 Special Function Register A

See description of 'Channel 0 Special Function Register A'.

3.3.16 Channel 3 Special Function Register B (0x11)

Bit	Symbol	Description	Access	Reset Value
7	-	Reserved	R	0
6	RTS_OUT3	Set value of RTS3_OUT (at Connector), when in 'Clock Mode 4' (see next line)	R/W	0
5	CM9_EN3	0: Normal Mode 1: Change Signal Routing to 'Clock Mode 9' (CM9): 10 MHz to TxCLK3, RTS3 to TxC_OUT3, external RxC3	R/W	0
4	CTS_VAL3	Set value of CTS3 Pin, when CTS_IN_SRC3 is '1'	R/W	0
3	CTS_SRC3	Select CTS3 input source 0: CTS3 from external, 1: Set CTS3 value to CTS_VAL3	R/W	0
2	CD_OUT3	Set value of CD3_OUT line (at Connector), when Output; value of CTS3 Pin is always low	R/W	0
1	CD_SRC3	Select CD3 input source 0: CD3 from external, 1: Pull CD3 Pin high	R/W	0
0	CD_DIR3	0: CD3 is input, 1: CD3 is output	R/W	0

Figure 3-21: Channel 3 Special Function Register B

See description of 'Channel 0 Special Function Register B'.

Read accesses to all other addresses will return 0x00.

4 PEF 20534 Serial Controller

4.1 PCI Configuration Registers (PCR)

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	2102 110A
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	028000 21
0x0C	BIST	Header Type	Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	Base Address Register 1: base address of DSCC4 on-chip registers				Y	FFFFF800
0x14	Base Address Register 2: base address of Local Bus Interface				Y	FFFF0000
0x18	Base Address Register 3 (not used)				Y	00000000
0x1C	Base Address Register 4 (not used)				Y	00000000
0x20	Base Address Register 5 (not used)				Y	00000000
0x24	Base Address Register 6 (not used)				Y	00000000
0x28	Reserved				N	00000000
0x2C	Reserved				N	00000000
0x30	Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved				N	00000000
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	0A 03 01 00

Figure 4-1 : PEF 20534 Header

5 Application Information

5.1 Clock Modes

5.1.1 Overview of Clock Modes

The DSCC4 has several clock modes (CM) for internal or external clock sources. Possible sources are the global OSC input (connected to the 14.7456 MHz or 24 MHz oscillator), the RxCLKn (n: 0..3) inputs and TxCLKn. The RxCLKn inputs can be connected to the external RxCn signal coming from the transceivers, to the 14.7456 MHz or 24 MHz oscillator, or to GND. Depending on the clock mode, TxCLKn pins can be inputs for transmit (tx) clock or the 10 MHz oscillator or transmit clock monitor outputs.

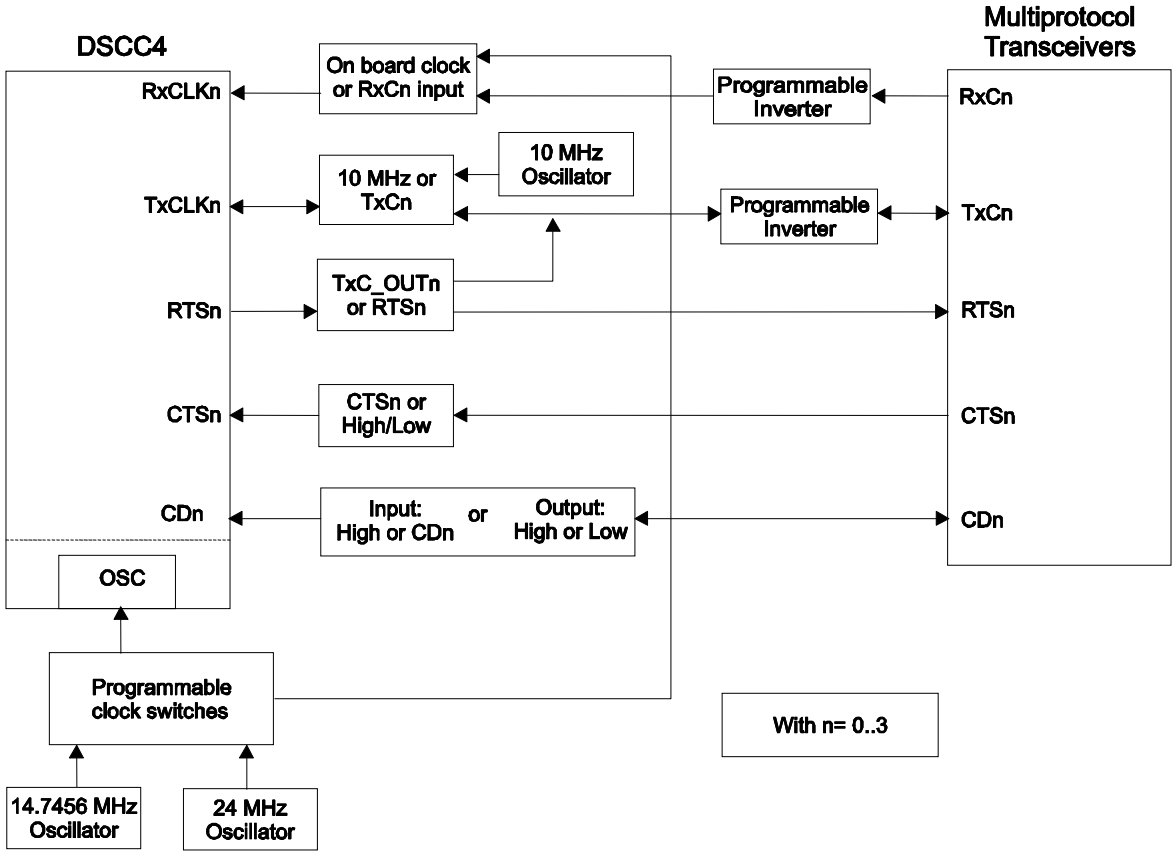

Figure 5-1 : Clock Sources

Clock mode	Clock source		Protocol	Maximum data rate		Comments
	transmit	receive		send	receive	
0a	TxCLK (directly)	RxCLK (directly)	sync / async	10 Mbit/s (sync) 2 Mbit/s (async)	10 Mbit/s (sync) 2 Mbit/s (async)	
0b	OSC over BRG	RxCLK (directly)	sync / async	1.8432 Mbit/s (sync) 921.6 Kbit/s (async)	10 Mbit/s (sync) 2 Mbit/s (async)	14.7456 MHz oscillator
				2 Mbit/s (sync) 1.5 Mbit/s (async)		24 MHz oscillator
3b	RxCLK over BRG		async	2 Mbit/s		
4	TxCLK (directly)	RxCLK (directly)	sync	10 Mbit/s		TxC_OUT at RTS
7b	OSC over BRG		async	921.6 Kbit/s (async)		14.7456 MHz oscillator
				1.5 Mbit/s (async)		24 MHz oscillator
8 (SCC in CM **3b**)	RxCLK over BRG		async	921.6 Kbit/s		14.7456 MHz oscillator
				1.5 Mbit/s		24 MHz on board Oscillator
9 (SCC in CM **4**)	TxCLK (directly)	RxCLK (directly)	sync	10 Mbit/s		10 MHz oscillator, enable CM 9 in SFR B

Figure 5-2 : Common used clock modes

The maximum data rates given in the table above refer to EIA-530 (V.11) and V.35 transceiver modes only. Maximum data rate of EIA-232 (V.28) is always 115.2 kbit/s.

When clock mode 0a is used for synchronous communication, an external Tx clock signal passes the transceivers before reaching the transmit control unit of the SCC. The resulting delay can be up to 90ns (t_P of V.11 receiver). The clock data signal controlled by this clock also passes the transceiver and can have a delay of 65ns (t_P of V.11 driver). Therefore a delay of more than 150ns can occur between the signal edge of Tx clock and the resulting change of Tx data.

In asynchronous mode some clock frequencies are divided by 16, see DSCC4 Data Sheet, p. 138.

5.1.2 Clock Mode 0a

Transmit and receive clock are directly supplied from external.

Figure 5-3 : Clock Mode 0a

5.1.3 Clock Mode 0b

Receive clock is directly supplied from external, transmit clock is generated by the BRG which is driven by the global OSC clock input, set to 14.7456 MHz or the 24 MHz oscillator. Transmit clock signal can be monitored on TxCLK, when bit 5 'TOE' in register CCR0 is set and bit DCE / DTE# in CPLD mode register is set.

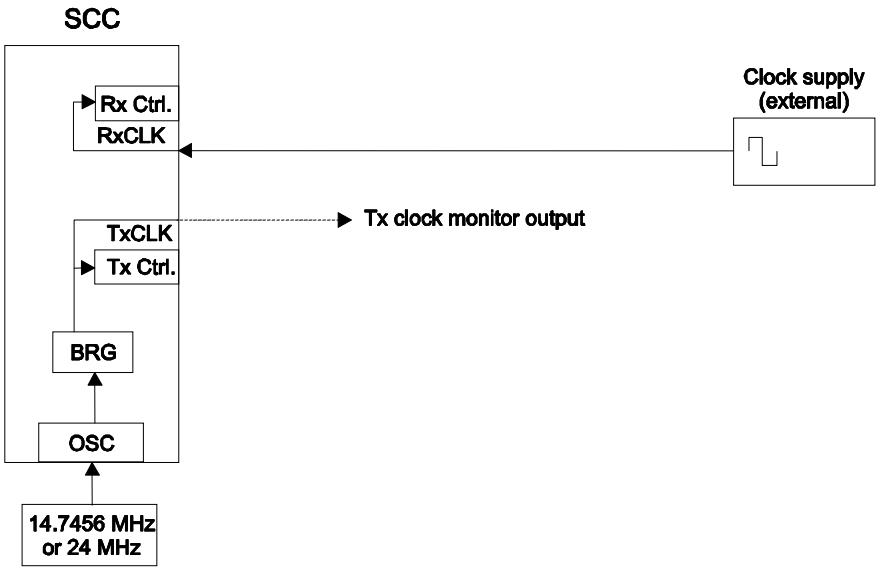

Figure 5-4 : Clock Mode 0b

5.1.4 Clock Mode 3b

Transmit and receive clock are generated by the BRG which is driven by RxCLK. Transmit clock signal can be monitored on TxCLK, when bit 5 ‘TOE’ in register CCR0 is set and bit DCE / DTE# in CPLD mode register is set.

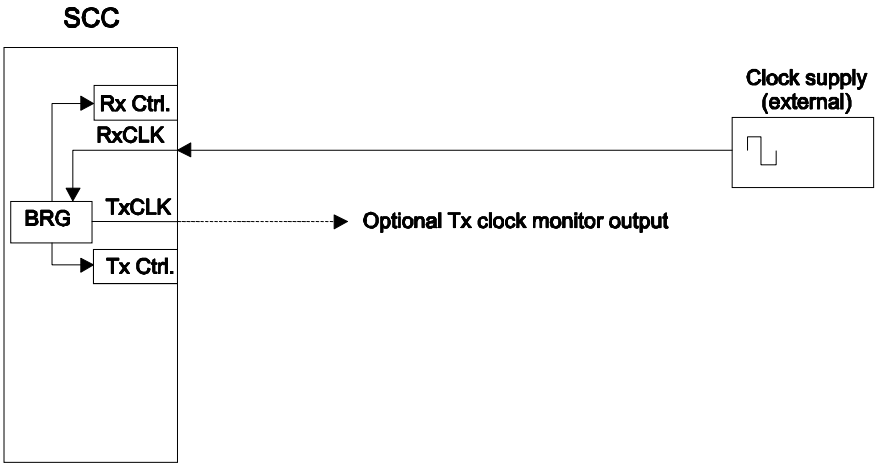

Figure 5-5 : Clock Mode 3b

5.1.5 Clock Mode 4

Receive and transmit clock are directly supplied from external. The TxC_OUT signal is provided at the RTS pin of the DSCC4 in CM4 and at the RTS output of the transceiver. CTS and CD inputs are low active clock gating signals, if receive and transmit clock should never be gated these pins can be set permanently high by setting the bits CTS_SRCn, CTS_VALn and CD_SRCn in SFR B to ‘1’.

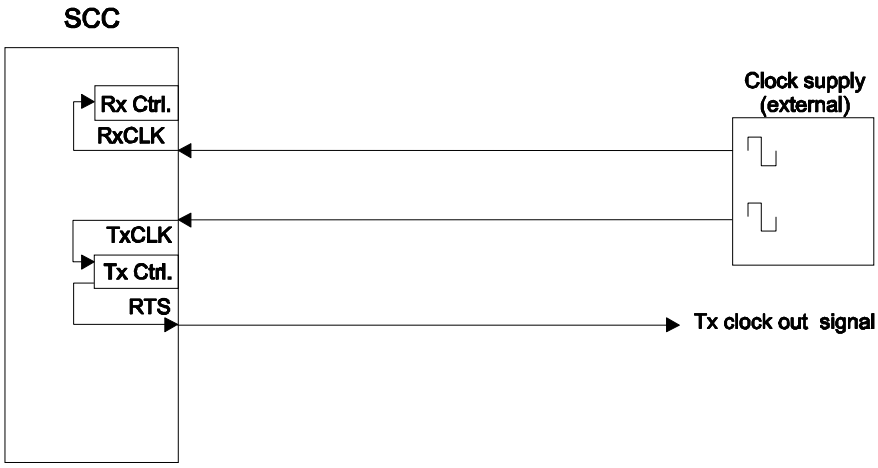

Figure 5-6 : Clock Mode 4

5.1.6 Clock Mode 7b

Similar to CM3b, except that BRG is driven by the 14.7456 MHz or 24 MHz on board oscillator signal, supplied via global OSC. Transmit clock signal can be monitored on TxCLK, when bit 5 ‘TOE’ in register CCR0 is set and bit DCE / DTE# in CPLD SFR A is set. In the SFR A of the corresponding channel the receive clock selection RXC_SRCn should be set to “00” to pull RxCLKn pin low.

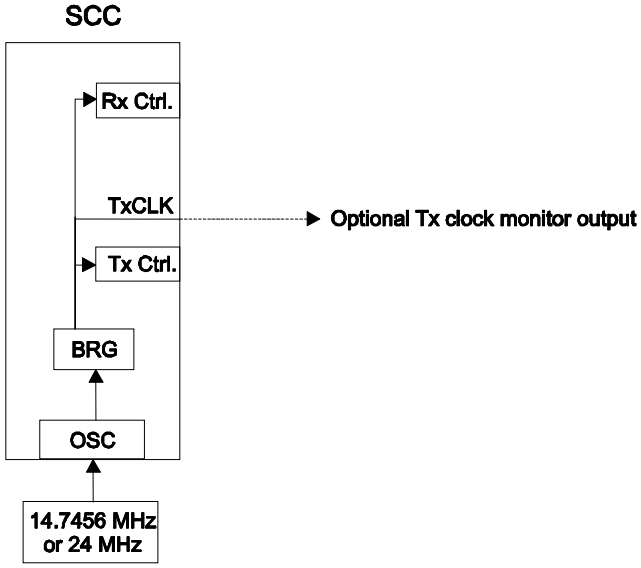

Figure 5-7 : Clock Mode 7b

5.1.7 Clock Mode 8a/b

Similar to CM3b, except that BRG is driven by the 14.7456 MHz (**CM8a**) or 24 MHz (**CM8b**) on board oscillator signal, supplied via RxCLK pin. Transmit clock signal can be monitored on TxCLK, when bit 5 'TOE' in register CCR0 is set and bit DCE / DTE# in CPLD SFR A register is set.

These modes allow supplying 24 MHz to one channel BRG while the global OSC input is supplied with 14.7456 MHz or vice versa.

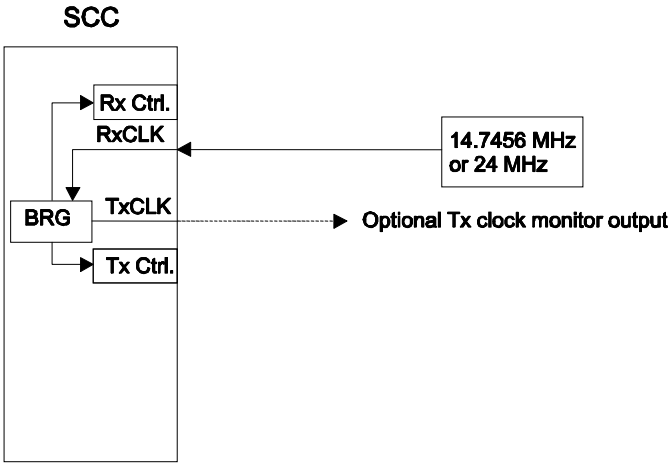

Figure 5-8 : Clock Mode 8a/b

5.1.8 Clock Mode 9

This Clock Mode is similar to CM4 but with some special signal routing. Receive clock is directly supplied from external, transmit clock is connected to the 10 MHz on board oscillator, when CM9_ENn (bit 5 in SFR B) is set. Setting this bit also changes the routing of the TxC_OUT source. This signal normally is provided at RTS pin of the DSCC4 when it is set to Clock Mode 4 (see description above). In CM9, the TxC_OUT signal is routed to the TxCn pin of the transceiver and TxCn is always output (DCE_DTEn is insignificant in CM9). CTS and CD inputs are low active clock gating signals. If receive and transmit clock should never be gated, these pins can be set permanently high by setting the bits CTS_SRCn, CTS_VALn and CD_SRCn in SFR B to '1'.

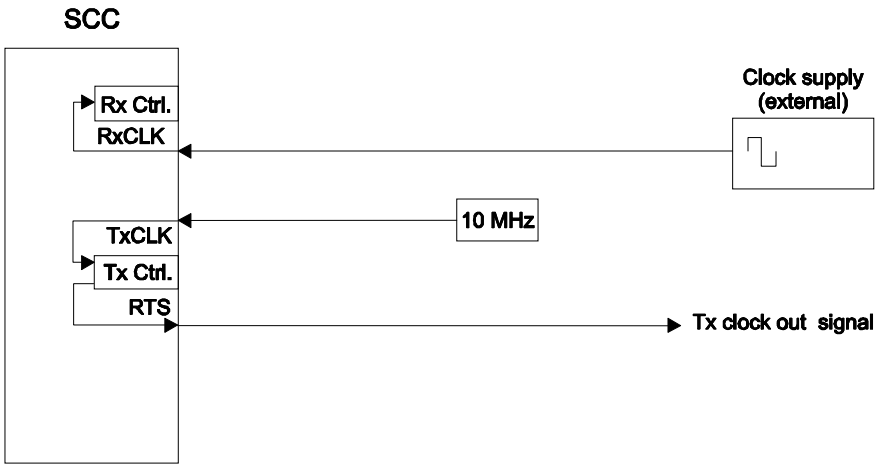

Figure 5-9 : Clock Mode 9

5.2 Baud Rate Generation

Each of the four channels has its own Baud Rate Generator (BRG). They are controlled by registers BRR (0x012C, 0x01AC, 0x022C, 0x02AC).

The Baud Rate Frequency is: $f_{BRG} = f_{in} / k$
with the divisor: $k = (N + 1) \times 2^{M}$

N (BRR[5:0]) = 0..63

M (BRR[11:8]) = 0..14, not 0..15 (see errata sheet)

When asynchronous mode is selected (register CCR0, bit BCR = '1'), k is multiplied by 16.

5.3 Configuration Hints

Local Bus Interface (for CPLD access):

LBI Clock Division should be set to CLK/2: LCD[1:0]='01', GMODE[20:19]

The LBI is selected by: PERCFG[2:0]='000' (reset value), GMODE[18:16]

→ GMODE (offset address 0x0008) typically has the value 0x00080001

LBI access has to be activated after reset: Set EBCRES#='1', LCONF[22]

LBI Bus Type is 8 bit, de-multiplexed: BTYP[1:0]='00' (reset value), LCONF[7:6]

DSCC4 is always LBI Master: ABM='1', LCONF[4]

LBI wait states can be set to 0: MCTC[3:0]='1111', LCONF[3:0]

→ LCONF (offset address 0x0300) typically has the value 0x0040001F.

6 Pin Assignment – P14 I/O Connector

Pin	Signal	Port	Pin	Signal	Port
1	CDA/-	0	33	CDA/-	2
2	CDB/+		34	CDB/+	
3	RXDA/-		35	RXDA/-	
4	RTSA/-		36	RTSA/-	
5	TXDA/-		37	TXDA/-	
6	CTSA/-		38	CTSA/-	
7	RTSB/+		39	RTSB/+	
8	CTSB/+		40	CTSB/+	
9	GND		41	GND	
10	TXDB/+		42	TXDB/+	
11	RXDB/+		43	RXDB/+	
12	TXCA/-		44	TXCA/-	
13	TXCB/+		45	TXCB/+	
14	GND		46	GND	
15	RXCA/-		47	RXCA/-	
16	RXCB/+		48	RXCB/+	
17	CDA/-	1	49	CDA/-	3
18	CDB/+		50	CDB/+	
19	RXDA/-		51	RXDA/-	
20	RTSA/-		52	RTSA/-	
21	TXDA/-		53	TXDA/-	
22	CTSA/-		54	CTSA/-	
23	RTSB/+		55	RTSB/+	
24	CTSB/+		56	CTSB/+	
25	GND		57	GND	
26	TXDB/+		58	TXDB/+	
27	RXDB/+		59	RXDB/+	
28	TXCA/-		60	TXCA/-	
29	TXCB/+		61	TXCB/+	
30	GND		62	GND	
31	RXCA/-		63	RXCA/-	
32	RXCB/+		64	RXCB/+	

Figure 6-1 : P14 I/O Pin Assignment

In V.28 (single-ended) mode, only the signals ending with “A” are used.