

The Embedded I/O Company



TPMC372

Conduction Cooled 4 Channel Serial Interface RS232/RS422

Version 1.1

User Manual

Issue 1.1.6

August 2014

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TPMC372-10R

Conduction cooled 4 Channel Serial RS232
(1x full modem), P14 I/O

TPMC372-11R

Conduction cooled 4 Channel Serial RS422
(1x plus RTS+/-, CTS+/-), P14 I/O

TPMC372-12R

Conduction cooled 2 Channel Serial RS232
(1x full modem), 2 Channel Serial RS422,
P14 I/O

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an 'Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0	Initial Issue	July 2004
1.1	Update to Version 1.1 Updated Power Specifications & Expanded Configuration EEPROM data	November 2004
1.2	Configuration EEPROM data & Pinout clarification	October 2005
1.3	Channel numbering clarification	August 2006
1.4	New address TEWS LLC	September 2006
1.0.5	New notation for HW Engineering Documentation Releases	April 2012
1.1.6	General Revision	August 2014

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1 Product Description

The TPMC372 is a conduction cooled single-width 32 bit PMC module and offers 4 channels of high performance serial interface.

Three different standard modules are available: The TPMC372-10R provides 4 RS232 interfaces. The TPMC372-11R provides 4 RS422 interfaces. The TPMC372-12R provides 2 RS232 and 2 RS422 interfaces.

Other configurations are available as factory build option on a per channel base.

All modules offer P14 I/O. Each RS232 channel supports RxD, TxD, RTS, CTS and GND. Each RS422 channel supports RxD+/-, TxD+/- and GND. One channel of the TPMC372-10R/-12R offers full modem support (TxD, RxD, CTS, RTS, DSR, DTR, CD, RI and GND) for RS232. One channel of the TPMC372-11R supports RxD+/-, TxD+/-, RTS+/-, CTS+/- and GND for RS422.

Each channel has 64 byte transmit and receive FIFOs to significantly reduce the overhead required to provide data to and get data from the transmitters and receivers. The FIFO trigger levels are programmable and the baud rate is individually programmable up to 921.6 kbps for RS232 channels and 5.5296 Mbps for RS422 channels. The UART offers readable FIFO levels.

All channels generate interrupts on PCI interrupt INTA. For fast interrupt source detection the UART provides a special Global Interrupt Source Register.

All serial channels use ESD protected transceivers. ESD protection is up to $\pm 15\text{KV}$.

The TPMC372 can operate with 3.3V and 5.0V PCI I/O signaling voltage.

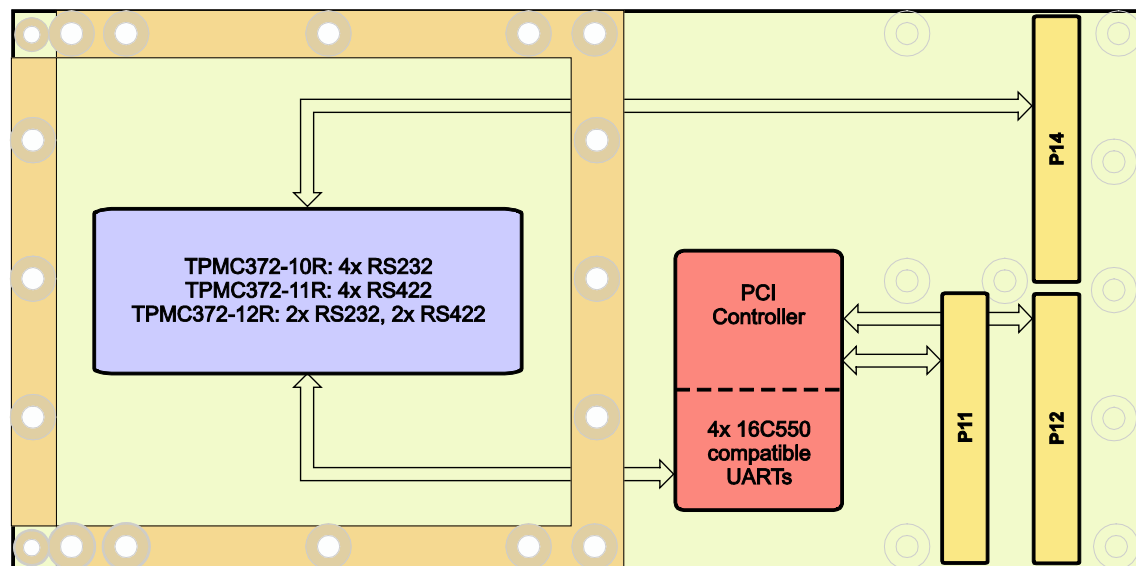


Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	Conduction Cooled PCI Mezzanine Card (PMC) Interface Single Size
Electrical Interface	PCI Rev. 2.3 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage
On Board Devices	
PCI Target Chip	XR17D154 (Exar)
Quad UART	XR17D154 (Exar)
Transceiver	RS232: MAX3225E (or equivalent) RS232 Full Modem: MAX3245E (or equivalent) RS422: MAX3087E (or equivalent)
I/O Interface	
Interface Type	Asynchronous serial interface
Number of Channels	4
Physical Interface	TPMC372-10R: 4 RS232 (1 Full Modem) TPMC372-11R: 4 RS422 (1 with RTS+/- & CTS+/-) TPMC372-12R: 2 RS232 (1 Full Modem), 2 RS422
Serial Channel I/O Signals	RS232: TxD, RxD, RTS, CTS, GND RS232 Full Modem: TxD, RxD, RTS, CTS, DTR, DSR, CD, RI, GND RS422: TxD+/-, RxD+/-, GND (TPMC372-11R: RTS+/-, CTS+/-)
Termination	RS422: 120Ω between RxD+ and RxD- of each channel (TPMC372-11R: also between CTS+, CTS-)
Programmable Baud Rates	RS232: up to 921.6 kbps RS422: up to 5.5296 Mbps
ESD Protection	RS232: ±15kV—Human Body Model ±8kV—IEC 1000-4-2, Contact Discharge ±15kV—IEC 1000-4-2, Air-Gap Discharge RS422: ±15kV—Human Body Model
I/O Connector	PMC P14 I/O (64 pin Mezzanine Connector)
Physical Data	
Power Requirements	TPMC372-10R: 30 mA typical @ +5V DC (no load) TPMC372-11R: 40 mA typical @ +5V DC (no load) TPMC372-12R: 35 mA typical @ +5V DC (no load)
Temperature Range	Operating -40°C to +85°C Storage -55°C to +125°C

MTBF	TPMC372-10R: 740 000 h TPMC372-11R: 650 000 h TPMC372-12R: 710 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G _B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	52 g

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 XR17D154 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the XR17D154 local space.

XR17D154 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	4096	32	BIG	Device Configuration Space

Table 3-1 : XR17D154 Local Space Configuration

3.2 Device Configuration Space

PCI Base Address: XR17D154 PCI Base Address 0 (Offset 0x10 in PCI Configuration Space).

The TPMC372 uses the Exar XR17D154 Quad UART to provide and control the 4 channels.

Device Configuration Space Content	PCI Address	Size (Bit)
UART 0 Register Set	PCI Base Address 0 + (0x0000 to 0x007F)	32
Device Configuration Registers	PCI Base Address 0 + (0x0080 to 0x009F)	32
UART 0 Register Set	PCI Base Address 0 + (0x0100 to 0x01FF)	32
UART 1 Register Set	PCI Base Address 0 + (0x0200 to 0x03FF)	32
UART 2 Register Set	PCI Base Address 0 + (0x0400 to 0x05FF)	32
UART 3 Register Set	PCI Base Address 0 + (0x0600 to 0x07FF)	32

Table 3-2 : Device Configuration Space

All registers can be accessed in 8, 16 or 32 bit width with exception to one special case: When reading the receive data together with its LSR register content, the host must read them in 16 or 32 bits format in order to maintain integrity of the data byte with its associated error flags.

3.2.1 UART Register Sets

The Device Configuration Space provides a register set for each of the 4 UARTs.

UART Register Set	Register Set Offset
Serial Channel 0	0x0000
Serial Channel 1	0x0200
Serial Channel 2	0x0400
Serial Channel 3	0x0600

Table 3-3 : UART Register Set Offset

Offset Address	Description	Access	Data Width
0x000 – 0x00F	UART Channel Configuration Registers First 8 registers are 16550 compatible	R/W	8, 16, 32
0x010 – 0x07F	Reserved	-	-
0x080 – 0x093	Channel 0: Device Configuration Registers All other channels: Reserved	R/W	8, 16, 32
0x094 – 0x0FF	Reserved	-	-
0x100	Read FIFO – 64 bytes of RX FIFO data	R	8, 16, 32
	Write FIFO – 64 bytes of TX FIFO data	W	8, 16, 32
0x140 – 0x17F	Reserved	-	-
0x180 – 0x1FF	Read FIFO with errors – 64 bytes of RX FIFO data + LSR	R	16, 32

Table 3-4 : UART Register Set

3.2.2 Device Configuration Registers

The Device Configuration Registers control general operating conditions and monitor the status of various functions. This includes a 16 bit general purpose counter, multipurpose input/outputs (not supported by the TPMC372), sleep mode, soft-reset and device identification and revision. They are embedded inside the UART 0 Register Set.

Address	Register	Description	Access	Reset Value
0x080	INT0 [7:0]	Channel Interrupt Indicator	R	0x00
0x081	INT1 [15:8]	Interrupt Source Details	R	0x00
0x082	INT2 [23:16]		R	0x00
0x083	INT3 [31:24]		R	0x00
0x084	TIMERCNTL	Timer Control Register	R/W	0x00
0x085	TIMER	Reserved	-	0x00
0x086	TIMERLSB	Programmable Timer Value	R/W	0x00
0x087	TIMERMSB		R/W	0x00
0x088	8XMODE	Sampling Rate Select	R/W	0x00
0x089	REGA	Reserved	-	0x00
0x08A	RESET	UART Reset	W	0x00
0x08B	SLEEP	UART Sleep Mode Enable	R/W	0x00
0x08C	DREV	Device Revision	R	0x01
0x08D	DVID	Device Identification	R	0x28
0x08E	REGB	Simultaneous UART Write & EEPROM Interface	W	0x00
0x08F	MPIOINT	MPIO Interrupt Mask	R/W	0x00
0x090	MPIOLVL	MPIO Level Control	R/W	0x00
0x091	MPIO3T	MPIO Output Pin Tri-state Control	R/W	0x00
0x092	MPIOINV	MPIO Input Polarity Select	R/W	0x00
0x093	MPIOSEL	MPIO Input/Output Select	R/W	0xFF

Table 3-5 : Device Configuration Registers

For a detailed description of the Device Configuration Registers please refer to the XR17D154 data sheet which is available on the Exar website (www.exar.com).

3.2.3 UART Channel Configuration Registers

Each UART channel has its own set of internal UART configuration registers for its own operation control and status reporting. The following table provides the register offsets within a register set, access types and access control:

Register Offset	Comment	Register	Access	Reset Value
16550 Compatible				
0x00	LCR[7] = 0	RHR – Receive Holding Register	R	0xXX
		THR – Transmit Holding Register	W	
	LCR[7] = 1	DLL – Baud Rate Generator Divisor Latch Low	R/W	0xXX
0x01	LCR[7] = 0	IER – Interrupt Enable Register	R/W	0x00
		LCR[7] = 1	DLM – Baud Rate Generator Divisor Latch High	R/W
0x02		ISR – Interrupt Status Register	R	0x01
		FCR – FIFO Control Register	W	0x00
0x03		LCR – Line Control Register	R/W	0x00
0x04		MCR – Modem Control Register	R/W	0x00
0x05		LSR – Line Status Register	R	0x60
		Reserved	W	
0x06		MSR – Modem Status Register	R	0xX0
		– Auto RS485 Delay (not supported by the TPMC372)	W	
0x07	User Data	SPR – Scratch Pad Register	R/W	0xFF
Enhanced Registers				
0x08		FCTR – Feature Control Register	R/W	0x00
0x09		EFR – Enhanced Function Register	R/W	0x00
0x0A		TXCNT – Transmit FIFO Level Counter	R	0x00
		TXTRG – Transmit FIFO Trigger Level	W	
0x0B		RXCNT – Receiver FIFO Level Counter	R	0x00
		RXTRG – Receiver FIFO Trigger Level	W	
0x0C		Xchar – Xon, Xoff Received Flags	R	0x00
		Xoff-1 – Xoff Character 1	W	
0x0D		Reserved	R	0x00
		Xoff-2 – Xoff Character 2	W	
0x0E		Reserved	R	0x00
		Xon-1 – Xon Character 1	W	
0x0F		Reserved	R	0x00
		Xon-2 – Xon Character 2	W	

Table 3-6 : UART Channel Configuration Registers

The address for a UART Channel Configuration Register *x* in a UART Register Set for channel *y* is:

PCI Base Address 0 (PCI Base Address for the UART Register Space)
+ UART Register Set Offset for *channel y*
+ Register Offset for *register x*

Addressing example:

The address for the LCR register of UART channel 5 is:

PCI Base Address (PCI Base Address for the Device Configuration Space)

+ 0x0A00 (Offset of the UART register set for serial channel 5)

+ 0x0003 (Offset of the LCR register within a UART register set)

For a detailed description of the serial channel registers please refer to the XR17D154 data sheet which is available on the Exar website (www.exar.com).

4 XR17D154 Target Chip

4.1 PCI Configuration Registers (PCR)

PCI CFG Register Address	Write '0' to all unused (Reserved) bits							PCI writeable	Initial Values (Hex Values)	
	31	24	23	16	15	8	7			0
0x00	Device ID				Vendor ID				N	0174 1498
0x04	Status				Command				Y	0080 0000
0x08	Class Code					Revision ID			N	070002 ??
0x0C	BIST	Header Type		PCI Latency Timer		Cache Line Size		N	00 00 00 00	
0x10	Memory Base Address Register (BAR)							Y	FFFFFF00	
0x14	I/O Base Address Register (Unimplemented)							N	00000000	
0x18	Base Address Register 0 (Unimplemented)							N	00000000	
0x1C	Base Address Register 1 (Unimplemented)							N	00000000	
0x20	Base Address Register 2 (Unimplemented)							N	00000000	
0x24	Base Address Register 3 (Unimplemented)							N	00000000	
0x28	Reserved							N	00000000	
0x2C	Subsystem ID			Subsystem Vendor ID				N	s.b. 1498	
0x30	Expansion ROM Base Address (Unimplemented)							N	00000000	
0x34	Reserved							N	00000000	
0x38	Reserved							N	00000000	
0x3C	Max_Lat	Min_Gnt	Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00		

Table 4-1 : PCI Header

Device ID: 0x0174 TPMC372
 Vendor ID: 0x1498 TEWS TECHNOLOGIES
 Revision ID: XR17D154 silicon revision
 Subsystem ID: 0x000A -10R
 0x000B -11R
 0x000C -12R
 Subsystem Vendor ID: 0x1498 TEWS TECHNOLOGIES

4.2 Configuration EEPROM

After power-on or PCI reset, the XR17D154 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Vendor ID
- Vendor Device ID
- SubSystem Vendor ID
- SubSystem Device ID

See the XR17D154 Manual for more information.

Address	Configuration Register	Configuration Register Offset	Value
0x00	Vendor ID	0x02	0x1498
0x01	Device ID	0x00	0x0174
0x02	Subsystem Vendor ID	0x2E	0x1498
0x03	Subsystem ID	0x2C	s.b.

Table 4-2 : Configuration EEPROM TPMC372-xx

Subsystem ID Value (Offset 0x0C):
 TPMC372-10R 0x000A
 TPMC372-11R 0x000B
 TPMC372-12R 0x000C

The words following the configuration data contain:

- The module version and revision
- The UART clock frequency in Hz
- The physical interface attached to the serial channels
- The maximal baud rate of the transceivers in bps
- The supported control signals of the serial channels

For the physical interfaces and the control signals applies: Bit 3 represents UART channel 3 and bit 0 represents UART channel 0. The appropriate bit is set to '1' for each UART channel attached to the physical interface represented by the word. Bit 15 to bit 4 are always '0'.

Address	Configuration Register	TPMC372-10R	TPMC372-11R	TPMC372-12R
0x04	Module Version	0x0101	0x0101	0x0101
0x05	Module Revision	0x0000	0x0000	0x0000
0x06	EEPROM Revision	0x0002	0x0002	0x0002
0x07	Oscillator Frequency (high)	0x02A3	0x02A3	0x02A3
0x08	Oscillator Frequency (low)	0x0000	0x0000	0x0000
0x09-0x0F	Reserved	-	-	-
0x10	RS232 Channels	0x000F	0x0000	0x0003
0x11	RS422 Channels	0x0000	0x000F	0x000C
0x12	TTL Channels	0x0000	0x0000	0x0000
0x13	RS485 Full Duplex Channels	0x0000	0x0000	0x0000
0x14	RS485 Half Duplex Channels	0x0000	0x0000	0x0000
0x15-0x1E	Reserved	-	-	-
0x1F	Programmable Interfaces	0x0000	0x0000	0x0000
0x20	Max Data Rate RS232 (high)	0x000F	0x000F	0x000F
0x21	Max Data Rate RS232 (low)	0x4240	0x4240	0x4240
0x22	Max Data Rate RS422 (high)	0x0098	0x0098	0x0098
0x23	Max Data Rate RS422 (low)	0x9680	0x9680	0x9680
0x24	Max Data Rate TTL (high)	0x0098	0x0098	0x0098
0x25	Max Data Rate TTL (low)	0x9680	0x9680	0x9680
0x26	Max Data Rate RS485 Full Duplex (high)	0x0000	0x0000	0x0000
0x27	Max Data Rate RS485 Full Duplex (low)	0x0000	0x0000	0x0000
0x28	Max Data Rate RS485 Half Duplex (high)	0x0000	0x0000	0x0000
0x29	Max Data Rate RS485 Half Duplex (low)	0x0000	0x0000	0x0000
0x2A-0x2F	Reserved	-	-	-
0x30	RxD & TxD	0x000F	0x000F	0x000F
0x31	RTS & CTS	0x000F	0x0001	0x0003
0x32	Full modem	0x0001	0x0000	0x0001
0x33-0x37	Reserved	-	-	-
0x38	Enhanced RTS & CTS (Front or Back I/O only)	0x0000	0x0000	0x0000
0x39	Enhanced Full modem (Front or Back I/O only)	0x0000	0x0000	0x0000
0x3A	Channels with enhanced RTS & CTS Support for RS232 only	0x0000	0x0000	0x0000
0x3B-0x3F	Reserved	-	-	-

Table 4-3 : Physical Configuration EEPROM Data

5 Configuration Hints

The following chart shows the UART interface mapping of the different variants of the TPMC372.

	TPMC372-10R		TPMC372-11R		TPMC372-12R	
	RS232	RS422	RS232	RS422	RS232	RS422
UART0	X			X	X	
UART1	X			X	X	
UART2	X			X		X
UART3	X			X		X

Table 5-1 : UART interface mapping

Other configurations are available as factory build option on a per channel base.

RS422 channels provide on board 120Ω termination resistors. Do not apply additional external termination resistors here.

6 Programming Hints

6.1 UART Baud Rate Programming

Each of the 4 UART channels of the TPMC372 provides a programmable Baud Rate Generator. The clock of the XR17D154 UART can be divided by any divisor from 1 to $2^{16} - 1$. The divisor can be programmed by the UART channel DLM (Divisor MSB) and DLL (Divisor LSB) registers. After a reset bit 7 of the UART channels MCR register defaults to '0' and the divisor value is 0xFFFF.

The basic formula of baud rate programming is:

$$\text{Baud Rate} = \frac{44.2368\text{MHz}}{16 \cdot \text{Divisor} \cdot (1 + 3 \cdot \text{MCR}[7])}$$

Examples for standard baud rates are given in following chart:

Baud Rate MCR[7] = 0	Baud Rate MCR[7] = 1	Divisor	DLM Value	DLL Value
400	100	0x1B00	0x1B	0x00
600	150	0x1200	0x12	0x00
1200	300	0x0900	0x09	0x00
2400	600	0x0480	0x04	0x80
4800	1200	0x0240	0x02	0x40
9600	2400	0x0120	0x01	0x20
19.2k	4800	0x0090	0x00	0x90
38.4k	9600	0x0048	0x00	0x48
57.6k	14.4k	0x0030	0x00	0x30
115.2k	28.8k	0x0018	0x00	0x18
230.4k	57.6k	0x000C	0x00	0x0C
460.8k	115.2k	0x0006	0x00	0x06
921.6k	230.4k	0x0003	0x00	0x03
1382.4k	345.6k	0x0002	0x00	0x02
2764.8k	691.2k	0x0001	0x00	0x01

Table 6-1 : UART Baud Rate Programming

To calculate a divisor value for a given baud rate, use following formula:

$$\text{Divisor} = \frac{44.2368\text{MHz}}{16 \cdot \text{Baud Rate} \cdot (1 + 3 \cdot \text{MCR}[7])}$$

The sampling rate for a UART channel can be set to 8x (normal operation is 16x) in the 8XMODE register. Transmit and receive data rates will double by selecting 8x sample rate.

The maximum achievable baud rate is 5.5296 Mbps (Divisor = 0x0001 & 8x sampling rate).

These steps should be used to modify the DLM, DLL registers of an UART channel:

1. Write 0x80 to the LCR register of the UART channel (enable access to the DLM, DLL registers).
2. Program the DLM, DLL registers of the UART channel.
3. Write normal operation byte value to the LCR register of the UART channel.

These steps should be used to modify MCR register bit 7 of an UART channel (set baud rate generator prescaler):

1. Set UART channel EFR register bit 4 to '1' (enable modification of MCR register bits 5-7).
2. Modify UART channel MCR register bit 7.
3. Set UART channel EFR register bit 4 to '0' (latch modified MCR register setting).

Note that the maximum baud rate for RS232 channel is 921.6 kps. Thus the minimum divisor value for RS232 channels is 0x0003 with MCR[7] = 0.

6.2 RS422 Flow Control

Only UART channel 0 allows using RS422 with RTS/CTS flow control. On channels 1 – 3 the CTS# input is hardwired to '1', so that no RTS/CTS flow control is possible.

7 Pin Assignment – I/O Connector

RS422 channels provide on board 120Ω termination resistors. Do not apply additional external termination resistors here.

7.1 TPMC372-10R Back I/O PMC Connector (P14)

Pin	Signal	Signal Level
1	GND	-
2	TxD0	RS232
3	RxD0	RS232
4	RTS0	RS232
5	CTS0	RS232
6	GND	-
7	-	-
8	-	-
9	-	-
10	-	-
11	GND	-
12	TxD1	RS232
13	RxD1	RS232
14	RTS1	RS232
15	CTS1	RS232
16	GND	-
17	-	-
18	-	-
19	-	-
20	-	-
21	GND	-
22	TxD2	RS232
23	RxD2	RS232
24	RTS2	RS232
25	CTS2	RS232
26	GND	-
27	-	-
28	-	-
29	-	-
30	-	-
31	GND	-
32	TxD3	RS232

Pin	Signal	Signal Level
33	RxD3	RS232
34	RTS3	RS232
35	CTS3	RS232
36	GND	-
37	-	-
38	-	-
39	-	-
40	-	-
41	GND	-
42	+5V Termination Supply (unfused!)	
43	CD0	RS232
44	DTR0	RS232
45	RI0	RS232
46	DSR0	RS232
47	-	-
48	-	-
49	-	-
50	-	-
51	-	-
52	-	-
53	-	-
54	-	-
55	-	-
56	-	-
57	-	-
58	-	-
59	-	-
60	-	-
61	-	-
62	-	-
63	-	-
64	-	-

Table 7-1 : TPMC372-10R Pin Assignment Back I/O PMC Connector (P14)

7.2 TPMC372-11R Back I/O PMC Connector (P14)

Pin	Signal	Signal Level	Pin	Signal	Signal Level
1	GND	-	33	TxD3+	RS422
2	TxD0-	RS422	34	RxD3-	RS422
3	TxD0+	RS422	35	RxD3+	RS422
4	RxD0-	RS422	36	GND	-
5	RxD0+	RS422	37	-	-
6	GND	-	38	-	-
7	-	-	39	-	-
8	-	-	40	-	-
9	-	-	41	GND	-
10	-	-	42	+5V Termination Supply (unfused!)	
11	GND	-	43	RTS0-	RS422
12	TxD1-	RS422	44	RTS0+	RS422
13	TxD1+	RS422	45	CTS0-	RS422
14	RxD1-	RS422	46	CTS0+	RS422
15	RxD1+	RS422	47	-	-
16	GND	-	48	-	-
17	-	-	49	-	-
18	-	-	50	-	-
19	-	-	51	-	-
20	-	-	52	-	-
21	GND	-	53	-	-
22	TxD2-	RS422	54	-	-
23	TxD2+	RS422	55	-	-
24	RxD2-	RS422	56	-	-
25	RxD2+	RS422	57	-	-
26	GND	-	58	-	-
27	-	-	59	-	-
28	-	-	60	-	-
29	-	-	61	-	-
30	-	-	62	-	-
31	GND	-	63	-	-
32	TxD3-	RS422	64	-	-

Table 7-2 : TPMC372-11R Pin Assignment Back I/O PMC Connector (P14)

7.3 TPMC372-12R Back I/O PMC Connector (P14)

Pin	Signal	Signal Level	Pin	Signal	Signal Level
1	GND	-	33	TxD3+	RS422
2	TxD0	RS232	34	RxD3-	RS422
3	RxD0	RS232	35	RxD3+	RS422
4	RTS0	RS232	36	GND	-
5	CTS0	RS232	37	-	-
6	GND	-	38	-	-
7	-	-	39	-	-
8	-	-	40	-	-
9	-	-	41	GND	-
10	-	-	42	+5V Termination Supply (unfused!)	
11	GND	-	43	CD0	RS232
12	TxD1	RS232	44	DTR0	RS232
13	RxD1	RS232	45	RI0	RS232
14	RTS1	RS232	46	DSR0	RS232
15	CTS1	RS232	47	-	-
16	GND	-	48	-	-
17	-	-	49	-	-
18	-	-	50	-	-
19	-	-	51	-	-
20	-	-	52	-	-
21	GND	-	53	-	-
22	TxD2-	RS422	54	-	-
23	TxD2+	RS422	55	-	-
24	RxD2-	RS422	56	-	-
25	RxD2+	RS422	57	-	-
26	GND	-	58	-	-
27	-	-	59	-	-
28	-	-	60	-	-
29	-	-	61	-	-
30	-	-	62	-	-
31	GND	-	63	-	-
32	TxD3-	RS422	64	-	-

Table 7-3 : TPMC372-12R Pin Assignment Back I/O PMC Connector (P14)