

The Embedded I/O Company



TPMC385

**Conduction Cooled, 4x 10/100/1000 Mbit/s Ethernet
Adapter**

Version 1.0

User Manual

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TPMC385-10R

Conduction Cooled, Four Channel 10/100/1000 Mbit/s Ethernet interface back I/O, extended temperature range (RoHS compliant)

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an 'Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0.0	Initial issue	November 2010
1.0.1	Note on Ethernet Device Numbering added to PCI Device Topology chapter	May 2011
1.0.2	PCI Device Topology chapter revised	March 2012
1.0.3	Hardware revision update to Rev.B	August 2012
1.0.4	Hardware revision update to Rev.C	October 2014

Table of Contents

1	PRODUCT DESCRIPTION	6
2	TECHNICAL SPECIFICATION	7
3	PCI DEVICE TOPOLOGY ON TPMC385.....	8
4	GIGABIT ETHERNET CONTROLLER.....	9
4.1	Intel 82574IT PCI Header	9
4.2	LEDs	10
5	PIN ASSIGNMENT – I/O CONNECTOR P14.....	11

List of Figures

FIGURE 1-1 : BLOCK DIAGRAM.....	6
FIGURE 3-1 : PCI DEVICE TOPOLOGY	8
FIGURE 5-1 : LEDS AND MARKINGS (TPMC385-10R BOTTOM VIEW)	10

List of Tables

TABLE 2-1 : TECHNICAL SPECIFICATION.....	7
TABLE 4-1 : INTEL 82574IT PCI HEADER	9
TABLE 5-1 : LED STATUS.....	10
TABLE 6-1 : P14 PIN ASSIGNMENT.....	11

1 Product Description

The TPMC385 is a Conduction Cooled PCI Mezzanine Card (CCPMC) compatible module providing a four channel Ethernet 10BASE-T / 100BASE-TX / 1000BASE-T interface.

A transparent 64 bit, up to 133 MHz PCI-X/PCI to PCIe Bridge and a PCIe Switch provide access to the Intel 82574IT Gigabit Ethernet controllers. Each Ethernet interface supports 10, 100 and 1000 Mbit/s transmission rates for full duplex operation, 10 and 100 Mbit/s transmissions for half duplex operation, and is equipped with a 32 Kbit Serial EEPROM.

The four Ethernet interfaces of the TPMC385 are capable of performing an auto negotiation algorithm which allows both link-partners to find out the best link-parameters by themselves. The TPMC385 is widely user configurable via configuration and status register access over the PCI bus.

The TPMC385-10R routes all four Ethernet ports to the back I/O P14 connector.

All ports are galvanically isolated from the Ethernet controllers and LEDs on the board indicate the different network activities.

The module meets the requirements to operate in extended temperature range from -40° to +85°C.

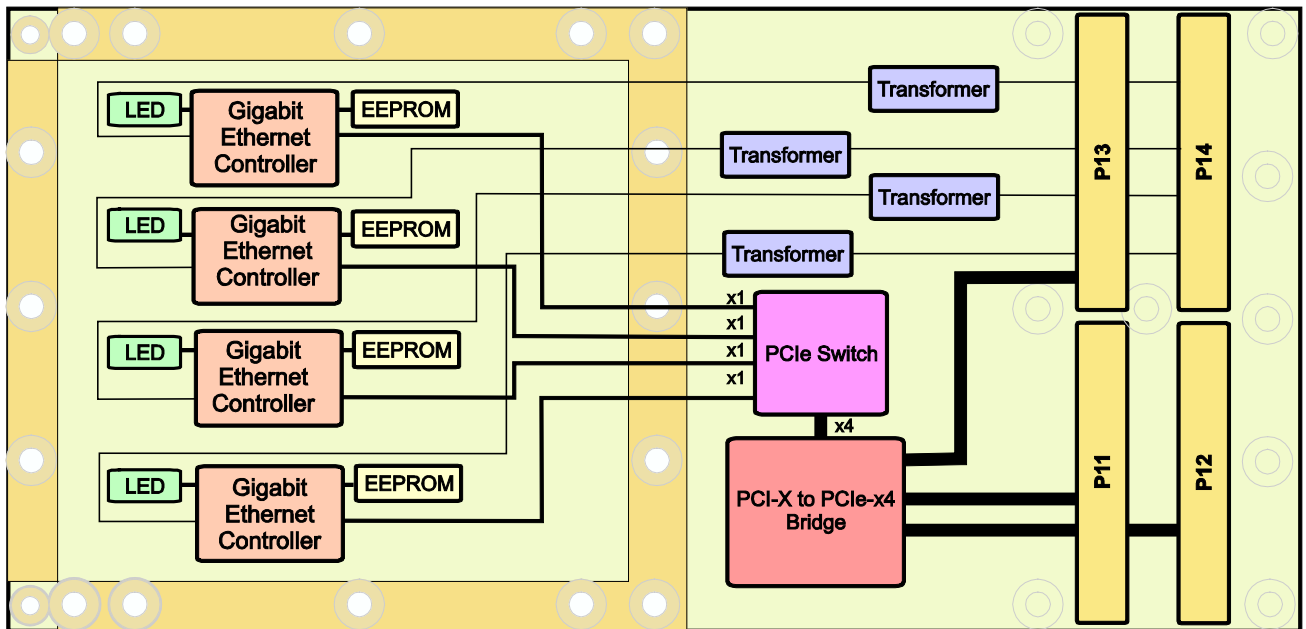


Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	Conduction Cooled PCI Mezzanine Card (CCPMC) Interface confirming to IEEE P1386/P1386.1 and ANSI/VITA 20-2001 (R2005) Single Size
Electrical Interface	PCI Rev. 3.0 compliant and PCI-X Rev. 2.0a compliant 66 MHz / 64 bit PCI and 133 MHz / 64 bit PCI-X 3.3V and 5V PCI Signaling Voltage
On Board Devices	
PCI/PCI-X to PCIe Bridge	PI7C9X130 (Pericom)
PCIe Switch	89HPES8T5A (IDT)
Gigabit Ethernet Controller	For each interface: 82574IT (Intel)
Ethernet Interface	
Number of Interfaces	4
FIFO	For each interface: Configurable receive and transmit data FIFO, programmable in 1 KB increments
Interrupts	Using PCI INTA, INTB, INTC and INTD
I/O Connector	PMC P14 back I/O (64-pin Mezzanine Connector)
Physical Data	
Power Requirements	1500mA typical @ +3.3V DC (no link) app. additional 70mA per 100Mbit/s link app. additional 300mA per 1Gbit/s link
Temperature Range	Operating -40°C to +85°C Storage -40°C to +85°C
MTBF	502000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G _B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	62 g

Table 2-1 : Technical Specification

3 PCI Device Topology on TPMC385

The TPMC385 uses four Gigabit Ethernet Controllers (Intel 82574IT) each communicating via a PCIe Rev. 1.1 compliant x1 Interface. To be able to access the Ethernet controllers they are connected to the x1 Downstream Ports of a PCIe Switch (IDT 89HPES8T5A). The x4 Upstream Port of the Switch is connected to a PCI/PCI-X to PCIe Bridge (Pericom PI7C9X130) which communicates with the host system.

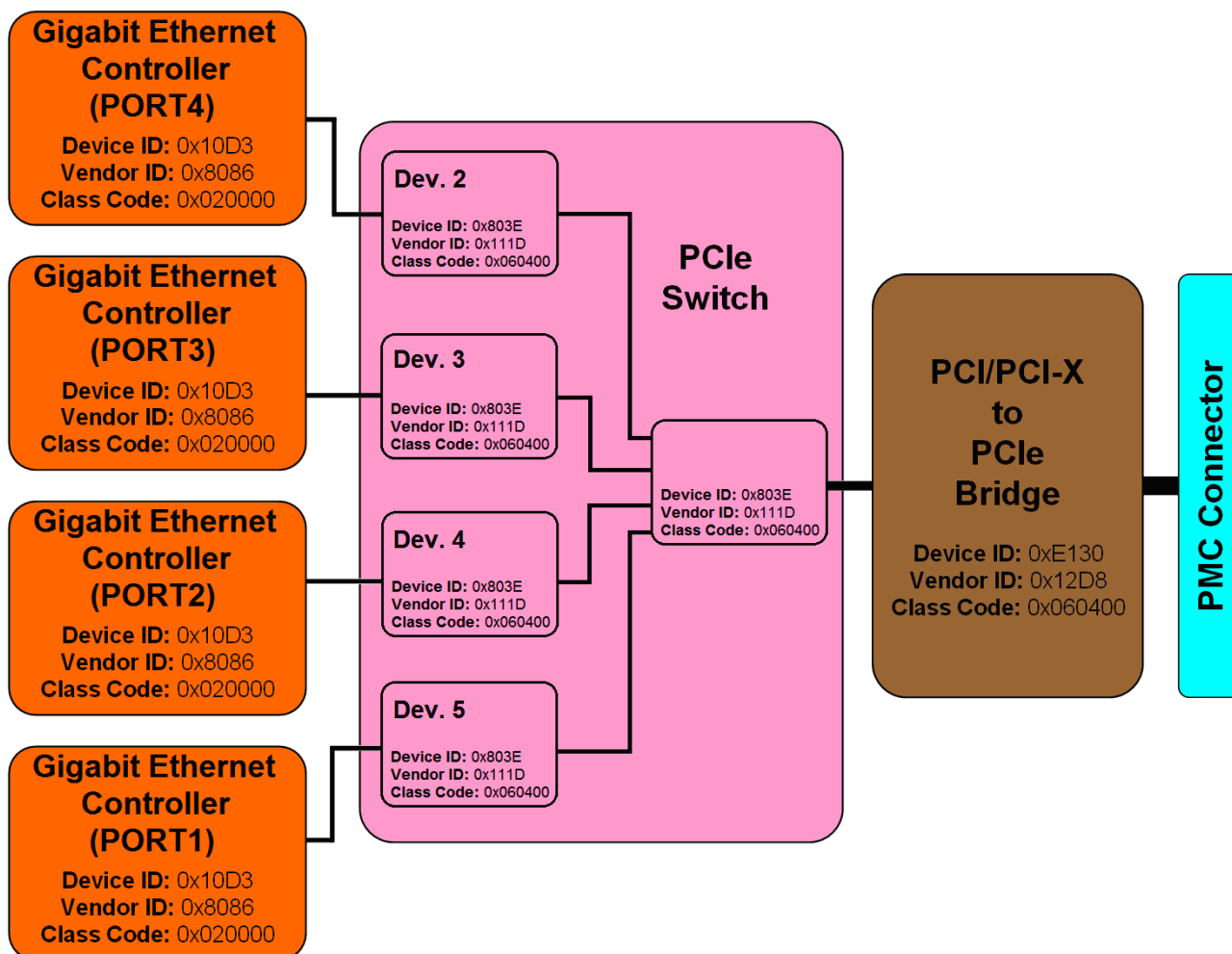


Figure 3-1 : PCI Device Topology

NOTE: Operating systems typically assign the lowest available Ethernet device number to PORT4 (ETHERNET 4 interface on I/O Connector P14), thus initializing the four ports in descending order.

4 Gigabit Ethernet Controller

4.1 Intel 82574IT PCI Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits							Initial Values (Hex Values)
	31	24	23	16	15	8	7	
0x00	Device ID			Vendor ID				10D3 8086
0x04	Status Register			Command Register				0010 0000
0x08	Class Code				Revision ID			020000 00
0x0C	BIST	Header Type		Latency Timer		Cache Line Size		00 00 00 10
0x10	Base Address 0 (Memory BAR)							FFFE0000 (128 KByte)
0x14	Base Address 1 (Flash BAR)							00000000
0x18	Base Address 2 (IO BAR)							FFFFFFE1 (32 Byte)
0x1C	Base Address 3 (MSI-X BAR)							FFFC000 (16 KByte)
0x20	Base Address 4							00000000
0x24	Base Address 5							00000000
0x28	CardBus CIS Pointer							00000000
0x2C	Subsystem ID			Subsystem Vendor ID				0000 8086
0x30	Expansion ROM Base Address							00000000
0x34	Reserved				Cap_Ptr			000000 C8
0x38	Reserved							00000000
0x3C	Max_Latency	Min_Grant	Interrupt Pin		Interrupt Line		00 00 01 00	

Table 4-1 : Intel 82574IT PCI Header

4.2 LEDs

The TPMC385 provides four Status LEDs for quick visual inspection and debugging.

Due to the fact that PMCs are mounted headfirst on the carrier card, the LED indicators are visible on the back side of the TPMC385. A marking is placed close to each LED, to indicate the Ethernet Port the LED corresponds to.

Each Ethernet Port has one LED indicator. See figures below for more details:

LED Status	Description
OFF	No cable is connected or no link is established
ON	A link is established at the corresponding Ethernet Port
BLINKING	Indicates activity: The Ethernet Port transmits or receives data

Table 4-2 : LED Status

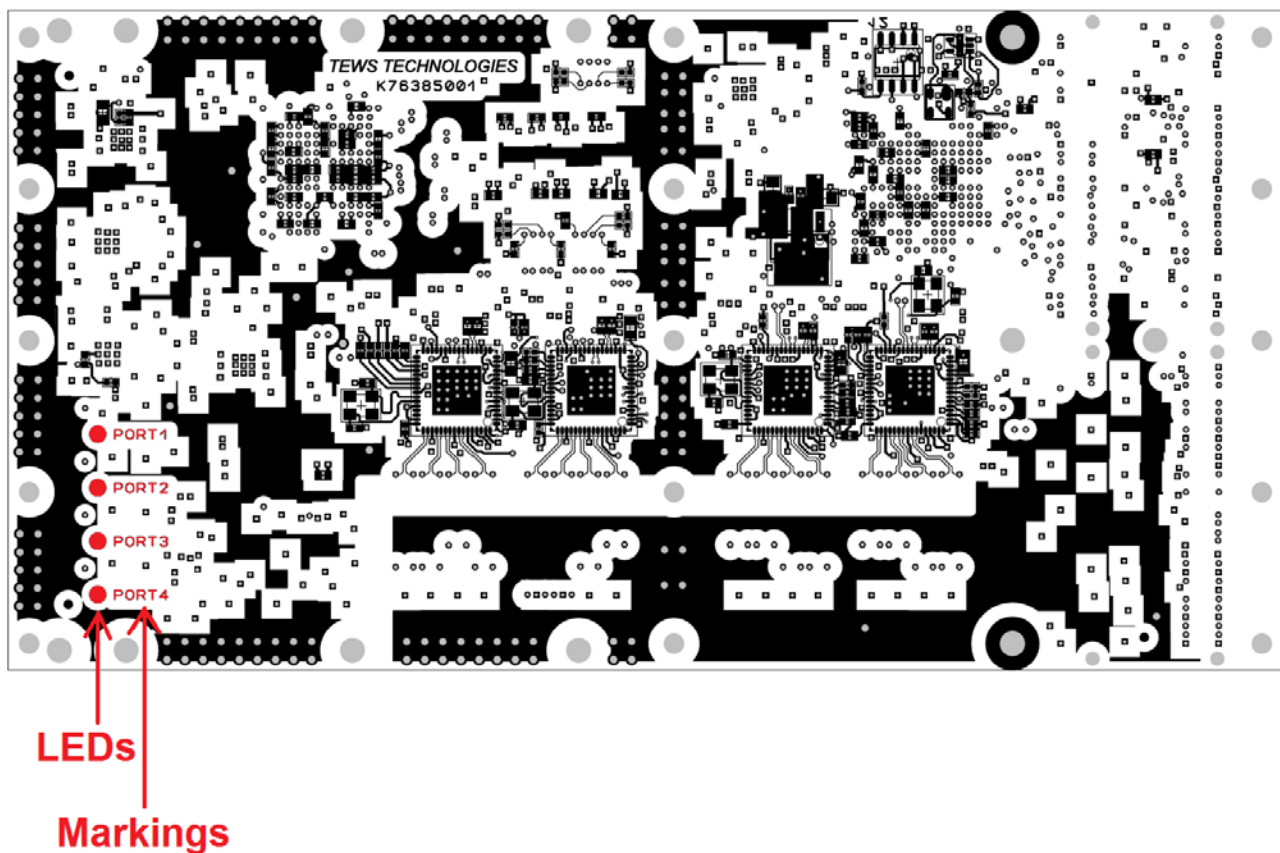


Figure 4-1 : LEDs and markings (TPMC385-10R bottom view)

5 Pin Assignment – I/O Connector P14

The TPMC385 routes the Ethernet lines to the P14 mezzanine connector. In most cases, the P14 is connected to the PMC Carrier that routes the Ethernet lines from P14 to the Backplane. A Transition Module is connected to the backside of the Backplane and routes the Ethernet lines to a RJ45 PIM module. Care must be taken to avoid impedance mismatches and high resistive routing in the Ethernet lines, because this leads to signal distortion and low voltage amplitude.

Pin	Signal	Pin	Signal
1	Termination Plane	2	Termination Plane
3	ETHERNET 4 TX3/RX3+	4	ETHERNET 3 TX3/RX3+
5	ETHERNET 4 TX3/RX3-	6	ETHERNET 3 TX3/RX3-
7	Termination Plane	8	Termination Plane
9	ETHERNET 4 TX2/RX2+	10	ETHERNET 3 TX2/RX2+
11	ETHERNET 4 TX2/RX2-	12	ETHERNET 3 TX2/RX2-
13	Termination Plane	14	Termination Plane
15	ETHERNET 4 TX0/RX0+	16	ETHERNET 4 TX1/RX1+
17	Termination Plane	18	Termination Plane
19	ETHERNET 4 TX0/RX0-	20	ETHERNET 4 TX1/RX1-
21	Termination Plane	22	Termination Plane
23	Termination Plane	24	Termination Plane
25	ETHERNET 3 TX0/RX0+	26	ETHERNET 3 TX1/RX1+
27	Termination Plane	28	Termination Plane
29	ETHERNET 3 TX0/RX0-	30	ETHERNET 3 TX1/RX1-
31	Termination Plane	32	Termination Plane
33	Termination Plane	34	Termination Plane
35	ETHERNET 2 TX0/RX0+	36	ETHERNET 2 TX1/RX1+
37	Termination Plane	38	Termination Plane
39	ETHERNET 2 TX0/RX0-	40	ETHERNET 2 TX1/RX1-
41	Termination Plane	42	Termination Plane
43	Termination Plane	44	Termination Plane
45	ETHERNET 1 TX0/RX0+	46	ETHERNET 1 TX1/RX1+
47	Termination Plane	48	Termination Plane
49	ETHERNET 1 TX0/RX0-	50	ETHERNET 1 TX1/RX1-
51	Termination Plane	52	Termination Plane
53	ETHERNET 2 TX2/RX2+	54	ETHERNET 1 TX2/RX2+
55	ETHERNET 2 TX2/RX2-	56	ETHERNET 1 TX2/RX2-
57	Termination Plane	58	Termination Plane
59	ETHERNET 2 TX3/RX3+	60	ETHERNET 1 TX3/RX3+
61	ETHERNET 2 TX3/RX3-	62	ETHERNET 1 TX3/RX3-
63	Termination Plane	64	Termination Plane

Table 5-1 : P14 pin assignment