The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC461

8 Channel Serial Interface RS232/RS422

Version 2.0

User Manual

Issue 2.0.0

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TEWS Technologies GmbH
Eggerstedter Weg 14, 25421 Pinneberg, Germany
Phone: +49 (0) 4101 4058 0
info@tews.com www.tews.com

TPMC461-10R

8 Channel Serial RS232 (2x full modem), front panel and P14 I/O

TPMC461-11R

8 Channel Serial RS422 (2x plus RTS+/- & CTS+/-), front panel and P14 I/O

TPMC461-12R

4 Channel Serial RS232 (2x full modem), 4 Channel RS422, front panel and P14 I/O

Document History

Issue	Description	Date
1.0	First Issue	October 2004
1.1	Expanded Configuration EEPROM Data	November 2004
1.2	Configuration EEPROM Data & Pinout Clarification	September 2005
1.3	Channel Numbering Clarification	August 2006
1.4	New Address TEWS LLC	September 2006
1.0.5	New Notation for HW Engineering Documentation Releases	February 2009
1.0.6	General Revision	August 2014
2.0.0	Card: PCI UART ASIC Replacement (now FPGA based PCI UART), new PCB, different I/O transceivers	January 2026

Table of Contents

List of Figures

List of Tables

1 Product Description

The TPMC461 is a standard single-width 32 bit PMC module and offers 8 UART based serial interface channels.

Three different standard order options are available: The TPMC461-10R provides 8 RS232 interfaces. The TPMC461-11R provides 8 RS422 interfaces. The TPMC461-12R provides 4 RS232 and 4 RS422 interfaces. Other configurations are available as factory build option on a per channel base.

All modules offer front panel I/O with a HD50 SCSI-2 type connector and P14 rear I/O.

Each RS232 channel supports TXD, RXD, RTS, CTS and GND. Each RS422 channel supports TXD+/-, RXD+/- and GND. Two channels of the TPMC461-10R/-12R offer full modem support (TXD, RXD, RTS, CTS, DTR, DSR, CD, RI and GND) for RS232. Two channels of the TPMC461-11R support TXD+/-, RXD+/-, RTS+/-, CTS+/- and GND for RS422.

Each channel has 64 byte transmit and receive FIFOs to significantly reduce the overhead required to provide data to and get data from the transmitters and receivers. The FIFO trigger levels are programmable per channel. The baud rate is individually programmable for up to 921.6 kbps for RS232 channels (16x sampling rate) and up to 2.7648/5.5296 Mbps for RS422 channels (16x/8x sampling rate). The UART offers readable FIFO levels per channel.

All channels generate interrupts on PCI interrupt INTA. For fast interrupt source detection the UART provides a global Interrupt Source Register.

All serial channels are using ESD protected transceivers.

The TPMC461 generates 3.3V PCI I/O signal levels and tolerates 5.0V PCI I/O signal levels.

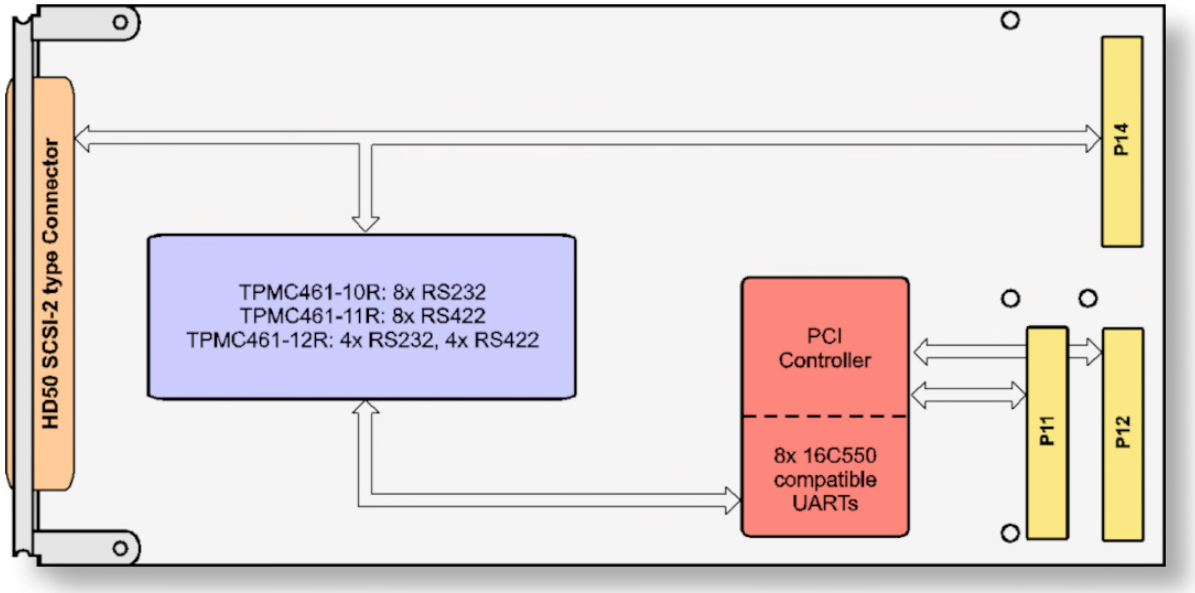

Figure 1-1 : Block Diagram

2 Technical Specification

General	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1, Single Size
Electrical Interface	PCI Rev. 3.0 compatible 33 MHz / 32 bit PCI Target 3.3V and 5V PCI Signaling Voltage compatible

Main On Board Devices	
PCI Target Chip & Octal UART	FPGA based (AMD/Xilinx 7 Series)
I/O Transceiver	RS232 Full-Modem: TRSF3243E (or equivalent) RS232: TRS3122E (or equivalent) RS422: THVD1452 (or equivalent)

I/O Interface	
Number of Serial Channels	8
Physical I/O Interface	TPMC461-10R: 8 RS232 (2 Full-Modem) TPMC461-11R: 8 RS422 (2 with RTS & CTS) TPMC461-12R: 4 RS232 (2 Full-Modem), 4 RS422
Serial Channel I/O Signals	RS232 Full-Modem: TXD, RXD, RTS, CTS, DTR, DSR, CD, RI, GND RS232: TXD, RXD, RTS, CTS, GND RS422: TXD+/, RXD+/-, GND (TPMC461-11R: RTS+/-, CTS+/-)
On-Board Termination	RS422: 120Ω between RXD+ and RXD- inputs of each RS422 channel (TPMC461-11R also between CTS+ and CTS- inputs)
Programmable Baud Rates	RS232: Up to 921.6 kbps (16x Sampling Rate) RS422: Up to 2.7648 Mbps (16x Sampling Rate), 5.5296 Mbps (8x Sampling Rate)
ESD Protection	IEC 61000-4-2, ±30kV contact, ±30kV air
I/O Connectors	HD50 SCSI-2 type connector (e.g. AMP# 787395-5) PMC P14 I/O (64 pin Mezzanine Connector)

Physical Data	
Power Requirements	Condition: All channels connected to remote channel, line idle. TPMC461-10R: 155 mA typical @ +5V DC TPMC461-11R: 310 mA typical @ +5V DC TPMC461-12R: 215 mA typical @ +5V DC
Temperature Range	Operating -40 °C to +85 °C Storage -40 °C to +85 °C
MTBF	660.0000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	70 g

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with the appropriate care!

3.2 Forced Air Cooling

This PMC module requires adequate forced air cooling!
Forced air cooling is mandatory at ambient temperatures exceeding 35°C!

4 Terms and Definitions

4.1 Register Bit Access Types

Register Bit Access Type		Description
R	Read	The bit is readable by software (not writeable)
W	Write	The bit is writeable by software (not readable)
R/W	Read/Write	The bit is readable and writeable by software
R/C	Read/Clear	The bit is readable by software The bit is set by firmware Software may clear the bit by writing a '1'
R/S	Read/Set	The bit is readable by software Software may set this bit to '1' The bit is cleared by firmware

Table 4-1 : Register Bit Access Types

When reading reserved register bits, the read value is undefined.

For future software compatibility: For register write access, reserved bits shall be written '0'.

4.2 Signal Direction Types

Signal Direction Types as stated in Pin Assignment tables.

Signal Direction (Dir)	Description
I	TEWS card input Externally driven signal into the TEWS card
O	TEWS card output Signal driven out by TEWS card
I/O	Bi-Directional Signal
OD	TEWS card Open Drain output Signal driven low or tri-stated by TEWS card

Table 4-2 : Signal Direction Types

4.3 Style Conventions

Hexadecimal values are shown with prefix 0x (i.e. 0x029E).

Binary values are shown with prefix 0b (i.e. 0b0110).

"Active Low" signals are shown with a # suffix (i.e. RESET#).

5 Addressing

5.1 PCI Configuration Space

5.1.1 PCI Device Identification

	Offset	
Vendor ID	0x00	0x1498 (TEWS Technologies)
Device ID	0x02	0x01CD (TPMC461)
Revision ID	0x08	0x00
Class Code	0x09	0x070002 Simple communication controllers, 16550-compatible serial controller
Subsystem Vendor ID	0x2C	0x1498 (TEWS Technologies)
Subsystem ID	0x2E	0x000A (TPMC461-10R) 0x000B (TPMC461-11R) 0x000C (TPMC461-12R)

Table 5-1 : PCI Device Identification

5.1.2 Other PCI Configuration Registers

	Offset	
Cache Line Size	0x0C	Not supported
Latency Timer	0x0D	Not supported
Header Type	0x0E	0x00
Built-In Self-Test	0x0F	Not supported
Capabilities Pointer	0x34	0x00 (no capability list)
Interrupt Line	0x3C	Supported
Interrupt Pin	0x3D	0x01 (INTA#)
MIN_GNT	0x3E	Not supported
MAX_LAT	0x3F	Not supported

Table 5-2 : Other PCI Configuration Registers

5.1.3 PCI Base Address Registers

BAR	Offset in PCI Config Space	Space Mapping	Size (Byte)	Prefetch	Port Width (Bit)	Endian Mode	Description
0	0x10	MEM	4096	No	8 16 32	Little	Device Register Space

Table 5-3 : PCI Base Address Registers

All addressable regions and registers are located in the Device Register Space accessible via PCI BAR 0.

5.2 Device Register Space

PCI Base Address:	PCI Base Address 0 (Offset 0x10 in PCI Configuration Space).

The Device Register Space map consists of UART channel specific address regions and a global Device Configuration Register Set, embedded within the UART channel 0 address region.

Offset to PCI BAR 0	Address Region
0x0000 … 0x007F	UART Channel 0 Region
0x0080 … 0x009F	Device Configuration Registers
0x0100 … 0x01FF	UART Channel 0 Region (continued)
0x0200 … 0x02FF	UART Channel 1 Region
0x0400 … 0x05FF	UART Channel 2 Region
0x0600 … 0x07FF	UART Channel 3 Region
0x0800 … 0x09FF	UART Channel 4 Region
0x0A00 … 0x0BFF	UART Channel 5 Region
0x0C00 … 0x0DFF	UART Channel 6 Region
0x0E00 … 0x0FFF	UART Channel 7 Region

Table 5-4 : Device Register Space Map (Overview)

The following table shows a more detailed view of the Device Register Space Map.
A UART channel specific address region includes the channel control & status registers and also Read and Write FIFO ranges. The UART channel control & status registers are typically accessed in 8 bit width.

Offset to PCI BAR 0	Description
0x000 … 0x00F	UART 0 – Channel Registers
0x010 … 0x07F	Reserved
0x080 … 0x093	(Global) Device Configuration Registers
0x094 … 0x0FF	Reserved
0x100 … 0x13F	UART 0 – Read Data FIFO (Read Operation)
0x100 … 0x13F	UART 0 – Write Data FIFO (Write Operation)
0x140 … 0x17F	Reserved
0x180 … 0x1FF	UART 0 - Read Data FIFO with Error Status (Read Operation)
0x200 … 0x20F	UART 1 – Channel Registers
0x210 … 0x2FF	Reserved
0x300 … 0x33F	UART 1 – Read Data FIFO (Read Operation)
0x300 … 0x33F	UART 1 – Write Data FIFO (Write Operation)
0x340 … 0x37F	Reserved
0x380 … 0x3FF	UART 1 - Read Data FIFO with Error Status (Read Operation)
0x400 … 0x40F	UART 2 – Channel Registers
0x410 … 0x4FF	Reserved
0x500 … 0x53F	UART 2 – Read Data FIFO (Read Operation)
0x500 … 0x53F	UART 2 – Write Data FIFO (Write Operation)
0x540 … 0x57F	Reserved
0x580 … 0x5FF	UART 2 - Read Data FIFO with Error Status (Read Operation)
0x600 … 0x60F	UART 3 – Channel Registers
0x610 … 0x6FF	Reserved

0x700 … 0x73F	UART 3 – Read Data FIFO (Read Operation)
0x700 … 0x73F	UART 3 – Write Data FIFO (Write Operation)
0x740 … 0x77F	Reserved
0x780 … 0x7FF	UART 3 - Read Data FIFO with Error Status (Read Operation)
0x800 … 0x80F	UART 4 – Channel Registers
0x810 … 0x8FF	Reserved
0x900 … 0x93F	UART 4 – Read Data FIFO (Read Operation)
0x900 … 0x93F	UART 4 – Write Data FIFO (Write Operation)
0x940 … 0x97F	Reserved
0x980 … 0x9FF	UART 4 - Read Data FIFO with Error Status (Read Operation)
0xA00 … 0xA0F	UART 5 – Channel Registers
0xA10 … 0xAFF	Reserved
0xB00 … 0xB3F	UART 5 – Read Data FIFO (Read Operation)
0xB00 … 0xB3F	UART 5 – Write Data FIFO (Write Operation)
0xB40 … 0xB7F	Reserved
0xB80 … 0xBFF	UART 5 - Read Data FIFO with Error Status (Read Operation)
0xC00 … 0xC0F	UART 6 – Channel Registers
0xC10 … 0xCFF	Reserved
0xD00 … 0xD3F	UART 6 – Read Data FIFO (Read Operation)
0xD00 … 0xD3F	UART 6 – Write Data FIFO (Write Operation)
0xD40 … 0xD7F	Reserved
0xD80 … 0xDFF	UART 6 - Read Data FIFO with Error Status (Read Operation)
0xE00 … 0xE0F	UART 7 – Channel Registers
0xE10 … 0xEFF	Reserved
0xF00 … 0xF3F	UART 7 – Read Data FIFO (Read Operation)
0xF00 … 0xF3F	UART 7 – Write Data FIFO (Write Operation)
0xF40 … 0xF7F	Reserved
0xF80 … 0xFFF	UART 7 - Read Data FIFO with Error Status (Read Operation)

Table 5-5 : Device Register Space Map (More Details)

The Read (Receive) Data FIFO and Write (Transmit) Data FIFO regions can be accessed in 8/16/32 bit transfer size. These regions may be used instead of the UART (byte-wide) Channel Registers RHR and THR. Because of the FIFO-like behavior, there is no need to use address increments for successive reads from or writes to these regions.

The *Read Data FIFO With LSR Error Status* regions must be read in either 16 bit transfer size (one character and dedicated status) or 32 bit transfer size (two characters, each with dedicated status). It provides each receive character (MSB) with a corresponding status byte (LSB).

Bit	Description
7	Indicator for the sum of all error bits in the RX FIFO. Set when at least one parity error, framing error or break indication is anywhere in the RX FIFO data (RX FIFO Error)
6	Current LSR bit 6 setting (TSR Empty)
5	Current LSR bit 5 setting (THR Empty)

4	LSR bit 4 that has been stored along with the receive character (RX Break)
3	LSR bit 3 that has been stored along with the receive character (RX Framing Error)
2	LSR bit 2 that has been stored along with the receive character (RX Parity Error)
1	Current LSR bit 1 setting (RX Overrun)
0	Set when RX FIFO Level > 0 (RX Data Ready)

Table 5-6 : Status Byte of the Read Data FIFO With Error Status Region

5.2.1 Device Configuration Register Map

The (Global) Device Configuration Registers control general operating conditions and monitor the status of various functions. This includes a 16 bit general purpose timer/counter, multipurpose input/outputs (not utilized by the TPMC461), soft-reset and device identification and revision. The Device Configuration Registers are embedded within the UART Channel 0 address region.

Offset to PCI BAR 0	Register	Description	Access	Reset Value
0x080	INT0 [7:0]	UART Channel Interrupt Indicator	R	0x00
0x081	INT1 [15:8]	(Priority) Interrupt Source Details	R	0x00
0x082	INT2 [23:16]		R	0x00
0x083	INT3 [31:24]		R	0x00
0x084	TIMERCNTL	Timer Control Register	R/W	0x00
0x085	Reserved	Reserved	-	0x00
0x086	TIMERLSB	Programmable Timer Value	R/W	0x00
0x087	TIMERMSB		R/W	0x00
0x088	8XMODE	UART Channel 8x Sampling Rate Select	R/W	0x00
0x089	Reserved	Reserved	-	0x00
0x08A	RESET	UART Channel Reset	W	0x00
0x08B	Reserved	Reserved	-	0x00
0x08C	DREV	Device Revision	R	0xXX
0x08D	DVID	Device Identification	R	0xXX
0x08E	REGB	Simultaneous UART Write & EEPROM Interface	R/W	0x00
0x08F	MPIOINT	MPIO Interrupt Mask/Enable	R/W	0x00
0x090	MPIOLVL	MPIO Level Control	R/W	0x00
0x091	MPIO3T	MPIO Output Pin Tri-State Control	R/W	0x00
0x092	MPIOINV	MPIO Input Polarity Select	R/W	0x00
0x093	MPIOSEL	MPIO Input/Output Select	R/W	0xFF

Table 5-7 : Device Configuration Register Map

5.2.2 UART Channel Register Map

There is a dedicated address region for each of the 8 UART channels.

Base Offset to PCI BAR 0	Description
0x000	UART Channel 0 Region
0x200	UART Channel 1 Region
0x400	UART Channel 2 Region
0x600	UART Channel 3 Region
0x800	UART Channel 4 Region
0xA00	UART Channel 5 Region
0xC00	UART Channel 6 Region
0xE00	UART Channel 7 Region

Table 5-8 : UART Channel Address Regions

A UART channel address region contains the UART channel registers and UART channel FIFOs. The global Device Configuration Registers are embedded in an otherwise reserved section of the UART channel 0 address region.

Offset to Channel Region Base	Description	Access	Data Width
0x000 … 0x00F	UART Channel Registers	R/W	8
0x010 … 0x07F	Reserved	-	
0x080 … 0x093	Channel 0: Device Configuration Registers Other Channels: Reserved	R/W	8, 16, 32
0x094 … 0x0FF	Reserved	-	
0x100 … 0x13F	Read FIFO (64 Bytes of RX FIFO Data)	R	8, 16, 32
	Write FIFO (64 Bytes of TX FIFO Data)	W	8, 16, 32
0x140 … 0x17F	Reserved	-	
0x180 … 0x1FF	Read FIFO Data with Error Status 64 Bytes of RX FIFO Data & Error Status	R	16, 32

Table 5-9 : UART Channel Address Region Map

Each UART channel has a dedicated set of control & status registers (the UART channel registers).

Channel Register Offset	Register	Access	Reset Value
0x0	LCR[7] = 0: RHR – Receive Holding Register	R	0xXX
	LCR[7] = 1: DLL – Baud Rate Generator Divisor Latch Low		0x00
	LCR[7] = 0: THR – Transmit Holding Register	W	0xXX
	LCR[7] = 1: DLL – Baud Rate Generator Divisor Latch Low		0x00
0x1	LCR[7] = 0: IER – Interrupt Enable Register	R/W	0x00
	LCR[7] = 1: DLM – Baud Rate Generator Divisor Latch High		0x01
0x2	ISR – Interrupt Status Register	R	0x01
	FCR – FIFO Control Register	W	0x00
0x3	LCR – Line Control Register	R/W	0x00
0x4	MCR – Modem Control Register	R/W	0x00
0x5	LSR – Line Status Register	R	0x60

0x6	MSR – Modem Status Register	R	0xX0
	Auto RS485 Delay (not supported by TPMC461)	W	
0x7	SPR – Scratch Pad Register	R/W	0xFF
0x8	FCTR – Feature Control Register	R/W	0x00
0x9	EFR – Enhanced Function Register	R/W	0x00
0xA	TXCNT – Transmit FIFO Level Counter	R	0x00
	TXTRG – Transmit FIFO Trigger Level	W	
0xB	RXCNT – Receive FIFO Level Counter	R	0x00
	RXTRG – Receive FIFO Trigger Level	W	
0xC	Xchar – Xon, Xoff Receive Flags	R	0x00
	Xoff-1 – Xoff Character 1	W	
0xD	Reserved	R	0x00
	Xoff-2 – Xoff Character 2	W	
0xE	Reserved	R	0x00
	Xon-1 – Xon Character 1	W	
0xF	Reserved	R	0x00
	Xon-2 – Xon Character 2	W	

Table 5-10 : UART Channel Registers

The PCI address of UART channel register y on UART channel x is:

PCI Base Address 0 (PCI Base Address for all Device Registers)

+ Offset of the UART Channel x Address Region

+ Offset of Register y within a UART Channel Register Set

Addressing example:

The PCI address for the LCR register of UART channel 5 is:

PCI Base Address 0 (PCI Base Address for all Device Registers)

+ 0x0A00 (Offset of the UART Channel 5 Address Region

+ 0x0003 (Offset of the LCR register within a UART Channel Register Set)

OFFS	REG	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	COMMENT
0x00	RHR	R	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
	THR	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
	DLL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1
0x01	DLM	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1
	IER	R/W	0/ CTS/DSR Int. Enable	0/ RTS/DTR Int. Enable	0/ Xon/Xoff/ Sp. Char Int. Enable	0	Modem Status Int. Enable	RX Line Int. Enable	TX Empty Int. Enable	RX Data Int. Enable	LCR[7]=0
0x02	ISR	R	FIFOs Enable	FIFOs Enable	0/ Delta Flow Control	0/ Xon/Xoff/ Sp. Char	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
	FCR	W	RF FIFO Trigger	RX FIFO Trigger	0/ TX FIFO Trigger	0/ TX FIFO Trigger	0	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0x03	LCR	R/W	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
0x04	MCR	R/W	0/ BRG Prescaler	0/ IR Enable	0/ XonAny	Internal Loopback Enable	(OP2)	(OP1) RTS/DTR Flow Sel	RTS# Pin Control	DTR# Pin Control	
0x05	LSR	R/W	RX FIFO Error	TSR Empty	THR Empty	RX Break	RX Framing Error	RX Polarity Error	RX Overrun	RX Data Ready	
0x06	MSR	R	CD	RI	DSR	CTS	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
	MSR	W	RS485 DLY-3	RS485 DLY-2	RS485 DLY-1	RS485 DLY-0	Rsv.	Rsv.	Rsv.	Rsv.	
0x07	SPR	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	User Data
0x08	FCTR	R/W	TRG Table Bit-1	TRG Table Bit-0	Auto RS485 Enable	Invert IR RX Input	RTS/DTR Hyst Bit-3	RTS/DTR Hyst Bit-2	RTS/DTR Hyst Bit-1	RTS/DTR Hyst Bit-0	
0x09	EFR	R/W	Auto CTS/DSR Enable	Auto RTS/DTR Enable	Special Char Enable	Enable IER[7:5] FCR[5:4] MCR[7:5] MSR[7:4]	SW Flow Cntl. Bit-3	SW Flow Cntl. Bit-2	SW Flow Cntl. Bit-1	SW Flow Cntl. Bit-0	
0x0A	TXCNT	R	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
	TXTRG	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x0B	RXCNT	R	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
	RXTRG	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x0C	XCHAR	R	0	0	0	0	0	0	Xon Det. Indic.	Xoff Det. Indic.	Self Clear on Read
0x0C	XOFF1	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x0D	XOFF2	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x0E	XON1	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x0F	XON2	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

Table 5-11 : UART Channel Registers (II)

Note that some registers are Read-Only or Write-Only registers.

Note that some Read-Only and Write-Only registers share the same address offset!

Shaded fields are only writeable while EFR bit 4 is set. Clearing EFR bit 4 latches the register bit values.

5.3 Device Configuration Registers

Stated address offsets are to the PCI BAR 0 base address. The Device Configuration Registers are embedded in an otherwise reserved section of the UART channel 0 address region.

5.3.1 Global Interrupt Register(s)

Typically the global Interrupt Registers (INT3, INT2, INT1, INT0) are read as a single (32 bit) DWord.

5.3.1.1 INT0 – Global Interrupt 0 Register

This register is used for an interrupt pending look-up for the different UART channels.

Bit	Symbol	Description	Access	Reset Value
7	CH7_ INT_STAT	Channel 7 Interrupt Status See Channel 0 Interrupt Status description.	R	0
6	CH6_ INT_STAT	Channel 6 Interrupt Status See Channel 0 Interrupt Status for a description.	R	0
5	CH5_ INT_STAT	Channel 5 Interrupt Status See Channel 0 Interrupt Status description.	R	0
4	CH4_ INT_STAT	Channel 4 Interrupt Status See Channel 0 Interrupt Status description.	R	0
3	CH3_ INT_STAT	Channel 3 Interrupt Status See Channel 0 Interrupt Status description.	R	0
2	CH2_ INT_STAT	Channel 2 Interrupt Status See Channel 0 Interrupt Status description.	R	0
1	CH1_ INT_STAT	Channel 1 Interrupt Status See Channel 0 Interrupt Status description.	R	0
0	CH0_ INT_STAT	Channel 0 Interrupt Status Indicates an interrupt condition in the corresponding channel interrupt status register (ISR bit-0). The status is cleared by reading the appropriate interrupting channel register. 0: No channel interrupt pending 1: Channel interrupt pending	R	0

Table 5-12 : INT0 – Interrupt 0 Register (0x080)

5.3.2.1 INT1, INT2, INT3 – Global Interrupt 1, 2, 3 Register

These registers are providing a current (highest priority) interrupt source encoding for the various UART channels.

Bit	Symbol	Description	Access	Reset Value
7	CH2_BIT1	Channel 2 Interrupt Source (Bits [1:0])	R	0
6	CH2_BIT0		R	0
5	CH1_BIT2	Channel 1 Interrupt Source (Bits [2:0])	R	0
4	CH1_BIT1		R	0
3	CH1_BIT0		R	0
2	CH0_BIT2	Channel 0 Interrupt Source (Bits [2:0])	R	0
1	CH0_BIT1		R	0
0	CH0_BIT0		R	0

Table 5-13 : INT1 – Global Interrupt 1 Register (0x081)

Bit	Symbol	Description	Access	Reset Value
7	CH5_BIT0	Channel 5 Interrupt Source (Bit [0])	R	0
6	CH4_BIT2	Channel 4 Interrupt Source (Bits [2:0])	R	0
5	CH4_BIT1		R	0
4	CH4_BIT0		R	0
3	CH3_BIT2	Channel 3 Interrupt Source (Bits [2:0])	R	0
2	CH3_BIT1		R	0
1	CH3_BIT0		R	0
0	CH2_BIT2	Channel 2 Interrupt Source (Bit [2])	R	0

Table 5-14 : INT2 – Global Interrupt 2 Register (0x082)

Bit	Symbol	Description	Access	Reset Value
7	CH7_BIT2	Channel 7 Interrupt Source (Bits [2:0])	R	0
6	CH7_BIT1		R	0
5	CH7_BIT0		R	0
4	CH6_BIT2	Channel 6 Interrupt Source (Bits [2:0])	R	0
3	CH6_BIT1		R	0
2	CH6_BIT0		R	0
1	CH5_BIT2	Channel 5 Interrupt Source (Bits [2:1])	R	0
0	CH5_BIT1		R	0

Table 5-15 : INT3 – Global Interrupt 3 Register (0x083)

5.3.2.3 Interrupt Register Notes

The table below shows the DWord (32 bit) composition for the (global) interrupt registers.

DWord Bits	31:24	23:16	15:08	07:00
(Byte) Register	INT3	INT2	INT	INT0
(Byte) Offset	0x83	0x82	0x81	0x80

Table 5-16 : Interrupt DWord Register Composition

Bit	Symbol	Description	Access	Reset Value
31	CH7_BIT2	Channel 7 Interrupt Source	R	0
30	CH7_BIT1		R	0
29	CH7_BIT0		R	0
28	CH6_BIT2	Channel 6 Interrupt Source	R	0
27	CH6_BIT1		R	0
26	CH6_BIT0		R	0
25	CH5_BIT2	Channel 5 Interrupt Source	R	0
24	CH5_BIT1		R	0
23	CH5_BIT0		R	0
22	CH4_BIT2	Channel 4 Interrupt Source	R	0
21	CH4_BIT1		R	0
20	CH4_BIT0		R	0
19	CH3_BIT2	Channel 3 Interrupt Source	R	0
18	CH3_BIT1		R	0
17	CH3_BIT0		R	0
16	CH2_BIT2	Channel 2 Interrupt Source	R	0
15	CH2_BIT1		R	0
14	CH2_BIT0		R	0
13	CH1_BIT2	Channel 1 Interrupt Source	R	0
12	CH1_BIT1		R	0
11	CH1_BIT0		R	0
10	CH0_BIT2	Channel 0 Interrupt Source	R	0
9	CH0_BIT1		R	0
8	CH0_BIT0		R	0
7	CH7_ INT_STAT	Channel 7 Interrupt Status See Channel 0 Interrupt Status description.	R	0
6	CH6_ INT_STAT	Channel 6 Interrupt Status See Channel 0 Interrupt Status for a description.	R	0
5	CH5_ INT_STAT	Channel 5 Interrupt Status See Channel 0 Interrupt Status description.	R	0
4	CH4_ INT_STAT	Channel 4 Interrupt Status See Channel 0 Interrupt Status description.	R	0
3	CH3_ INT_STAT	Channel 3 Interrupt Status See Channel 0 Interrupt Status description.	R	0

Bit	Symbol	Description	Access	Reset Value
2	CH2_ INT_STAT	Channel 2 Interrupt Status See Channel 0 Interrupt Status description.	R	0
1	CH1_ INT_STAT	Channel 1 Interrupt Status See Channel 0 Interrupt Status description.	R	0
0	CH0_ INT_STAT	Channel 0 Interrupt Status Indicates an interrupt condition in the corresponding channel interrupt status register (ISR bit-0). The status is cleared by reading the appropriate channel register. 0: No channel interrupt pending 1: Channel interrupt pending	R	0

Table 5-17 : Interrupt DWord Register (0x80)

The table below shows the interrupt source encoding for the Global Interrupt Register(s).

Interrupt priorities 1 to 4 are UART channel based interrupts. Interrupt priorities 6 & 7 are device configuration register based interrupts. Note that for UART channel based interrupts, the channel individual Interrupt Status Registers (ISR) provide even more information regarding the interrupt source.

Priority Level	Interrupt Source Bit Group			Interrupt Source
	[2]	[1]	[0]	
x	0	0	0	None
1	0	0	1	RXRDY and RX Line Status (Logic OR of LSR[4:1])
2	0	1	0	RXRDY Time-Out
3	0	1	1	TXRDY, THR or TSR (Auto RS485 Mode) empty
4	1	0	0	MSR, RTS/CTS or DTR/DSR Delta or Xoff/Xon Det. or Special Char. detected
5	1	0	1	Reserved
6	1	1	0	MPIO Pins (available only within Channel 0)
7	1	1	1	Timer Time-Out (available only within Channel 0)

Table 5-18 : Interrupt Source Encoding

The table below shows means for clearing the various interrupt sources.

Interrupt Clearing
RXRDY is cleared by reading data in the RX FIFO until it falls below the trigger level
RXRDY Time-Out is cleared by reading data and/or by reception of a next character
RX Line Status interrupt is cleared by reading the LSR register
Modem Status Register interrupt is cleared by reading the MSR register
RTS/CTS or DTR/DSR Delta interrupt is cleared by reading the MSR register
Xoff/Xon interrupt is cleared by reading the ISR register
Special Character interrupt is cleared by reading the ISR register and/or by reception of a next character
Timer Time-Out interrupt is cleared by reading the TIMERCNTL register
MPIO interrupt is cleared by reading the MPIOLVL register

Table 5-19 : Interrupt Clearing

5.3.3 Timer Registers

5.3.3.1 TMRCTRL – Timer Control Register

This register provides timer/counter related control functions.

Bit	Symbol	Description	Access	Reset Value
7:5	-	Reserved	R	0
4	TMR_ OUT_EN	Timer/Counter Output Enable 0: MPIOLVL[0] controls the MPIO[0] level 1: Timer/Counter Time-Out status is routed to MPIO[0] Timer output is high while counting and low when expired.	R/W	0
3	TMR_ CLK_SEL	Timer/Counter Clock Select Selects the timer/counter clock source. 0: Main UART base clock signal (44.2368 MHz) 1: External clock signal (TMRCLK pin) **[Not supported]**	R/W	0
2	TMR_ MODE	Timer/Counter Operation Mode 0: Timer/Counter is automatically re-loaded & re-triggered when done 1: One-shot (Timer/Counter stops counting when expired)	R/W	0
1	TMR_ CNT_EN	Timer/Counter Count Enable 0: Stops/pauses the timer/counter 1: Starts/re-starts the timer/counter	R/W	0
0	TMR_ INT_EN	Timer/Counter Interrupt Enable 0: Disabled 1: Enabled Reading TMRCTRL clears the interrupt.	R/W	0

Table 5-20 : TMRCTRL – Timer Control Register (0x084)

5.3.3.2 TMRLSB – Timer LSB Load Value

The two eight-bit registers TMRMSB and TMRLSB form a 16-bit timer load value with the least-significant bit is defined by TMRLSB bit-0 and the most-significant-bit is defined by TMRMSB bit-7.

Bit	Symbol	Description	Access	Reset Value
7:0	TMR_LSB	Timer Load Value, Least Significant Byte	R/W	0

Table 5-21 : TMRLSB – Timer Load Value, Least Significant Byte Register (0x086)

5.3.3.3 TMRMSB – Timer MSB Load Value

The two eight-bit registers TMRMSB and TMRLSB form a 16-bit timer load value with the least-significant bit is defined by TMRLSB bit-0 and the most-significant-bit is defined by TMRMSB bit-7.

Bit	Symbol	Description	Access	Reset Value
7:0	TMR_MSB	Timer Load Value, Most Significant Byte	R/W	0

Table 5-22 : TMRMSB – Timer Load Value, Most Significant Byte Register (0x087)

5.3.4 8XMODE – UART Channel Sampling Rate Selection Register

The register allows selecting the UART channel sampling rate.

Bit	Symbol	Description	Access	Reset Value
7	SRATE_CH7	Sampling Rate Channel 7 See Sampling Rate UART Channel 0 description	R/W	0
6	SRATE_CH6	Sampling Rate Channel 6 See Sampling Rate UART Channel 0 description	R/W	0
5	SRATE_CH5	Sampling Rate Channel 5 See Sampling Rate UART Channel 0 description	R/W	0
4	SRATE_CH4	Sampling Rate Channel 4 See Sampling Rate UART Channel 0 description	R/W	0
3	SRATE_CH3	Sampling Rate Channel 3 See Sampling Rate UART Channel 0 description	R/W	0
2	SRATE_CH2	Sampling Rate Channel 2 See Sampling Rate UART Channel 0 description	R/W	0
1	SRATE_CH1	Sampling Rate Channel 1 See Sampling Rate UART Channel 0 description	R/W	0
0	SRATE_CH0	Sampling Rate Channel 0 0: 16X Sampling Rate (default) 1: 8X Sampling Rate Transmit and receive data rates will double in 8X mode. Also see *Baud Rate Programming*.	R/W	0

Table 5-23 : 8XMODE – UART Channel Sampling Rate Selection Register (0x088)

5.3.5 RESET – UART Channel Reset Register

The register provides the ability to perform a reset per UART channel.

Bit	Symbol	Description	Access	Reset Value
7	RST_CH7	Reset Channel 7 See Reset Channel 0 description	R/W	0
6	RST_CH6	Reset Channel 6 See Reset Channel 0 description	R/W	0
5	RST_CH5	Reset Channel 5 See Reset Channel 0 description	R/W	0
4	RST_CH4	Reset Channel 4 See Reset Channel 0 description	R/W	0
3	RST_CH3	Reset Channel 3 See Reset Channel 0 description	R/W	0
2	RST_CH2	Reset Channel 2 See Reset Channel 0 description	R/W	0
1	RST_CH1	Reset Channel 1 See Reset Channel 0 description	R/W	0
0	RST_CH0	Reset Channel 0 0: Normal operation (default) 1: Channel Reset The channel control logic is reset and the channel registers will reset to their reset value. This bit is self-clearing.	R/S	0

Table 5-24 : RESET – UART Channel Reset Register (0x08A)

5.3.6 Global (Device) Information Registers

There are two registers (DREV, DVID) that provide global (device) identification and revision information.

5.3.6.1 DVID – Global (Device) ID Register

Bit	Symbol	Description	Access	Reset Value
7:0	DVID_ VAL	Global (device) UART Core Identification 0x22: Dual-Channel UART 0x24: Quad-Channel UART 0x28: Octal-Channel UART	R	0

Table 5-25 : DVID – Global (Device) ID Register (0x08C)

5.3.6.2 DREV – Global (Device) Revision Register

Bit	Symbol	Description	Access	Reset Value
7:0	DREV_ VAL	Global (device) UART Revision Identification 0x01: Revision A 0x02: Revision B … (and so forth)	R	0

Table 5-26 : DREV – Global (Device) Revision Register (0x08D)

5.3.7 REGB – Optional Control Register

This register provides miscellaneous global control and interface options.

Bit	Symbol	Description	Access	Reset Value
7	EEP_DO	EEPROM Data Output Status Represents the (serial) data output value of the non-volatile memory.	R	-
6	EEP_DI	EEPROM Data Input Control Sets the (serial) data input value of the non-volatile memory.	W	0
5	EEP_CS	EEPROM Chip Select Control Sets the chip select input value of the non-volatile memory.	W	0
4	EEP_CLK	EEPROM Clock Control Sets the clock input value of the non-volatile memory.	W	0
3:1	-	Reserved	-	
0	CH_CFG_ REG_WR_ CTRL	Channel Configuration Register Write Control Selects whether write access to the UART channel configuration registers is performed individually on the selected channel or simultaneously for all channels. 0: Individual configuration register writes (default) 1: Simultaneous configuration register writes Use channel 0 register offsets for simultaneous configuration register setup on all channels. Note that the THR is not included!	R/W	0

Table 5-27 : REGB – Optional Control Register (0x08E)

5.3.8 MPIO Registers

On the TPMC461, the MPIO signals are not user accessible.

5.3.8.1 MPIOINT – MPIO Interrupt Enable Register

This register is used for Multipurpose I/O interrupt enable control.

Bit	Symbol	Description	Access	Reset Value
7	MPI7_ INT_EN	Multipurpose Input 7 Interrupt Enable See Multipurpose Input 0 Interrupt Enable description	R/W	0
6	MPI6_ INT_EN	Multipurpose Input 6 Interrupt Enable See Multipurpose Input 0 Interrupt Enable description	R/W	0
5	MPI5_ INT_EN	Multipurpose Input 5 Interrupt Enable See Multipurpose Input 0 Interrupt Enable description	R/W	0
4	MPI4_ INT_EN	Multipurpose Input 4 Interrupt Enable See Multipurpose Input 0 Interrupt Enable description	R/W	0
3	MPI3_ INT_EN	Multipurpose Input 3 Interrupt Enable See Multipurpose Input 0 Interrupt Enable description	R/W	0
2	MPI2_ INT_EN	Multipurpose Input 2 Interrupt Enable See Multipurpose Input 0 Interrupt Enable description	R/W	0
1	MPI1_ INT_EN	Multipurpose Input 1 Interrupt Enable See Multipurpose Input 0 Interrupt Enable description	R/W	0
0	MPI0_ INT_EN	Multipurpose Input 0 Interrupt Enable This bit controls the MPIO input interrupt functionality. An interrupt event is internally detected by a rising edge of the MPIO level (for falling edge detection, input inversion by MPIOINV is required). 0: Interrupt generation is disabled (default) 1: Enables interrupt generation An MPIO interrupt clears after reading the MPIOLVL register. Note that MPIO interrupt edge detection and generation enable also requires that the MPIO pin is configured as input by MPIOSEL.	R/W	0

Table 5-28 : MPIOINT – MPIO Interrupt Enable Register (0x08F)

5.3.8.2 MPIOLVL – MPIO Output Level Register

This register is used for reading and setting the Multipurpose I/O pin level.

Bit	Symbol	Description	Access	Reset Value
7	MPIO7_ LVL	Multipurpose Input/Output 7 Level See Multipurpose Input/Output 0 Level description	R/W	0
6	MPIO6_ LVL	Multipurpose Input/Output 6 Level See Multipurpose Input/Output 0 Level description	R/W	0
5	MPIO5_ LVL	Multipurpose Input/Output 5 Level See Multipurpose Input/Output 0 Level description	R/W	0
4	MPIO4_ LVL	Multipurpose Input/Output 4 Level See Multipurpose Input/Output 0 Level description	R/W	0
3	MPIO3_ LVL	Multipurpose Input/Output 3 Level See Multipurpose Input/Output 0 Level description	R/W	0

Bit	Symbol	Description	Access	Reset Value
2	MPIO2_ LVL	Multipurpose Input/Output 2 Level See Multipurpose Input/Output 0 Level description	R/W	0
1	MPIO1_ LVL	Multipurpose Input/Output 1 Level See Multipurpose Input/Output 0 Level description	R/W	0
0	MPIO0_ LVL	Multipurpose Input/Output 0 Level On read the current status of the MPIO input level is returned (may include inversion by MPIOINV). On write the MPIO output level is set when corresponding I/O is configured as output (MPIOSEL) and not tri-stated (MPIO3T). 0: Input/Output is level LOW (default) 1: Input/Output is level HIGH	R/W	0

Table 5-29 : MPIOLVL – MPIO Output Level Register (0x090)

5.3.8.3 MPIO3T – MPIO Output/Tristate Enable Register

This register is used for Multipurpose I/O output enable control.

Bit	Symbol	Description	Access	Reset Value
7	MPIO7_ TS_EN	Multipurpose Input/Output 7 Output/Tristate Enable See Multipurpose Input/Output 0 Level description	R/W	0
6	MPIO6_ TS_EN	Multipurpose Input/Output 6 Output/Tristate Enable See Multipurpose Input/Output 0 Level description	R/W	0
5	MPIO5_ TS_EN	Multipurpose Input/Output 5 Output/Tristate Enable See Multipurpose Input/Output 0 Level description	R/W	0
4	MPIO4_ TS_EN	Multipurpose Input/Output 4 Output/Tristate Enable See Multipurpose Input/Output 0 Level description	R/W	0
3	MPIO3_ TS_EN	Multipurpose Input/Output 3 Output/Tristate Enable See Multipurpose Input/Output 0 Level description	R/W	0
2	MPIO2_ TS_EN	Multipurpose Input/Output 2 Output/Tristate Enable See Multipurpose Input/Output 0 Level description	R/W	0
1	MPIO1_ TS_EN	Multipurpose Input/Output 1 Output/Tristate Enable See Multipurpose Input/Output 0 Level description	R/W	0
0	MPIO0_ TS_EN	Multipurpose Input/Output 0 Output/Tristate Enable Controls (along with MPIOSEL) whether the MPIO output is active or in tristate. 0: MPIO output is active (when not configured as input by MPIOSEL) 1: MPIO output is tristated (default)	R/W	0

Table 5-30 : MPIO3T – MPIO Tristate Register (0x091)

5.3.8.4 MPIOINV – MPIO Input State Inversion

This register controls Multipurpose I/O input level inversion.

Bit	Symbol	Description	Access	Reset Value
7	MPI7_ INV_EN	Multipurpose Input 7 Level Inversion Enable See Multipurpose Input 0 State Inversion Enable description	R/W	0
6	MPI6_ INV_EN	Multipurpose Input 6 Level Inversion Enable See Multipurpose Input 0 State Inversion Enable description	R/W	0

Bit	Symbol	Description	Access	Reset Value
5	MPI5_ INV_EN	Multipurpose Input 5 Level Inversion Enable See Multipurpose Input 0 State Inversion Enable description	R/W	0
4	MPI4_ INV_EN	Multipurpose Input 4 Level Inversion Enable See Multipurpose Input 0 State Inversion Enable description	R/W	0
3	MPI3_ INV_EN	Multipurpose Input 3 Level Inversion Enable See Multipurpose Input 0 State Inversion Enable description	R/W	0
2	MPI2_ INV_EN	Multipurpose Input 2 Level Inversion Enable See Multipurpose Input 0 State Inversion Enable description	R/W	0
1	MPI1_ INV_EN	Multipurpose Input 1 Level Inversion Enable See Multipurpose Input 0 State Inversion Enable description	R/W	0
0	MPI0_ INV_EN	Multipurpose Input 0 Level Inversion Enable Enables or disables the inversion circuit for the corresponding MPIO input level. 0: Do not invert MPIO input level (default) 1: Invert MPIO input level Effective for MPIOLVL read value and interrupt edge detection.	R/W	0

Table 5-31 : MPIOINV – MPIO Input State Inversion (0x092)

5.3.8.5 MPIOSEL – MPIO Input/Output Selection

This register is used for Multipurpose I/O input/output direction control. The setting also has an impact on interrupt edge detection and generation control.

Bit	Symbol	Description	Access	Reset Value
7	MPIO7_ MODE	Multipurpose Input/Output 7 Operation Mode See Multipurpose Input/Output 0 Operation Mode description	R/W	1
6	MPIO6_ MODE	Multipurpose Input/Output 6 Operation Mode See Multipurpose Input/Output 0 Operation Mode description	R/W	1
5	MPIO5_ MODE	Multipurpose Input/Output 5 Operation Mode See Multipurpose Input/Output 0 Operation Mode description	R/W	1
4	MPIO4_ MODE	Multipurpose Input/Output 4 Operation Mode See Multipurpose Input/Output 0 Operation Mode description	R/W	1
3	MPIO3_ MODE	Multipurpose Input/Output 3 Operation Mode See Multipurpose Input/Output 0 Operation Mode description	R/W	1
2	MPIO2_ MODE	Multipurpose Input/Output 2 Operation Mode See Multipurpose Input/Output 0 Operation Mode description	R/W	1
1	MPIO1_ MODE	Multipurpose Input/Output 1 Operation Mode See Multipurpose Input/Output 0 Operation Mode description	R/W	1

Bit	Symbol	Description	Access	Reset Value
0	MPIO0_ MODE	Multipurpose Input/Output 0 Operation Mode Controls (along with MPIO3T) whether the MPIO output is active or in tristate. 0: Select output operation mode The corresponding output level (MPIOLVL) is driven-out on the MPIO output (when not tristated by MPIO3T). 1: Select input operation mode (default) MPIO output is in tristate and externally sourced. Note that MPIO interrupt edge detection and generation enable requires that the MPIO pin is configured as input by MPIOSEL.	R/W	1

Table 5-32 : MPIOSEL – MPIO Input/Output Selection (0x093)

5.4 UART Channel Registers

Stated address offsets are to the PCI BAR 0 base address and given for the various channels 0-7.

These registers are intended to be accessed with 8 bit (byte) transfer size.

5.4.1 RHR – Receive Holding Register

Accessible when LCR[7] is clear. Only read-accessible.

The receive holding register (RHR) is an 8-bit register that holds a receive data byte from the receive shift register (RSR). It provides the basic receive data interface. Receive data can be read from this register whenever a data byte is transferred from the RSR. LSR bit 0 indicates valid receive data in the RHR. The least-significant-bit (bit-0) is the first data bit received at the RXD input.

RHR is also part of the receive FIFO (RHR is the RX FIFO first-out register when enabled by FCR bit-0).

The RHR can generate a receive data ready interrupt upon receiving a character (in Non-FIFO mode) or when the RX-FIFO level reaches the programmed trigger level (in FIFO mode).

Bit	Symbol	Description	Access	Reset Value
7:0	RX_ DATA	Inbound/Receive Data	R	-

Table 5-33 : RHR – Receive Holding Register (0x000, 0x200, …, 0xE00)

5.4.2 THR – Transmit Holding Register

Accessible when LCR[7] is clear. Only write-accessible.

The transmit holding register is an 8-bit register providing a transmit data interface. Transmit data bytes written to the THR are converted into a serial data stream including start-bit, data bits, optional parity-bit and stop-bit(s). The least-significant-bit (bit-0) is the first data bit presented at the TXD output.

The THR is also part of the transmit FIFO (THR is the TX FIFO input register when enabled by FCR bit-0).

THR can generate a THR empty interrupt when the THR becomes empty (in Non-FIFO mode) or when the TX-FIFO level falls below the programmed trigger level (in FIFO mode).

Bit	Symbol	Description	Access	Reset Value
7:0	TX_ DATA	Outbound/Transmit Data	W	-

Table 5-34 : THR – Transmit Holding Register (0x000, 0x200, …, 0xE00)

5.4.4 DLL/DLM – Baud Rate Generator

Accessible when LCR[7] is set.

The Baud Rate Generator (BRG) is a 16-bit counter that generates the data rate for the transmitter and receiver. The baud rate clock divider is programmed through registers DLL and DLM. Access to these registers needs to be enabled by setting LCR bit-7. LCR bit-7 should be cleared again after setting the baud rate clock divider.

Bit	Symbol	Description	Access	Reset Value
7:0	DLL	Lower 8-bit BRG Divider Value [7:0]	R/W	0x00

Table 5-35 : DLL – Baud Rate Generator Divisor (0x000, 0x200, …, 0xE00)

Bit	Symbol	Description	Access	Reset Value
7:0	DLM	Upper 8-bit BRG Divider Value [15:8]	R/W	0x01

Table 5-36 : DLM – Baud Rate Generator Divisor (0x001, 0x201, …, 0xE01)

Also see the *Baud Rate Programming* chapter.

5.4.5 IER – Interrupt Enable Register

Accessible when LCR[7] is clear.

The Interrupt Enable Register (IER) enables or disables (masks) the interrupts from receive data ready, transmit empty, line status, modem status register and other sources.

Bit	Symbol	Description	Access	Reset Value
7	CTS_DSR_ INT_EN	EFR[4] must be set to modify this bit. 0: Disable the CTS#/DSR# interrupt (default) 1: Enable the CTS#/DSR# interrupt The UART issues an interrupt when the CTS#/DSR# input makes a transition from Low to High (= de-assertion) in Auto CTS/DSR flow control mode (indicating an incoming request to stop/hold the channel's transmitter). Auto CTS/DSR flow control mode must be enabled (EFR bit-7). CTS# or DSR# mode is selected via MCR (bit-2).	R/W	0
6	RTS_DTR_ INT_EN	EFR[4] must be set to modify this bit. 0: Disable the RTS#/DTR# interrupt (default) 1: Enable the RTS#/DTR# interrupt The UART issues an interrupt when the RTS#/DTR# output makes a transition from Low to High (= de-assertion) in Auto RTS/DTR flow control mode (indicating an outgoing request to stop/hold the remote transmitter). Auto RTS/DTR flow control mode must enabled (EFR bit-6). RTS# or DTR# mode is selected via MCR (bit-2).	R/W	0

Bit	Symbol	Description	Access	Reset Value
5	XON_ XOFF_ SPCH_ INT_EN	EFR[4] must be set to modify this bit. 0: Disable the software flow control Xon/Xoff/SpecialChar received interrupt (default) 1: Enable the software flow control Xon/Xoff/SpecialChar received interrupt A software flow control interrupt requires a software flow control mode via EFR bits 3-0. A special char interrupt requires EFR bit 5 = 1 (Special Character Detect Enable) to detect the event. The special character is defined via the XOFF2 register.	R/W	0
4	-	Reserved	R	0
3	MSR_STAT_ INT_EN	Modem Status Interrupt Enable Controls whether MSR register bits 0-3 will generate an MSR interrupt (when set). 0: Disable the modem status register interrupt (default) 1: Enable the modem status register interrupt	R/W	0
2	RX_LINE_ INT_EN	Receive Line Status Interrupt Enable Controls whether LSR register bits 1-4 will generate an LSR interrupt when a received character has an error. 0: Disable the receiver line status interrupt (default) 1: Enable the receiver line status interrupt In FIFO mode, the LSR interrupt would be generated upon reception of the character and again when the character becomes available in the RHR (RX FIFO output).	R/W	0
1	TX_RDY_ INT_EN	Transmit Ready Interrupt Enable In non-FIFO mode, a TX interrupt is issued whenever the THR is empty. In FIFO mode, an interrupt is issued twice: once when the number of bytes in the TX FIFO falls below the programmed trigger level and again when the TX FIFO becomes empty. When autoRS485 mode is enabled (FCTR bit-5 = 1), the second interrupt is delayed until the transmitter (both the TX FIFO and the TX Shift Register) is empty. 0: Disable Transmit ready interrupt (default) 1: Enable Transmit ready interrupt	R/W	0
0	RX_RDY_ INT_EN	Receive Data Ready Interrupt Enable The receive data ready interrupt will be issued upon transferring a data character to the RHR in non-FIFO mode or when the receive FIFO level has reached the configured trigger level in FIFO mode. A receive data timeout interrupt will be issued in FIFO mode when the receive FIFO has not reached the configured trigger level and the RX input has been idle for approx. 4 character plus 12 bit times. The timeout interrupt is cleared and the timer is (re-) set/loaded upon receive data reception and/or receive data reading. 0: Disable the receive data ready interrupt (default) 1: Enable the receiver data ready interrupt	R/W	0

Table 5-37 : IER – Interrupt Enable Register (0x001, 0x201, …, 0xE01)

These interrupts are reported in the (channel specific) Interrupt Status Register (ISR) register and are also encoded in the (global) INT (INT0-INT3) register in the Device Configuration Register region.

Note that disabling an interrupt typically only masks the interrupt but does not clear the corresponding internal interrupt flag.

5.4.6 ISR – Interrupt Status Register

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The (read only) Interrupt Status Register (ISR) provides six interrupt status bits. Performing a read cycle on the ISR will indicate the current highest priority pending interrupt level to be serviced with others queued up for next service. No other interrupts are acknowledged until the pending interrupt is serviced. Interrupts in the ISR are masked when the corresponding IER bit is clear.

Bit	Symbol	Description	Access	Reset Value
7:6	FIFO_EN_ STAT	FIFO Enable Status These bits reflect the state of the Tx/Rx FIFOs. 00: FIFOs disabled 11: FIFOs enabled	R	0
5	CTS_RTS_ INT_STAT	Indicates that CTS#/DSR# or RTS#/DTR# has changed state from Low to High while operating in the corresponding Auto HW Flow Control mode. 0: No change detected 1: CTS#/DSR# input or RTS#/DTR# output has changed state from Low to High The interrupt is cleared by reading the MSR register.	R	0
4	XOFF_XON_ INT_STAT	Indicates a Xon, Xoff reception while operating in the corresponding Auto SW Flow Control mode or a Special Character reception. 0: No match detected 1: Receiver detected a data match of the Xon/Xoff/SpCh character(s). A software flow control Xoff/Xon interrupt is cleared by reading the ISR register. Register XCHAR will indicate which character/pattern (Xoff or Xon) was received last. The software flow control character/pattern must alternate to generate a next software flow control interrupt (e.g. a Xoff must be followed by a Xon). A special character interrupt is cleared by reading the ISR register or automatically when a next character (that is not a special character) is received. A next special char interrupt requires at least one received character that is not a special character.	R	0
3:1	ENC_INT_ STAT	Encoded Interrupt Status These bits indicate the source for a pending interrupt. The highest priority interrupt will be shown (suppressing lower priority interrupt levels). See Interrupt Source Table below.	R	0
0	INT_ STAT	(Pending) Interrupt Status 0: An Interrupt is pending 1: No interrupt pending (default)	R	1

Table 5-38 : ISR – Interrupt Status Register (0x002, 0x202, …, 0xE02)

Priority Level	Interrupt Status Register Bit Encoding						Interrupt Source
	5	4	3	2	1	0	
1	0	0	0	1	1	0	LSR - Receive Line Status Register
2	0	0	0	1	0	0	RXRDY - Receive Data Ready
3	0	0	1	1	0	0	RXRDY - Receive Data Timeout
4	0	0	0	0	1	0	TXRDY - Transmit Ready (RS485 Mode dependent)
5	0	0	0	0	0	0	MSR - Modem Status Register
6	0	1	0	0	0	0	RXRDY - Received Xon/Xoff or Special Character
7	1	0	0	0	0	0	CTS#/DSR# or RTS#/DTR# Change Of State (Low to High transition = de-assertion)
X	0	0	0	0	0	1	None (default)

Table 5-39 : Channel Interrupt Source and Priority Level

Interrupt	Generation	Clearing
LSR	By any of the LSR bits 1, 2, 3 and 4	By read to LSR register
RXRDY	By RX Trigger Level	By reading data until FIFO level falls below the trigger level
RXRDY Time-Out	By 4-Char plus 12 bits delay timer expiration if the RX FIFO level is less than the RX trigger level	By reading data or receiving next character
TXRDY	By LSR bit-5 (or bit-6 in Auto RS485 control mode)	By read to ISR register
MSR	By any of the MSR bits 0, 1, 2 and 3	By read to MSR register
Xon/Xoff/Special Char.	By detection of Xon, Xoff or Special Character	By read to ISR register Special Character: Or automatically when the next character (that is not a special character) has been received.
CTS#/DSR# Input	By a L-to-H change of state of the input pin when Auto Flow Control is enabled by EFR bit-7 and depending on MCR bit-2	By read to MSR register
RTS#/DTR# Output	By a L-to-H change of state of the output pin when Auto Flow Control is enabled by EFR bit-6 and depending on MCR bit-2	By read to MSR register

Table 5-40 : Interrupt Generation & Clearing

5.4.7 FCR – FIFO Control Register

This (write only) register is used to control various FIFO-related functions.

Bit	Symbol	Description	Access	Reset Value
7:6	RX_ FIFO_TRG_ SEL	Receive FIFO Trigger Level Select Applies for trigger tables A, B, C as selected by FCTR bits 7-6. Does not apply for trigger table D. These two bits set the (pre-defined) trigger level for the receive FIFO. The receive FIFO trigger level has an impact on RXRDY interrupt generation and Auto RTS/DTR flow control signal assertion. The RXRDY interrupt will be generated when the RX FIFO level reaches the trigger level. It will be cleared when the RX FIFO level drops below the configured trigger level. See table below for the complete selections.	W	00
5:4	TX_ FIFO_TRG_ SEL	Transmit FIFO Trigger Level Select EFR[4] must be set to modify these bits. Applies for trigger tables A, B, C as selected by FCTR bits 7-6. Does not apply for trigger table D. These two bits set the (pre-defined) trigger level for the transmit FIFO interrupt. The UART will generate a transmit interrupt when the FIFO fill level drops below the trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. It will be cleared when the ISR register is read. See table below for the complete selections.	W	00
3	RSV	Reserved	-	0
2	TX_FIFO_ RST	TX FIFO Reset *(Requires FCR bit-0 to be set)* 0: No transmit FIFO reset (default) 1: Resets the receive FIFO pointers and FIFO level counter logic. The receive shift register is not affected. This bit will return to a logic 0 after resetting the FIFO.	W	0
1	RX_FIFO_ RST	RX FIFO Reset *(Requires FCR bit-0 to be set)* 0: No receive FIFO reset (default) 1: Resets the receive FIFO pointers and FIFO level counter logic. The receive shift register is not affected. This bit will return to a logic 0 after resetting the FIFO.	W	0
0	TX_RX_ FIFO_EN	TX and RX FIFO Enable 0: Disable the transmit and receive FIFO (default) 1: Enable the transmit and receive FIFOs This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.	W	0

Table 5-41 : FCR – FIFO Control Register (0x002, 0x202, …, 0xE02)

Trigger Table	FCTR		FCR				RX FIFO Trigger Level	TX FIFO Trigger Level
	Bit-7	Bit-6	Bit-7	Bit-6	Bit-5	Bit-4		
Table A	0	0			0	0		1
			0	0			1	
			0	1			4	
			1	0			8	
			1	1			14	
Table B	0	1			0	0		16
					0	1		8
					1	0		24
					1	1		30
			0	0			8	
			0	1			16	
			1	0			24	
			1	1			28	
Table C	1	0			0	0		8
					0	1		16
					1	0		32
					1	1		56
			0	0			8	
			0	1			16	
			1	0			56	
			1	1			60	
Table D	1	1	X	X	X	X	Programmable (RXTRG)	Programmable (TXTRG)

Table 5-42 : Transmit & Receive FIFO Trigger Level Selection

Trigger tables A-C are providing pre-defined trigger levels while trigger table D is user programmable. FCTR bits 7-6 are selecting the trigger table. FCR bits 7-4 are selecting the pre-defined trigger levels for the selected trigger table (only for trigger tables A-C).

The transmit interrupt is generated (when enabled) when the TX FIFO level falls below the selected TX trigger level (or when the TX FIFO becomes empty).

The receive interrupt is generated (when enabled) when the RX FIFO level reaches the RX FIFO trigger level. When RTS# flow control is enabled, the RTS# output is set high (telling the remote transmitter to hold the transmission) when the RX FIFO level reaches the next upper RX FIFO trigger level (or the RX FIFO trigger level in case there is no next upper trigger level). The RTS# output is set low again (telling the remote transmitter to resume transmission) when the RX FIFO level falls below the next lower RX FIFO trigger level (or when the RX FIFO becomes empty in case there is no next lower trigger level).

E.g. if Table C is used with RX FIFO trigger level set to 56 characters, the RTS/DTR# output will de-assert at RX FIFO level 60 and re-assert at RX FIFO level 16 – 1.

5.4.8 LCR – Line Control Register

The Line Control Register is mainly used to specify the asynchronous data communication format.

Characters are transmitted and expected to be received in the form:

Start-Bit (Low), 5-to-8 Character-Bits, Parity-Bit (Optional), Stop-Bit(s) (High)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>7</td><td>BRD_
DIV_EN</td><td>Baud Rate Divisors Access Enable
Baud rate generator divisor (DLL/DLM) access enable.
0: THR/RHR registers and IER register are selected (default)
1: Divisor latch registers are selected</td><td>R/W</td><td>0</td></tr>
<tr><td>6</td><td>TX_BRK_EN</td><td>Transmit Break Enable (Transmitter)
When enabled the Break control bit causes a break condition to be transmitted, meaning that the TX output is forced to a “space" (LOW state).
This condition remains until the bit is cleared.
0: No TX break condition (default)
1: Forces the transmitter output (TX) to a “space” (Low), for alerting the remote receiver</td><td>R/W</td><td>0</td></tr>
<tr><td>5:3</td><td>PAR_SEL</td><td>Parity Bit Select (Transmitter & Receiver)
<table><tr><th>5:3</th><th>Parity Selection</th></tr><tr><td>xx0</td><td>No parity</td></tr><tr><td>001</td><td>Odd parity</td></tr><tr><td>011</td><td>Even parity</td></tr><tr><td>101</td><td>Force parity to mark (‘1’)</td></tr><tr><td>111</td><td>Force parity to space (‘0’)</td></tr></table></td><td>R/W</td><td>000</td></tr>
<tr><td>2</td><td>SBL_SEL</td><td>Stop-Bit Length Select (Transmitter & Receiver)
The length of the stop bit is associated with the programmed word length.
<table><tr><th>2</th><th>Word Length</th><th>Stop Bit Length (Bit Time(s))</th></tr><tr><td>0</td><td>5, 6, 7, 8</td><td>1 (default)</td></tr><tr><td>1</td><td>5</td><td>1.5</td></tr><tr><td>1</td><td>6, 7, 8</td><td>2</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>1:0</td><td>WLEN_SEL</td><td>Word Length Select (Transmitter & Receiver)
These bits specify the word length (in bits) to be transmitted or received. Characters are LS-bit aligned in a data byte.
<table><tr><th>1:0</th><th>Word Length (Bits)</th></tr><tr><td>00</td><td>5 (default)</td></tr><tr><td>01</td><td>6</td></tr><tr><td>10</td><td>7</td></tr><tr><td>11</td><td>8</td></tr></table></td><td>R/W</td><td>00</td></tr>
</table>

Table 5-43 : LCR – Line Control Register (0x003, 0x203, …, 0xE03)

5.4.9 MCR – Modem Control Register

The MCR register is used for controlling the modem interface signals or general purpose inputs/outputs.

Bit	Symbol	Description	Access	Reset Value
7	BRG_ PRSCL_SEL	EFR[4] must be set to modify this bit. 0: Direct The primary input clock is fed directly to the programmable Baud Rate Generator. 1: Divide by four The primary input clock is pre-divided by four and then fed to the programmable Baud Rate Generator.	R/W(*)	0
6	RSV	Reserved	-	0
5	XON_ ANY_EN	EFR[4] must be set to modify this bit. 0: Disable Xon-Any function (for 16C550 compatibility) (default) 1: Enable Xon-Any function In this mode any RX character received will enable Xon, resuming data transmission in Auto SW Flow Control Mode.	R/W(*)	0
4	LOOPBACK_ MODE_EN	Internal Loopback Mode Enable 0: Disable internal loopback (default) 1: Enable internal loopback The loopback mode facilitates a near-end data transfer without any output activity. For that, all UART inputs (RX, CTS#, DSR#, RI# and CD#) are disconnected from their regular input pins. All outputs are switched to static HIGH levels (TX, RTS# and DTR#). Corresponding I/O's are internally connected (TX to RX, RTS# to CTS#, DTR# to DSR#) while enhanced functionality inputs are connected to register bits OP1 (RI#) and OP2 (CD#).	R/W	0
3	OP2	(Output 2) Not available as an output. Controls the CD# input status in Internal Loopback Mode.	R/W	0

2	RTS_DTR_ AFC_MODE (OP1)	RTS# or DTR# Automatic Flow Control Mode This bit is only effective when auto RTS/DTR is enabled by EFR bit-6. RTS# selection is associated with CTS# and DTR# selection is associated with DSR#. 0: RTS# pin is used for Automatic Hardware Flow Control Mode 1: DTR# pin is used for Automatic Hardware Flow Control Mode Additionally this bit (as Output 1) controls the RI# input status in Internal Loopback Mode.	R/W	0
1	RTS_ OUT	RTS# Output The RTS# output may be used for automatic hardware flow control by enabling EFR bit-6 and MCR bit-2 = 0. The RTS# output must be asserted (LOW) before the auto RTS can take effect. If the modem interface is not used, this output may be used for general purpose. 0: Force RTS# output HIGH (default) 1: EFR bit-6 = 1 AND MCR bit-2 = 0: RTS# output is under auto control 1: EFR bit-6 = 0 OR MCR bit-2 = 1: Force RTS# output LOW	R/W	0
0	DTR_ OUT	DTR# Output The DTR# output may be used for automatic hardware flow control by enabling EFR bit-6 and MCR bit-2 = 1. The DTR# output must be asserted (LOW) before the auto DTR can take effect. If the modem interface is not used, this output may be used for general purpose. 0: Force DTR# output HIGH (default) 1: EFR bit-6 = 1 AND MCR bit-2 = 1: DTR# output is under auto control 1: EFR bit-6 = 0 OR MCR bit-2 = 0: Force DTR# output LOW	R/W	0

Table 5-44 : MCR – Modem Control Register (0x004, 0x204, …, 0xE04)

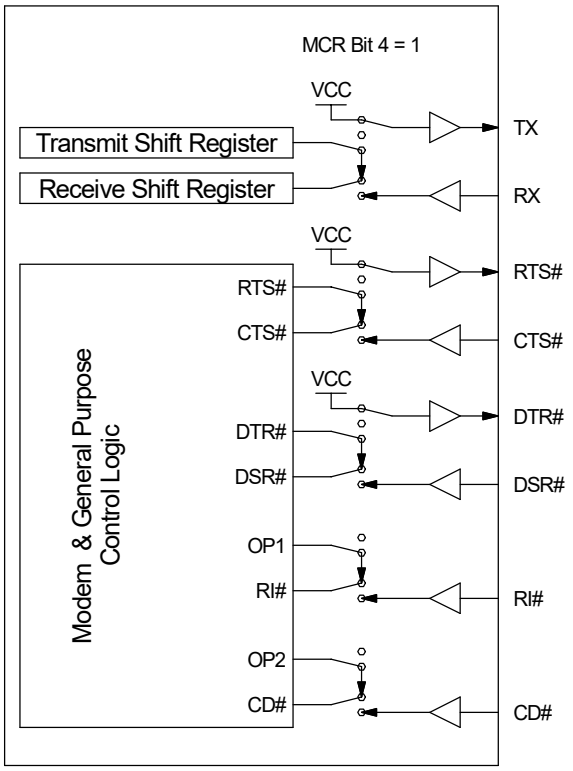

Figure 5-1 : Internal Loopback Connections

5.4.10 LSR – Line Status Register

This register provides status information. Reading the LSR will clear LSR bits 4-1.

Bit	Symbol	Description	Access	Reset Value
7	RX_ FIFO_ DATA_ ERR	Receive FIFO Data Error 0: No FIFO error (default) 1: FIFO contains receive data with error(s) At least one or more parity error, framing error or break indication is in the FIFO data. This bit clears when there are no more errors in the RX FIFO.	R	0
6	TSR_ EMPTY	Transmit Shift Register Empty This bit indicates a Transmit Shift Register (TSR) empty condition. The bit is set to a logic 1 whenever the transmitter goes idle (THR and TSR are both empty). It is cleared to logic 0 whenever either the THR or TSR contains data. In FIFO mode this bit is set to logic 1 whenever the transmit FIFO and transmit shift register are both empty.	R	1
5	THR_ EMPTY	This bit is the Transmit FIFO Empty indicator. This bit is set to a logic HIGH when the last data byte is transferred from the transmit FIFO to the transmit shift register. The bit is reset to logic 0 as soon as a data byte is loaded into the transmit FIFO. In the non-FIFO mode this bit is set when the transmit holding register (THR) is empty; it is cleared when at a byte is written to the THR.	R	1

Bit	Symbol	Description	Access	Reset Value
4	RX_ BRK_ DET	Receive Break Detected 0: No break condition detected (default) 1: Break condition detected (RX was a logic 0 for one data frame time). Only one break character (all-zeroes) per break condition is loaded to the FIFO. This bit is cleared by reading the LSR	R	0
3	RX_ DATA_ FERR	Receive Data Framing Error 0: No framing error (default) 1: Framing error The receive data did not have a valid stop bit(s). This error is associated with the data available for reading in the RHR. This bit is cleared by reading the LSR	R	0
2	RX_ DATA_ PERR	Receive Data Parity Error 0: No parity error (default) 1: Parity error The receive data in the RHR does not have correct parity information. This error is associated with the data available for reading in the RHR. This bit is cleared by reading the LSR	R	0
1	RX_ OVER RUN_ ERR	Receiver Overrun Error 0: No overrun error (default) 1: Overrun error In FIFO mode, this error occurs when additional data arrives while the RX FIFO is full. The new receive data is discarded. In Non-FIFO mode, this error occurs when additional data arrives while the RHR is still loaded. The RHR is overwritten with the new receive data. This bit is cleared after LSR is read.	R	0
0	RX_ DATA_ RDY	Receive Data Valid (Receive Data Ready) 0: No valid data in receive holding register or FIFO (default) 1: Valid receive data is available in the receive holding register or FIFO	R	0

Table 5-45 : LSR – Line Status Register (0x005, 0x205, …, 0xE05)

5.4.11 MSR – Modem Status Register

Only read-accessible (same address/offset as the RS485 Direction Control Register).

This register provides the current state of the modem interface signals, or other peripheral device signals that are connected to the UART I/O.

Bit	Symbol	Description	Access	Reset Value
7	CD_ STAT	CD Input Status This bit represents the compliment of the CD# input (the bit is set when CD# is low). In loopback mode this bit reflects bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.	R	-
6	RI_ STAT	RI Input Status This bit represents the compliment of the RI# input (the bit is set when RI# is low). In loopback mode this bit reflects bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.	R	-
5	DSR_ STAT	DSR Input Status DSR# input may function as automatic hardware flow control signal if enabled and selected by Automatic CTS/DSR (EFR bit-7) and DTR/DSR flow control select (MCR bit-2). Automatic DSR flow control allows starting and stopping local data transmissions based on the DSR# signal. A logic 1 on the DSR# input will stop the transmitter as soon as the current transmission has finished, and a logic 0 will resume data transmission. If automatic hardware flow control is not used, this bit represents the compliment of the DSR# input (the bit is set when DSR# is low). In loopback mode, this bit reflects the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.	R	-
4	CTS_ STAT	CTS Input Status CTS# input may function as automatic hardware flow control signal if it is enabled and selected by Automatic CTS/DSR (EFR bit-7) and RTS/CTS flow control select (MCR bit-2). Automatic CTS flow control allows starting and stopping local data transmissions based on the CTS# signal. A logic 1 on the CTS# input will stop the transmitter as soon as the current transmission has finished, and a logic 0 will resume data transmission. If automatic hardware flow control is not used, this bit represents the compliment of the CTS# input (the bit is set when CTS# is low). In loopback mode, this bit reflects the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.	R	-
3	CD_ CHG_DET	Delta CD# Input Status 0: No change on CD# input (default) 1: The CD# input has changed state since the last time it was monitored. The bit is automatically cleared when read. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).	R	0

Bit	Symbol	Description	Access	Reset Value
2	RI_ CHG_DET	Delta RI# Input Status 0: No change on RI# input (default) 1: The RI# input has changed state since the last time it was monitored. The bit is automatically cleared when read. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).	R	0
1	DSR_ CHG_DET	Delta DSR# Input Status 0: No change on DSR# input (default) 1: The DSR# input has changed state since the last time it was monitored. The bit is automatically cleared when read. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).	R	0
0	CTS_ CHG_DET	Delta CTS# Input Status 0: No change on CTS# input (default) 1: The CTS# input has changed state since the last time it was monitored. The bit is automatically cleared when read. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).	R	0

Table 5-46 : MSR – Modem Status Register (0x006, 0x206, …, 0xE06)

5.4.12 RS485 – Direction Control Delay Register

Only write-accessible (same address/offset as the MSR Register).

This registers contains additional control values for the AUTO RS485 Mode (see FCTR bit 5).

Note that the TPMC461 does not support/feature any RS485 mode.

Bit	Symbol	Description	Access	Reset Value
7:4	AUTO_ RS485_ DLY	AUTO RS485 Direction Control Delay Only writeable/configurable while EFR[4] = 1. Used in conjunction with FCTR[5] (AUTO RS485 Enable). In AUTO RS485 Mode, the RTS# signal indicates the data direction (0 for receive/default direction and 1 for transmit direction). RS485 transceivers typically feature DE (active high driver enable) and RE# (active low receiver enable) direction control inputs. In Auto RS485 mode the RTS# signal is intended to be connected to both of these control inputs of the RS485 transceiver. In Auto RS485 mode the RTS# signal is low by default (receive direction). RTS# is automatically set high (transmit direction) approx. 1 bit time before the start-bit is transmitted. The Auto RS485 Direction Control Delay selects the bit-time delay after the end of the last stop-bit of the last transmitted character before changing the state of RTS# back to low again (receive direction). Value specifies the Delay in Data Bit(s) Time.	W	0x0
3:0	-	Reserved	W	0x0

Table 5-47 : RS485 – Direction Control Delay Register (0x006, 0x206, …, 0xE06)

5.4.13 SPR – Scratch Pad Register

This is an 8-bit general purpose read/write register for storing temporary data.

Bit	Symbol	Description	Access	Reset Value
7:0	USR_ DATA	General User Data	R/W	0xFF

Table 5-48 : SPR – Scratch Pad Register (0x007, 0x207, …, 0xE07)

5.4.15 FCTR – Feature Control Register

Bit	Symbol	Description	Access	Reset Value
7:6	RX_TX_ FIFO_ TRGTBL_ SEL	RX and TX FIFO Trigger-Table Select These bits select either of the transmit and receive FIFO trigger level tables A, B, C or D. When table A, B, or C is selected, the automatic RTS flow control trigger level is set to "next FIFO trigger level " for compatibility to ST16C550 and ST16C650 series. RTS#/DTR# triggers on the next RX FIFO Trigger Level (one FIFO level above or one FIFO level below). Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side. See FCR Register description for more trigger table/level information.	R/W	00
5	AUTO_ RS485_ EN	Automatic RS485 Enable Automatic RS485 half-duplex direction control. 0: Standard Mode RTS#/DTR# output is either used by Auto HW Flow Control or as a general purpose output. In Non-FIFO Mode, the Transmitter generates an interrupt in case its transmit holding register (THR) becomes empty. The transmit shift register (TSR) may still be shifting data bit out. 1: Auto RS485 Half-Duplex Direction Control Mode RTS#/DTR# output indicates data direction. The RTS#/DTR# output is set LOW when the last stop bit of the TSR register has been send and the THR or TX FIFO are empty. It is set to HIGH when a data byte is loaded into the THR or transmit FIFO. The change to HIGH occurs prior to sending the start-bit. In Non-FIFO Mode, it also changes the transmit interrupt generation from THR empty to TSR empty (see IER bit-1). **Not applicable with the TPMC461!**	R/W	0
4	RSV	Reserved	-	0
3:0	RTS_DTR_ AFC_HYST_ SEL	RTS/DTR Automatic Flow Control Hysteresis Select These bits select the automatic RTS/DTR flow control hysteresis when the Transmit and Receive FIFO Trigger-Table D is selected (FCTR bit-6 and bit-7). The RTS/DTR hysteresis is referenced to the configured/programmed RX FIFO trigger level. RTS#/DTR# is asserted (low), when the RX FIFO level reaches the RX trigger level + hysteresis (or when the RX FIFO is full). RTS#/DTR# is de-asserted (high), when the RX FIFO level falls below RX trigger level + hysteresis (or when the RX FIFO is empty). After reset, the next upper/lower RX FIFO trigger level triggers for hardware flow control. See table below.	R/W	0000

Table 5-49 : FCTR – Feature Control Register (0x008, 0x208, …, 0xE08)

FCTR Bit Encoding				RTS/DTR Hysteresis (Characters)
3	**2**	**1**	**0**	
0	0	0	0	0 (next upper/lower RX FIFO trigger level)
0	0	0	1	±4
0	0	1	0	±6
0	0	1	1	±8
0	1	0	0	±8
0	1	0	1	±16
0	1	1	0	±24
0	1	1	1	±32
1	1	0	0	±12
1	1	0	1	±20
1	1	1	0	±28
1	1	1	1	±36
1	0	0	0	±40
1	0	0	1	±44
1	0	1	0	±48
1	0	1	1	±52

Table 5-50 : Hysteresis Levels for Receive FIFO Trigger Level Selection Table D

5.4.16 EFR – Enhanced Feature Register

Enhanced features are enabled or disabled using this register.

Bit	Symbol	Description	Access	Reset Value
7	CTS_DSR_ AFC_EN	Auto CTS (or DSR) Flow Control Enable 0: Automatic CTS/DSR Flow Control is disabled 1: Enable Automatic CTS/DSR Flow Control Automatic CTS/DSR Flow Control: Transmission stops when CTS#/DSR# pin is High. Transmission resumes when CTS#/DSR# pin is Low. Selection for CTS# or DSR# is by MCR bit-2.	R/W	0
6	RTS_DTR_ AFC_EN	Auto RTS (or DTR) Flow Control Enable 0: Automatic RTS/DTR Flow Control is disabled 1: Enable Automatic RTS/DTR Flow Control Automatic RTS/DTR Flow Control: An interrupt will be generated when the receive FIFO is filled to the programmed trigger level and the RTS#/DTR# pin de-asserts High at the next upper trigger or selected hysteresis level. RTS#/DTR# pin returns Low when the receive FIFO level falls below the next lower trigger level or selected hysteresis level (see FCTR bits 4-7). Selection for RTS# or DTR# is by MCR bit-2. RTS#/DTR# pin will function as a general purpose output when RTS/DTR flow control is disabled.	R/W	0
5	RX_SCHR_ DET_EN	Special Character Detect Enable 0: Special Character Detect Disabled 1: Special Character Detect Enabled Special Character Detect: The UART compares each incoming character with the data in the Xoff-2 register. If a match exists, the received data will be transferred to the FIFO and (if enabled via IER bit 5) ISR bit-4 will be set to indicate special character detection. If software flow control is set for comparing Xon1, Xoff1 (EFR[1:0] = “10”) then flow control and special character work normally. If software flow control involves comparing Xoff2 (EFR[1:0] = “01” and “11”) then flow control works normally, but Xoff2 (special character) will not go to the FIFO and will generate an Xoff interrupt and a special character interrupt.	R/W	0
4	ENH_ FUNCBIT_ EN	Enhanced Function Bits Enable 0: Disables/Latches modification of enhanced register bit functions 1: Enables modification of enhanced register bit functions. Enables the functions in IER bits 5-7, FCR bits 4-5, MCR bits 5-7 and MSR bits 4-7 to be modified. After modifying any enhanced register bits, EFR bit-4 can be (re-) set 0 to latch the new values.	R/W	0

Bit	Symbol	Description	Access	Reset Value
3:0	SFC_ MODE_ SEL	Software Flow Control (SFC) Select See table below. Note : It is recommended to clear these bits before a new setting is programmed. The XOFF1/XOFF2 characters are transmitted when the RX FIFO Count Level has reached the RX trigger level, irrespective of which trigger table is used (Trigger Tables A-D). The XON1/XON2 characters are transmitted when the RX FIFO Count Level falls below the next lower trigger level for Trigger Tables A-C and are transmitted when the RX FIFO Count Level falls below the RX trigger level – hysteresis level for Trigger Table D. Example: If Trigger Table D is used with an RX trigger level of 56 and a hysteresis level of 16, the XON1/XON2 characters are sent when the RX FIFO Count Level falls below 40.	R/W	0000

Table 5-51 : EFR – Enhanced Feature Register (0x009, 0x209, …, 0xE09)

TX S/W Flow Control		Rx S/W Flow Control		Software Flow Control (SFC) Function
EFR SFC Bit Encoding				
3	2	1	0	
0	0	X	X	No Transmit Flow Control
0	1	X	X	Transmit Xon2, Xoff2
1	0	X	X	Transmit Xon1, Xoff1
1	1	X	X	Transmit Xon1 and Xon2, Xoff1 and Xoff2
X	X	0	0	No Receive Flow Control
X	X	0	1	Receiver compares Xon2, Xoff2
X	X	1	0	Receiver compares Xon1, Xoff1
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	0	1	1	No Transmit Flow Control Receiver compares Xon1 and Xon2, Xoff1 and Xoff2 (must be consecutive with Xon1/Xoff1 first)
1	1	1	1	Transmit Xon1 and Xon2, Xoff1 and Xoff2 Receiver compares Xon1 and Xon2, Xoff1 and Xoff2 (must be consecutive with Xon1/Xoff1 first)

Table 5-52 : Software Flow Control Functions

Also see chapter *Functional Notes*.

5.4.17 TXCNT – Transmit FIFO Level Counter Register

The Transmit FIFO Level Counter indicates the number of characters in the transmit FIFO. Should be read until the same value is returned twice.

Bit	Symbol	Description	Access	Reset Value
7:0	TX_FIFO_ LVLCNT	Transmit FIFO Level Byte Count This value gives an indication of the number of characters currently in the transmit FIFO. The value range is from 0x00 (0) to 0x40 (64). Due to the dynamic nature of the FIFO counters, this register should be read until the same value is returned twice.	R	0

Table 5-53 : TXCNT – Transmit FIFO Level Counter Register (0x00A, 0x20A, …, 0xE0A)

5.4.18 TXTRG – Transmit FIFO Trigger Level Register

The value written to this registers sets the TX FIFO trigger level when Trigger Tabel D is used. Only valid for Trigger Table D.

A transmit interrupt is generated (once) when the transmit FIFO level falls below the trigger level and/or (once) when the transmit FIFO level changes to 0 (empty). The interrupt is cleared by reading the ISR register.

Bit	Symbol	Description	Access	Reset Value
7:0	TX_FIFO_ TRGLVL	Transmit FIFO Trigger Level This value sets the TX FIFO trigger level when using trigger table D (see FCTR register). The value range is from 0x00 (zero) to 0x40 (64). An interrupt might be generated when the data level in the transmit FIFO is or falls below the preset trigger level.	W	0

Table 5-54 : TXTRG – Transmit FIFO Trigger Level Register (0x00A, 0x20A, …, 0xE0A)

5.4.19 RXCNT – Receive FIFO Level Counter Register

The Receive FIFO Level Counter indicates the number of characters in the receive FIFO. Should be read until the same value is returned twice.

Bit	Symbol	Description	Access	Reset Value
7:0	RX_FIFO_ LVLCNT	Receive FIFO Level Byte Count This value gives an indication of the number of characters currently in the receive FIFO. The value range is from 0x00 (0) to 0x40 (64). Due to the dynamic nature of the FIFO counters, this register should be read until the same value is returned twice.	R	0

Table 5-55 : RXCNT – Receive FIFO Level Counter Register (0x00B, 0x20B, …, 0xE0B)

5.4.20 RXTRG – Receive FIFO Trigger Level Register

The value written to this registers sets the RX FIFO trigger level when Trigger Tabel D is used. Only valid for Trigger Table D.

A receive interrupt is generated when the receive FIFO level reaches the trigger level. The interrupt is cleared by reading data until the receive FIFO level falls below the trigger level.

Bit	Symbol	Description	Access	Reset Value
7:0	RX_FIFO_ TRGLVL	Receive FIFO Trigger Level This value sets the RX FIFO trigger level when using trigger table D (see FCTR register). The value range is from 0x00 (zero) to 0x40 (64). An interrupt might be generated whenever the data level in the receive FIFO rises to the preset trigger level.	W	0

Table 5-56 : RXTRG – Receive FIFO Trigger Level Register (0x00B, 0x20B, …, 0xE0B)

5.4.21 Xchar – XCharacter Status Register

Bit	Symbol	Description	Access	Reset Value
7:2	-	Reserved	R	0
1	XON_DET	Indicates whether the most recent Software Flow Control character/pattern reception was an Xon Status is cleared by reading (or by Xoff reception). XON/XOFF characters/patterns must alternate to trigger a next detection. 0 when Software Flow Control is disabled	R	0
0	XOFF_DET	Indicates whether the most recent Software Flow Control character/pattern reception was an Xoff Status is cleared by reading (or by Xon reception). XON/XOFF characters/patterns must alternate to trigger a next detection. 0 when Software Flow Control is disabled	R	0

Table 5-57 : Xchar – XCharacter Status Register (0x00C, 0x20C, …, 0xE0C)

5.4.22 Xoff1 – Xoff Character 1 Register

Bit	Symbol	Description	Access	Reset Value
7:0	XOFF1_ CHR	Software Flow Control Xoff Character 1 See EFR register for Software Flow Control options.	W	0

Table 5-58 : Xoff1 – Xoff Character 1 Register (0x00C, 0x20C, …, 0xE0C)

5.4.23 Xoff2 – Xoff Character 2

Bit	Symbol	Description	Access	Reset Value
7:0	XOFF2_ CHR	Software Flow Control Xoff Character 2 This is also the Special Character compare value (when enabled by EFR[5]). See EFR register for Software Flow Control options.	W	0

Table 5-59 : Xoff2 – Xoff Character 2 Register (0x00D, 0x20D, …, 0xE0D)

5.4.24 Xon1 – Xon Character 1 Register

Bit	Symbol	Description	Access	Reset Value
7:0	XON1_ CHR	Software Flow Control Xon Character 1 See EFR register for Software Flow Control options.	W	0

Table 5-60 : Xon1 – Xon Character 1 Register (0x00E, 0x20E, …, 0xE0E)

5.4.25 Xon2 – Xon Character 2 Register

Bit	Symbol	Description	Access	Reset Value
7:0	XON2_ CHR	Software Flow Control Xon Character 2 See EFR register for Software Flow Control options.	W	0

Table 5-61 : Xon2 – Xon Character 2 Register (0x00F, 0x20F, …, 0xE0F)

6 Functional Notes

6.1 FIFO Trigger Levels

Transmit and Receive FIFO trigger levels are configurable via predefined trigger tables A-C or via programmable trigger table D.

The transmit FIFO trigger level has an impact (only) on transmit interrupt generation.

A transmit interrupt is generated (once) when the TX FIFO level falls below the selected trigger level and (once) when the TX FIFO becomes empty. The transmit interrupt is cleared by reading the ISR.

The receive FIFO trigger level has an impact on both receive interrupt generation and on automatic flow control output signal assertion/de-assertion (i.e. RTS# or DTR# output signal) in Auto HW flow control mode, respectively on XON and XOFF character/pattern transmission (e.g. XON1 and XOFF1 transmission) in Auto SW flow control mode.

A receive interrupt is generated when the RX FIFO level reaches (matches) the selected trigger level. The receive interrupt is cleared when the RF FIFO level falls below the selected trigger level.

6.2 Auto HW Flow Control

Auto HW flow control:

- Typically the signals RTS# (output) and CTS# (input) are used for Auto HW flow control. Alternatively the signals DTR# (output) and DSR# (input) may be used. This is configured via MCR bit-2.
- Auto RTS (DTR) HW flow control: The receiver controls the RTS# (DTR#) output depending on the RX FIFO level. RTS# (DTR#) is set low (active) when the RX FIFO level is considered being low and RTS# (DTR#) is set high when the RX FIFO level is considered being high.
- Typically the RTS# (DTR#) output of a serial port is connected to the CTS# (DSR#) input of the connected (remote) serial port.
- Auto CTS (DSR) HW flow control: The transmitter pauses/holds transmission of the next character when the CTS# (DSR#) input is high and resumes character transmission when the CTS# (DSR#) input is low (again).

In HW flow control mode with trigger tables A-C, the RTS# (DTR#) signal is taken high when the RX FIFO level reaches the next upper trigger level or when it reaches the trigger level in case the selected trigger level is the highest configurable trigger level. The RTS# (DTR#) signal is taken low when the RX FIFO level falls below the next lower trigger level or when the RX FIFO gets empty.

In HW flow control mode with trigger table D, the RTS# signal is taken high when the RX FIFO level reaches the trigger level + hysteresis or when the FIFO gets full. The RTS# signal is taken low when the RX FIFO level falls below the trigger level – hysteresis or when the RX FIFO gets empty. The sum of trigger level + hysteresis level shall not exceed the RX FIFO size (64).

6.3 Auto SW Flow Control

Auto SW flow control:

- Transmitter SW flow control: Transmitter sends XON/XOFF flow control characters/patterns, depending on the channel's RX FIFO level.
- Receiver SW flow control: Receiver checks/compares incoming characters for XON/XOFF flow control characters/patterns and controls the transmitter (or channel state) accordingly (resumes or pauses normal user data transmission).

In SW flow control mode, a channel is either in XON or XOFF state. In XON state, the channel transmits normally. In XOFF state, normal user data transmission is halted/paused until the channel state changes back to XON state.

If enabled, a software flow control interrupt is generated, when the channel state changes from XON to XOFF or vice versa. A software flow control interrupt is cleared by reading the Interrupt Status Register.

In SW flow control mode, XOFF characters/patterns are transmitted when the RX FIFO level has reached the selected trigger level (trigger tables A-D). The trigger level must not exceed the FIFO size (64).

Upon receiving an XOFF character/pattern, a channel's transmitter stops normal data transmission.

When the RX data is read and the RX FIFO level drops low enough, the transmitter sends an XON character/pattern.

Upon receiving an XON character/pattern, a channel's transmitter resumes normal user data transmission.

For trigger tables A-C, XON characters/patterns are transmitted when the RX FIFO level falls below the next lower trigger level or when the RX FIFO gets empty. For trigger table D, XON characters/patterns are transmitted when the RX FIFO level falls below *selected trigger level – hysteresis value* or when the RX FIFO gets empty.

Example (SW flow control): If trigger table D is used with a RX trigger level of 56 and a hysteresis value of 16, XOFF characters/patterns are sent when the RX FIFO level reaches 56 and XON characters/patterns are sent when the RX FIFO level falls below 40.

Sending SW flow control characters always alternates between XOFF and XON characters/patterns, e.g. when an XOFF character has been sent, the receive FIFO level must drop low enough to send out a XON character/pattern, before a next XOFF character/pattern may be sent.

(Active) Software flow control characters/patterns are not stored in the RX FIFO, regardless if the actual reception has an effect on software flow control or not. E.g. when receiving a sequence of XOFF characters/patterns while in XON state (with XonAny mode disabled), only the first XOFF character/pattern has an effect on software flow control, however none of the XOFF characters/patterns are stored in the RX FIFO.

When XonAny mode is enabled, any character reception (including software flow control characters) while the channel is in XOFF state will change the channel state to XON. E.g. a receive sequence of XOFF characters/patterns would toggle the channel state between XON and XOFF when XonAny mode is enabled.

6.4 Software Flow Control, Special Character, XonAny

6.4.1 XON1/XOFF1 Software Flow Control & Special Character (XOFF2)

(Assuming that XON1, XOFF1 and XOFF2 are set to different characters and that the mentioned interrupts and modes are enabled)

In this mode, the software flow control characters XON1 and XOFF1 are not stored into the RX FIFO. A software flow control interrupt is generated, when the channel is in XON state and receives an XOFF1 software flow control character or vice versa. In other words, the software flow control interrupt is generated, when the channel changes its state (XON, XOFF). A software flow control interrupt is cleared by reading the Interrupt Status Register.

When XonAny Mode is enabled, any character reception while the channel is in XOFF state (including the XOFF1 and special character) changes the channel state to XON and generates the software flow control interrupt. All characters except the XON1 and XOFF1 characters are stored in the RX FIFO.

Special Characters are stored in the RX FIFO. A Special character interrupt is generated when a special character is received and the receive character one before has not been the special character. Two consecutive special characters are both stored to the RX FIFO, but only the first will generate the special character interrupt (provided that the character received one before has not been the special character). A special character interrupt is cleared by reading the Interrupt Status Register. A special character interrupt is

also cleared automatically by the next character reception (provided that the character is not a special character, it may be a software flow control character though).

Software Flow Control and Special Character interrupt generation work independently from each other. E.g. when the channel is in XOFF state and XonAny mode is enabled, a special character reception will both change the channel state to XON and generate the Software Flow Control interrupt and will also generate a special character interrupt (provided that the receive character one before was not a special character).

Note that software flow control interrupts have the same interrupt encoding as the special character interrupt, so these two could not be distinguished by looking at the interrupt status (they also share the same interrupt enable bit and the same interrupt status bit in the IER and ISR registers).

6.4.2 XON2/XOFF2 Software Flow Control & Special Character (XOFF2)

This mode operates similar to the XON1/XOFF1 Software Flow Control Mode described above. However, since the Special Character is defined via the same XOFF2 register used as the software flow control XOFF character, there is a slight difference. The main difference is, that the special character(s) (just as the XON2 and XOFF2 software flow control characters) are not stored in the RX FIFO.

In this mode, the software flow control characters XON2 and XOFF2 are not stored into the RX FIFO. Since the Special Character is also defined by the XOFF2 register, the special character is also not stored in the RX FIFO (regardless if the actual XOFF2 reception has an effect on software flow control or not).

An XOFF2 character reception will generate a Special Character Interrupt, provided that the character received one before has been different.

When the channel is in XON state, an XOFF2 reception would generate both a Software Flow Control Interrupt (and a change of state to XOFF) and a Special Character Interrupt.

When the channel is in XOFF state, an XOFF2 reception would generate a Special Character Interrupt if the receive character one before was not a special character (i.e. was different from XOFF2). (Only) when XonAny mode is enabled, the XOFF2 reception would also change to channel's state to XON and would generate a software flow control interrupt.

When XonAny Mode is enabled, any character reception while the channel is in XOFF state (including the XOFF2 = special character) changes the channel state to XON and generates the software flow control interrupt. All characters except the XON2 and XOFF2 characters are stored in the RX FIFO.

6.5 RX Timeout

RX timeout is an additional interrupt source that is (automatically) enabled along with the normal receive data interrupt.

A change of the RX FIFO level (either by character reception or by reading data) clears a pending RX timeout interrupt and forces a re-set/pre-load of the RX timeout counter. When not expired or currently being pre-loaded, the RX timeout counter counts until it expires after approx. 4 character plus 12 data bit times.

When the RX timeout counter expires and the RX FIFO level is *0 < RX FIFO Level (RXCNT) < RX Trigger Level (RXTRG),* the RX timeout interrupt is generated.

When the RX timeout counter expires and the RX FIFO level is *0 (empty) or >= RX Trigger Level (RXCNT)*, the RX timeout interrupt is not generated.

In the Interrupt Enable Register, the RX Timeout Interrupt is enabled along with the normal Receive Data Ready interrupt (shared/common interrupt enable bit). In the Interrupt Status Register, the RX Timeout Interrupt is distinguished from the normal Receive Data Ready Interrupt (different interrupt source encodings).

7 Configuration EEPROM

After power-on or PCI reset, the PCI target loads initial configuration data from the on-board configuration EEPROM.

The configuration EEPROM contains the following configuration data for the PCI Configuration Registers:

- Vendor ID
- Vendor Device ID
- Subsystem Vendor ID
- Subsystem Device ID

EEPROM Offset	PCI Configuration Register	PCI Configuration Register Offset	Value
0x00	Vendor ID	0x02	0x1498
0x01	Device ID	0x00	0x01CD
0x02	Subsystem Vendor ID	0x2E	0x1498
0x03	Subsystem ID	0x2C	s.b.

Table 7-1 : Configuration EEPROM Data (PCI Configuration Registers)

Subsystem ID Value: TPMC461-10R 0x000A
TPMC461-11R 0x000B
TPMC461-12R 0x000C

The EEPROM words following the PCI Configuration Register data contain:

- The module version & revision
- The UART input clock frequency in Hz
- The physical interfaces attached to the serial channels
- The maximum baud rate of the transceivers in bps
- The supported signals for the serial channels

For the physical interfaces and signals applies: Bit 7 of the EEPROM word represents UART channel 7 and bit 0 represents UART channel 0. The appropriate bit is set to ‘1’ for each UART channel supporting the physical interface or signal. Bits 15 to 8 are always ‘0’ here.

EEPROM Offset	Configuration Register	TPMC461-10R	TPMC461-11R	TPMC461-12R
0x04	Module Version	0x0200		
0x05	Module Revision	0x0000		
0x06	EEPROM Revision	0x0002		
0x07	Oscillator Frequency (high)	0x02A3		
0x08	Oscillator Frequency (low)	0x0000		
0x09-0x0F	Reserved	-		
0x10	RS232 Channels	0x00FF	0x0000	0x000F
0x11	RS422 Channels	0x0000	0x00FF	0x00F0
0x12	TTL Channels	0x0000		
0x13	RS485 Full-Duplex Channels	0x0000		
0x14	RS485 Half-Duplex Channels	0x0000		
0x15-0x1E	Reserved	-		
0x1F	Programmable Interfaces	0x0000		
0x20	Max Data Rate RS232 (high)	0x000F		
0x21	Max Data Rate RS232 (low)	0x4240		
0x22	Max Data Rate RS422 (high)	0x0098		
0x23	Max Data Rate RS422 (low)	0x9680		
0x24	Max Data Rate TTL (high)	0x0000		
0x25	Max Data Rate TTL (low)	0x0000		
0x26	Max Data Rate RS485 Full-Duplex (high)	0x0000		
0x27	Max Data Rate RS485 Full-Duplex (low)	0x0000		
0x28	Max Data Rate RS485 Half-Duplex (high)	0x0000		
0x29	Max Data Rate RS485 Half-Duplex (low)	0x0000		
0x2A-0x2F	Reserved	-		
0x30	RXD & TXD Signals	0x00FF		
0x31	RTS & CTS	0x00FF	0x0003	0x000F
0x32	Full Modem	0x0003	0x0000	0x0003
0x33-0x37	Reserved	-		
0x38	Enhanced RTS & CTS (Front or Back I/O only)	0x0000		
0x39	Enhanced Full Modem (Front or Back I/O only)	0x0000		
0x3A	Channels with Enhanced RTS & CTS (RS232 only)	0x0000		
0x3B-0x3F	Reserved	-		

Table 7-2 : Configuration EEPROM Data (Physical Configuration)

The USTAT LED is lit (on) when the Configuration EEPROM values have been loaded after power-up and/or reset.

8 Programming Hints

8.1 Baud Rate Programming

Each of the 8 UART channels features a dedicated programmable Baud Rate Generator (BRG). The BRG input clock can be divided by any divisor from 1 to $2^{16} - 1$. The divisor can be programmed via the UART channel DLM (Divisor Latch MSB) and DLL (Divisor Latch LSB) registers.

An additional *by-4 divider* can be enabled by UART channel MCR register bit-7. After a reset, bit 7 of the MCR register defaults to '0' and the divisor value is 0x0100.

The Baud Rate represents the transmit and receive data rate. Due to the oversampling nature, the receiver's data sample clock is the baud rate clock multiplied by 16 (or 8).

The basic formula for baud rate programming with 16x oversampling is:

$$Baud\ Rate = \frac{44.2368\ MHz}{16 * Divisor * (1 + 3 * MCR[7])}$$

To calculate the divisor value for a given baud rate use following formula:

$$Divisor = \frac{44.2368\ MHz}{16 * Baud\ Rate * (1 + 3 * MCR[7])}$$

Example values for standard baud rates:

Baud Rate MCR[7] = 0	Baud Rate MCR[7] = 1	Divisor	DLM Value	DLL Value
400	100	0x1B00	0x1B	0x00
600	150	0x1200	0x12	0x00
1200	300	0x0900	0x09	0x00
2400	600	0x0480	0x04	0x80
4800	1200	0x0240	0x02	0x40
9600	2400	0x0120	0x01	0x20
19.2k	4800	0x0090	0x00	0x90
38.4k	9600	0x0048	0x00	0x48
57.6k	14.4k	0x0030	0x00	0x30
115.2k	28.8k	0x0018	0x00	0x18
230.4k	57.6k	0x000C	0x00	0x0C
460.8k	115.2k	0x0006	0x00	0x06
921.6k	230.4k	0x0003	0x00	0x03
1.3824M	345.6k	0x0002	0x00	0x02
2.7648M	691.2k	0x0001	0x00	0x01

Table 8-1 : Example Values for Standard Baud Rates

The sampling rate for a UART channel can also be set to 8x (normal operation is 16x) in the 8XMODE register. Transmit and receive data (baud) rates will double when selecting x8 sampling rate!

Note that the maximum supported baud rate for RS232 channels is 921.6 kbps. Therefore the minimum divisor for RS232 channels is 0x0003 (with MCR[7] = 0 and 16x sampling rate).

The maximum achievable baud rate for RS422 channels is 5.5296 Mbps, with divisor 0x0001 and 8x sampling rate.

These steps should be used to program the UART channel DLM & DLL registers:

1. Write 0x80 to the UART channel LCR register (enable access to the DLM & DLL registers)
2. Program the UART channel DLM & DLL registers
3. Write normal operation byte value to the UART channel LCR register

These steps should be used to modify the UART channel MCR register bit 7 (BRG pre-scaler):

1. Set UART channel EFR register bit 4 to ‘1’ (enable modification of MCR register bits 5-7)
2. Modify UART channel MCR register bit 7
3. Set UART channel EFR register bit 4 to ‘0’ (latch modified MCR register setting)

9 I/O Interface Description

Please note that the P14 back I/O connector is always populated and connected to board I/O signals. Do not use the PMC on carrier boards where P14/J14 is reserved for other system signals but PMC I/O. In case ask support for special order/build options without P14 back I/O connector.

Connect channel I/O either to front I/O or P14 back I/O at a time. Do not connect an I/O channel both at front I/O and P14 back I/O at the same time!

RS422 channels feature on-board 120Ω termination resistors on differential inputs. Do not apply additional external termination resistors here!

9.1 Order Options

The following table shows the UART channel I/O interface type for the different TPMC461 order options.

UART Channel	TPMC461-10R		TPMC461-11R		TPMC461-12R	
	RS232	RS422	RS232	RS422	RS232	RS422
0	X			X	X	
1	X			X	X	
2	X			X	X	
3	X			X	X	
4	X			X		X
5	X			X		X
6	X			X		X
7	X			X		X

Table 9-1 : UART Channel I/O Interface vs. Order Option

The following table shows the available UART channel I/O signals for the different TPMC461 order options.

UART Channel	TPMC461-10R		TPMC461-11R		TPMC461-12R	
	Signals	Level	Signals	Level	Signals	Level
0	TXD, RXD, RTS, CTS, DTR, DSR, CD, RI	RS232	TXD+/-, RXD+/-, RTS+/-, CTS+/-	RS422	TXD, RXD, RTS, CTS, DTR, DSR, CD, RI	RS232
1						
2	TXD, RXD, RTS, CTS		TXD+/-, RXD+/-		TXD, RXD, RTS, CTS	
3						
4					TXD+/-, RXD+/-	RS422
5						
6						
7						

Table 9-2 : UART Channel I/O Signals vs. Order Option

Signals that are not available on a channel are hardwired to ‘1’ (not active).

All RS232 channels provide HW Flow Control Signals RTS and CTS. RS232 channels 0 & 1 provide a full modem signal interface. For RS422, only channels 0 & 1 provide HW Flow Control Signals RTS and CTS.

RS422 channels provide on-board 120Ω line termination resistors on differential inputs. Do not apply additional external termination resistors here!

9.2 Front Panel I/O Connector

The TPMC461 front panel I/O connector is a HD50 SCSI-2 type female connector (e.g. AMP# 787395-5).

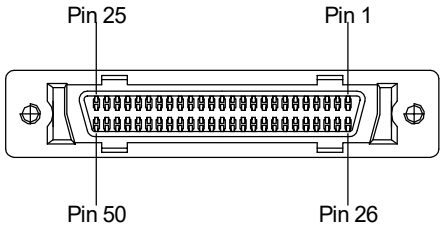

Figure 9-1 : Front I/O Connector Pin Count

9.2.1 TPMC461-10R

Pin	Signal	Direction	Level
1	GND	-	-
2	TXD0	Out	RS232
3	RXD0	In	RS232
4	RTS0	Out	RS232
5	CTS0	In	RS232
6	GND	-	-
7	TXD1	Out	RS232
8	RXD1	In	RS232
9	RTS1	Out	RS232
10	CTS1	In	RS232
11	GND	-	-
12	TXD2	Out	RS232
13	RXD2	In	RS232
14	RTS2	Out	RS232
15	CTS2	In	RS232
16	GND	-	-
17	TXD3	Out	RS232
18	RXD3	In	RS232
19	RTS3	Out	RS232
20	CTS3	In	RS232
21	GND	-	-
22	TXD4	Out	RS232
23	RXD4	In	RS232
24	RTS4	Out	RS232
25	CTS4	In	RS232

Pin	Signal	Direction	Level
26	GND	-	-
27	TXD5	Out	RS232
28	RXD5	In	RS232
29	RTS5	Out	RS232
30	CTS5	In	RS232
31	GND	-	-
32	TXD6	Out	RS232
33	RXD6	In	RS232
34	RTS6	Out	RS232
35	CTS6	In	RS232
36	GND	-	-
37	TXD7	Out	RS232
38	RXD7	In	RS232
39	RTS7	Out	RS232
40	CTS7	In	RS232
41	GND	-	-
42	+5V Termination Supply (fused)		
43	CD0	In	RS232
44	DTR0	Out	RS232
45	RI0	In	RS232
46	DSR0	In	RS232
47	CD1	In	RS232
48	DTR1	Out	RS232
49	RI1	In	RS232
50	DSR1	In	RS232

Table 9-3 : TPMC461-10R Pin Assignment Front Panel I/O Connector

9.2.2 TPMC461-11R

Pin	Signal	Direction	Level
1	GND	-	-
2	TXD0-	Out	RS422
3	TXD0+	Out	RS422
4	RXD0-	In	RS422
5	RXD0+	In	RS422
6	GND	-	-
7	TXD1-	Out	RS422
8	TXD1+	Out	RS422
9	RXD1-	In	RS422
10	RXD1+	In	RS422
11	GND	-	-
12	TXD2-	Out	RS422
13	TXD2+	Out	RS422
14	RXD2-	In	RS422
15	RXD2+	In	RS422
16	GND	-	-
17	TXD3-	Out	RS422
18	TXD3+	Out	RS422
19	RXD3-	In	RS422
20	RXD3+	In	RS422
21	GND	-	-
22	TXD4-	Out	RS422
23	TXD4+	Out	RS422
24	RXD4-	In	RS422
25	RXD4+	In	RS422

Pin	Signal	Direction	Level
26	GND	-	-
27	TXD5-	Out	RS422
28	TXD5+	Out	RS422
29	RXD5-	In	RS422
30	RXD5+	In	RS422
31	GND	-	-
32	TXD6-	Out	RS422
33	TXD6+	Out	RS422
34	RXD6-	In	RS422
35	RXD6+	In	RS422
36	GND	-	-
37	TXD7-	Out	RS422
38	TXD7+	Out	RS422
39	RXD7-	In	RS422
40	RXD7+	In	RS422
41	GND	-	-
42	+5V Termination Supply (fused)		
43	RTS0-	Out	RS422
44	RTS0+	Out	RS422
45	CTS0-	In	RS422
46	CTS0+	In	RS422
47	RTS1-	Out	RS422
48	RTS1+	Out	RS422
49	CTS1-	In	RS422
50	CTS1+	In	RS422

Table 9-4 : TPMC461-11R Pin Assignment Front Panel I/O Connector

9.2.3 TPMC461-12R

Pin	Signal	Direction	Level
1	GND	-	-
2	TXD0	Out	RS232
3	RXD0	In	RS232
4	RTS0	Out	RS232
5	CTS0	In	RS232
6	GND	-	-
7	TXD1	Out	RS232
8	RXD1	In	RS232
9	RTS1	Out	RS232
10	CTS1	In	RS232
11	GND	-	-
12	TXD2	Out	RS232
13	RXD2	In	RS232
14	RTS2	Out	RS232
15	CTS2	In	RS232
16	GND	-	-
17	TXD3	Out	RS232
18	RXD3	In	RS232
19	RTS3	Out	RS232
20	CTS3	In	RS232
21	GND	-	-
22	TXD4-	Out	RS422
23	TXD4+	Out	RS422
24	RXD4-	In	RS422
25	RXD4+	In	RS422

Pin	Signal	Direction	Level
26	GND	-	-
27	TXD5-	Out	RS422
28	TXD5+	Out	RS422
29	RXD5-	In	RS422
30	RXD5+	In	RS422
31	GND	-	-
32	TXD6-	Out	RS422
33	TXD6+	Out	RS422
34	RXD6-	In	RS422
35	RXD6+	In	RS422
36	GND	-	-
37	TXD7-	Out	RS422
38	TXD7+	Out	RS422
39	RXD7-	In	RS422
40	RXD7+	In	RS422
41	GND	-	-
42	+5V Termination Supply (fused)		
43	CD0	In	RS232
44	DTR0	Out	RS232
45	RI0	In	RS232
46	DSR0	In	RS232
47	CD1	In	RS232
48	DTR1	Out	RS232
49	RI1	In	RS232
50	DSR1	In	RS232

Table 9-5 : TPMC461-12R Pin Assignment Front Panel I/O Connector

9.3 Back I/O PMC Connector (P14)

9.3.1 TPMC461-10R

Pin	Signal	Direction	Level
1	GND	-	-
2	TXD0	Out	RS232
3	RXD0	In	RS232
4	RTS0	Out	RS232
5	CTS0	In	RS232
6	GND	-	-
7	TXD1	Out	RS232
8	RXD1	In	RS232
9	RTS1	Out	RS232
10	CTS1	In	RS232
11	GND	-	-
12	TXD2	Out	RS232
13	RXD2	In	RS232
14	RTS2	Out	RS232
15	CTS2	In	RS232
16	GND	-	-
17	TXD3	Out	RS232
18	RXD3	In	RS232
19	RTS3	Out	RS232
20	CTS3	In	RS232
21	GND	-	-
22	TXD4	Out	RS232
23	RXD4	In	RS232
24	RTS4	Out	RS232
25	CTS4	In	RS232
26	GND	-	-
27	TXD5	Out	RS232
28	RXD4	In	RS232
29	RTS4	Out	RS232
30	CTS4	In	RS232
31	GND	-	-
32	TXD6	Out	RS232

Pin	Signal	Direction	Level
33	RXD6	In	RS232
34	RTS6	Out	RS232
35	CTS6	In	RS232
36	GND	-	-
37	TXD7	Out	RS232
38	RXD7	In	RS232
39	RTS7	Out	RS232
40	CTS7	In	RS232
41	GND	-	-
42	+5V Termination Supply (fused)		
43	CD0	In	RS232
44	DTR0	Out	RS232
45	RI0	In	RS232
46	DSR0	In	RS232
47	CD1	In	RS232
48	DTR1	Out	RS232
49	RI1	In	RS232
50	DSR1	In	RS232
51	-	-	-
52	-	-	-
53	-	-	-
54	-	-	-
55	-	-	-
56	-	-	-
57	-	-	-
58	-	-	-
59	-	-	-
60	-	-	-
61	-	-	-
62	-	-	-
63	-	-	-
64	-	-	-

Table 9-6 : TPMC461-10R Pin Assignment Back I/O PMC Connector (P14)

9.3.2 TPMC461-11R

Pin	Signal	Direction	Level
1	GND	-	-
2	TXD0-	Out	RS422
3	TXD0+	Out	RS422
4	RXD0-	In	RS422
5	RXD0+	In	RS422
6	GND	-	-
7	TXD1-	Out	RS422
8	TXD1+	Out	RS422
9	RXD1-	In	RS422
10	RXD1+	In	RS422
11	GND	-	-
12	TXD2-	Out	RS422
13	TXD2+	Out	RS422
14	RXD2-	In	RS422
15	RXD2+	In	RS422
16	GND	-	-
17	TXD3-	Out	RS422
18	TXD3+	Out	RS422
19	RXD3-	In	RS422
20	RXD3+	In	RS422
21	GND	-	-
22	TXD4-	Out	RS422
23	TXD4+	Out	RS422
24	RXD4-	In	RS422
25	RXD4+	In	RS422
26	GND	-	-
27	TXD5-	Out	RS422
28	TXD5+	Out	RS422
29	RXD5-	In	RS422
30	RXD5+	In	RS422
31	GND	-	-
32	TXD6-	Out	RS422

Pin	Signal	Direction	Level
33	TXD6+	Out	RS422
34	RXD6-	In	RS422
35	RXD6+	In	RS422
36	GND	-	-
37	TXD7-	Out	RS422
38	TXD7+	Out	RS422
39	RXD7-	In	RS422
40	RXD7+	In	RS422
41	GND	-	-
42	+5V Termination Supply (fused)		
43	RTS0-	Out	RS422
44	RTS0+	Out	RS422
45	CTS0-	In	RS422
46	CTS0+	In	RS422
47	RTS1-	Out	RS422
48	RTS1+	Out	RS422
49	CTS1-	In	RS422
50	CTS1+	In	RS422
51	-	-	-
52	-	-	-
53	-	-	-
54	-	-	-
55	-	-	-
56	-	-	-
57	-	-	-
58	-	-	-
59	-	-	-
60	-	-	-
61	-	-	-
62	-	-	-
63	-	-	-
64	-	-	-

Table 9-7 : TPMC461-11R Pin Assignment Back I/O PMC Connector (P14)

9.3.3 TPMC461-12R

Pin	Signal	Direction	Level
1	GND	-	-
2	TXD0	Out	RS232
3	RXD0	In	RS232
4	RTS0	Out	RS232
5	CTS0	In	RS232
6	GND	-	-
7	TXD1	Out	RS232
8	RXD1	In	RS232
9	RTS1	Out	RS232
10	CTS1	In	RS232
11	GND	-	-
12	TXD2	Out	RS232
13	RXD2	In	RS232
14	RTS2	Out	RS232
15	CTS2	In	RS232
16	GND	-	-
17	TXD3	Out	RS232
18	RXD3	In	RS232
19	RTS3	Out	RS232
20	CTS3	In	RS232
21	GND	-	-
22	TXD4-	Out	RS422
23	TXD4+	Out	RS422
24	RXD4-	In	RS422
25	RXD4+	In	RS422
26	GND	-	-
27	TXD5-	Out	RS422
28	TXD5+	Out	RS422
29	RXD5-	In	RS422
30	RXD5+	In	RS422
31	GND	-	-
32	TXD6-	Out	RS422

Pin	Signal	Direction	Level
33	TXD6+	Out	RS422
34	RXD6-	In	RS422
35	RXD6+	In	RS422
36	GND	-	-
37	TXD7-	Out	RS422
38	TXD7+	Out	RS422
39	RXD7-	In	RS422
40	RXD7+	In	RS422
41	GND	-	-
42	+5V Termination Supply (fused)		
43	CD0	In	RS232
44	DTR0	Out	RS232
45	RI0	In	RS232
46	DSR0	In	RS232
47	CD1	In	RS232
48	DTR1	Out	RS232
49	RI1	In	RS232
50	DSR1	In	RS232
51	-	-	-
52	-	-	-
53	-	-	-
54	-	-	-
55	-	-	-
56	-	-	-
57	-	-	-
58	-	-	-
59	-	-	-
60	-	-	-
61	-	-	-
62	-	-	-
63	-	-	-
64	-	-	-

Table 9-8 : TPMC461-12R Pin Assignment Back I/O PMC Connector (P14)