The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC533

32x ADC, 16x/0x DAC and 8x Digital I/O

Version 1.0

User Manual

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TPMC533-10R

32 Channels of Simultaneous Sampling Differential 16 bit A/D, 16 Channels of Simultaneous Update Single-Ended 16 bit D/A and 8 Channels of TTL Digital I/O, with HDRA100 front panel I/O

(RoHS compliant)

TPMC533-20R

32 Channels of Simultaneous Sampling Differential 16 bit A/D and 8 Channels of TTL Digital I/O, with HDRA100 front panel I/O

(RoHS compliant)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial issue	December 2017
1.0.1	Power Requirements revised	May 2018
1.0.2	IRQ_ACK_CONF description revised	January 2019
1.0.3	Added chapter *Programming Hints* and sub-chapter *Global DAC Status Register Read*	May 2022

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1 Product Description

The TPMC533 is a standard single-wide PCI Mezzanine Card (PMC) compatible module providing 32 channels of simultaneous sampling true differential bipolar 16bit analog input, 16 or no channels of simultaneous update single-ended unipolar/bipolar 16bit analog output and 8 channels of tri-state 5V-tolerant TTL digital input/output. All signals are accessible through a HDRA100 type front I/O connector.

The PMC-Connectors P11 and P12 provide access to the control logic via a 32bit 33MHz PCI interface.

The ADCs offer true differential inputs with software selectable ±5V and ±10V bipolar input voltage ranges (one common setting for all eight channels of each ADC). The maximum sample rate of the ADCs is 200kSPS and they offer an oversampling capability with digital filter.

The DACs offer software selectable 0-5V, 0-10V, 0-10.8V, ±5V, ±10V and ±10.8V output voltage ranges (individual setting for each of the four channels of each DAC). The settling time is typically 10µs and the DAC channels are capable to drive a load of 2kΩ, with a capacitance up to 4000pF.

Each TPMC533 is factory calibrated. The correction data is stored in an on-board serial EEPROM unique to each PMC module. These correction values can be used to perform a hardware correction of every analog-to-digital and digital-to-analog conversion. Additionally, measurement data read out of a temperature sensor on-board can be used to compensate temperature dependent errors.

The TPMC533 provides two Sequencers, one for AD Conversions and another one for DA Conversions. To perform periodic simultaneous conversions the conversion rates are programmable and can be output to other modules on PMC Back I/O Connector P14 or Front I/O Connector DIO pins for synchronization purposes. The TPMC533 can also operate as a target which means that the conversion rates can be sourced from P14 or Front I/O, created by another module.

A Frame Trigger signal, which can also either be generated by the TPMC533 and output on P14/Front I/O or generated by other modules and input from P14/Front I/O, can be used to synchronize ADC frames and DAC frames.

The signals on PMC Back I/O Connector P14 are ESD protected and driven or read by tri-state 5V-tolerant TTL buffers.

To be able to collect ADC frames and to output DAC frames the TPMC533 provides input and output FIFOs. Data transfer on the PCI bus is handled by TPMC533 initiated block transfer mode DMA cycles with minimum host/CPU intervention.

The 8 Digital TTL tri-state I/O lines with 4.7kΩ pull resistors are ESD protected. The voltage, the pull resistors are connected to, is programmable by software and can be 3.3V, 5V, GND or floating level (one common setting for all eight Digital I/Os). All 8 DIOs can be programmed whether to have their Digital I/O transmitters enabled or disabled individually per I/O line. The Digital I/O receivers are always enabled, so each DIO level can always be monitored and can generate an interrupt, triggered on rising edge, falling edge or both. Additionally, a debounce filter can be configured to get rid of bounce on the Digital I/O lines.

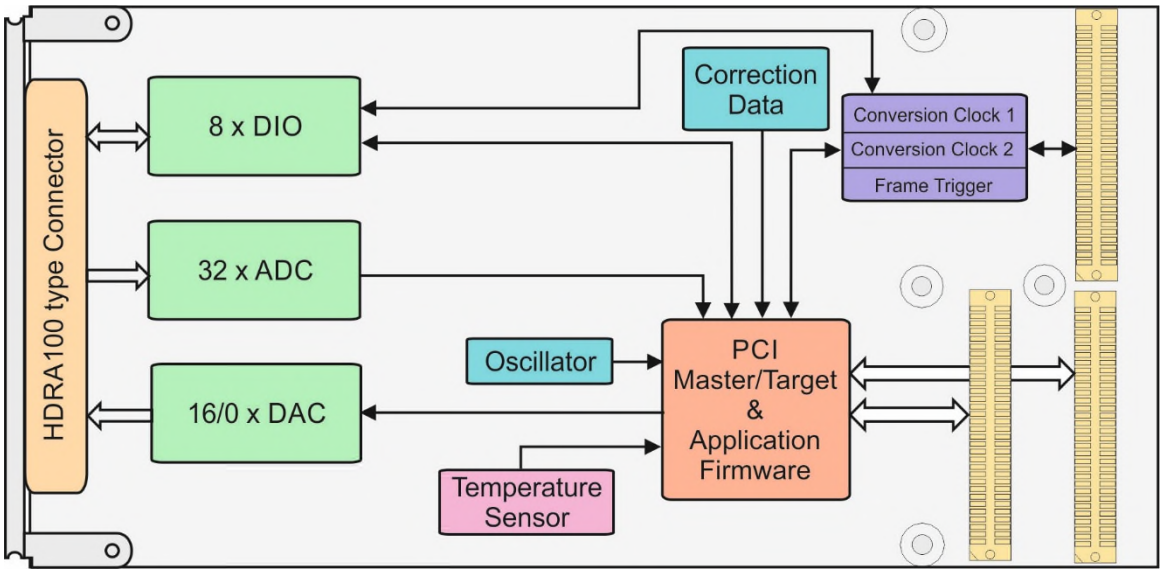


Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Standard single-wide
Electrical Interface	PCI Rev. 3.0 compatible 33MHz / 32bit PCI Initiator/Target 3.3V and 5V PCI Signaling Voltage
On-Board Devices	
FPGA	Spartan-6 (Xilinx)
ADC	AD7609 (Analog Devices)
DAC	AD5754R (Analog Devices)
Digital I/O	74LVT126 (NXP)
Non-Volatile Memory	
FPGA Configuration: 32 Mbit Serial Flash	W25Q32JV (Winbond)
Correction Data: 16 Kbit Serial EEPROM	M93C86-W (ST)
ADC Interface	
Number of ADC Channels	32
Input Type	True bipolar differential
Input Voltage Ranges	±5V and ±10V (one common setting for all eight channels of each ADC)
Sample Rate	200kSPS
DAC Interface	
Number of DAC Channels	**TPMC533-10R:** 16 **TPMC533-20R:** 0
Output Type	Unipolar/bipolar single-ended
Output Voltage Ranges	±5V, ±10V, ±10.8V, +5V, +10V and +10.8V (individual setting for each of the four channels of each DAC)
Settling Time	10µs
DIO Interface	
Number of DIO Channels	8
Driver Level	LVTTL (3.3V)
Receiver	5V tolerant
Source Current	15mA
Sink Current	6mA
I/O Connectors	
Front I/O	100-pin HDRA (Honda HDRA-EC100LFDT-SL+ or compatible)
P14 Back I/O	64-pin Mezzanine Connector (Molex 71436-2864 or compatible)

Physical Data		
Power Requirements	550mA max. @ +5V DC (without I/O Load)	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	**TPMC533-10R:** 487000h **TPMC533-20R:** 497000h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	**TPMC533-10R:** 72.8g **TPMC533-20R:** 72.5g	

Table 2-1 : Technical Specification

3 PCI Interface

3.1 Identifiers

Vendor-ID	0x1498 (TEWS TECHNOLOGIES)
Device-ID	0x0215 (TPMC533)
Class Code	0x118000 (Other data acquisition/signal processing controllers)
Subsystem Vendor-ID	0x1498 (TEWS TECHNOLOGIES)
Subsystem Device-ID	0x000A (TPMC533-10R) 0x0014 (TPMC533-20R)

Table 3-1 : PCI Identifier

3.2 PCI Base Address Register Configuration

The two address spaces on the TPMC533 are accessed from the PCI side by addressing two PCI Base Address Registers mapped in the PCI Memory Space.

PCI Base Address Register (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	1024	32	Little	Register Space
1 (0x14)	MEM	2048	32	Little	Correction Data ROM

Table 3-2 : PCI Base Address Registers

3.2.1 Register Space

PCI Base Address Register 0 (Offset 0x10 in PCI Configuration Space).

Offset to BAR0	Description	Size (Bit)
ADC Global Registers		
0x000	Global ADC Control Register	32
0x004	Global ADC Status Register	32
0x008	Reserved	-
0x00C	Reserved	-
ADC Device Registers		
0x010	ADC1 Configuration Register	32
0x014	Reserved	-
0x018	ADC1 Correction Register A	32
0x01C	ADC1 Correction Register B	32
0x020	ADC1 Correction Register C	32
0x024	ADC1 Correction Register D	32
0x028	ADC1 Correction Register E	32
0x02C	ADC1 Correction Register F	32
0x030	ADC1 Correction Register G	32
0x034	ADC1 Correction Register H	32
0x038	ADC1 Data Register A & B	32
0x03C	ADC1 Data Register C & D	32
0x040	ADC1 Data Register E & F	32
0x044	ADC1 Data Register G & H	32
0x048	ADC1 Mode Register	32
0x04C	Reserved	-
0x050	Reserved	-
0x054	ADC2 Configuration Register	32
0x058	Reserved	-
0x05C	ADC2 Correction Register A	32
0x060	ADC2 Correction Register B	32
0x064	ADC2 Correction Register C	32
0x068	ADC2 Correction Register D	32
0x06C	ADC2 Correction Register E	32
0x070	ADC2 Correction Register F	32
0x074	ADC2 Correction Register G	32
0x078	ADC2 Correction Register H	32
0x07C	ADC2 Data Register A & B	32
0x080	ADC2 Data Register C & D	32
0x084	ADC2 Data Register E & F	32

Offset to BAR0	Description	Size (Bit)
0x088	ADC2 Data Register G & H	32
0x08C	ADC2 Mode Register	32
0x090	Reserved	-
0x094	Reserved	-
0x098	ADC3 Configuration Register	32
0x09C	Reserved	-
0x0A0	ADC3 Correction Register A	32
0x0A4	ADC3 Correction Register B	32
0x0A8	ADC3 Correction Register C	32
0x0AC	ADC3 Correction Register D	32
0x0B0	ADC3 Correction Register E	32
0x0B4	ADC3 Correction Register F	32
0x0B8	ADC3 Correction Register G	32
0x0BC	ADC3 Correction Register H	32
0x0C0	ADC3 Data Register A & B	32
0x0C4	ADC3 Data Register C & D	32
0x0C8	ADC3 Data Register E & F	32
0x0CC	ADC3 Data Register G & H	32
0x0D0	ADC3 Mode Register	32
0x0D4	Reserved	-
0x0D8	Reserved	-
0x0DC	ADC4 Configuration Register	32
0x0E0	Reserved	-
0x0E4	ADC4 Correction Register A	32
0x0E8	ADC4 Correction Register B	32
0x0EC	ADC4 Correction Register C	32
0x0F0	ADC4 Correction Register D	32
0x0F4	ADC4 Correction Register E	32
0x0F8	ADC4 Correction Register F	32
0x0FC	ADC4 Correction Register G	32
0x100	ADC4 Correction Register H	32
0x104	ADC4 Data Register A & B	32
0x108	ADC4 Data Register C & D	32
0x10C	ADC4 Data Register E & F	32
0x110	ADC4 Data Register G & H	32
0x114	ADC4 Mode Register	32
0x118	Reserved	-
0x11C	Reserved	-

Offset to BAR0	Description	Size (Bit)
ADC Sequencer Registers		
0x120	ADC Sequencer Control Register	32
0x124	ADC Sequencer Status Register	32
0x128	Reserved	-
0x12C	Number of Conversions Register	32
0x130	Conversion Count Register	32
0x134	FIFO Level Register	32
0x138	Reserved	-
0x13C	Reserved	-
0x140	DMA Buffer Base Address Register	32
0x144	DMA Buffer Length Register	32
0x148	DMA Buffer Next Address Register	32
0x14C	DMA Status Base Address Register	32
0x150	Reserved	-
0x154	Reserved	-
DAC Global Registers		
0x158	Global DAC Control Register	32
0x15C	Global DAC Status Register	32
0x160	Reserved	-
0x164	Reserved	-
DAC Device Registers		
0x168	DAC1 Configuration Register	32
0x16C	Reserved	-
0x170	DAC1 Correction Register A	32
0x174	DAC1 Correction Register B	32
0x178	DAC1 Correction Register C	32
0x17C	DAC1 Correction Register D	32
0x180	DAC1 Data Register A & B	32
0x184	DAC1 Data Register C & D	32
0x188	DAC1 Status Register	32
0x18C	DAC1 Mode Register	32
0x190	Reserved	-
0x194	Reserved	-
0x198	DAC2 Configuration Register	32
0x19C	Reserved	-
0x1A0	DAC2 Correction Register A	32
0x1A4	DAC2 Correction Register B	32
0x1A8	DAC2 Correction Register C	32
0x1AC	DAC2 Correction Register D	32
0x1B0	DAC2 Data Register A & B	32

Offset to BAR0	Description	Size (Bit)
0x1B4	DAC2 Data Register C & D	32
0x1B8	DAC2 Status Register	32
0x1BC	DAC2 Mode Register	32
0x1C0	Reserved	-
0x1C4	Reserved	-
0x1C8	DAC3 Configuration Register	32
0x1CC	Reserved	-
0x1D0	DAC3 Correction Register A	32
0x1D4	DAC3 Correction Register B	32
0x1D8	DAC3 Correction Register C	32
0x1DC	DAC3 Correction Register D	32
0x1E0	DAC3 Data Register A & B	32
0x1E4	DAC3 Data Register C & D	32
0x1E8	DAC3 Status Register	32
0x1EC	DAC3 Mode Register	32
0x1F0	Reserved	-
0x1F4	Reserved	-
0x1F8	DAC4 Configuration Register	32
0x1FC	Reserved	-
0x200	DAC4 Correction Register A	32
0x204	DAC4 Correction Register B	32
0x208	DAC4 Correction Register C	32
0x20C	DAC4 Correction Register D	32
0x210	DAC4 Data Register A & B	32
0x214	DAC4 Data Register C & D	32
0x218	DAC4 Status Register	32
0x21C	DAC4 Mode Register	32
0x220	Reserved	-
0x224	Reserved	-
0x228 to 0x2E4	Reserved	-
DAC Sequencer Registers		
0x2E8	DAC Sequencer Control Register	32
0x2EC	DAC Sequencer Status Register	32
0x2F0	Reserved	-
0x2F4	Number of Conversions Register	32
0x2F8	Conversion Count Register	32
0x2FC	FIFO Level Register	32
0x300	Reserved	-
0x304	Reserved	-
0x308	DMA Buffer Base Address Register	32

Offset to BAR0	Description	Size (Bit)
0x30C	DMA Buffer Length Register	32
0x310	DMA Buffer Next Address Register	32
0x314	Reserved	-
0x318	Reserved	-
0x31C	Reserved	-
Conversion Signals Registers		
0x320	Conversion Clock 1 Generator Register	32
0x324	Conversion Clock 2 Generator Register	32
0x328	Reserved	-
0x32C	Frame Trigger Generator Register 1	32
0x330	Frame Trigger Generator Register 2	32
0x334	Reserved	-
0x338	Reserved	-
0x33C	Conversion Signals Generator Enable Register	32
0x340	Conversion Signals Generator Output Driver Register	32
0x344	Conversion Signals Source Selection Register	32
0x348	Frame Timer Register	32
0x34C	Reserved	-
0x350	Reserved	-
DIO Registers		
0x354	DIO Input Register	32
0x358	DIO Input Filter Debounce Register	32
0x35C	DIO Output Register	32
0x360	DIO Output Enable Register	32
0x364	Reserved	-
0x368	Reserved	-
Interrupt Registers		
0x36C	Interrupt Enable Register	32
0x370	Error Interrupt Enable Register	32
0x374	DIO Rising Edge Interrupt Enable Register	32
0x378	DIO Falling Edge Interrupt Enable Register	32
0x37C	Reserved	-
0x380	Reserved	-
0x384	Interrupt Status Register	32
0x388	Error Interrupt Status Register	32
0x38C	DIO Interrupt Status Register	32
0x390	Reserved	-
0x394	Reserved	-

Offset to BAR0	Description	Size (Bit)
Other Registers		
0x398	Global Configuration Register	32
0x39C	DIO Pull Resistors Register	32
0x3A0	P14 Back I/O Pull Resistors Register	32
0x3A4	Correction Data EEPROM Control/Status Register	32
0x3A8	Temperature Sensor Trigger Register	32
0x3AC	Temperature Sensor Data Register	32
0x3B0 to 0x3F8	Reserved	-
0x3FC	Firmware Version Register	32

Table 3-3 : Register Space

For the TPMC533-20R the DAC Global Registers, DAC Device Registers and DAC Sequencer Registers are reserved.

Register Bit Access Type		Description
R	Read	The bit is readable by software.
R/W	Read/Write	The bit is readable and writeable by software.
R/C	Read/Clear	The bit is readable by software. The bit is set by firmware. Software may clear the bit by writing a '1'.
R/S	Read/Set	The bit is readable by software. Software may set this bit to '1'. The bit is cleared by firmware.

Table 3-4 : Register Bit Access Types

When reading reserved register bits, the value is undefined.

Reserved register bits shall be written as '0'.

3.2.1.1 ADC Global Registers

The following registers exist only once and deal with all ADCs on-board the TPMC533.

3.2.1.1.1 Global ADC Control Register (0x000)

The Global ADC Control Register provides control options for each ADC (for all eight ADC Channels of each ADC) on-board the TPMC533.

Bit	Symbol	Description	Access	Reset Value
31:4	-	Reserved	-	-
3	ADC4_CONV_REQ	ADC4 Conversion Request Refer to the ADC1 Conversion Request bit for description.	R/S	0
2	ADC3_CONV_REQ	ADC3 Conversion Request Refer to the ADC1 Conversion Request bit for description.	R/S	0
1	ADC2_CONV_REQ	ADC2 Conversion Request Refer to the ADC1 Conversion Request bit for description.	R/S	0
0	ADC1_CONV_REQ	ADC1 Conversion Request Write '1' to start the conversion of the eight ADC Channels of ADC1. Before requesting ADC1 Conversion, software should check the ADC1 Busy Bit to be clear in the Global ADC Status Register. This bit is self-clearing. **Note: If ADC1 is configured to operate in Sequencer Mode ADC1 Conversion Requests are ignored.**	R/S	0

Table 3-5 : Global ADC Control Register

3.2.1.1.2 Global ADC Status Register (0x004)

For each ADC (for all eight ADC Channels of each ADC) on-board the TPMC533, status information can be read from this read-only register.

Bit	Symbol	Description	Access	Reset Value
31:4	-	Reserved	-	-
3	ADC4_BUSY	ADC4 Busy Refer to the ADC1 Busy bit for description.	R	0
2	ADC3_BUSY	ADC3 Busy Refer to the ADC1 Busy bit for description.	R	0
1	ADC2_BUSY	ADC2 Busy Refer to the ADC1 Busy bit for description.	R	0
0	ADC1_BUSY	ADC1 Busy Set when • analog sampling is in progress • data is transferred from the ADC If ADC1 Operating Mode is set to "Manual Mode" in the corresponding ADC Mode Register, this bit is set by writing to ADC1_CONV_REQ in the Global ADC Control Register. This bit must be read as '0' before data can be read from the corresponding ADC Data Register.	R	0

Table 3-6 : Global ADC Status Register

3.2.1.2 ADC Device Registers

The following registers exist multiple times and each of the registers deals with a single ADC (eight ADC Channels) on-board the TPMC533.

3.2.1.2.1 ADC Configuration Registers (0x010, 0x054, 0x098 and 0x0DC)

There is a dedicated ADC Configuration Register for each ADC (for all eight ADC Channels of each ADC).

After power-up the ADCs should be configured before switching to Sequencer Mode or using them in Manual Mode.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:4</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>3:1</td><td>ADCx_OS</td><td>Oversampling Ratio
If oversampling is active, the ADC takes multiple samples and averages them. This improves the signal-to-noise ratio. The ADCx_BUSY high time in the Global ADC Status Register is extended until all samples are taken.
Note: If Oversampling is turned on the maximum AD Sample Rate of the ADC is less than 200kSPS.
<table>
<tr><th>OS</th><th>Oversampling Ratio</th></tr>
<tr><td>000</td><td>No Oversampling</td></tr>
<tr><td>001</td><td>2</td></tr>
<tr><td>010</td><td>4</td></tr>
<tr><td>011</td><td>8</td></tr>
<tr><td>100</td><td>16</td></tr>
<tr><td>101</td><td>32</td></tr>
<tr><td>110</td><td>64</td></tr>
<tr><td>111</td><td>Not valid</td></tr>
</table>
When changing the Oversampling Mode, a dummy sample is required to set the ADC to the new Oversampling Ratio.</td><td>R/W</td><td>000</td></tr>
<tr><td>0</td><td>ADCx_IR</td><td>ADC Input Range
This setting describes the allowed input voltage on the ADC Channel± pins. Also see chapter “ADC Data Coding”.
<table>
<tr><th>IR</th><th>Input Voltage Range</th></tr>
<tr><td>0</td><td>±5V</td></tr>
<tr><td>1</td><td>±10V</td></tr>
</table>
Allow a settling time of about 100µs when the ADC input range is changed.</td><td>R/W</td><td>0</td></tr>
</table>

Table 3-7 : ADC Configuration Register

3.2.1.2.2 ADC Correction Registers (0x018, 0x01C, 0x020, 0x024, 0x028, 0x02C, 0x030, 0x034, 0x05C, 0x060, 0x064, 0x068, 0x06C, 0x070, 0x074, 0x078, 0x0A0, 0x0A4, 0x0A8, 0x0AC, 0x0B0, 0x0B4, 0x0B8, 0x0BC, 0x0E4, 0x0E8, 0x0EC, 0x0F0, 0x0F4, 0x0F8, 0x0FC and 0x100)

There are eight dedicated ADC Correction Registers for each ADC (one register for each of the eight ADC Channels of each ADC).

The correction values for the specific ADC Channels and Voltage Ranges must be read from the Correction Data ROM at PCI Base Address Register 1 (BAR1).

After power-up and ADC Configuration the ADC Correction Registers should be written with the values for the desired Voltage Range read from the Correction Data ROM, before switching to Sequencer Mode or using the ADCs in Manual Mode.

Leaving the ADC Correction Registers unmodified at their Reset Value means that ADC Correction is disabled.

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_GAIN_A	Gain Correction Value ADC Channel A	R/W	0x0000
15:0	ADCx_OFFSET_A	Offset Correction Value ADC Channel A	R/W	0x0000

Table 3-8 : ADC Correction Register A

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_GAIN_B	Gain Correction Value ADC Channel B	R/W	0x0000
15:0	ADCx_OFFSET_B	Offset Correction Value ADC Channel B	R/W	0x0000

Table 3-9 : ADC Correction Register B

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_GAIN_C	Gain Correction Value ADC Channel C	R/W	0x0000
15:0	ADCx_OFFSET_C	Offset Correction Value ADC Channel C	R/W	0x0000

Table 3-10: ADC Correction Register C

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_GAIN_D	Gain Correction Value ADC Channel D	R/W	0x0000
15:0	ADCx_OFFSET_D	Offset Correction Value ADC Channel D	R/W	0x0000

Table 3-11: ADC Correction Register D

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_GAIN_E	Gain Correction Value ADC Channel E	R/W	0x0000
15:0	ADCx_OFFSET_E	Offset Correction Value ADC Channel E	R/W	0x0000

Table 3-12: ADC Correction Register E

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_GAIN_F	Gain Correction Value ADC Channel F	R/W	0x0000
15:0	ADCx_OFFSET_F	Offset Correction Value ADC Channel F	R/W	0x0000

Table 3-13: ADC Correction Register F

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_GAIN_G	Gain Correction Value ADC Channel G	R/W	0x0000
15:0	ADCx_OFFSET_G	Offset Correction Value ADC Channel G	R/W	0x0000

Table 3-14: ADC Correction Register G

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_GAIN_H	Gain Correction Value ADC Channel H	R/W	0x0000
15:0	ADCx_OFFSET_H	Offset Correction Value ADC Channel H	R/W	0x0000

Table 3-15: ADC Correction Register H

3.2.1.2.3 ADC Data Registers (0x038, 0x03C, 0x040, 0x044, 0x07C, 0x080, 0x084, 0x088, 0x0C0, 0x0C4, 0x0C8, 0x0CC, 0x104, 0x108, 0x10C and 0x110)

These registers are intended to be used for ADCs operating in Manual Mode (not for Sequencer Mode).

To accelerate data access, each ADC Data Register holds two ADC channel values.

The ADC Data Registers always hold sampled data of the latest conversion.

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_DATA_B	ADC Data ADC Channel B	R/W	0x0000
15:0	ADCx_DATA_A	ADC Data ADC Channel A	R/W	0x0000

Table 3-16: ADC Data Register A & B

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_DATA_D	ADC Data ADC Channel D	R/W	0x0000
15:0	ADCx_DATA_C	ADC Data ADC Channel C	R/W	0x0000

Table 3-17: ADC Data Register C & D

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_DATA_F	ADC Data ADC Channel F	R/W	0x0000
15:0	ADCx_DATA_E	ADC Data ADC Channel E	R/W	0x0000

Table 3-18: ADC Data Register E & F

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_DATA_H	ADC Data ADC Channel H	R/W	0x0000
15:0	ADCx_DATA_G	ADC Data ADC Channel G	R/W	0x0000

Table 3-19: ADC Data Register G & H

3.2.1.2.4 ADC Mode Registers (0x048, 0x08C, 0x0D0 and 0x114)

For each ADC (for all eight ADC Channels of each ADC) it is configurable whether to use the ADC Sequencer to periodically write AD samples into Host RAM or whether AD samples are only read manually from ADC Data Registers.

Bit	Symbol	Description	Access	Reset Value
31:1	-	Reserved	-	-
0	ADCx_MODE	ADC Operating Mode 0: Manual Mode 1: Sequencer Mode This bit sets the general ADC Operating Mode. In Manual Mode, analog sampling is requested by software commands (there is no periodic conversion rate). In Sequencer Mode, analog inputs are sampling periodically at a configurable conversion rate.	R/W	0

Table 3-20: ADC Mode Register

Note that all eight channels of an ADC are always operating in the same Operating Mode.

3.2.1.3 ADC Sequencer Registers

The ADC Sequencer is used to periodically convert analog signals to digital values and write them to Host RAM via DMA transfers at a configurable Conversion Rate.

All ADCs configured to "Sequencer Mode" in their corresponding ADC Mode Registers are always performing their conversions simultaneously.

For each conversion, all eight ADC Channels of each ADC assigned to the ADC Sequencer are sampled.

The ADC Sequencer may operate in Normal Mode or Frame Mode. Normal Mode is used for generating a single block of analog-to-digital conversions or for generating continuous conversions by software request. Frame Mode is used for repetitive blocks of analog-to-digital conversions triggered by a Frame Trigger at a configurable Frame Trigger Rate.

3.2.1.3.1 ADC Sequencer Control Register (0x120)

Bit	Symbol	Description	Access	Reset Value
31:19	-	Reserved	-	-
18	DMA_STAT_ENA	DMA Status Transfer Enable 0: DMA Status Transfer Disabled 1: DMA Status Transfer Enabled If enabled, after a DMA Buffer termination event, the DMA Status is transferred to the Host RAM location configured in the DMA Status Base Address Register.	R/W	0
17	WR_DMA_RESET	DMA Reset Writing '1' to this bit resets the DMA Controller. This bit is self-clearing	R/S	0
16	WR_DMA_ENA	DMA Enable 0: DMA Controller Disabled 1: DMA Controller Enabled Enables the Sequencer's DMA Controller to allow the initiation of DMA transfers by writing to the DMA Buffer Length Register. When being disabled, any active DMA transfer is completed before the DMA Engine enters Idle or Error state. The DMA Controller operation is stopped in case of a DMA Error. In this case the DAC Sequencer Status Register must be read and the DMA Controller can be disabled. The DMA Controller is reset when disabled.	R/W	0
15:9	-	Reserved	-	-
8	ADC_SEQ_FIFO_CLR	FIFO Clear When set to 1, the ADC Sequencer's internal FIFO is cleared. This bit is self-clearing	R/S	0

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>7:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5</td><td>IU_CLK_SRC</td><td>Input Unit Conversion Clock Source
These bits select the Input Unit Conversion Clock signal source. The Input Unit Conversion Clock signal defines the ADC Sequencer’s Conversion Rate.
Note that in Frame Mode, the Input Unit Conversion Clock signal must be phase locked to the Frame Trigger signal.
<table><tr><th>IU_CLK_SRC</th><th>Clock Source</th></tr><tr><td>0</td><td>Conversion Clock 1</td></tr><tr><td>1</td><td>Conversion Clock 2</td></tr></table>
Setting the ADC Sequencer's Conversion Rate to a period shorter than the ADC conversion time (~5µs) is not allowed.
If the Input Unit triggers the next conversion as long as the ADC inputs are still busy performing the previous conversion, conversion is stopped and the CONV_ERR bit in the ADC Sequencer Status Register is set.</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>3</td><td>IU_CONV_START</td><td>Input Unit Start Conversion (Normal Mode)
Set this bit to start a conversion process in Normal Mode.
The FIFO Level may be checked before setting this bit.
This bit is self-clearing</td><td>R/S</td><td>0</td></tr>
<tr><td>2</td><td>IU_MODE</td><td>Input Unit Mode
0: Normal Mode
1: Frame Mode
In Normal Mode, the configured Number of Conversions is performed starting with the next Conversion Clock after the IU_CONV_START bit has been set by software.
In Frame Mode, the configured Number of Conversions is performed starting with the next Conversion Clock after a Frame Trigger occurred.</td><td>R/W</td><td>0</td></tr>
<tr><td>1</td><td>IU_RESET</td><td>Input Unit Reset
Writing '1' to this bit resets the Input Unit.
This bit is self-clearing</td><td>R/S</td><td>0</td></tr>
<tr><td>0</td><td>IU_ENA</td><td>Input Unit Enable
0: Input Unit Disabled
1: Input Unit Enabled
Enables the Input Unit.
The Input Unit handles the ADC Data transfer from the ADCs to the Sequencer's internal FIFO and the ADC Sequencer's Conversion Rate generation.
The Input Unit operation is stopped in case of an Input Unit Error. In this case the ADC Sequencer Status Register must be read and the Input Unit can be disabled.
The Input Unit is reset when disabled.</td><td>R/W</td><td>0</td></tr>
</table>

Table 3-21: ADC Sequencer Control Register

3.2.1.3.2 ADC Sequencer Status Register (0x124)

Bit	Symbol	Description	Access	Reset Value
31:23	-	Reserved	-	-
22:20	WR_DMA_TERM	DMA Buffer Termination After a DMA Buffer was terminated, depending on which bits are set in this array, the reason(s) for the termination are indicated. These bits are automatically cleared when a new DMA Buffer is provided by writing to the DMA Buffer Length Register. Bit 22: Error The Input Unit operation is stopped before the desired Number of Conversions has been performed because a Conversion Error or a FIFO Overflow occurred. Bit 21: Block/Frame End The desired number of samples (configured in the Number of Conversions Register) has been written to DMA Buffers. Bit 20: Buffer End The end of the DMA Buffer was reached (the DMA Buffer is full). A new DMA Buffer must be provided.	R	000
19	-	Reserved	-	-
18	WR_DMA_ERR	DMA Error A PCI Master Abort occurred because the addressed PCI Target did not respond or a PCI Target Abort occurred because the addressed PCI Target detected a fatal error. In case of an error, the DMA Controller operation is automatically stopped. This bit is cleared when the DMA Controller is disabled.	R	0
17	WR_DMA_BUSY	DMA Busy Indicates that the DMA Controller is currently busy (active).	R	0
16	WR_DMA_IDLE	DMA Idle Indicates that the DMA Controller is currently in Idle State. A DMA transfer may be started (a DMA buffer may be provided) by writing to the DMA Buffer Length Register.	R	0

Bit	Symbol	Description	Access	Reset Value
15:7	-	Reserved	-	-
6	IU_FRAME_ERR	Input Unit Frame Error A Frame Trigger event occurs, but the configured Number of Conversions has not been processed so far. In case of this error, the conversion process is terminated (no more conversion pulses are generated) and the Input Unit operation is stopped. This bit is automatically cleared when the Input Unit is disabled.	R	0
5	CONV_ERR	Input Unit Conversion Error The Sequencer Conversion Clock Source requests the next conversion, but the ADCs are still busy performing the conversion process of the previous conversion. In case of this error, the conversion process is terminated (no more conversion pulses are generated) and the Input Unit operation is stopped. This bit is automatically cleared when the Input Unit is disabled.	R	0
4	FIFO_OF	Input Unit FIFO Overflow Error The Input Unit wants to write sampled values from the ADCs to the FIFO but the FIFO is full because AD samples could not be written to Host RAM fast enough. In case of this error, the conversion process is terminated (no more conversion pulses are generated) and the Input Unit operation is stopped. This bit is automatically cleared when the Input Unit is disabled.	R	0
3	-	Reserved	-	-
2	IU_CONV_ACTIVE	Input Unit Conversion Process Active Indicates that the conversion process is active. In Normal Mode, this bit is set when the software sets the Input Unit Start Conversion bit. This bit is cleared when the configured Number of Conversions has been performed. In Frame Mode, this bit is set when a Frame Trigger starts the conversion process (except in a frame error case). This bit is cleared when the configured Number of Conversions has been performed (for a single frame).	R	0
1	-	Reserved	-	-
0	IU_IDLE	Input Unit Idle Indicates that the Input Unit is currently in Idle State.	R	0

Table 3-22: ADC Sequencer Status Register

3.2.1.3.3 Number of Conversions Register (0x12C)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	ADC_SEQ_NUM_CONV	Number of Conversions to be performed Set to '0' for continuous analog-to-digital conversions. Normal Mode: Number of conversions (after IU_CONV_START was set) per requested block of analog-to-digital conversions. When the configured Number of Conversions has been performed, the conversion process is stopped (until software sets the IU_CONV_START bit again) and the IU_CONV_ACTIVE bit in the ADC Sequencer Status Register is cleared. Frame Mode: Number of analog-to-digital conversions per Frame Trigger. When the configured Number of Conversions (per frame) has been performed, the conversion process is stopped (until the next Frame Trigger event occurs) and the IU_CONV_ACTIVE bit in the ADC Sequencer Status Register is cleared.	R/W	0x000 0000

Table 3-23: Number of Conversions Register

Note that every time the ADC Sequencer triggers a conversion, all eight ADC Channels of all ADCs configured to operate in Sequencer Mode are updated simultaneously.

3.2.1.3.4 Conversion Count Register (0x130)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	ADC_SEQ_CONV_COUNT	Number of Conversions that have been performed Normal Mode: The value is automatically reset when the (next) Input Unit Start Conversion is initiated in the ADC Sequencer Control Register. Frame Mode: The value is automatically reset at a Frame Trigger event (except for the case when an Input Unit Frame Error occurred).	R	0x000 0000

Table 3-24: Conversion Count Register

3.2.1.3.5 FIFO Level Register (0x134)

Bit	Symbol	Description	Access	Reset Value
31:0	ADC_SEQ_FIFO_LEVEL	FIFO Level This value shows the current fill level of the Sequencer's internal FIFO. It is measured in number of bytes. (an ADC Data value consists of two bytes)	R	0x0000 0000

Table 3-25: FIFO Level Register

3.2.1.3.6 DMA Buffer Base Address Register (0x140)

Bit	Symbol	Description	Access	Reset Value
31:0	WR_DMA_BUF_ADDR	DMA Buffer Base Address PCI memory mapped base address of the DMA Buffer in Host RAM where sampled ADC Data is written to. The DMA Buffer Base Address is latched when the DMA Buffer Length Register is written.	R/W	0x0000 0000

Table 3-26: DMA Buffer Base Address Register

3.2.1.3.7 DMA Buffer Length Register (0x144)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	WR_DMA_BUF_LEN	DMA Buffer Length Byte Length of the provided DMA Buffer in Host RAM. **A write to the DMA Buffer Length Register initiates the DMA transfer.** The Initiation of DMA transfers is only possible if WR_DMA_IDLE in the ADC Sequencer Status Register is '1'.	R/W	0x0000 0000

Table 3-27: DMA Buffer Length Register

3.2.1.3.8 DMA Buffer Next Address Register (0x148)

Bit	Symbol	Description	Access	Reset Value
31:0	WR_DMA_NEXT_ADDR	DMA Buffer Next Address This register holds the PCI address of the address location in Host RAM the next ADC Data is written to. It can be used to determine how much space is left in the provided DMA Buffer.	R	0x0000 0000

Table 3-28: DMA Buffer Next Address Register

3.2.1.3.9 DMA Status Base Address Register (0x14C)

Bit	Symbol	Description	Access	Reset Value
31:0	DMA_STAT_ADDR	DMA Status Base Address PCI memory mapped base address of the address location in Host RAM the DMA Status information is written to (if enabled) as soon as the processing of a DMA Buffer is done.	R/W	0x0000 0000

Table 3-29: DMA Status Base Address Register

Like the registers of the TPMC533, the DMA Status must be interpreted Little Endian.

Bit	Symbol	Description
31	-	Reserved
30:28	DMA_TERM_STAT	DMA Buffer Termination Status After a DMA Buffer was terminated, depending on which bits are set in this array, the reason(s) for the termination are indicated. Bit 30: Error The Input Unit operation is stopped before the desired Number of Conversions has been performed because a Conversion Error or a FIFO Overflow occurred. Bit 29: Block/Frame End The desired number of samples (configured in the Number of Conversions Register Register) has been written to DMA Buffers. Bit 28: Buffer End The end of the DMA Buffer was reached (the DMA Buffer is full). A new DMA Buffer must be provided.
27:0	DMA_NUM_BYTES	Number of Transferred Bytes

Table 3-30: DMA Status (Host RAM)

3.2.1.4 DAC Global Registers

The following registers exist only once and deal with all DACs on-board the TPMC533.

These Registers are Reserved on TPMC533-20R.

3.2.1.4.1 Global DAC Control Register (0x158)

The Global DAC Control Register provides control options for each DAC (for all four DAC Channels of each DAC) on-board the TPMC533.

Bit	Symbol	Description	Access	Reset Value
31:4	-	Reserved	-	-
3	DAC4_CONV_REQ	DAC4 Conversion Request Refer to the DAC1 Conversion Request bit for description.	R/S	0
2	DAC3_CONV_REQ	DAC3 Conversion Request Refer to the DAC1 Conversion Request bit for description.	R/S	0
1	DAC2_CONV_REQ	DAC2 Conversion Request Refer to the DAC1 Conversion Request bit for description.	R/S	0
0	DAC1_CONV_REQ	DAC1 Conversion Request Write '1' to start the conversion of the four DAC Channels of DAC1. Before requesting DAC1 Conversion, software should check the DAC1 Busy Bit to be clear in the Global DAC Status Register (also see chapter *Programming Hints / Global DAC Status Register Read*!). This bit is self-clearing. **Note: If DAC1 is configured to operate in Sequencer Mode or to operate in Immediate Conversion in Manual Mode, DAC1 Conversion Requests are ignored.**	R/S	0

Table 3-31: Global DAC Control Register

3.2.1.4.2 Global DAC Status Register (0x15C)

For each DAC (for all four DAC Channels of each DAC) on-board the TPMC533, status information can be read from this read-only register.

Bit	Symbol	Description	Access	Reset Value
31:12	-	Reserved	-	-
11	DAC4_SETTLE	DAC4 Settle Refer to the DAC1 Settle bit for description.	R	0
10	DAC3_SETTLE	DAC3 Settle Refer to the DAC1 Settle bit for description.	R	0
9	DAC2_SETTLE	DAC2 Settle Refer to the DAC1 Settle bit for description.	R	0
8	DAC1_SETTLE	DAC1 Settle Indicates the analog output settling time of the four DAC Channels of DAC1. Set when DAC1 Channels are settling. Clear when DAC1 Channels are stable. This is no physical representation of any kind, just an internal timer that expires 10µs (typical specified settling time) after an update of the DAC1 analog outputs.	R	0
7:4	-	Reserved	-	-
3	DAC4_BUSY	DAC4 Busy Refer to the DAC1 Busy bit for description.	R	0
2	DAC3_BUSY	DAC3 Busy Refer to the DAC1 Busy bit for description.	R	0
1	DAC2_BUSY	DAC2 Busy Refer to the DAC1 Busy bit for description.	R	0
0	DAC1_BUSY	DAC1 Busy Set when • Configuration data has been written to DAC1 Configuration Register or is currently transferred to DAC1 • Digital values have been written to DAC1 Data Register or are currently transferred to DAC1 • Status Read has been requested in DAC1 Status Register or status data is currently transferred from DAC1 Clear when DAC1 control logic is in idle state.	R	0

Table 3-32: Global DAC Status Register

Also see chapter *Programming Hints / Global DAC Status Register Read*!

3.2.1.5 DAC Device Registers

The following registers exist multiple times and each of the registers deals with a single DAC (four DAC Channels) on-board the TPMC533.

These Registers are Reserved on TPMC533-20R.

3.2.1.5.1 DAC Configuration Registers (0x168, 0x198, 0x1C8 and 0x1F8)

There is a dedicated DAC Configuration Register for each DAC (for all four DAC Channels of each DAC).

A write to a DAC Configuration Register requests the configuration of the DAC (the DAC Configuration Register setting is transferred to the DAC internal configuration registers as soon as possible). If not already set because of ongoing communication with the DAC, the DAC Busy bit in the Global DAC Status Register is set and remains set until the configuration data transfer to the DAC is done.

After power-up the DACs should be configured before switching to Sequencer Mode or using the DACs in Manual Mode.

Each DAC must be configured before it can be used. The DAC Channels can only be used when their corresponding PUx-bit in the DAC Status Register is set. For verification after configuration write the DAC Busy Bit in the Global DAC Status Register should be monitored whether it was cleared again. Also see chapter *Programming Hints / Global DAC Status Register Read*!

When powered on, the DAC outputs are clamped to 0V via a low impedance path until the first digital-to-analog conversion was performed.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:30</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>29</td><td>DACx_PU_D</td><td>DAC Channel D Power-Up
When set, this bit places DAC Channel D in normal operating mode.
When cleared, this bit places DAC Channel D in power-down mode (default).</td><td>R/W</td><td>0</td></tr>
<tr><td>28:27</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>26:24</td><td>DACx_OR_D</td><td>DAC Channel D Output Range
Also see chapter “DAC Data Coding”.

<table><tr><th>OR_D</th><th>Output Voltage Range</th></tr><tr><td>000</td><td>+5V (unipolar)</td></tr><tr><td>001</td><td>+10V (unipolar)</td></tr><tr><td>010</td><td>+10.8V (unipolar)</td></tr><tr><td>011</td><td>±5V (bipolar)</td></tr><tr><td>100</td><td>±10V (bipolar)</td></tr><tr><td>101</td><td>±10.8V (bipolar)</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table></td><td>R/W</td><td>000</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>23:22</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>21</td><td>DACx_PU_C</td><td>DAC Channel C Power-Up
When set, this bit places DAC Channel C in normal operating mode.
When cleared, this bit places DAC Channel C in power-down mode (default).</td><td>R/W</td><td>0</td></tr>
<tr><td>20:19</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>18:16</td><td>DACx_OR_C</td><td>DAC Channel C Output Range
Also see chapter “DAC Data Coding”.
<table><tr><th>OR_C</th><th>Output Voltage Range</th></tr><tr><td>000</td><td>+5V (unipolar)</td></tr><tr><td>001</td><td>+10V (unipolar)</td></tr><tr><td>010</td><td>+10.8V (unipolar)</td></tr><tr><td>011</td><td>±5V (bipolar)</td></tr><tr><td>100</td><td>±10V (bipolar)</td></tr><tr><td>101</td><td>±10.8V (bipolar)</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table></td><td>R/W</td><td>000</td></tr>
<tr><td>15:14</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>13</td><td>DACx_PU_B</td><td>DAC Channel B Power-Up
When set, this bit places DAC Channel B in normal operating mode.
When cleared, this bit places DAC Channel B in power-down mode (default).</td><td>R/W</td><td>0</td></tr>
<tr><td>12:11</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>10:8</td><td>DACx_OR_B</td><td>DAC Channel B Output Range
Also see chapter “DAC Data Coding”.
<table><tr><th>OR_B</th><th>Output Voltage Range</th></tr><tr><td>000</td><td>+5V (unipolar)</td></tr><tr><td>001</td><td>+10V (unipolar)</td></tr><tr><td>010</td><td>+10.8V (unipolar)</td></tr><tr><td>011</td><td>±5V (bipolar)</td></tr><tr><td>100</td><td>±10V (bipolar)</td></tr><tr><td>101</td><td>±10.8V (bipolar)</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table></td><td>R/W</td><td>000</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>7:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5</td><td>DACx_PU_A</td><td>DAC Channel A Power-Up
When set, this bit places DAC Channel A in normal operating mode.
When cleared, this bit places DAC Channel A in power-down mode (default).</td><td>R/W</td><td>0</td></tr>
<tr><td>4:3</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>2:0</td><td>DACx_OR_A</td><td>DAC Channel A Output Range
Also see chapter “DAC Data Coding”.

<table><tr><th>OR_A</th><th>Output Voltage Range</th></tr><tr><td>000</td><td>+5V (unipolar)</td></tr><tr><td>001</td><td>+10V (unipolar)</td></tr><tr><td>010</td><td>+10.8V (unipolar)</td></tr><tr><td>011</td><td>±5V (bipolar)</td></tr><tr><td>100</td><td>±10V (bipolar)</td></tr><tr><td>101</td><td>±10.8V (bipolar)</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table></td><td>R/W</td><td>000</td></tr>
</table>

Table 3-33: DAC Configuration Register

3.2.1.5.2 DAC Correction Registers (0x170, 0x174, 0x178, 0x17C, 0x1A0, 0x1A4, 0x1A8, 0x1AC, 0x1D0, 0x1D4, 0x1D8, 0x1DC, 0x200, 0x204, 0x208 and 0x20C)

There are four dedicated DAC Correction Registers for each DAC (one register for each of the four DAC Channels of each DAC).

The correction values for the specific DAC Channels and Voltage Ranges must be read from the Correction Data ROM at PCI Base Address Register 1 (BAR1).

After power-up and DAC Configuration the DAC Correction Registers should be written with the values for the desired Voltage Range read from the Correction Data ROM, before switching to Sequencer Mode or using the DACs in Manual Mode.

Leaving the DAC Correction Registers unmodified at their Reset Value means that DAC Correction is disabled.

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_GAIN_A	Gain Correction Value DAC Channel A	R/W	0x0000
15:0	DACx_OFFSET_A	Offset Correction Value DAC Channel A	R/W	0x0000

Table 3-34: DAC Correction Register A

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_GAIN_B	Gain Correction Value DAC Channel B	R/W	0x0000
15:0	DACx_OFFSET_B	Offset Correction Value DAC Channel B	R/W	0x0000

Table 3-35: DAC Correction Register B

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_GAIN_C	Gain Correction Value DAC Channel C	R/W	0x0000
15:0	DACx_OFFSET_C	Offset Correction Value DAC Channel C	R/W	0x0000

Table 3-36: DAC Correction Register C

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_GAIN_D	Gain Correction Value DAC Channel D	R/W	0x0000
15:0	DACx_OFFSET_D	Offset Correction Value DAC Channel D	R/W	0x0000

Table 3-37: DAC Correction Register D

3.2.1.5.3 DAC Data Registers (0x180, 0x184, 0x1B0, 0x1B4, 0x1E0, 0x1E4, 0x210 and 0x214)

These registers are intended to be used for DACs operating in Manual Mode (not for Sequencer Mode).

To accelerate data access, each DAC Data Register holds two DAC Channel values.

A write to a DAC Data Register requests the transfer of two digital values to the corresponding DAC (the DAC Data is transferred to the DAC internal data registers as soon as possible). If not already set because of ongoing communication with the DAC, the DAC Busy bit in the Global DAC Status Register is set and remains set until the configuration data transfer to the DAC is done.

For verification after data write the DAC Busy Bit in the Global DAC Status Register should be monitored whether it was cleared again.

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_DATA_B	DAC Data DAC Channel B	R/W	0x0000
15:0	DACx_DATA_A	DAC Data DAC Channel A	R/W	0x0000

Table 3-38: DAC Data Register A & B

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_DATA_D	DAC Data DAC Channel D	R/W	0x0000
15:0	DACx_DATA_C	DAC Data DAC Channel C	R/W	0x0000

Table 3-39: DAC Data Register C & D

3.2.1.5.4 DAC Status Registers (0x188, 0x1B8, 0x1E8 and 0x218)

Each DAC device provides an internal status register, which is reflected in the corresponding DAC Status Register. The DAC Status Register is updated when a status register read is requested by writing a '1' to the DACx_RDSTA bit.

Bit	Symbol	Description	Access	Reset Value
31	DACx_RDSTA	Read DAC internal Status Register When set, a request for reading the DAC status is logged and the status valid bit (DACx_SVAL) is cleared. When the DAC status read is done, the DAC Status Register is updated and the DACx_SVAL bit is set again. This bit clears immediately.	R/S	0
30	DACx_SVAL	Status is valid 0: Outdated Status Information 1: Updated Status Information This bit indicates that the other register bits of the DAC Status Register have been updated after a DAC status read. The bit is cleared upon a DAC status read request (DACx_RDSTA) or by writing a '1' to this bit.	R/C	0
29	-	Reserved	-	-
28	DACx_AUTOSTA	Automatic DAC internal Status Register Read 0: No Automatic DAC Status Read 1: Automatic DAC Status Read after each conversion In automatic mode, the DAC Status is read automatically after a DAC conversion.	R/W	0
27:10	-	Reserved	-	-
9	DACx_TSD	DAC Thermal Shutdown Alert In the event of an over-temperature situation, the DAC is powered down and this bit is set.	R	0
8	DACx_OCD	DAC Channel D Over-current Alert. See OCA description.	R	0
7	DACx_OCC	DAC Channel C Over-current Alert. See OCA description.	R	0
6	DACx_OCB	DAC Channel B Over-current Alert. See OCA description.	R	0
5	DACx_OCA	DAC Channel A Over-current Alert In the event of an over-current situation on DAC channel A it is powered down and this bit is set.	R	0
4	DACx_PUREF	DAC Reference Power-Up When set, this bit indicates that the DAC internal reference is powered-up. Since the DACs are operating with the internal reference, this bit should always be set for any status read from the DACs.	R	0
3	DACx_PUD	DAC Channel D Power-Up. See PUA description.	R	0
2	DACx_PUC	DAC Channel C Power-Up. See PUA description.	R	0
1	DACx_PUB	DAC Channel B Power-Up. See PUA description.	R	0
0	DACx_PUA	DAC Channel A Power-Up '0' when powered down, '1' when powered up. On detection of an over-current or thermal overtemperature condition, DAC channel A will power down automatically. DACx_PUA will be cleared to reflect this.	R	0

Table 3-40: DAC Status Register

3.2.1.5.5 DAC Mode Registers (0x18C, 0x1BC, 0x1EC and 0x21C)

For each DAC (for all four DAC Channels of each DAC) it is configurable whether to use the DAC Sequencer to periodically read DA values, that shall be converted, from Host RAM or whether DA values are only written manually into DAC Data Registers.

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1	DACx_MAN	DAC Manual Mode Configuration 0: Immediate Conversion in Manual Mode 1: Controlled Conversion in Manual Mode If set to Immediate Conversion, a DAC Channel is updated immediately after a DAC Data transfer. If set to Controlled Conversion, the DAC Channels are updated simultaneously by a write to the Global DAC Control Register. (DAC Data must have been transferred before, also see chapter *Programming Hints / Global DAC Status Register Read*!)	R/W	0
0	DACx_MODE	DAC Operating Mode 0: Manual Mode 1: Sequencer Mode This bit sets the general DAC Operating Mode. In Manual Mode, the analog outputs are updated by software commands (there is no periodic conversion rate). In Sequencer Mode, the analog outputs are updated simultaneously and periodically at a configurable conversion rate.	R/W	0

Table 3-41: DAC Mode Register

Note that all four channels of a DAC are always operating in the same Operating Mode.

3.2.1.6 DAC Sequencer Registers

The DAC Sequencer is used to periodically read digital values from Host RAM via DMA transfers and convert them to analog signals at a configurable Conversion Rate.

All DACs configured to "Sequencer Mode" in their corresponding DAC Mode Registers are always performing their conversions simultaneously.

For each conversion, data is updated for all four DAC Channels of each DAC assigned to the DAC Sequencer.

The DAC Sequencer may operate in Normal Mode or Frame Mode. Normal Mode is used for generating a single block of digital-to-analog conversions or for generating continuous conversions by software request. Frame Mode is used for repetitive blocks of digital-to-analog conversions triggered by a Frame Trigger at a configurable Frame Trigger Rate.

These Registers are Reserved on TPMC533-20R.

3.2.1.6.1 DAC Sequencer Control Register (0x2E8)

Bit	Symbol	Description	Access	Reset Value
31:18	-	Reserved	-	-
17	RD_DMA_RESET	DMA Reset Writing '1' to this bit resets the DMA Controller. This bit is self-clearing	R/S	0
16	RD_DMA_ENA	DMA Enable 0: DMA Controller Disabled 1: DMA Controller Enabled Enables the Sequencer's DMA Controller to allow the initiation of DMA transfers by writing to the DMA Buffer Length Register. When being disabled, any active DMA transfer is completed before the DMA Engine enters Idle or Error state. The DMA Controller operation is stopped in case of a DMA Error. In this case the DAC Sequencer Status Register must be read and the DMA Controller can be disabled. The DMA Controller is reset when disabled.	R/W	0
15:9	-	Reserved	-	-
8	DAC_SEQ_FIFO_CLR	FIFO Clear When set to 1, the DAC Sequencer's internal FIFO is cleared. This bit is self-clearing	R/S	0

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>7:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5</td><td>OU_CLK_SRC</td><td>Output Unit Conversion Clock Source
These bits select the Output Unit Conversion Clock signal source. The Output Unit Conversion Clock signal defines the DAC Sequencer’s Conversion Rate.
Note that in Frame Mode, the Output Unit Conversion Clock signal must be phase locked to the Frame Trigger signal.
<table><tr><th>OU_CLK_SRC</th><th>Clock Source</th></tr><tr><td>0</td><td>Conversion Clock 1</td></tr><tr><td>1</td><td>Conversion Clock 2</td></tr></table>
Setting the DAC Sequencer's Conversion Rate to a period shorter than the DAC settling time (~10µs) is not allowed.
If the Output Unit triggers the next conversion as long as the DAC outputs are still settling from the previous conversion or the DACs are not properly pre-loaded with DAC Data, conversion is stopped and the OU_CONV_ERR bit in the DAC Sequencer Status Register is set.</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>PRELOAD_CLEAR</td><td>Output Unit Pre-Load Clear
Setting this bit marks the DACs operating in Sequencer Mode as being ‘un-loaded’. The DACs are automatically pre-loaded again when DAC Data is/becomes available in the DAC Sequencer's internal FIFO.
This bit is self-clearing.</td><td>R/S</td><td>0</td></tr>
<tr><td>3</td><td>OU_CONV_START</td><td>Output Unit Start Conversion (Normal Mode)
Set this bit to start a conversion process in Normal Mode.
The FIFO Level may be checked before setting this bit.
This bit is self-clearing</td><td>R/S</td><td>0</td></tr>
<tr><td>2</td><td>OU_MODE</td><td>Output Unit Mode
0: Normal Mode
1: Frame Mode
In Normal Mode, the configured Number of Conversions is performed starting with the next Conversion Clock after the OU_CONV_START bit has been set by software.
In Frame Mode, the configured Number of Conversions is performed starting with the next Conversion Clock after a Frame Trigger occurred.</td><td>R/W</td><td>0</td></tr>
<tr><td>1</td><td>OU_RESET</td><td>Output Unit Reset
Writing '1' to this bit resets the Output Unit.
This bit is self-clearing</td><td>R/S</td><td>0</td></tr>
</table>

Bit	Symbol	Description	Access	Reset Value
0	OU_ENA	Output Unit Enable 0: Output Unit Disabled 1: Output Unit Enabled Enables the Output Unit. The Output Unit handles the DAC Data transfer from the Sequencer's internal FIFO to the DACs and the DAC Sequencer's Conversion Rate generation. While the DACs operating in Sequencer Mode are not completely pre-loaded with DAC Data, these values are automatically transferred from the FIFO to the DACs' internal registers to pre-load them for the first/next conversion (except in an error case). The Output Unit operation is stopped in case of an Output Unit Error. In this case the DAC Sequencer Status Register must be read and the Output Unit can be disabled. The Output Unit is reset when disabled.	R/W	0

Table 3-42: DAC Sequencer Control Register

3.2.1.6.2 DAC Sequencer Status Register (0x2EC)

Bit	Symbol	Description	Access	Reset Value
31:21	-	Reserved	-	-
20	RD_DMA_TERM	DMA Buffer Termination The end of the DMA Buffer was reached (all values have been read out of the DMA Buffer and written to the FIFO). This bit is automatically cleared when a new DMA Buffer is provided by writing to the DMA Buffer Length Register.	R	0
19	-	Reserved	-	-
18	RD_DMA_ERR	DMA Error A PCI Master Abort occurred because the addressed PCI Target did not respond or a PCI Target Abort occurred because the addressed PCI Target detected a fatal error. In case of an error, the DMA Controller operation is automatically stopped. This bit is cleared when the DMA Controller is disabled.	R	0
17	RD_DMA_BUSY	DMA Busy Indicates that the DMA Controller is currently busy (active).	R	0
16	RD_DMA_IDLE	DMA Idle Indicates that the DMA Controller is currently in Idle State. A DMA transfer may be started (a DMA buffer may be provided) by writing to the DMA Buffer Length Register.	R	0
15:7	-	Reserved	-	-
6	OU_FRAME_ERR	Output Unit Frame Error A Frame Trigger event occurs, but the configured Number of Conversions has not been processed so far. In case of this error, the conversion process is terminated (no more conversion pulses are generated) and the Output Unit operation is stopped. This bit is automatically cleared when the Output Unit is disabled.	R	0
5	TIMING_ERR	Output Unit DAC Timing Error The DAC Sequencer's Conversion Rate requests the next conversion, but at least one of the involved DACs does not allow a conversion at the moment because a serial data transfer is about to start or has just been finished. In case of this error, the conversion process is terminated (no more conversion pulses are generated) and the Output Unit operation is stopped. This bit is automatically cleared when the Output Unit is disabled.	R	0
4	DATA_ERR	Output Unit Data Underrun Error The DAC Sequencer's Conversion Rate requests the next conversion, but not all DACs are properly pre-loaded with data. In case of this error, the conversion process is terminated (no more conversion pulses are generated) and the Output Unit operation is stopped. This bit is automatically cleared when the Output Unit is disabled.	R	0

Bit	Symbol	Description	Access	Reset Value
3	-	Reserved	-	-
2	OU_CONV_ACTIVE	Output Unit Conversion Process Active Indicates that the conversion process is active. In Normal Mode, this bit is set when the software sets the Output Unit Start Conversion bit. This bit is cleared when the configured Number of Conversions has been performed. In Frame Mode, this bit is set when a Frame Trigger starts the conversion process (except in a frame error case). This bit is cleared when the configured Number of Conversions has been performed (for a single frame).	R	0
1	PRELOAD	Output Unit Pre-Load Done Indicates that all DACs configured to Sequencer Mode are pre-loaded with DAC Data on all four DAC Channels. This bit is automatically cleared upon a DAC conversion pulse or when the software sets the Output Unit Pre-Load Clear bit.	R	0
0	OU_IDLE	Output Unit Idle Indicates that the Output Unit is currently in Idle State.	R	0

Table 3-43: DAC Sequencer Status Register

3.2.1.6.3 Number of Conversions Register (0x2F4)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	DAC_SEQ_NUM_CONV	Number of Conversions to be performed Set to '0' for continuous digital-to-analog conversions. Normal Mode: Number of conversions (after OU_CONV_START was set) per requested block of digital-to-analog conversions. When the configured Number of Conversions has been performed, the conversion process is stopped (until software sets the OU_CONV_START bit again) and the OU_CONV_ACTIVE bit in the DAC Sequencer Status Register is cleared. Frame Mode: Number of digital-to-analog conversions per Frame Trigger. When the configured Number of Conversions (per frame) has been performed, the conversion process is stopped (until the next Frame Trigger event occurs) and the OU_CONV_ACTIVE bit in the DAC Sequencer Status Register is cleared.	R/W	0x000 0000

Table 3-44: Number of Conversions Register

Note that every time the DAC Sequencer triggers a conversion, all four DAC Channels of all DACs configured to operate in Sequencer Mode are updated simultaneously. After each sequencer controlled conversion, the DACs are pre-loaded with DAC Data for the next conversion (if data is available in the DAC Sequencer's internal FIFO).

3.2.1.6.4 Conversion Count Register (0x2F8)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	DAC_SEQ_CONV_COUNT	Number of Conversions that have been performed Normal Mode: The value is automatically reset when the (next) Output Unit Start Conversion is initiated in the DAC Sequencer Control Register. Frame Mode: The value is automatically reset at a Frame Trigger event (except for the case when an Output Unit Frame Error occurred).	R	0x000 0000

Table 3-45: Conversion Count Register

3.2.1.6.5 FIFO Level Register (0x2FC)

Bit	Symbol	Description	Access	Reset Value
31:0	DAC_SEQ_FIFO_LEVEL	FIFO Level This value shows the current fill level of the Sequencer's internal FIFO. It is measured in number of bytes. (a DAC Data value consists of two bytes)	R	0x0000 0000

Table 3-46: FIFO Level Register

3.2.1.6.6 DMA Buffer Base Address Register (0x308)

Bit	Symbol	Description	Access	Reset Value
31:0	RD_DMA_BUF_ADDR	DMA Buffer Base Address PCI memory mapped base address of the DMA Buffer in Host RAM that provides DAC Data. The DMA Buffer Base Address is latched when the DMA Buffer Length Register is written.	R/W	0x0000 0000

Table 3-47: DMA Buffer Base Address Register

3.2.1.6.7 DMA Buffer Length Register (0x30C)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	RD_DMA_BUF_LEN	DMA Buffer Length Byte Length of the provided DMA Buffer in Host RAM. **A write to the DMA Buffer Length Register initiates the DMA transfer.** The Initiation of DMA transfers is only possible if RD_DMA_IDLE in the DAC Sequencer Status Register is '1'.	R/W	0x0000 0000

Table 3-48: DMA Buffer Length Register

3.2.1.6.8 DMA Buffer Next Address Register (0x310)

Bit	Symbol	Description	Access	Reset Value
31:0	RD_DMA_NEXT_ADDR	DMA Buffer Next Address This register holds the PCI address of the address location in Host RAM the next DAC Data is read from. It can be used to determine how much information is left in the provided DMA Buffer.	R	0x0000 0000

Table 3-49: DMA Buffer Next Address Register

3.2.1.7 Conversion Signals Registers

The following registers are only relevant for ADCs and DACs configured to operate in Sequencer Mode.

3.2.1.7.1 Conversion Clock 1 Generator Register (0x320)

This register determines the frequency of the Conversion Clock 1 Generator output.

Conversion Clock 1 generation is started in the Conversion Signals Generator Enable Register.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>30:29</td><td>CLK1_GEN_SRC</td><td>Internal Clock Source
<table><tr><th>CLK1_GEN_SRC</th><th>Internal Clock Source</th></tr><tr><td>00</td><td>20 MHz</td></tr><tr><td>01</td><td>22.05 MHz</td></tr><tr><td>10</td><td>60 MHz</td></tr><tr><td>11</td><td>Reserved</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>28</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>27:0</td><td>CLK1_GEN_DIV</td><td>Clock Divider
These bits set the divider for the selected Internal Clock Source.</td><td>R/W</td><td>0xFFF FFFF</td></tr>
</table>

Table 3-50: Conversion Clock 1 Generator Register

The frequency of the Conversion Clock 1 Generator output is: $\frac{CLK1\_GEN\_SRC}{CLK1\_GEN\_DIV+1}$

3.2.1.7.2 Conversion Clock 2 Generator Register (0x324)

This register determines the frequency of the Conversion Clock 2 Generator output.

Conversion Clock 2 generation is started in the Conversion Signals Generator Enable Register.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>30:29</td><td>CLK2_GEN_SRC</td><td>Internal Clock Source
<table><tr><th>CLK2_GEN_SRC</th><th>Internal Clock Source</th></tr><tr><td>00</td><td>20 MHz</td></tr><tr><td>01</td><td>22.05 MHz</td></tr><tr><td>10</td><td>60 MHz</td></tr><tr><td>11</td><td>Reserved</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>28</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>27:0</td><td>CLK2_GEN_DIV</td><td>Clock Divider
These bits set the divider for the selected Internal Clock Source.</td><td>R/W</td><td>0xFFF FFFF</td></tr>
</table>

Table 3-51: Conversion Clock 2 Generator Register

The frequency of the Conversion Clock 2 Generator output is: $\frac{CLK2\_GEN\_SRC}{CLK2\_GEN\_DIV+1}$

3.2.1.7.3 Frame Trigger Generator Register 1 (0x32C)

This register determines the frequency of the Frame Trigger Generator output (Frame Trigger Rate).

Bit	Symbol	Description	Access	Reset Value
31:30	-	Reserved	-	-
29	FRAME_TRIG_GEN_SRC	Frame Trigger Generator Clock Source FRAME_TRIG_GEN_SRC: 0 → Conversion Clock 1 Generator FRAME_TRIG_GEN_SRC: 1 → Conversion Clock 2 Generator	R/W	0
28	-	Reserved	-	-
27:0	FRAME_TRIG_GEN_DIV	Frame Trigger Generator Divider These bits set the divider for the selected Conversion Clock Generator output.	R/W	0xFFFFFFFF

Table 3-52: Frame Trigger Generator Register 1

The frequency of the Frame Trigger Generator output is: $\frac{\text{FRAME\_TRIG\_GEN\_SRC}}{\text{FRAME\_TRIG\_GEN\_DIV+1}}$

3.2.1.7.4 Frame Trigger Generator Register 2 (0x330)

This register determines the number of Frame Triggers generated on-board.

Frame Trigger generation is started in the Conversion Signals Generator Enable Register.

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	FRAME_TRIG_GEN_NUM	Number of Frame Triggers to be generated Sets the number of Frame Triggers to be generated. If set to '0', Frame Triggers are generated continuously at the configured Frame Trigger frequency.	R/W	0x0000000

Table 3-53: Frame Trigger Generator Register 2

3.2.1.7.5 Conversion Signals Generator Enable Register (0x33C)

This register can be used for a synchronized start of the two Conversion Clocks and the Frame Trigger generated on-board.

Bit	Symbol	Description	Access	Reset Value
31:9	-	Reserved	-	-
8	FRAME_TRIG_GEN_ENA	Frame Trigger Generation Enable 0: Frame Trigger Generation Disabled 1: Frame Trigger Generation Enabled If enabled, the configured Number of Frame Triggers to be generated (Frame Trigger Generator Register 2) is generated, starting with the next rising edge of the associated Conversion Clock Generator output. The Frame Trigger is output at the configured Frame Trigger frequency but, of course, requires a running Conversion Clock Generator Clock Source signal. If disabled, the Frame Trigger output is '1'.	R/W	0
7:2	-	Reserved	-	-
1	CLK2_GEN_ENA	Conversion Clock 2 Generation Enable 0: Conversion Clock 2 Generation Disabled 1: Conversion Clock 2 Generation Enabled If disabled, the clock output is '1'.	R/W	0
0	CLK1_GEN_ENA	Conversion Clock 1 Generation Enable 0: Conversion Clock 1 Generation Disabled 1: Conversion Clock 1 Generation Enabled If disabled, the clock output is '1'.	R/W	0

Table 3-54: Conversion Signals Generator Enable Register

3.2.1.7.6 Conversion Signals Generator Output Driver Register (0x340)

This register is used to configure whether the three Conversion Signals generated on-board are output or not.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5:4</td><td>FRAME_TRIG_GEN_OUT</td><td>Frame Trigger Generator Output Driver Configuration

<table><tr><th>FRAME_TRIG_GEN_OUT</th><th>Output Driver Configuration</th></tr><tr><td>0x</td><td>Output Driver disabled</td></tr><tr><td>10</td><td>P14 Back I/O
Global Frame Trigger</td></tr><tr><td>11</td><td>Front I/O
Digital I/O 5</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>3:2</td><td>CLK2_GEN_OUT</td><td>Conversion Clock 2 Generator Output Driver Configuration

<table><tr><th>CLK2_GEN_OUT</th><th>Output Driver Configuration</th></tr><tr><td>0x</td><td>Output Driver disabled</td></tr><tr><td>10</td><td>P14 Back I/O
Global Conversion Clock 2</td></tr><tr><td>11</td><td>Front I/O
Digital I/O 3</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>1:0</td><td>CLK1_GEN_OUT</td><td>Conversion Clock 1 Generator Output Driver Configuration

<table><tr><th>CLK1_GEN_OUT</th><th>Output Driver Configuration</th></tr><tr><td>0x</td><td>Output Driver disabled</td></tr><tr><td>10</td><td>P14 Back I/O
Global Conversion Clock 1</td></tr><tr><td>11</td><td>Front I/O
Digital I/O 1</td></tr></table></td><td>R/W</td><td>00</td></tr>
</table>

Table 3-55: Conversion Signals Generator Output Driver Register

Note that for driving out a Conversion Clock and/or Frame Trigger generator signal on the appropriate DIO Front I/O pin, the corresponding bit combination must be set in the Conversion Signals Generator Output Driver Register **and the corresponding bit in the DIO Output Enable Register must be clear.**

The regular DIO output operation dominates, thus if a bit is set in the DIO Output Enable Register, the corresponding value set in the DIO Output Register is driven out on the DIO Front I/O pin (regardless of the Conversion Signals Generator Output Driver Register setting).

3.2.1.7.7 Conversion Signals Source Selection Register (0x344)

This register is used to select the signal source for the three Conversion Signals.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5:4</td><td>FRAME_TRIG_SRC</td><td>Frame Trigger Source
<table><tr><th>FRAME_TRIG_SRC</th><th>Source</th></tr><tr><td>0x</td><td>Frame Trigger Generator</td></tr><tr><td>10</td><td>P14 Back I/O
Global Frame Trigger</td></tr><tr><td>11</td><td>Front I/O
Digital I/O 5</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>3:2</td><td>CLK2_SRC</td><td>Conversion Clock 2 Source
<table><tr><th>CLK2_SRC</th><th>Source</th></tr><tr><td>0x</td><td>Conversion Clock 2
Generator</td></tr><tr><td>10</td><td>P14 Back I/O
Global Conversion Clock 2</td></tr><tr><td>11</td><td>Front I/O
Digital I/O 3</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>1:0</td><td>CLK1_SRC</td><td>Conversion Clock 1 Source
<table><tr><th>CLK1_SRC</th><th>Source</th></tr><tr><td>0x</td><td>Conversion Clock 1
Generator</td></tr><tr><td>10</td><td>P14 Back I/O
Global Conversion Clock 1</td></tr><tr><td>11</td><td>Front I/O
Digital I/O 1</td></tr></table></td><td>R/W</td><td>00</td></tr>
</table>

Table 3-56: Conversion Signals Source Selection Register

System Configuration	Conversion Signals Generator Output Driver	Conversion Signals Source Selection
Single Card	Output Driver disabled	Conversion Signal Generators
Multiboard Master Card	P14 Back I/O or Front I/O	P14 Back I/O or Front I/O
Multiboard Target Card	Output Driver disabled	P14 Back I/O or Front I/O

3.2.1.7.8 Frame Timer Register (0x348)

Bit	Symbol	Description	Access	Reset Value
31	FRAME_TIMER_ENA	Frame Timer Enable 0: Frame Timer Disabled 1: Frame Timer Enabled If enabled, a Frame Trigger event resets the Frame Timer and (re-)starts it.	R/W	0
30	FRAME_TIMER_SRC	Frame Timer Clock Source 0: Conversion Clock 1 1: Conversion Clock 2	R/W	0
29	FRAME_TIMER	Frame Timer Status This bit is set when (after a Frame Trigger event) the configured Frame Timer has expired. This bit is automatically cleared every time a Frame Trigger occurs.	R	0
28	-	Reserved	-	-
27:0	FRAME_TIMER_VAL	Frame Timer Value The Frame Timer expires after FRAME_TIMER_VAL + 1 clock cycles of the selected Frame Timer Clock Source.	R/W	0xFFF FFFF

Table 3-57: Frame Timer Register

3.2.1.8 DIO Registers

The following registers deal with the Digital I/O interface on the Front I/O connector of the TPMC533.

3.2.1.8.1 DIO Input Register (0x354)

The Digital I/O receivers are always enabled, so each DIO level can always be monitored.

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	IN8	DIO8 Input Refer to the DIO1 Input bit for description.	R	0
6	IN7	DIO7 Input Refer to the DIO1 Input bit for description.	R	0
5	IN6	DIO6 Input Refer to the DIO1 Input bit for description.	R	0
4	IN5	DIO5 Input Refer to the DIO1 Input bit for description.	R	0
3	IN4	DIO4 Input Refer to the DIO1 Input bit for description.	R	0
2	IN3	DIO3 Input Refer to the DIO1 Input bit for description.	R	0
1	IN2	DIO2 Input Refer to the DIO1 Input bit for description.	R	0
0	IN1	DIO1 Input Reflects the actual input state of Digital I/O 1 at all times, even if DIO1 is configured as output in the DIO Direction Register 0: Digital I/O 1 is logic low. 1: Digital I/O 1 is logic high.	R	0

Table 3-58: DIO Input Register

3.2.1.8.2 DIO Input Filter Debounce Register (0x358)

A debounce filter can be configured to get rid of bouncing on the Digital I/O Inputs.

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	-	-
15:0	DEB	Digital I/O Input Filter Debounce Configuration T_{REJECT} = (DEB+1) * 50ns The rejection time can be configured from 50ns to 3.2768ms. Pulses with a duration smaller than T_{REJECT} are filtered and are not passed on to the internal logic. Please note that pulses with a duration between T_{PASS} and T_{REJECT} may or may not be filtered. T_{PASS} = (DEB+1) * 75ns = 1.5 * T_{REJECT} The pass time can be configured from 75ns to 4.9152ms. Pulses with a duration greater than T_{PASS} are not filtered and are passed on to the internal logic. After an input pin performs a rising or a falling edge, T_{PASS} defines how long this new logic level must be stable before the level change is passed on to the internal logic.	R/W	0x0000

Table 3-59: DIO Input Filter Debounce Register

3.2.1.8.3 DIO Output Register (0x35C)

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	OUT8	DIO8 Output Refer to the DIO1 Output bit for description.	R/W	0
6	OUT7	DIO7 Output Refer to the DIO1 Output bit for description.	R/W	0
5	OUT6	DIO6 Output Refer to the DIO1 Output bit for description.	R/W	0
4	OUT5	DIO5 Output Refer to the DIO1 Output bit for description.	R/W	0
3	OUT4	DIO4 Output Refer to the DIO1 Output bit for description.	R/W	0
2	OUT3	DIO3 Output Refer to the DIO1 Output bit for description.	R/W	0
1	OUT2	DIO2 Output Refer to the DIO1 Output bit for description.	R/W	0
0	OUT1	DIO1 Output Sets the output state of Digital I/O 1. If DIO1 is configured as input in the DIO Direction Register writes to this bit will take no effect 0: Digital I/O 1 is driven logic low. 1: Digital I/O 1 is driven logic high.	R/W	0

Table 3-60: DIO Output Register

3.2.1.8.4 DIO Output Enable Register (0x360)

All 8 DIOs can be programmed whether the Digital I/O transmitters are enabled or disabled per I/O line. The reset value of the DIO Output Enable Register is 0x0000 which means that all transmitters of the Digital I/O pins are disabled at system start.

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	OE8	DIO8 Output Enable Refer to the DIO1 Output Enable bit for description.	R/W	0
6	OE7	DIO7 Output Enable Refer to the DIO1 Output Enable bit for description.	R/W	0
5	OE6	DIO6 Output Enable Refer to the DIO1 Output Enable bit for description.	R/W	0
4	OE5	DIO5 Output Enable Refer to the DIO1 Output Enable bit for description.	R/W	0
3	OE4	DIO4 Output Enable Refer to the DIO1 Output Enable bit for description.	R/W	0
2	OE3	DIO3 Output Enable Refer to the DIO1 Output Enable bit for description.	R/W	0
1	OE2	DIO2 Output Enable Refer to the DIO1 Output Enable bit for description.	R/W	0
0	OE1	DIO1 Output Enable 0: Digital I/O 1 output transmitter is disabled. 1: Digital I/O 1 output transmitter is enabled.	R/W	0

Table 3-61: DIO Output Enable Register

3.2.1.9 Interrupt Registers

For an interrupt status bit to be set, the interrupt must be enabled prior to the interrupt event.

Disabling an interrupt clears the appropriate interrupt status bit.

An interrupt is asserted if at least one bit is set in the Interrupt Status Register.

3.2.1.9.1 Interrupt Enable Register (0x36C)

Bit	Symbol	Description	Access	Reset Value
31:30	-	Reserved	-	-
29	FRAME_TIMER_IRQ_ENA	Enable IRQ at Frame Timer event 0: disabled 1: enabled If enabled, an interrupt will be generated when the Frame Timer has expired.	R/W	0
28	FRAME_TRIG_ENA	Enable IRQ at Frame Trigger event 0: disabled 1: enabled If enabled, an interrupt will be generated when the Frame Trigger signal is detected.	R/W	0
27	ADC4_DONE_ENA	Enable IRQ after ADC4 Conversion is done Refer to the Enable IRQ after ADC1 Conversion is done bit for description.	R/W	0
26	ADC3_DONE_ENA	Enable IRQ after ADC3 Conversion is done Refer to the Enable IRQ after ADC1 Conversion is done bit for description.	R/W	0
25	ADC2_DONE_ENA	Enable IRQ after ADC2 Conversion is done Refer to the Enable IRQ after ADC1 Conversion is done bit for description.	R/W	0
24	ADC1_DONE_ENA	Enable IRQ after ADC1 Conversion is done 0: disabled 1: enabled If enabled, in Manual Mode an interrupt will be generated after a conversion of ADC1 is finished and ADC Data is available (ADC1_BUSY changes from '1' to '0' in Global ADC Status Register).	R/W	0

Bit	Symbol	Description	Access	Reset Value
23:20	-	Reserved	-	-
19	DAC4_DONE_ENA	Enable IRQ after DAC4 Conversion is done Refer to the Enable IRQ after DAC1 Conversion is done bit for description. For TPMC533-20R: Reserved	R/W	0
18	DAC3_DONE_ENA	Enable IRQ after DAC3 Conversion is done Refer to the Enable IRQ after DAC1 Conversion is done bit for description. For TPMC533-20R: Reserved	R/W	0
17	DAC2_DONE_ENA	Enable IRQ after DAC2 Conversion is done Refer to the Enable IRQ after DAC1 Conversion is done bit for description. For TPMC533-20R: Reserved	R/W	0
16	DAC1_DONE_ENA	Enable IRQ after DAC1 Conversion is done 0: disabled 1: enabled If enabled, in Manual Mode an interrupt will be generated after DAC1 has settled (DAC1_SETTLE changes from '1' to '0' in Global DAC Status Register). For TPMC533-20R: Reserved	R/W	0

Bit	Symbol	Description	Access	Reset Value
15:13	-	Reserved	-	-
12	IU_CONV_DONE_IRQ_ENA	Enable IRQ at Input Unit Number of Conversions done 0: disabled 1: enabled If enabled, an interrupt is asserted when the configured Number of ADC Conversions have been performed.	R/W	0
11:9	-	Reserved	-	-
8	WR_DMA_TERM_IRQ_ENA	Enable IRQ at ADC Sequencer DMA Buffer Termination 0: disabled 1: enabled If enabled, an interrupt is asserted when the DMA Controller of the ADC Sequencer terminates its provided DMA Buffer. The interrupt status bits indicate the reason for the termination.	R/W	0
7:5	-	Reserved	-	-
4	OU_CONV_DONE_IRQ_ENA	Enable IRQ at Output Unit Number of Conversions done 0: disabled 1: enabled If enabled, an interrupt is asserted when the configured Number of DAC Conversions have been performed. For TPMC533-20R: Reserved	R/W	0
3:1	-	Reserved	-	-
0	RD_DMA_TERM_IRQ_ENA	Enable IRQ at DAC Sequencer DMA Buffer Termination 0: disabled 1: enabled If enabled, an interrupt is asserted when the DMA Controller of the DAC Sequencer terminates its provided DMA Buffer. For TPMC533-20R: Reserved	R/W	0

Table 3-62: Interrupt Enable Register

3.2.1.9.2 Error Interrupt Enable Register (0x370)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27	IU_FRAME_ERR_IRQ_ENA	Enable IRQ at ADC Sequencer Input Unit Frame Error 0: disabled 1: enabled If enabled, an interrupt is asserted if a Frame Trigger event occurs, but the configured Number of Conversions has not been processed so far.	R/W	0
26	CONV_ERR_IRQ_ENA	Enable IRQ at ADC Sequencer Input Unit Conversion Error 0: disabled 1: enabled If enabled, an interrupt is asserted when the Sequencer Conversion Clock Source requests the next conversion, but the ADCs are still busy performing the conversion process of the previous conversion.	R/W	0
25	FIFO_OF_IRQ_ENA	Enable IRQ at ADC Sequencer Input Unit FIFO Overflow Error 0: disabled 1: enabled If enabled, an interrupt is asserted when the Input Unit wants to write sampled values from the ADCs to the FIFO but the FIFO is full because AD samples could not be written to Host RAM fast enough.	R/W	0
24	WR_DMA_ERR_IRQ_ENA	Enable IRQ at ADC Sequencer DMA Error 0: disabled 1: enabled If enabled, an interrupt is asserted when the DMA Controller of the ADC Sequencer faces a PCI Bus Abort.	R/W	0

Bit	Symbol	Description	Access	Reset Value
23:20	-	Reserved	-	-
19	OU_FRAME_ERR_IRQ_ENA	Enable IRQ at DAC Sequencer Output Unit Frame Error 0: disabled 1: enabled If enabled, an interrupt is asserted if a Frame Trigger event occurs, but the configured Number of Conversions has not been processed so far. For TPMC533-20R: Reserved	R/W	0
18	TIMING_ERR_IRQ_ENA	Enable IRQ at DAC Sequencer Output Unit DAC Timing Error 0: disabled 1: enabled If enabled, an interrupt is asserted when the DAC Sequencer's Conversion Rate requests the next conversion, but at least one of the involved DACs is still busy. For TPMC533-20R: Reserved	R/W	0
17	DATA_ERR_IRQ_ENA	Enable IRQ at DAC Sequencer Output Unit Data Underrun Error 0: disabled 1: enabled If enabled, an interrupt is asserted when the Output Unit wants to perform a DAC Conversion but the DAC channels are not properly pre-loaded. For TPMC533-20R: Reserved	R/W	0
16	RD_DMA_ERR_IRQ_ENA	Enable IRQ at DAC Sequencer DMA Error 0: disabled 1: enabled If enabled, an interrupt is asserted when the DMA Controller of the DAC Sequencer faces a PCI Bus Abort. For TPMC533-20R: Reserved	R/W	0

Bit	Symbol	Description	Access	Reset Value
15:4	-	Reserved	-	-
3	DAC4_ALERT_ENA	Enable IRQ at DAC4 Alert Refer to the Enable IRQ at DAC1 Alert bit for description. For TPMC533-20R: Reserved	R/W	0
2	DAC3_ALERT_ENA	Enable IRQ at DAC3 Alert Refer to the Enable IRQ at DAC1 Alert bit for description. For TPMC533-20R: Reserved	R/W	0
1	DAC2_ALERT_ENA	Enable IRQ at DAC2 Alert Refer to the Enable IRQ at DAC1 Alert bit for description. For TPMC533-20R: Reserved	R/W	0
0	DAC1_ALERT_ENA	Enable IRQ at DAC1 Alert 0: disabled 1: enabled If enabled, an interrupt is asserted when the DAC1 status is read and any of the over-current bits or the thermal shutdown bit is set. For TPMC533-20R: Reserved	R/W	0

Table 3-63: Error Interrupt Enable Register

3.2.1.9.3 DIO Rising Edge Interrupt Enable Register (0x374)

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	DIO8_RISE	Enable IRQ at DIO 8 Rising Edge See the Enable IRQ at DIO 1 Rising Edge bit for description.	R/W	0
6	DIO7_RISE	Enable IRQ at DIO 7 Rising Edge See the Enable IRQ at DIO 1 Rising Edge bit for description.	R/W	0
5	DIO6_RISE	Enable IRQ at DIO 6 Rising Edge See the Enable IRQ at DIO 1 Rising Edge bit for description.	R/W	0
4	DIO5_RISE	Enable IRQ at DIO 5 Rising Edge See the Enable IRQ at DIO 1 Rising Edge bit for description.	R/W	0
3	DIO4_RISE	Enable IRQ at DIO 4 Rising Edge See the Enable IRQ at DIO 1 Rising Edge bit for description.	R/W	0
2	DIO3_RISE	Enable IRQ at DIO 3 Rising Edge See the Enable IRQ at DIO 1 Rising Edge bit for description.	R/W	0
1	DIO2_RISE	Enable IRQ at DIO 2 Rising Edge See the Enable IRQ at DIO 1 Rising Edge bit for description.	R/W	0
0	DIO1_RISE	Enable IRQ at DIO 1 Rising Edge 0: disabled 1: enabled If enabled, an interrupt is asserted when a rising edge is detected at DIO1.	R/W	0

Table 3-64: DIO Rising Edge Interrupt Enable Register

3.2.1.9.4 DIO Falling Edge Interrupt Enable Register (0x378)

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	DIO8_FALL	Enable IRQ at DIO 8 Falling Edge See the Enable IRQ at DIO 1 Falling Edge bit for description.	R/W	0
6	DIO7_FALL	Enable IRQ at DIO 7 Falling Edge See the Enable IRQ at DIO 1 Falling Edge bit for description.	R/W	0
5	DIO6_FALL	Enable IRQ at DIO 6 Falling Edge See the Enable IRQ at DIO 1 Falling Edge bit for description.	R/W	0
4	DIO5_FALL	Enable IRQ at DIO 5 Falling Edge See the Enable IRQ at DIO 1 Falling Edge bit for description.	R/W	0
3	DIO4_FALL	Enable IRQ at DIO 4 Falling Edge See the Enable IRQ at DIO 1 Falling Edge bit for description.	R/W	0
2	DIO3_FALL	Enable IRQ at DIO 3 Falling Edge See the Enable IRQ at DIO 1 Falling Edge bit for description.	R/W	0
1	DIO2_FALL	Enable IRQ at DIO 2 Falling Edge See the Enable IRQ at DIO 1 Falling Edge bit for description.	R/W	0
0	DIO1_FALL	Enable IRQ at DIO 1 Falling Edge 0: disabled 1: enabled If enabled, an interrupt is asserted when a falling edge is detected at DIO1.	R/W	0

Table 3-65: DIO Falling Edge Interrupt Enable Register

3.2.1.9.5 Interrupt Status Register (0x384)

Bit	Symbol	Description	Access	Reset Value
31	DIO_IRQ	DIO Interrupt Read DIO Interrupt Status Register for detailed interrupt status.	R	0
30	ERROR_IRQ	Error Interrupt Read Error Interrupt Status Register for detailed interrupt status.	R	0
29	FRAME_TIMER_IRQ	IRQ at Frame Timer event	R/C	0
28	FRAME_TRIG	IRQ at Frame Trigger	R/C	0
27	ADC4_DONE	IRQ after ADC4 Conversion is done (Manual Mode)	R/C	0
26	ADC3_DONE	IRQ after ADC3 Conversion is done (Manual Mode)	R/C	0
25	ADC2_DONE	IRQ after ADC2 Conversion is done (Manual Mode)	R/C	0
24	ADC1_DONE	IRQ after ADC1 Conversion is done (Manual Mode)	R/C	0
23:20	-	Reserved	-	-
19	DAC4_DONE	IRQ after DAC4 Conversion is done (Manual Mode) For TPMC533-20R: Reserved	R/C	0
18	DAC3_DONE	IRQ after DAC3 Conversion is done (Manual Mode) For TPMC533-20R: Reserved	R/C	0
17	DAC2_DONE	IRQ after DAC2 Conversion is done (Manual Mode) For TPMC533-20R: Reserved	R/C	0
16	DAC1_DONE	IRQ after DAC1 Conversion is done (Manual Mode) For TPMC533-20R: Reserved	R/C	0
15:13	-	Reserved	-	-
12	IU_CONV_DONE_IRQ	IRQ at Input Unit Number of Conversions done	R/C	0
11	-	Reserved	-	-
10:8	WR_DMA_TERM_IRQ	IRQ at ADC Sequencer DMA Buffer Termination	R/C	000
7:5	-	Reserved	-	-
4	OU_CONV_DONE_IRQ	IRQ at Output Unit Number of Conversions done For TPMC533-20R: Reserved	R/C	0
3:1	-	Reserved	-	-
0	RD_DMA_TERM_IRQ	IRQ at DAC Sequencer DMA Buffer Termination For TPMC533-20R: Reserved	R/C	0

Table 3-66: Interrupt Status Register

3.2.1.9.6 Error Interrupt Status Register (0x388)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27	IU_FRAME_ERR_IRQ	IRQ at ADC Sequencer Input Unit Frame Error	R/C	0
26	CONV_ERR_IRQ	IRQ at ADC Sequencer Input Unit Conversion Error	R/C	0
25	FIFO_OF_IRQ	IRQ at ADC Sequencer Input Unit FIFO Overflow Error	R/C	0
24	WR_DMA_ERR_IRQ	IRQ at ADC Sequencer DMA Error	R/C	0
23:20	-	Reserved	-	-
19	OU_FRAME_ERR_IRQ	IRQ at DAC Sequencer Output Unit Frame Error For TPMC533-20R: Reserved	R/C	0
18	TIMING_ERR_IRQ	IRQ at DAC Sequencer Output Unit DAC Timing Error For TPMC533-20R: Reserved	R/C	0
17	DATA_ERR_IRQ	IRQ at DAC Sequencer Output Unit Data Underrun Error For TPMC533-20R: Reserved	R/C	0
16	RD_DMA_ERR_IRQ	IRQ at DAC Sequencer DMA Error For TPMC533-20R: Reserved	R/C	0
15:4	-	Reserved	-	-
3	DAC4_ALERT	IRQ at DAC4 Alert For TPMC533-20R: Reserved	R/C	0
2	DAC3_ALERT	IRQ at DAC3 Alert For TPMC533-20R: Reserved	R/C	0
1	DAC2_ALERT	IRQ at DAC2 Alert For TPMC533-20R: Reserved	R/C	0
0	DAC1_ALERT	IRQ at DAC1 Alert For TPMC533-20R: Reserved	R/C	0

Table 3-67: Error Interrupt Status Register

3.2.1.9.7 DIO Interrupt Status Register (0x38C)

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	DIO8	IRQ at Digital I/O 8 Refer to the IRQ at Digital I/O 1 bit for description.	R/C	0
6	DIO7	IRQ at Digital I/O 7 Refer to the IRQ at Digital I/O 1 bit for description.	R/C	0
5	DIO6	IRQ at Digital I/O 6 Refer to the IRQ at Digital I/O 1 bit for description.	R/C	0
4	DIO5	IRQ at Digital I/O 5 Refer to the IRQ at Digital I/O 1 bit for description.	R/C	0
3	DIO4	IRQ at Digital I/O 4 Refer to the IRQ at Digital I/O 1 bit for description.	R/C	0
2	DIO3	IRQ at Digital I/O 3 Refer to the IRQ at Digital I/O 1 bit for description.	R/C	0
1	DIO2	IRQ at Digital I/O 2 Refer to the IRQ at Digital I/O 1 bit for description.	R/C	0
0	DIO1	IRQ at Digital I/O 1 Indicates a rising or/and falling edge at Digital I/O 1 depending on the configuration in the DIO Rising Edge Interrupt Enable Register and the DIO Falling Edge Interrupt Enable Register	R/C	0

Table 3-68: DIO Interrupt Status Register

3.2.1.10 Other Registers

3.2.1.10.1 Global Configuration Register (0x398)

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1	IRQ_ACK_CONF	Interrupt Acknowledge Configuration 0: a selected interrupt is cleared by writing a '1' to the corresponding bit in Interrupt Status Register, Error Interrupt Status Register or DIO Interrupt Status Register 1: all interrupts in an interrupt status register are cleared by reading Interrupt Status Register, Error Interrupt Status Register or DIO Interrupt Status Register	R/W	0
0	DMA_ENDIAN_CONF	DMA Endian Configuration Sets the Endian Mode for DMA access to Host RAM. 0: Little Endian Mode (16bit digital values are stored in Little Endian format in Host RAM) 1: Big Endian Mode (16bit digital values are stored in Big Endian format in Host RAM)	R/W	0

Table 3-69: Global Configuration Register

3.2.1.10.2 DIO Pull Resistors Register (0x39C)

All of the 8 Digital I/Os are connected to 4.7kΩ pull resistors. The voltage, the pull resistors are connected to, is programmable and can be configured to 3.3V, 5V, GND or floating level.

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1:0	VPULL_DIO	Digital I/O Pull Resistor Configuration VPULL_DIO: Pull Resistor Configuration 00: Floating 01: Pull-Ups to +5V 10: Pull-Ups to +3.3V 11: Pull-Downs to GND	R/W	00

Table 3-70: DIO Pull Resistor Register

Note that the default configuration for the Digital I/O Pull Resistors is floating.

3.2.1.10.3 P14 Back I/O Pull Resistors Register (0x3A0)

All P14 Back I/O Signals (Global Conversion Clock 1, Global Conversion Clock 2 and Global Frame Trigger) are connected to 4.7kΩ pull resistors. The voltage, the pull resistors are connected to, is programmable and can be configured to 3.3V, 5V, GND or floating level.

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1:0	VPULL_P14	P14 Back I/O Pull Resistor Configuration VPULL_P14: Pull Resistor Configuration 00: Floating 01: Pull-Ups to +5V 10: Pull-Ups to +3.3V 11: Pull-Downs to GND	R/W	00

Table 3-71: P14 Back I/O Pull Resistor Register

Note that the default configuration for the P14 Back I/O Pull Resistors is floating.

3.2.1.10.4 Correction Data EEPROM Control/Status Register (0x3A4)

Bit	Symbol	Description	Access	Reset Value
31:17	-	Reserved	-	-
16	EEBSY	Read-only Activity Status of the on-board Correction Data EEPROM 0: Correction Data loading is done 1: Correction Data loading in progress After power-up or PCI reset, the content of the Correction Data EEPROM is automatically copied to the Correction Data ROM. During this process, the EEBSY is set. The EEBSY bit is also set when the EELOCK nibble is changed from 0xABCD to a different value while data is written to (or read from) the EEPROM. Software should check that the EEBSY bit is '0' before reading data from the Correction Data ROM space.	R	0
15:0	EELOCK	Correction Data EEPROM Lock This nibble must be set to the value 0xABCD to allow write accesses to the Correction Data ROM. Writes to the Correction Data ROM are ignored while this nibble is not 0xABCD. When the value of this nibble is changed from 0xABCD to a different value, an automatic EEPROM update procedure is started: The content of the Correction Data ROM is stored in the on-board Correction Data EEPROM, and is immediately read back to the Correction Data ROM. The EEBSY bit is set during this procedure. Before setting the EELOCK nibble to 0xABCD, software should check that the EEBSY bit is clear.	R/W	0x0000

Table 3-72: Correction Data EEPROM Control/Status Register

3.2.1.10.5 Temperature Sensor Trigger Register (0x3A8)

This register is used to trigger a measurement of the on-board temperature sensor.

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1	AUTO	Temperature Sensor Auto Acquire Mode If this bit is set, the Temperature Sensor Data Register is automatically updated every second. If this bit is clear, the Temperature Sensor Trigger bit must be set for an update of the Temperature Sensor Data Register.	R/W	0
0	TRIG	Temperature Sensor Trigger Write '1' to start the temperature measurement of the on-board SE95 temperature sensor. This bit is cleared automatically when the data is valid in the Temperature Sensor Data Register.	R/S	0

Table 3-73: Temperature Sensor Trigger Register

3.2.1.10.6 Temperature Sensor Data Register (0x3AC)

This register holds the measured 13bit two's complement data of the on-board SE95 temperature sensor.

Bit	Symbol	Description	Access	Reset Value
31:0	TEMP	Measured data of the on-board temperature sensor The measured value of the temperature sensor is stored as a 32bit two's complement. To actually calculate the temperature from the two's complement data value, use the following formula: Temperature (°C) = TEMP/256	R	0x0000 0000

Table 3-74: Temperature Sensor Data Register

3.2.1.10.7 Firmware Version Register (0x3FC)

Bit	Symbol	Description	Access	Reset Value
31:0	FID	Major & minor version, revision and build number of the FPGA firmware.	R	-

Table 3-75: Firmware Version Register

3.2.2 Correction Data ROM

PCI Base Address Register 1 (Offset 0x14 in PCI Configuration Space).

The correction values are determined at factory and can be read from this space to write them to the ADC Correction Registers and DAC Correction Registers before the first conversion is performed.

There is an individual Offset Correction Value and an individual Gain Correction Value for each ADC Channel and each DAC Channel at each voltage range.

The correction values are loaded from a serial EEPROM on-board after power-up or PCI reset and are available approx. 8.6ms after PCI reset. To determine the moment the correction values are loaded completely from the EEPROM to the FPGA the EEBSY bit in the Correction Data EEPROM Control/Status Register can be polled.

Offset to BAR1	Description	Size (Bit)
Input Voltage Range: ±5 V		
0x000	ADC1 Channel A $Offset_{CORR}$	16
0x002	ADC1 Channel A $Gain_{CORR}$	16
0x004	ADC1 Channel B $Offset_{CORR}$	16
0x006	ADC1 Channel B $Gain_{CORR}$	16
0x008	ADC1 Channel C $Offset_{CORR}$	16
0x00A	ADC1 Channel C $Gain_{CORR}$	16
0x00C	ADC1 Channel D $Offset_{CORR}$	16
0x00E	ADC1 Channel D $Gain_{CORR}$	16
0x010	ADC1 Channel E $Offset_{CORR}$	16
0x012	ADC1 Channel E $Gain_{CORR}$	16
0x014	ADC1 Channel F $Offset_{CORR}$	16
0x016	ADC1 Channel F $Gain_{CORR}$	16
0x018	ADC1 Channel G $Offset_{CORR}$	16
0x01A	ADC1 Channel G $Gain_{CORR}$	16
0x01C	ADC1 Channel H $Offset_{CORR}$	16
0x01E	ADC1 Channel H $Gain_{CORR}$	16
0x020	ADC2 Channel A $Offset_{CORR}$	16
0x022	ADC2 Channel A $Gain_{CORR}$	16
0x024	ADC2 Channel B $Offset_{CORR}$	16
0x026	ADC2 Channel B $Gain_{CORR}$	16
0x028	ADC2 Channel C $Offset_{CORR}$	16
0x02A	ADC2 Channel C $Gain_{CORR}$	16
0x02C	ADC2 Channel D $Offset_{CORR}$	16
0x02E	ADC2 Channel D $Gain_{CORR}$	16
0x030	ADC2 Channel E $Offset_{CORR}$	16
0x032	ADC2 Channel E $Gain_{CORR}$	16

Offset to BAR1	Description	Size (Bit)
0x034	ADC2 Channel F $Offset_{CORR}$	16
0x036	ADC2 Channel F $Gain_{CORR}$	16
0x038	ADC2 Channel G $Offset_{CORR}$	16
0x03A	ADC2 Channel G $Gain_{CORR}$	16
0x03C	ADC2 Channel H $Offset_{CORR}$	16
0x03E	ADC2 Channel H $Gain_{CORR}$	16
0x040	ADC3 Channel A $Offset_{CORR}$	16
0x042	ADC3 Channel A $Gain_{CORR}$	16
0x044	ADC3 Channel B $Offset_{CORR}$	16
0x046	ADC3 Channel B $Gain_{CORR}$	16
0x048	ADC3 Channel C $Offset_{CORR}$	16
0x04A	ADC3 Channel C $Gain_{CORR}$	16
0x04C	ADC3 Channel D $Offset_{CORR}$	16
0x04E	ADC3 Channel D $Gain_{CORR}$	16
0x050	ADC3 Channel E $Offset_{CORR}$	16
0x052	ADC3 Channel E $Gain_{CORR}$	16
0x054	ADC3 Channel F $Offset_{CORR}$	16
0x056	ADC3 Channel F $Gain_{CORR}$	16
0x058	ADC3 Channel G $Offset_{CORR}$	16
0x05A	ADC3 Channel G $Gain_{CORR}$	16
0x05C	ADC3 Channel H $Offset_{CORR}$	16
0x05E	ADC3 Channel H $Gain_{CORR}$	16
0x060	ADC4 Channel A $Offset_{CORR}$	16
0x062	ADC4 Channel A $Gain_{CORR}$	16
0x064	ADC4 Channel B $Offset_{CORR}$	16
0x066	ADC4 Channel B $Gain_{CORR}$	16
0x068	ADC4 Channel C $Offset_{CORR}$	16
0x06A	ADC4 Channel C $Gain_{CORR}$	16
0x06C	ADC4 Channel D $Offset_{CORR}$	16
0x06E	ADC4 Channel D $Gain_{CORR}$	16
0x070	ADC4 Channel E $Offset_{CORR}$	16
0x072	ADC4 Channel E $Gain_{CORR}$	16
0x074	ADC4 Channel F $Offset_{CORR}$	16
0x076	ADC4 Channel F $Gain_{CORR}$	16
0x078	ADC4 Channel G $Offset_{CORR}$	16
0x07A	ADC4 Channel G $Gain_{CORR}$	16
0x07C	ADC4 Channel H $Offset_{CORR}$	16
0x07E	ADC4 Channel H $Gain_{CORR}$	16

Offset to BAR1	Description	Size (Bit)
Input Voltage Range: ±10 V		
0x080	ADC1 Channel A $Offset_{CORR}$	16
0x082	ADC1 Channel A $Gain_{CORR}$	16
0x084	ADC1 Channel B $Offset_{CORR}$	16
0x086	ADC1 Channel B $Gain_{CORR}$	16
0x088	ADC1 Channel C $Offset_{CORR}$	16
0x08A	ADC1 Channel C $Gain_{CORR}$	16
0x08C	ADC1 Channel D $Offset_{CORR}$	16
0x08E	ADC1 Channel D $Gain_{CORR}$	16
0x090	ADC1 Channel E $Offset_{CORR}$	16
0x092	ADC1 Channel E $Gain_{CORR}$	16
0x094	ADC1 Channel F $Offset_{CORR}$	16
0x096	ADC1 Channel F $Gain_{CORR}$	16
0x098	ADC1 Channel G $Offset_{CORR}$	16
0x09A	ADC1 Channel G $Gain_{CORR}$	16
0x09C	ADC1 Channel H $Offset_{CORR}$	16
0x09E	ADC1 Channel H $Gain_{CORR}$	16
0x0A0	ADC2 Channel A $Offset_{CORR}$	16
0x0A2	ADC2 Channel A $Gain_{CORR}$	16
0x0A4	ADC2 Channel B $Offset_{CORR}$	16
0x0A6	ADC2 Channel B $Gain_{CORR}$	16
0x0A8	ADC2 Channel C $Offset_{CORR}$	16
0x0AA	ADC2 Channel C $Gain_{CORR}$	16
0x0AC	ADC2 Channel D $Offset_{CORR}$	16
0x0AE	ADC2 Channel D $Gain_{CORR}$	16
0x0B0	ADC2 Channel E $Offset_{CORR}$	16
0x0B2	ADC2 Channel E $Gain_{CORR}$	16
0x0B4	ADC2 Channel F $Offset_{CORR}$	16
0x0B6	ADC2 Channel F $Gain_{CORR}$	16
0x0B8	ADC2 Channel G $Offset_{CORR}$	16
0x0BA	ADC2 Channel G $Gain_{CORR}$	16
0x0BC	ADC2 Channel H $Offset_{CORR}$	16
0x0BE	ADC2 Channel H $Gain_{CORR}$	16
0x0C0	ADC3 Channel A $Offset_{CORR}$	16
0x0C2	ADC3 Channel A $Gain_{CORR}$	16
0x0C4	ADC3 Channel B $Offset_{CORR}$	16
0x0C6	ADC3 Channel B $Gain_{CORR}$	16
0x0C8	ADC3 Channel C $Offset_{CORR}$	16
0x0CA	ADC3 Channel C $Gain_{CORR}$	16
0x0CC	ADC3 Channel D $Offset_{CORR}$	16

Offset to BAR1	Description	Size (Bit)
0x0CE	ADC3 Channel D $Gain_{CORR}$	16
0x0D0	ADC3 Channel E $Offset_{CORR}$	16
0x0D2	ADC3 Channel E $Gain_{CORR}$	16
0x0D4	ADC3 Channel F $Offset_{CORR}$	16
0x0D6	ADC3 Channel F $Gain_{CORR}$	16
0x0D8	ADC3 Channel G $Offset_{CORR}$	16
0x0DA	ADC3 Channel G $Gain_{CORR}$	16
0x0DC	ADC3 Channel H $Offset_{CORR}$	16
0x0DE	ADC3 Channel H $Gain_{CORR}$	16
0x0E0	ADC4 Channel A $Offset_{CORR}$	16
0x0E2	ADC4 Channel A $Gain_{CORR}$	16
0x0E4	ADC4 Channel B $Offset_{CORR}$	16
0x0E6	ADC4 Channel B $Gain_{CORR}$	16
0x0E8	ADC4 Channel C $Offset_{CORR}$	16
0x0EA	ADC4 Channel C $Gain_{CORR}$	16
0x0EC	ADC4 Channel D $Offset_{CORR}$	16
0x0EE	ADC4 Channel D $Gain_{CORR}$	16
0x0F0	ADC4 Channel E $Offset_{CORR}$	16
0x0F2	ADC4 Channel E $Gain_{CORR}$	16
0x0F4	ADC4 Channel F $Offset_{CORR}$	16
0x0F6	ADC4 Channel F $Gain_{CORR}$	16
0x0F8	ADC4 Channel G $Offset_{CORR}$	16
0x0FA	ADC4 Channel G $Gain_{CORR}$	16
0x0FC	ADC4 Channel H $Offset_{CORR}$	16
0x0FE	ADC4 Channel H $Gain_{CORR}$	16

Offset to BAR1	Description	Size (Bit)
Output Voltage Range: +5 V		
0x100	DAC1 Channel A $Offset_{CORR}$	16
0x102	DAC1 Channel A $Gain_{CORR}$	16
0x104	DAC1 Channel B $Offset_{CORR}$	16
0x106	DAC1 Channel B $Gain_{CORR}$	16
0x108	DAC1 Channel C $Offset_{CORR}$	16
0x10A	DAC1 Channel C $Gain_{CORR}$	16
0x10C	DAC1 Channel D $Offset_{CORR}$	16
0x10E	DAC1 Channel D $Gain_{CORR}$	16
0x110	DAC2 Channel A $Offset_{CORR}$	16
0x112	DAC2 Channel A $Gain_{CORR}$	16
0x114	DAC2 Channel B $Offset_{CORR}$	16
0x116	DAC2 Channel B $Gain_{CORR}$	16
0x118	DAC2 Channel C $Offset_{CORR}$	16
0x11A	DAC2 Channel C $Gain_{CORR}$	16
0x11C	DAC2 Channel D $Offset_{CORR}$	16
0x11E	DAC2 Channel D $Gain_{CORR}$	16
0x120	DAC3 Channel A $Offset_{CORR}$	16
0x122	DAC3 Channel A $Gain_{CORR}$	16
0x124	DAC3 Channel B $Offset_{CORR}$	16
0x126	DAC3 Channel B $Gain_{CORR}$	16
0x128	DAC3 Channel C $Offset_{CORR}$	16
0x12A	DAC3 Channel C $Gain_{CORR}$	16
0x12C	DAC3 Channel D $Offset_{CORR}$	16
0x12E	DAC3 Channel D $Gain_{CORR}$	16
0x130	DAC4 Channel A $Offset_{CORR}$	16
0x132	DAC4 Channel A $Gain_{CORR}$	16
0x134	DAC4 Channel B $Offset_{CORR}$	16
0x136	DAC4 Channel B $Gain_{CORR}$	16
0x138	DAC4 Channel C $Offset_{CORR}$	16
0x13A	DAC4 Channel C $Gain_{CORR}$	16
0x13C	DAC4 Channel D $Offset_{CORR}$	16
0x13E	DAC4 Channel D $Gain_{CORR}$	16
0x140 to 0x17E	Reserved	-

Offset to BAR1	Description	Size (Bit)
Output Voltage Range: +10 V		
0x180	DAC1 Channel A $Offset_{CORR}$	16
0x182	DAC1 Channel A $Gain_{CORR}$	16
0x184	DAC1 Channel B $Offset_{CORR}$	16
0x186	DAC1 Channel B $Gain_{CORR}$	16
0x188	DAC1 Channel C $Offset_{CORR}$	16
0x18A	DAC1 Channel C $Gain_{CORR}$	16
0x18C	DAC1 Channel D $Offset_{CORR}$	16
0x18E	DAC1 Channel D $Gain_{CORR}$	16
0x190	DAC2 Channel A $Offset_{CORR}$	16
0x192	DAC2 Channel A $Gain_{CORR}$	16
0x194	DAC2 Channel B $Offset_{CORR}$	16
0x196	DAC2 Channel B $Gain_{CORR}$	16
0x198	DAC2 Channel C $Offset_{CORR}$	16
0x19A	DAC2 Channel C $Gain_{CORR}$	16
0x19C	DAC2 Channel D $Offset_{CORR}$	16
0x19E	DAC2 Channel D $Gain_{CORR}$	16
0x1A0	DAC3 Channel A $Offset_{CORR}$	16
0x1A2	DAC3 Channel A $Gain_{CORR}$	16
0x1A4	DAC3 Channel B $Offset_{CORR}$	16
0x1A6	DAC3 Channel B $Gain_{CORR}$	16
0x1A8	DAC3 Channel C $Offset_{CORR}$	16
0x1AA	DAC3 Channel C $Gain_{CORR}$	16
0x1AC	DAC3 Channel D $Offset_{CORR}$	16
0x1AE	DAC3 Channel D $Gain_{CORR}$	16
0x1B0	DAC4 Channel A $Offset_{CORR}$	16
0x1B2	DAC4 Channel A $Gain_{CORR}$	16
0x1B4	DAC4 Channel B $Offset_{CORR}$	16
0x1B6	DAC4 Channel B $Gain_{CORR}$	16
0x1B8	DAC4 Channel C $Offset_{CORR}$	16
0x1BA	DAC4 Channel C $Gain_{CORR}$	16
0x1BC	DAC4 Channel D $Offset_{CORR}$	16
0x1BE	DAC4 Channel D $Gain_{CORR}$	16
0x1C0 to 0x1FE	Reserved	-

Offset to BAR1	Description	Size (Bit)
Output Voltage Range: +10.8 V		
0x200	DAC1 Channel A $Offset_{CORR}$	16
0x202	DAC1 Channel A $Gain_{CORR}$	16
0x204	DAC1 Channel B $Offset_{CORR}$	16
0x206	DAC1 Channel B $Gain_{CORR}$	16
0x208	DAC1 Channel C $Offset_{CORR}$	16
0x20A	DAC1 Channel C $Gain_{CORR}$	16
0x20C	DAC1 Channel D $Offset_{CORR}$	16
0x20E	DAC1 Channel D $Gain_{CORR}$	16
0x210	DAC2 Channel A $Offset_{CORR}$	16
0x212	DAC2 Channel A $Gain_{CORR}$	16
0x214	DAC2 Channel B $Offset_{CORR}$	16
0x216	DAC2 Channel B $Gain_{CORR}$	16
0x218	DAC2 Channel C $Offset_{CORR}$	16
0x21A	DAC2 Channel C $Gain_{CORR}$	16
0x21C	DAC2 Channel D $Offset_{CORR}$	16
0x21E	DAC2 Channel D $Gain_{CORR}$	16
0x220	DAC3 Channel A $Offset_{CORR}$	16
0x222	DAC3 Channel A $Gain_{CORR}$	16
0x224	DAC3 Channel B $Offset_{CORR}$	16
0x226	DAC3 Channel B $Gain_{CORR}$	16
0x228	DAC3 Channel C $Offset_{CORR}$	16
0x22A	DAC3 Channel C $Gain_{CORR}$	16
0x22C	DAC3 Channel D $Offset_{CORR}$	16
0x22E	DAC3 Channel D $Gain_{CORR}$	16
0x230	DAC4 Channel A $Offset_{CORR}$	16
0x232	DAC4 Channel A $Gain_{CORR}$	16
0x234	DAC4 Channel B $Offset_{CORR}$	16
0x236	DAC4 Channel B $Gain_{CORR}$	16
0x238	DAC4 Channel C $Offset_{CORR}$	16
0x23A	DAC4 Channel C $Gain_{CORR}$	16
0x23C	DAC4 Channel D $Offset_{CORR}$	16
0x23E	DAC4 Channel D $Gain_{CORR}$	16
0x240 to 0x27E	Reserved	-

Offset to BAR1	Description	Size (Bit)
Output Voltage Range: ±5 V		
0x280	DAC1 Channel A $Offset_{CORR}$	16
0x282	DAC1 Channel A $Gain_{CORR}$	16
0x284	DAC1 Channel B $Offset_{CORR}$	16
0x286	DAC1 Channel B $Gain_{CORR}$	16
0x288	DAC1 Channel C $Offset_{CORR}$	16
0x28A	DAC1 Channel C $Gain_{CORR}$	16
0x28C	DAC1 Channel D $Offset_{CORR}$	16
0x28E	DAC1 Channel D $Gain_{CORR}$	16
0x290	DAC2 Channel A $Offset_{CORR}$	16
0x292	DAC2 Channel A $Gain_{CORR}$	16
0x294	DAC2 Channel B $Offset_{CORR}$	16
0x296	DAC2 Channel B $Gain_{CORR}$	16
0x298	DAC2 Channel C $Offset_{CORR}$	16
0x29A	DAC2 Channel C $Gain_{CORR}$	16
0x29C	DAC2 Channel D $Offset_{CORR}$	16
0x29E	DAC2 Channel D $Gain_{CORR}$	16
0x2A0	DAC3 Channel A $Offset_{CORR}$	16
0x2A2	DAC3 Channel A $Gain_{CORR}$	16
0x2A4	DAC3 Channel B $Offset_{CORR}$	16
0x2A6	DAC3 Channel B $Gain_{CORR}$	16
0x2A8	DAC3 Channel C $Offset_{CORR}$	16
0x2AA	DAC3 Channel C $Gain_{CORR}$	16
0x2AC	DAC3 Channel D $Offset_{CORR}$	16
0x2AE	DAC3 Channel D $Gain_{CORR}$	16
0x2B0	DAC4 Channel A $Offset_{CORR}$	16
0x2B2	DAC4 Channel A $Gain_{CORR}$	16
0x2B4	DAC4 Channel B $Offset_{CORR}$	16
0x2B6	DAC4 Channel B $Gain_{CORR}$	16
0x2B8	DAC4 Channel C $Offset_{CORR}$	16
0x2BA	DAC4 Channel C $Gain_{CORR}$	16
0x2BC	DAC4 Channel D $Offset_{CORR}$	16
0x2BE	DAC4 Channel D $Gain_{CORR}$	16
0x2C0 to 0x2FE	Reserved	-

Offset to BAR1	Description	Size (Bit)
Output Voltage Range: ±10 V		
0x300	DAC1 Channel A $Offset_{CORR}$	16
0x302	DAC1 Channel A $Gain_{CORR}$	16
0x304	DAC1 Channel B $Offset_{CORR}$	16
0x306	DAC1 Channel B $Gain_{CORR}$	16
0x308	DAC1 Channel C $Offset_{CORR}$	16
0x30A	DAC1 Channel C $Gain_{CORR}$	16
0x30C	DAC1 Channel D $Offset_{CORR}$	16
0x30E	DAC1 Channel D $Gain_{CORR}$	16
0x310	DAC2 Channel A $Offset_{CORR}$	16
0x312	DAC2 Channel A $Gain_{CORR}$	16
0x314	DAC2 Channel B $Offset_{CORR}$	16
0x316	DAC2 Channel B $Gain_{CORR}$	16
0x318	DAC2 Channel C $Offset_{CORR}$	16
0x31A	DAC2 Channel C $Gain_{CORR}$	16
0x31C	DAC2 Channel D $Offset_{CORR}$	16
0x31E	DAC2 Channel D $Gain_{CORR}$	16
0x320	DAC3 Channel A $Offset_{CORR}$	16
0x322	DAC3 Channel A $Gain_{CORR}$	16
0x324	DAC3 Channel B $Offset_{CORR}$	16
0x326	DAC3 Channel B $Gain_{CORR}$	16
0x328	DAC3 Channel C $Offset_{CORR}$	16
0x32A	DAC3 Channel C $Gain_{CORR}$	16
0x32C	DAC3 Channel D $Offset_{CORR}$	16
0x32E	DAC3 Channel D $Gain_{CORR}$	16
0x330	DAC4 Channel A $Offset_{CORR}$	16
0x332	DAC4 Channel A $Gain_{CORR}$	16
0x334	DAC4 Channel B $Offset_{CORR}$	16
0x336	DAC4 Channel B $Gain_{CORR}$	16
0x338	DAC4 Channel C $Offset_{CORR}$	16
0x33A	DAC4 Channel C $Gain_{CORR}$	16
0x33C	DAC4 Channel D $Offset_{CORR}$	16
0x33E	DAC4 Channel D $Gain_{CORR}$	16
0x340 to 0x37E	Reserved	-

Offset to BAR1	Description	Size (Bit)
Output Voltage Range: ±10.8 V		
0x380	DAC1 Channel A $Offset_{CORR}$	16
0x382	DAC1 Channel A $Gain_{CORR}$	16
0x384	DAC1 Channel B $Offset_{CORR}$	16
0x386	DAC1 Channel B $Gain_{CORR}$	16
0x388	DAC1 Channel C $Offset_{CORR}$	16
0x38A	DAC1 Channel C $Gain_{CORR}$	16
0x38C	DAC1 Channel D $Offset_{CORR}$	16
0x38E	DAC1 Channel D $Gain_{CORR}$	16
0x390	DAC2 Channel A $Offset_{CORR}$	16
0x392	DAC2 Channel A $Gain_{CORR}$	16
0x394	DAC2 Channel B $Offset_{CORR}$	16
0x396	DAC2 Channel B $Gain_{CORR}$	16
0x398	DAC2 Channel C $Offset_{CORR}$	16
0x39A	DAC2 Channel C $Gain_{CORR}$	16
0x39C	DAC2 Channel D $Offset_{CORR}$	16
0x39E	DAC2 Channel D $Gain_{CORR}$	16
0x3A0	DAC3 Channel A $Offset_{CORR}$	16
0x3A2	DAC3 Channel A $Gain_{CORR}$	16
0x3A4	DAC3 Channel B $Offset_{CORR}$	16
0x3A6	DAC3 Channel B $Gain_{CORR}$	16
0x3A8	DAC3 Channel C $Offset_{CORR}$	16
0x3AA	DAC3 Channel C $Gain_{CORR}$	16
0x3AC	DAC3 Channel D $Offset_{CORR}$	16
0x3AE	DAC3 Channel D $Gain_{CORR}$	16
0x3B0	DAC4 Channel A $Offset_{CORR}$	16
0x3B2	DAC4 Channel A $Gain_{CORR}$	16
0x3B4	DAC4 Channel B $Offset_{CORR}$	16
0x3B6	DAC4 Channel B $Gain_{CORR}$	16
0x3B8	DAC4 Channel C $Offset_{CORR}$	16
0x3BA	DAC4 Channel C $Gain_{CORR}$	16
0x3BC	DAC4 Channel D $Offset_{CORR}$	16
0x3BE	DAC4 Channel D $Gain_{CORR}$	16
0x3C0 to 0x7FA	Reserved	-

Offset to BAR1	Description	Size (Bit)
	Serial Number	
0x7FC	Serial Number High Word	16
0x7FE	Serial Number Low Word	16

Table 3-76: Correction Data ROM

For the TPMC533-20R the correction values for the DACs are reserved.

4 I/O Electrical Interface

4.1 ADC

The TPMC533 provides thirty-two true differential analog input channels (ADC Channels) available at the Front I/O Connector.

Analog Devices AD7609 are used for the analog inputs. Each AD7609 provides eight 16Bit differential ADC channels (ADC Channels A-H).

- Both, the TPMC533-10R and the TPMC533-20R order option, provide four AD7609 (ADC1, ADC2, ADC3 & ADC4)
  → thirty-two analog input channels

Protection	7kV ESD rating ±16.5V Overvoltage Clamp Protection
Input Type	True bipolar differential
Input Impedance	1MΩ
Input Capacitance	5pF
Maximum Ground related Input Voltage	±5V and ±10V
Full Scale Range	±10V and ±20V
Common-Mode Input Range	±4V
Sample Rate	200kSPS

Table 4-1 : ADC Electrical Interface

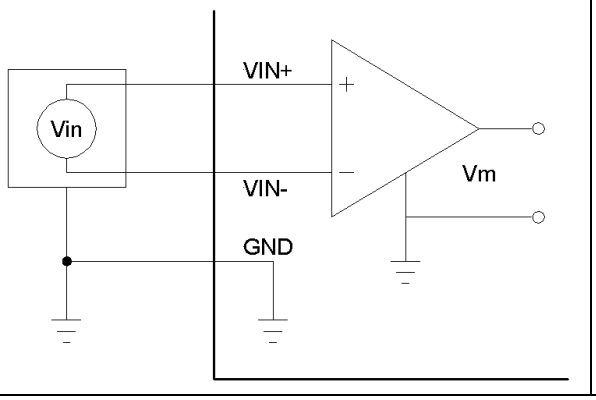
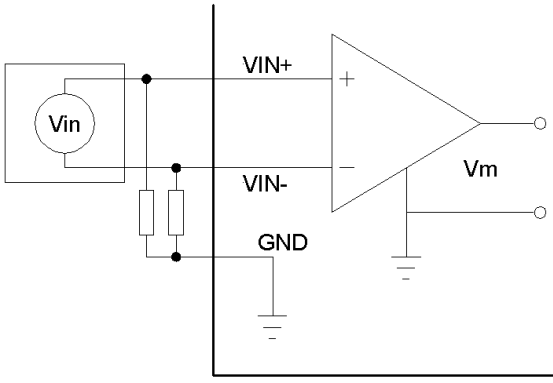
Differential with Ground Reference	Differential without Ground Reference
	

Table 4-2 : ADC Input Schemes

If signals without a ground reference shall be connected to TPMC533, connect VIN+ and VIN- to GND with a resistor to prevent the signal source to float out of the ADC's common-mode range. In most cases the VIN- connection suffices.

Unused ADC channels should be connected to GND.

4.2 DAC

The TPMC533 provides up to sixteen analog output channels (DAC Channels) available at the Front I/O Connector.

Analog Devices AD5754R are used for the analog outputs. Each AD5754R provides four 16Bit single-ended DAC channels (DAC Channels A-D).

- The TPMC533-10R order option provides four AD5754R (DAC1, DAC2, DAC3 & DAC4)
  → sixteen analog output channels
- The TPMC533-20R order option does not provide any AD5754R
  → zero analog output channels

Protection	3.5kV ESD rating 20mA current limit
Output Type	unipolar/bipolar single-ended
Output Voltage Ranges	±5V, ±10V, ±10,8V, +5V, +10V and +10.8V
DC Output Impedance	0.5Ω
Maximum Load	2kΩ
Capacitive Load	4000pF
Settling Time	10µs

Table 4-3 : DAC Electrical Interface

The TPMC533 provides an “Automatic Channel Power-Down” feature for the DACs.

In case of a DAC Channel overcurrent condition, the DAC Channel is powered down and its output is clamped to ground with a resistance of ~4 kΩ. This condition is indicated by the DACx_OCx bit set to ‘1’ and the DACx_PUx set to ‘0’ in the corresponding DAC Status Register.

The channel can be powered up again by setting the DACx_PU_x bit in the corresponding DAC Configuration Register back to ‘1’ after the overload condition is removed.

4.3 Digital I/O and P14 Back I/O

Each of the 8 Digital I/O lines on the Front I/O connector and each of the Global Conversion Signals on P14 Back I/O is realized by separated input and output buffers with a 4.7kΩ pull resistor which can be used for tri-state output functionality for example.

Additionally, each signal is equipped with an electronic protection array for ESD protection.

Protection	±15kV ESD protection
Driver Level	LVTTL (3.3V)
Receiver	5V tolerant
Source current per line	15mA
Sink current per line	6mA

Table 4-4 : Digital I/O and P14 Back I/O Electrical Interface

See the following figure for more information of the electrical circuitry.

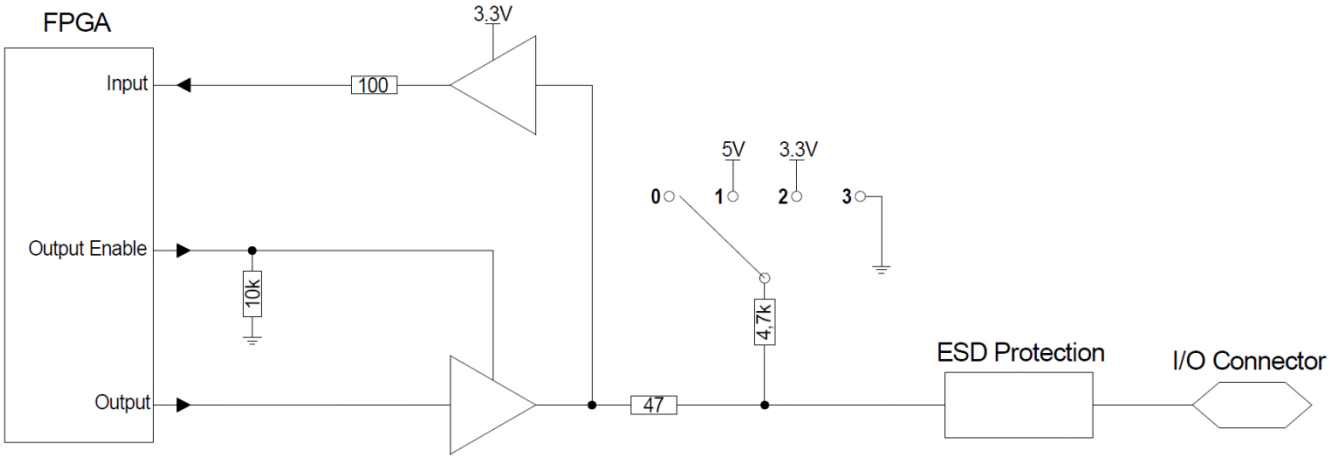


Figure 4-1 : Digital I/O and P14 Back I/O Scheme

At power-up and after reset all Digital I/O and P14 Back I/O lines are configured as inputs. The pull resistors are left floating (but they are still connected to each other) and have to be configured by software whether to operate as pull-downs to GND or as pull-ups to +3.3V or +5V. This pull resistor setting can be configured individually for DIO Front I/O and for P14 Back I/O.

The receiver function is always available and may be used to monitor the Digital I/O line level even when the line is operating as an output.

To achieve a 5V CMOS high-level (V_{OH} ≥ 3.5V), the external load must be high impedance and the pull resistors must be configured to +5V pull-ups. The corresponding bit in the DIO Output Register must be set to '0' while the DIO output level is controlled via the corresponding bit in the DIO Output Enable Register ('disabled' means logic high). To maintain a proper 5V CMOS high-level, the external load (leakage) current should not exceed 250µA.

Each Digital I/O input is capable of generating an interrupt on either rising edge or falling edge and a debounce filter can be configured to get rid of bounce on the Digital I/O Inputs.

5 Data Coding

5.1 ADC

Because of the ADC's true differential inputs, the ADC Data Coding differs significantly from a single-ended ADC's data coding.

Analogue to single-ended inputs, the Input Voltage Range setting directly describes the input voltage range of ground related voltages that can be tied to the ADC differential inputs.

But with true differential inputs this results in an extended input voltage range, since the ADC measures the voltage between the differential inputs ADCx Channel X+ and ADCx Channel X-.

An Example: The Input Voltage Range is ±10 V, so the allowed (single ended, ground related) voltage on each ADC input pin is ±10 V. When we examine the two largest differential voltages, we get the following results:

ADCx Channel X+ (ground related input voltage)	ADCx Channel X- (ground related input voltage)	ADC Input Value (differential input voltage)
+10 V	-10 V	+20 V
-10 V	+10 V	-20 V

Table 5-1 : ADC Data Coding Example

The example shows that the range of differential ADC input values is -20 V to +20 V, which results in a Full Scale Range of 40 V for the ±10 V Input Voltage Range setting. Similar, the Full Scale Range for the ±5 V Input Voltage Range setting is 20 V.

The data coding is two's complement.

Description	±5 V	±10 V	Digital Code
Full Scale Range	20 V	40 V	
Least Significant Bit	305.18 µV	610.35 µV	
Full Scale (pos.)	9.999695 V	19.99939 V	0x7FFF
FSR - 1LSB	9.99939 V	19.99878 V	0x7FFE
Midscale + 1LSB	305.18 µV	610.35 µV	0x0001
Midscale	0 V	0 V	0x0000
Midscale – 1LSB	-305.18 µV	-610.35 µV	0xFFFF
-FSR + 1LSB	-9.999695 V	-19.99939 V	0x8001
Full Scale (neg.)	-10 V	-20 V	0x8000

Table 5-2 : ADC Data Coding, Bipolar Input Range

5.2 DAC

For unipolar output ranges, the data coding is straight binary.

Description	+5 V	+10 V	+10.8 V	Digital Code
Full Scale Range	+5 V	+10 V	+10.8 V	
Least Significant Bit	76.295 µV	152.59 µV	164.79 µV	
Full Scale (pos.)	4.999924 V	9.999847 V	10.799835 V	0xFFFF
FSR - 1LSB	4.999847 V	9.999695 V	10.79967 V	0xFFFE
Midscale + 1LSB	2.500076 V	5.000153 V	5.400165 V	0x8001
Midscale	2.5 V	5 V	5.4 V	0x8000
Midscale – 1LSB	2.499924 V	4.999847 V	5.399835 V	0x7FFF
-FSR + 1LSB	76.295 µV	152.59 µV	164.79 µV	0x0001
Full Scale (neg.)	0 V	0 V	0 V	0x0000

Table 5-3 : DAC Data Coding, Unipolar Output Range

For bipolar output ranges, the data coding is two's complement.

Description	±5 V	±10 V	±10.8 V	Digital Code
Full Scale Range	±5 V	±10 V	±10.8 V	
Least Significant Bit	152.59 µV	305.18 µV	329.59 µV	
Full Scale (pos.)	4.999847 V	9.999695 V	10.79967 V	0x7FFF
FSR - 1LSB	4.999695 V	9.99939 V	10.79934 V	0x7FFE
Midscale + 1LSB	152.59 µV	305.18 µV	329.59 µV	0x0001
Midscale	0 V	0 V	0 V	0x0000
Midscale – 1LSB	-152.59 µV	-305.18 µV	-329.59 µV	0xFFFF
-FSR + 1LSB	-4.999847 V	-9.999695 V	-10.79967 V	0x8001
Full Scale (neg.)	-5 V	-10 V	-10.8 V	0x8000

Table 5-4 : DAC Data Coding, Bipolar Output Range

6 Correction Data

In the Correction Data ROM, there is an individual Offset Correction Value and an individual Gain Correction Value for each ADC Channel and for each DAC Channel at each voltage range.

The formula that is applied by the TPMC533 when ADC Data or DAC Data is corrected with the corresponding correction values stored in the Correction Data ROM is:

$$Data\_Corrected = Data \cdot \left(1 - \frac{Gain_{CORR}}{262144}\right) - \frac{Offset_{CORR}}{4}$$

- *Data* is the digital value that would be used if the ADC Channels and DAC Channels were ideal
- *Data_Corrected* is the corrected digital value that has to be used with the real ADC Channels and DAC Channels
- $Gain_{CORR}$ and $Offset_{CORR}$ are the correction values from the Correction Data ROM

The correction values are stored as two's complement 16bit wide values in the range from –32768 to +32767. For higher accuracy they are scaled to ¼ LSB. No correction is performed for $Gain_{CORR}$ = 0 and $Offset_{CORR}$ = 0.

To enable data correction performed by the TPMC533 firmware, the software must read the corresponding gain and offset correction values for the desired ADC/DAC Channel and voltage range from the Correction Data ROM and write the values to the corresponding ADC Correction Register or DAC Correction Register.

7 Operating Modes

The ADC Mode Registers and the DAC Mode Registers determine whether an ADC (all eight ADC Channels of the corresponding ADC) or a DAC (all four DAC Channels of the corresponding DAC) operate in "Manual Mode" or in "Sequencer Mode".

7.1 Manual Mode

In Manual Mode, analog-to-digital conversions and digital-to-analog conversions are requested by software commands (there is no periodic conversion rate).

ADC Data is only read manually from ADC Data Registers and DAC Data, that shall be converted, is only written manually to DAC Data Registers.

For the DACs there are two different ways of performing manual digital-to-analog conversions: "Immediate Conversion" and "Controlled Conversion".

7.1.1 DAC Immediate Conversion

If set to Immediate Conversion, a DAC Channel is updated immediately after a DAC Data transfer. Writing to the DAC Data Registers transfers the data to the DACs and also initiates the analog output update afterwards. The DACx Busy bits in the Global DAC Status Register may be used as an indication whether the analog output update is already completed.

"Immediate Conversion" is the most simple conversion mode. However, it is not suitable for simultaneous digital-to-analog conversions.

7.1.2 DAC Controlled Conversion

If set to Controlled Conversion, the four DAC Channels of a DAC are updated simultaneously by a write to the Global DAC Control Register. Writing to the DAC Data Registers does not automatically initiate an analog output update.

As the Conversion Request bits of all DACs are combined in the Global DAC Control Register, all DAC Channels of the TPMC533 can perform their digital-to-analog conversions simultaneously. Of course, DAC Data must have been written to DAC Data Registers before.

7.2 Sequencer Mode

In Sequencer Mode, analog-to-digital conversions and digital-to-analog conversions are performed periodically and equidistant at a configurable conversion rate.

All ADCs/DACs configured to Sequencer Mode in their corresponding ADC/DAC Mode Registers are always performing their conversions simultaneously.

For each conversion, **all eight ADC Channels** of each ADC assigned to the ADC Sequencer and **all four DAC Channels** of each DAC assigned to the DAC Sequencer are sampled.

The ADC Sequencer periodically writes ADC Data, which has just been sampled, into Host RAM and the DAC Sequencer periodically reads DAC Data, which shall be converted, from Host RAM.

The ADC Sequencer and the DAC Sequencer may operate in Normal Mode or Frame Mode, which is configured in the ADC Sequencer Control Register or the DAC Sequencer Control Register.

7.2.1 Normal Mode

Normal Mode is used for generating a single block of equidistant conversions or for generating continuous equidistant conversions by software request.

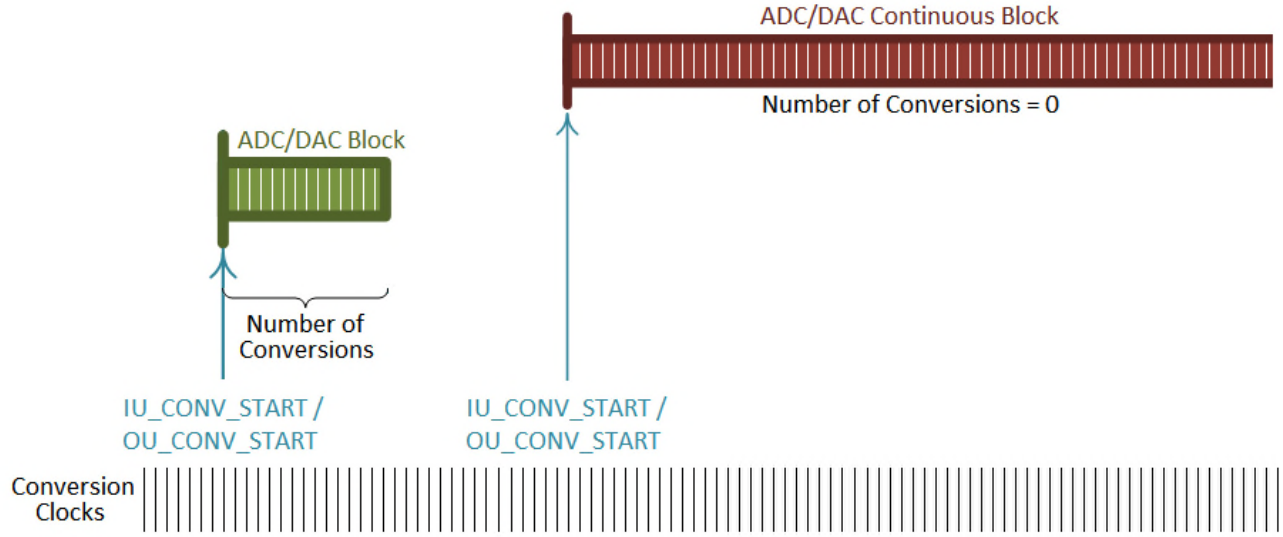


Figure 7-1 : Normal Mode

The configured Number of Conversions is performed starting with the next Conversion Clock after the IU_CONV_START bit (ADC Sequencer) or the OU_CONV_START bit (DAC Sequencer) has been set by software. Setting the Number of Conversions to 0 results in continuous conversions.

The IU_CONV_START and OU_CONV_START bits are synchronized internally to the Sequencer's selected Conversion Clock. They may be set while the Conversion Clock is already running (illustrated in the following figure) or before the Conversion Clock generation is enabled in the Conversion Signals Generator Enable Register.

The first falling Conversion Clock edge after the first rising Conversion Clock edge after the bit is set, triggers the first conversion.

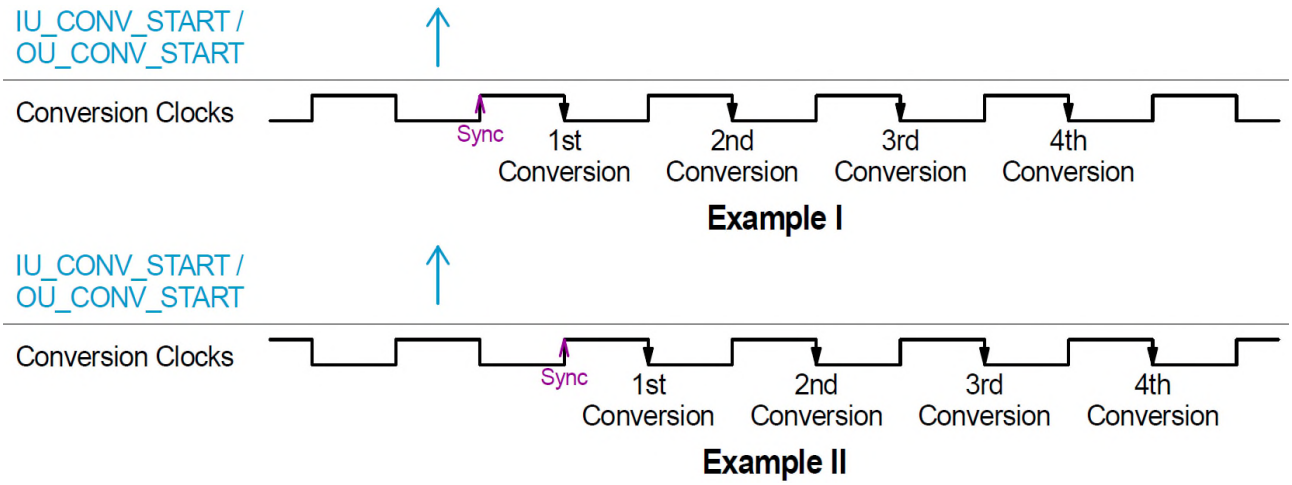


Figure 7-2 : Timing in Normal Mode

7.2.2 Frame Mode

Frame Mode is used for generating repetitive frames of conversions triggered by a Frame Trigger at a configurable Frame Trigger Rate. It can be used to synchronize ADC Frames and DAC Frames, for example.

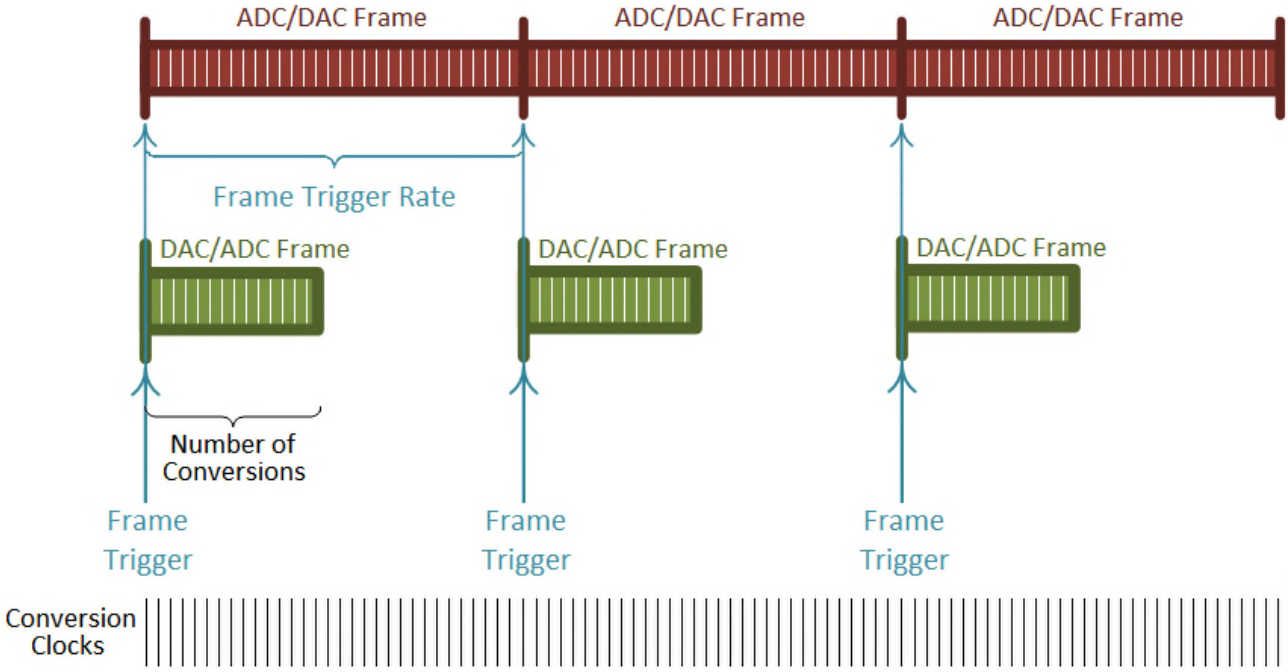


Figure 7-3 : Frame Mode

- The Number of Conversions Registers of both, the ADC Sequencer and the DAC Sequencer, define how many conversions are performed (per Frame) after a Frame Trigger occurs. This means ADCs and DACs can perform a different Number of Conversions per Frame.
- The Conversion Clock 1 or Conversion Clock 2 Register defines the Conversion Rate
- The Frame Trigger Generator Register 1 defines the Frame Trigger Rate by either selecting Conversion Clock 1 or Conversion Clock 2 for Frame Trigger creation and additionally defining how many of the selected Conversions Clocks shall occur between two Frame Triggers
- The Frame Trigger Generator Register 2 defines the number of Frame Triggers that shall be generated
- The Conversion Signals Generator Enable Register starts the creation of Frame Triggers and Conversion Clocks

Alternatively, the Frame Trigger and the Conversion Clock can be input from either P14 Back I/O or from Front I/O, which is configured in the Conversion Signals Source Selection Register.

Each Sequencer, either on-board or on other boards when performing multi-board synchronization, needs to set its Number of Conversion in the corresponding register; Even if the Number of Conversions is the same for all sequencers.

The first falling Conversion Clock edge after the Frame Trigger triggers the first conversion of each frame.

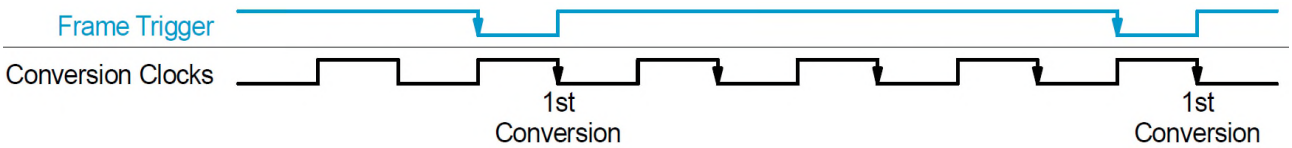


Figure 7-4 : Timing in Frame Mode

8 Sequencer

To be able to periodically sample analog values with ADCs or to periodically output analog values with DACs, "Sequencers" can be used.

Each ADC may be assigned to the ADC Sequencer by configuring it to operate in Sequencer Mode in its corresponding ADC Mode Register. Each DAC may be assigned to the DAC Sequencer by configuring it to operate in Sequencer Mode in its corresponding DAC Mode Register.

A Sequencer consists of an Input/Output Unit, a FIFO and a DMA Controller.

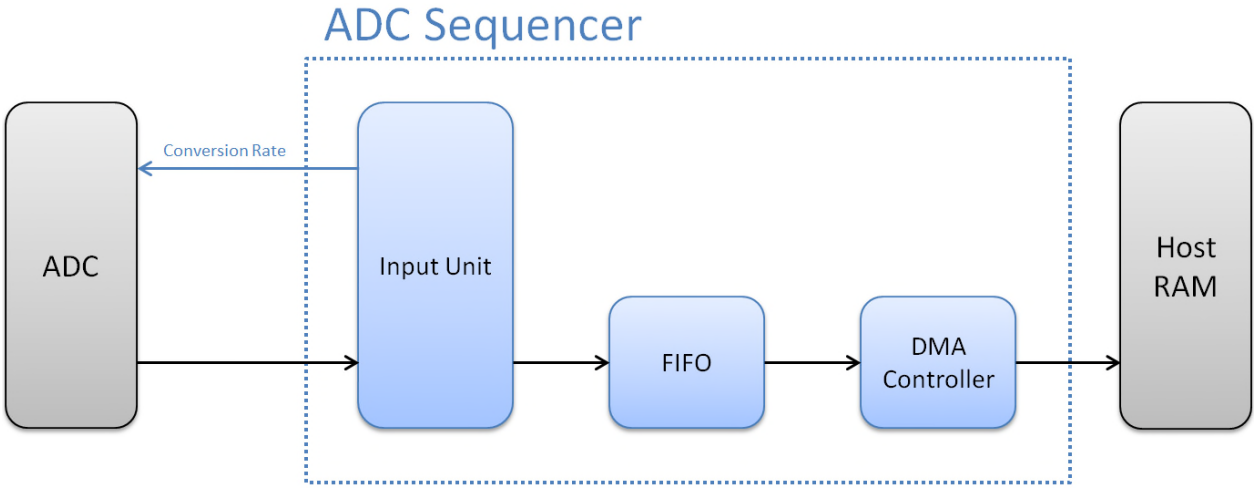


Figure 8-1 : ADC Sequencer

The Input Unit or Output Unit sets the Sequencer's Conversion Rate (the rate at which analog-to-digital conversions or digital-to-analog conversions are performed) by selecting one of the two Conversion Clocks.

The on-board FIFOs buffer ADC Data and DAC Data to make sure delays in DMA bus accesses don't affect ADC or DAC operation.

Since the TPMC533 can produce/require quite large data volumes when converting at full speed, bulk data transfers to/from the Host RAM Data Buffers are handled with PCI Bus DMA transfers. The TPMC533's DMA controllers use Block Transfer Mode DMA Cycles.

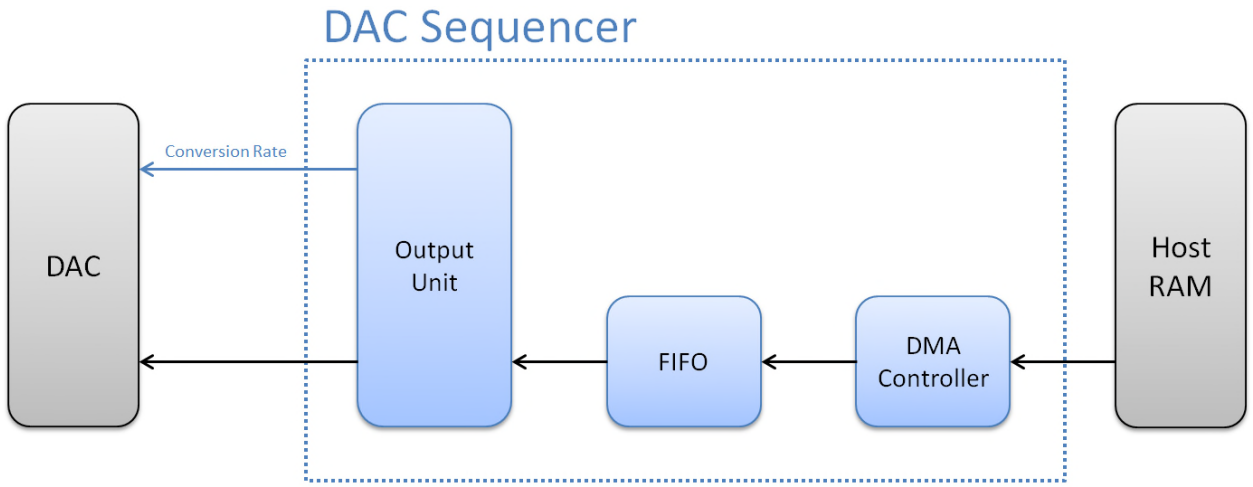


Figure 8-2 : DAC Sequencer

8.1 Host RAM Data Buffers

For ADC operation the TPMC533 writes the ADC Data to Host RAM via PCI Master DMA transfers. The ADC Data (for **all eight ADC Channels of each ADC** assigned to the ADC Sequencer) is written to Host RAM Data Buffers.

For DAC operation the TPMC533 reads the DAC Data from Host RAM via PCI Master DMA transfers. The DAC Data (for **all four DAC Channels of each DAC** assigned to the DAC Sequencer) is read from Host RAM Data Buffers.

The Host RAM Data Buffers must be mapped in 32bit PCI Memory Space and must be accessible from the PCI bus.

For each Sequencer, the ADC Sequencer and the DAC Sequencer, there are two main Registers for DMA access control:

- DMA Buffer Base Address Register
- DMA Buffer Length Register

The (PCI Memory mapped) base address of the next data buffer must be written to the DMA Buffer Base Address Register.

The DMA write transfer (ADC Sequencer) or DMA read transfer (DAC Sequencer) is started by writing the size of the Host RAM Data Buffer to the DMA Buffer Length register while the DMA Engine is in Idle state as indicated in the ADC Sequencer Status Register or DAC Sequencer Status Register.

When the current Host RAM Data Buffer is terminated, the reason for the termination can be read from the ADC Sequencer Status Register or DAC Sequencer Status Register.

To provide the next Host RAM Data Buffer, software must write the base address of the new Host RAM Data Buffer to the DMA Buffer Base Address Register and write the size to the DMA Buffer Length Register. The base address of the next Host RAM Data Buffer may be written immediately after a write to the DMA Buffer Length Register. The DMA Buffer Length Register must only be written if the previous Host RAM Data Buffer has been terminated.

The structure of a Host RAM Data Buffer is a gapless list of Conversion Data Sets which is produced by the ADC Sequencer and which has to be provided for the DAC Sequencer.

A single Conversion Data Set consists of the ADC Data or DAC Data for a single conversion event for all ADC Channels or DAC Channels of all ADCs or DACs assigned to the ADC Sequencer or DAC Sequencer, in ascending order.

8.1.1 ADC

The number of 16bit ADC Data words per Conversion Data Set is:

Number of ADCs assigned to the ADC Sequencer x 8

Host RAM Data Buffer Example I:

- ADC1 is assigned to the ADC Sequencer.
- ADC2, ADC3 and ADC4 are not assigned to the ADC Sequencer.

Conversion Data Set	Host RAM Address	ADC Data
1	DMA Buffer Base Address	16bit ADC Data for ADC1 Channel A
	DMA Buffer Base Address + 0x02	16bit ADC Data for ADC1 Channel B
	DMA Buffer Base Address + 0x04	16bit ADC Data for ADC1 Channel C
	DMA Buffer Base Address + 0x06	16bit ADC Data for ADC1 Channel D
	DMA Buffer Base Address + 0x08	16bit ADC Data for ADC1 Channel E
	DMA Buffer Base Address + 0x0A	16bit ADC Data for ADC1 Channel F
	DMA Buffer Base Address + 0x0C	16bit ADC Data for ADC1 Channel G
	DMA Buffer Base Address + 0x0E	16bit ADC Data for ADC1 Channel H
2	DMA Buffer Base Address + 0x10	16bit ADC Data for ADC1 Channel A
	DMA Buffer Base Address + 0x12	16bit ADC Data for ADC1 Channel B
	DMA Buffer Base Address + 0x14	16bit ADC Data for ADC1 Channel C
	DMA Buffer Base Address + 0x16	16bit ADC Data for ADC1 Channel D
	DMA Buffer Base Address + 0x18	16bit ADC Data for ADC1 Channel E
	DMA Buffer Base Address + 0x1A	16bit ADC Data for ADC1 Channel F
	DMA Buffer Base Address + 0x1C	16bit ADC Data for ADC1 Channel G
	DMA Buffer Base Address + 0x1E	16bit ADC Data for ADC1 Channel H
3	…	…

Table 8-1 : Host RAM Data Buffer Example I: Only ADC1 operating in Sequencer Mode

Host RAM Data Buffer Example II:

- ADC1 and ADC2 are assigned to the ADC Sequencer.
- ADC3 and ADC4 are not assigned to the ADC Sequencer.

Conversion Data Set	Host RAM Address	ADC Data
1	DMA Buffer Base Address	16bit ADC Data for ADC1 Channel A
	DMA Buffer Base Address + 0x02	16bit ADC Data for ADC1 Channel B
	DMA Buffer Base Address + 0x04	16bit ADC Data for ADC1 Channel C
	DMA Buffer Base Address + 0x06	16bit ADC Data for ADC1 Channel D
	DMA Buffer Base Address + 0x08	16bit ADC Data for ADC1 Channel E
	DMA Buffer Base Address + 0x0A	16bit ADC Data for ADC1 Channel F
	DMA Buffer Base Address + 0x0C	16bit ADC Data for ADC1 Channel G
	DMA Buffer Base Address + 0x0E	16bit ADC Data for ADC1 Channel H
	DMA Buffer Base Address + 0x10	16bit ADC Data for ADC2 Channel A
	DMA Buffer Base Address + 0x12	16bit ADC Data for ADC2 Channel B
	DMA Buffer Base Address + 0x14	16bit ADC Data for ADC2 Channel C
	DMA Buffer Base Address + 0x16	16bit ADC Data for ADC2 Channel D
	DMA Buffer Base Address + 0x18	16bit ADC Data for ADC2 Channel E
	DMA Buffer Base Address + 0x1A	16bit ADC Data for ADC2 Channel F
	DMA Buffer Base Address + 0x1C	16bit ADC Data for ADC2 Channel G
	DMA Buffer Base Address + 0x1E	16bit ADC Data for ADC2 Channel H
2	DMA Buffer Base Address + 0x20	16bit ADC Data for ADC1 Channel A
	DMA Buffer Base Address + 0x22	16bit ADC Data for ADC1 Channel B
	DMA Buffer Base Address + 0x24	16bit ADC Data for ADC1 Channel C
	DMA Buffer Base Address + 0x26	16bit ADC Data for ADC1 Channel D
	DMA Buffer Base Address + 0x28	16bit ADC Data for ADC1 Channel E
	DMA Buffer Base Address + 0x2A	16bit ADC Data for ADC1 Channel F
	DMA Buffer Base Address + 0x2C	16bit ADC Data for ADC1 Channel G
	DMA Buffer Base Address + 0x2E	16bit ADC Data for ADC1 Channel H
	DMA Buffer Base Address + 0x30	16bit ADC Data for ADC2 Channel A
	DMA Buffer Base Address + 0x32	16bit ADC Data for ADC2 Channel B
	DMA Buffer Base Address + 0x34	16bit ADC Data for ADC2 Channel C
	DMA Buffer Base Address + 0x36	16bit ADC Data for ADC2 Channel D
	DMA Buffer Base Address + 0x38	16bit ADC Data for ADC2 Channel E
	DMA Buffer Base Address + 0x3A	16bit ADC Data for ADC2 Channel F
	DMA Buffer Base Address + 0x3C	16bit ADC Data for ADC2 Channel G
	DMA Buffer Base Address + 0x3E	16bit ADC Data for ADC2 Channel H
3	…	…

Table 8-2 : Host RAM Data Buffer Example II: ADC1 and ADC2 are operating in Sequencer Mode

8.1.2 DAC

The number of 16bit DAC Data words per Conversion Data Set is:

Number of DACs assigned to the DAC Sequencer x 4

Host RAM Data Buffer Example I:

- DAC2 is assigned to the DAC Sequencer.
- DAC1, DAC3 and DAC4 are not assigned to the DAC Sequencer.

Conversion Data Set	Host RAM Address	DAC Data
1	DMA Buffer Base Address	16bit DAC Data for DAC2 Channel A
	DMA Buffer Base Address + 0x02	16bit DAC Data for DAC2 Channel B
	DMA Buffer Base Address + 0x04	16bit DAC Data for DAC2 Channel C
	DMA Buffer Base Address + 0x06	16bit DAC Data for DAC2 Channel D
2	DMA Buffer Base Address + 0x08	16bit DAC Data for DAC2 Channel A
	DMA Buffer Base Address + 0x0A	16bit DAC Data for DAC2 Channel B
	DMA Buffer Base Address + 0x0C	16bit DAC Data for DAC2 Channel C
	DMA Buffer Base Address + 0x0E	16bit DAC Data for DAC2 Channel D
3	…	…

Table 8-3 : Host RAM Data Buffer Example I: Only DAC2 operating in Sequencer Mode

Host RAM Data Buffer Example II:

- DAC1 and DAC2 are assigned to the DAC Sequencer.
- DAC3 and DAC4 are not assigned to the DAC Sequencer.

Conversion Data Set	Host RAM Address	DAC Data
1	DMA Buffer Base Address	16bit DAC Data for DAC1 Channel A
	DMA Buffer Base Address + 0x02	16bit DAC Data for DAC1 Channel B
	DMA Buffer Base Address + 0x04	16bit DAC Data for DAC1 Channel C
	DMA Buffer Base Address + 0x06	16bit DAC Data for DAC1 Channel D
	DMA Buffer Base Address + 0x08	16bit DAC Data for DAC2 Channel A
	DMA Buffer Base Address + 0x0A	16bit DAC Data for DAC2 Channel B
	DMA Buffer Base Address + 0x0C	16bit DAC Data for DAC2 Channel C
	DMA Buffer Base Address + 0x0E	16bit DAC Data for DAC2 Channel D
2	DMA Buffer Base Address + 0x10	16bit DAC Data for DAC1 Channel A
	DMA Buffer Base Address + 0x12	16bit DAC Data for DAC1 Channel B
	DMA Buffer Base Address + 0x14	16bit DAC Data for DAC1 Channel C
	DMA Buffer Base Address + 0x16	16bit DAC Data for DAC1 Channel D
	DMA Buffer Base Address + 0x18	16bit DAC Data for DAC2 Channel A
	DMA Buffer Base Address + 0x1A	16bit DAC Data for DAC2 Channel B
	DMA Buffer Base Address + 0x1C	16bit DAC Data for DAC2 Channel C
	DMA Buffer Base Address + 0x1E	16bit DAC Data for DAC2 Channel D
3	…	…

Table 8-4 : Host RAM Data Buffer Example II: DAC1 and DAC2 are operating in Sequencer Mode

9 Conversion Signals

There are three conversion signals:

- Conversion Clock 1
- Conversion Clock 2
- Frame Trigger

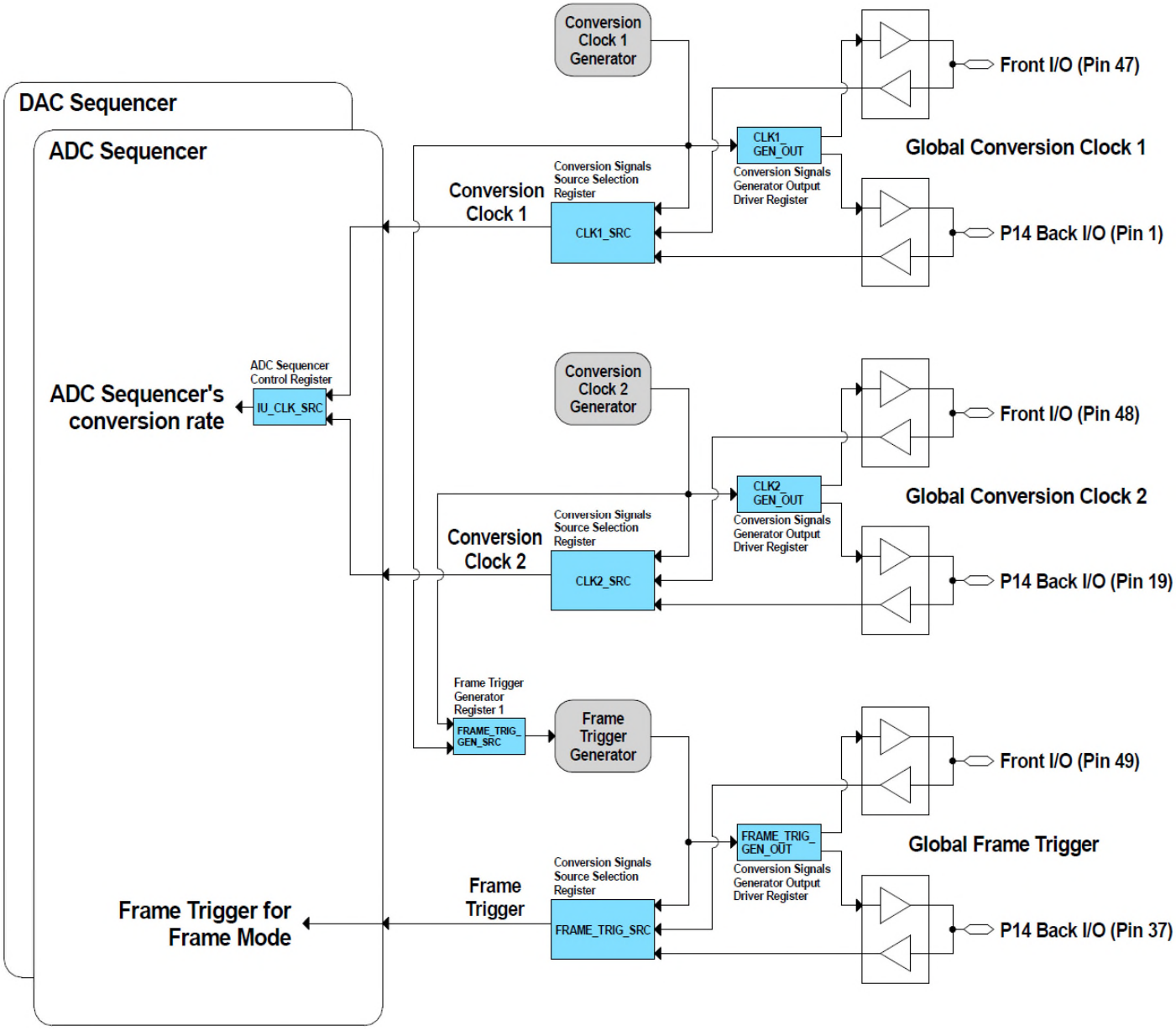


Figure 9-1 : Conversion Signals

Each of the two Conversion Clocks (Conversion Clock 1 and Conversion Clock 2) may be selected as the Sequencer Conversion Clock Source in the ADC Sequencer Control Register or the DAC Sequencer Control Register to define the ADC Sequencer's conversion rate or the DAC Sequencer's conversion rate.

The Frame Trigger (in combination with a Conversion Clock) is used for sequencers configured to operate in Frame Mode. For example, the Frame Trigger can be used to synchronize/align ADC Frames and DAC Frames. The Frame Trigger Generator output is generated (phase locked) to either the Conversion Clock 1 Generator output or to the Conversion Clock 2 Generator output.

Each of these three Conversion Signals can either be generated on-board or can be generated by an external device and input via Front I/O or P14 Back I/O.

If generated on-board, all three Conversion Signals may optionally be driven out on either Front I/O or Back I/O.

If a Global Frame Trigger and a Global Conversion Clock are input via Front I/O or P14 Back I/O these signals need to meet certain timing requirements:

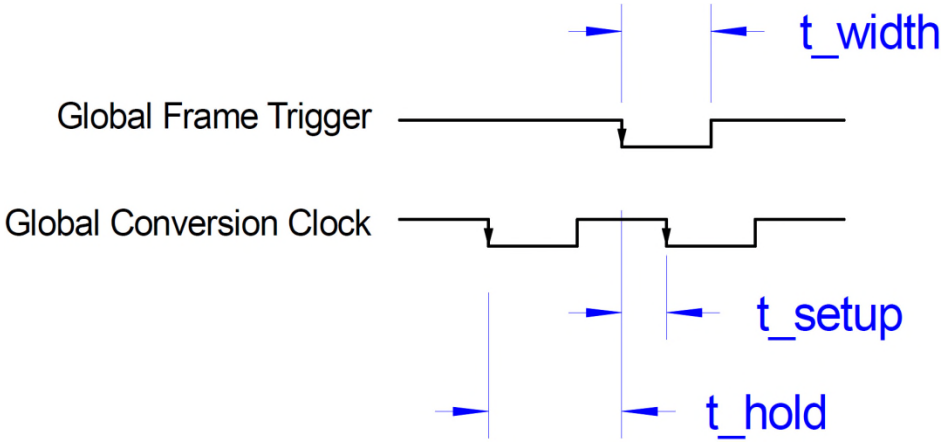


Figure 9-2 : Global Conversion Signals Timing Requirements

Timing Requirement	Description	Min	Max
t_width	Global Frame Trigger Pulse Width	500ns	½ $T_{GLO\_CON\_CLK}$
t_hold	Global Conversion Clock Event to next Global Frame Trigger Event	½ $T_{GLO\_CON\_CLK}$ - 250ns	-
t_setup	Global Frame Trigger Event to next Global Conversion Clock Event	250ns	-

Table 9-1 : Global Conversion Signals Timing Requirements

9.1 Multi-board Synchronization

Using the Frame Mode in the ADC Sequencer Control Register and in the DAC Sequencer Control Register allows multi-board synchronization.

In a multi-board application, one PMC is operating as the multi-board master card while the other cards are operating as multi-board target cards.

The Frame Trigger signal is generated by the Frame Trigger Generator on the master card. It is either aligned to Conversion Clock 1 or to Conversion Clock 2. The Frame Trigger and the associated Conversion Clock are distributed to all cards involved in the multi-board application either via Front I/O or via P14 Back I/O (Conversion Signals Generator Output Driver Register).

The multi-board master's Frame Trigger (Global Frame Trigger) and the multi-board master's Conversion Clock (Global Conversion Clock) must be connected to the Global Frame Trigger and Global Conversion Clock Front I/O or P14 Back I/O pins of all target cards in the multi-board application.

All cards involved in the multi-board application **(including the master card)** must use the Front I/O or P14 Back I/O pin input signals as the signal source for both the Frame Trigger signal and the Conversion Clock signal (Conversion Signals Source Selection Register).

All card's sequencers operating in Frame Mode are waiting for a Global Frame Trigger signal event to start the sequencer conversion process.

System Configuration	Conversion Signals Generator Enable	Conversion Signals Generator Output Driver	Conversion Signals Source Selection
Single Card	Enabled	Output Driver disabled	Conversion Signal Generators
Multi-board Master Card	Enabled	P14 Back I/O or Front I/O	P14 Back I/O or Front I/O
Multi-board Target Card	Disabled	Output Driver disabled	P14 Back I/O or Front I/O

Table 9-2 : Generator Enable, Generator Output Driver and Source Selection settings for different System Configurations

10 Pin Assignment – I/O Connector

10.1 Front I/O

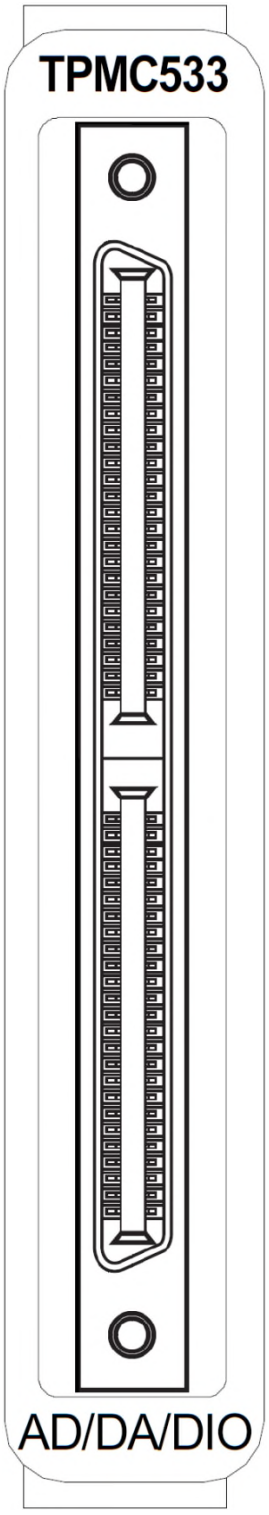
Signal	Pin		Pin	Signal
ADC1 Channel H+	1		51	ADC1 Channel H-
ADC1 Channel G+	2		52	ADC1 Channel G-
ADC1 Channel F+	3		53	ADC1 Channel F-
ADC1 Channel E+	4		54	ADC1 Channel E-
ADC1 Channel D+	5		55	ADC1 Channel D-
ADC1 Channel C+	6		56	ADC1 Channel C-
ADC1 Channel B+	7		57	ADC1 Channel B-
ADC1 Channel A+	8		58	ADC1 Channel A-
GND	9		59	GND
ADC2 Channel H+	10		60	ADC2 Channel H-
ADC2 Channel G+	11		61	ADC2 Channel G-
ADC2 Channel F+	12		62	ADC2 Channel F-
ADC2 Channel E+	13		63	ADC2 Channel E-
ADC2 Channel D+	14		64	ADC2 Channel D-
ADC2 Channel C+	15		65	ADC2 Channel C-
ADC2 Channel B+	16		66	ADC2 Channel B-
ADC2 Channel A+	17		67	ADC2 Channel A-
GND	18		68	GND
ADC3 Channel H+	19		69	ADC3 Channel H-
ADC3 Channel G+	20		70	ADC3 Channel G-
ADC3 Channel F+	21		71	ADC3 Channel F-
ADC3 Channel E+	22		72	ADC3 Channel E-
ADC3 Channel D+	23		73	ADC3 Channel D-
ADC3 Channel C+	24		74	ADC3 Channel C-
ADC3 Channel B+	25		75	ADC3 Channel B-
ADC3 Channel A+	26		76	ADC3 Channel A-
GND	27		77	GND
ADC4 Channel H+	28		78	ADC4 Channel H-
ADC4 Channel G+	29		79	ADC4 Channel G-
ADC4 Channel F+	30		80	ADC4 Channel F-
ADC4 Channel E+	31		81	ADC4 Channel E-
ADC4 Channel D+	32		82	ADC4 Channel D-
ADC4 Channel C+	33		83	ADC4 Channel C-
ADC4 Channel B+	34		84	ADC4 Channel B-
ADC4 Channel A+	35		85	ADC4 Channel A-
GND	36		86	GND
DAC1 Channel A	37		87	DAC2 Channel A
DAC1 Channel B	38		88	DAC2 Channel B
DAC1 Channel C	39		89	DAC2 Channel C
DAC1 Channel D	40		90	DAC2 Channel D
GND	41		91	GND
DAC3 Channel A	42		92	DAC4 Channel A
DAC3 Channel B	43		93	DAC4 Channel B
DAC3 Channel C	44		94	DAC4 Channel C
DAC3 Channel D	45		95	DAC4 Channel D
GND	46		96	GND
Digital I/O 1 (Global Conversion Clock 1)	47		97	Digital I/O 2
Digital I/O 3 (Global Conversion Clock 2)	48		98	Digital I/O 4
Digital I/O 5 (Global Frame Trigger)	49		99	Digital I/O 6
Digital I/O 7	50		100	Digital I/O 8

Table 10-1: Pin Assignment Front I/O

10.2 P14 Back I/O

Signal	Pin		Pin	Signal
-	63		64	-
-	61		62	-
-	59		60	-
GND	57		58	-
P14 GPIO	55		56	GND
-	53		54	-
-	51		52	-
-	49		50	-
-	47		48	-
-	45		46	-
-	43		44	-
-	41		42	-
GND	39		40	-
Global Frame Trigger	37		38	GND
-	35		36	-
-	33		34	-
-	31		32	-
-	29		30	-
-	27		28	-
-	25		26	-
-	23		24	-
GND	21		22	-
Global Conversion Clock 2	19		20	GND
-	17		18	-
-	15		16	-
-	13		14	-
-	11		12	-
-	9		10	-
-	7		8	-
-	5		6	-
GND	3		4	-
Global Conversion Clock 1	1		2	GND

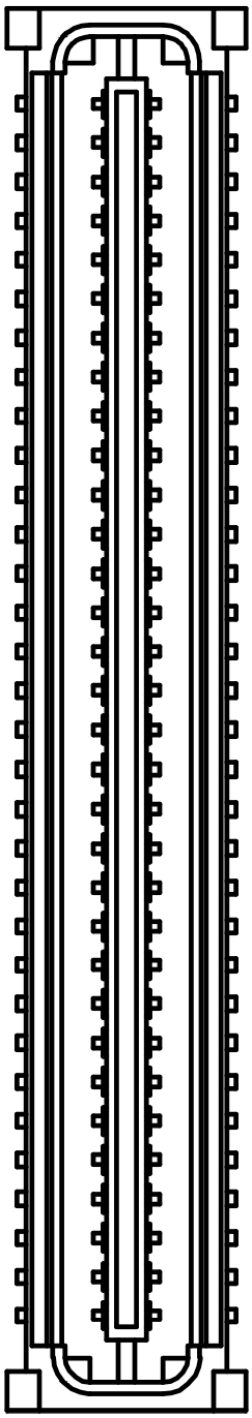


Table 10-2: Pin Assignment P14 Back I/O

11 TA114 Cable

TEWS TECHNOLOGIES offers a cable with one male HDRA100 connector and two male HD50 connectors which is called TA114. This cable can be used to adapt the TPMC533's Front I/O connection to two more common HD50 connectors.

11.1 X2 Connector

Pin-Count	50
Connector Type	SCSI-II, SCSI-III Connector
Source & Order Info	Honda PCS-XE50MB +

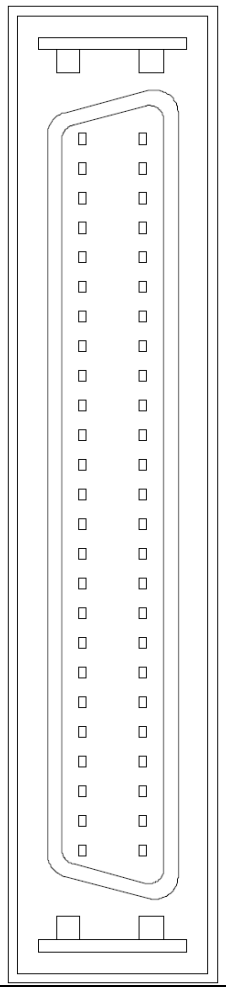
Signal	Pin		Pin	Signal
ADC1 Channel H-	26		1	ADC1 Channel H+
ADC1 Channel G-	27		2	ADC1 Channel G+
ADC1 Channel F-	28		3	ADC1 Channel F+
ADC1 Channel E-	29		4	ADC1 Channel E+
ADC1 Channel D-	30		5	ADC1 Channel D+
ADC1 Channel C-	31		6	ADC1 Channel C+
ADC1 Channel B-	32		7	ADC1 Channel B+
ADC1 Channel A-	33		8	ADC1 Channel A+
GND	34		9	GND
ADC2 Channel H-	35		10	ADC2 Channel H+
ADC2 Channel G-	36		11	ADC2 Channel G+
ADC2 Channel F-	37		12	ADC2 Channel F+
ADC2 Channel E-	38		13	ADC2 Channel E+
ADC2 Channel D-	39		14	ADC2 Channel D+
ADC2 Channel C-	40		15	ADC2 Channel C+
ADC2 Channel B-	41		16	ADC2 Channel B+
ADC2 Channel A-	42		17	ADC2 Channel A+
GND	43		18	GND
ADC3 Channel H-	44		19	ADC3 Channel H+
ADC3 Channel G-	45		20	ADC3 Channel G+
ADC3 Channel F-	46		21	ADC3 Channel F+
ADC3 Channel E-	47		22	ADC3 Channel E+
ADC3 Channel D-	48		23	ADC3 Channel D+
ADC3 Channel C-	49		24	ADC3 Channel C+
ADC3 Channel B-	50		25	ADC3 Channel B+

Table 11-1 : TA114 X2 Connector

11.2 X3 Connector

Pin-Count	50
Connector Type	SCSI-II, SCSI-III Connector
Source & Order Info	Honda PCS-XE50MB +

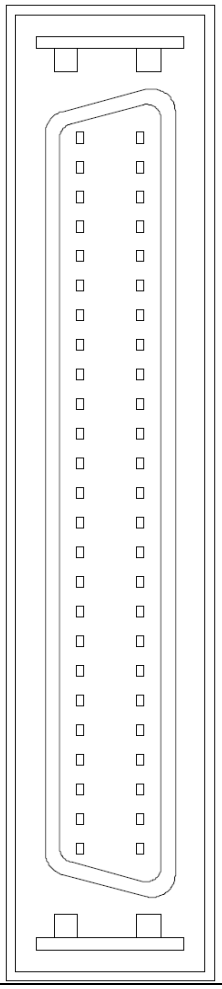
Signal	Pin		Pin	Signal
ADC3 Channel A-	**26**		**1**	ADC3 Channel A+
GND	**27**		**2**	GND
ADC4 Channel H-	**28**		**3**	ADC4 Channel H+
ADC4 Channel G-	**29**		**4**	ADC4 Channel G+
ADC4 Channel F-	**30**		**5**	ADC4 Channel F+
ADC4 Channel E-	**31**		**6**	ADC4 Channel E+
ADC4 Channel D-	**32**		**7**	ADC4 Channel D+
ADC4 Channel C-	**33**		**8**	ADC4 Channel C+
ADC4 Channel B-	**34**		**9**	ADC4 Channel B+
ADC4 Channel A-	**35**		**10**	ADC4 Channel A+
GND	**36**		**11**	GND
DAC2 Channel A	**37**		**12**	DAC1 Channel A
DAC2 Channel B	**38**		**13**	DAC1 Channel B
DAC2 Channel C	**39**		**14**	DAC1 Channel C
DAC2 Channel D	**40**		**15**	DAC1 Channel D
GND	**41**		**16**	GND
DAC4 Channel A	**42**		**17**	DAC3 Channel A
DAC4 Channel B	**43**		**18**	DAC3 Channel B
DAC4 Channel C	**44**		**19**	DAC3 Channel C
DAC4 Channel D	**45**		**20**	DAC3 Channel D
GND	**46**		**21**	GND
Digital I/O 2	**47**		**22**	Digital I/O 1 (Global Conversion Clock 1)
Digital I/O 4	**48**		**23**	Digital I/O 3 (Global Conversion Clock 2)
Digital I/O 6	**49**		**24**	Digital I/O 5 (Global Frame Trigger)
Digital I/O 8	**50**		**25**	Digital I/O 7

Table 11-2 : TA114 X3 Connector

12 Programming Hints

12.1 Global DAC Status Register Read

Whenever the Global DAC Status Register is read right after a register write (e.g. to evaluated the DAC Busy Status right after a manual DAC Reset Request write, DAC Configuration Register write or DAC Data Register write) the read data of the first Global DAC Status Register read must be discarded.

In other words: Whenever the Global DAC Status Register is read right after a register write, a single leading dummy read of the Global DAC Status Register is required.