The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC542

16/8 Channel Voltage & Current Range D/A and 20 Channel LVTTL/TTL Digital I/O

Version 1.0

User Manual

Issue 1.0.3

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TPMC542-10R

16 Channels of Simultaneous Update Single-Ended 16 bit Voltage & Current Range D/A and 20 Channels of LVTTL/TTL Digital I/O, with MDR68 front panel I/O

(RoHS compliant)

TPMC542-20R

8 Channels of Simultaneous Update Single-Ended 16 bit Voltage & Current Range D/A and 20 Channels of LVTTL/TTL Digital I/O, with MDR68 front panel I/O

(RoHS compliant)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial issue	April 2017
1.0.1	Description Block Diagram	June 2017
1.0.2	Added notes to *Technical Specification Table*, *D/A Channel Output* section Added notes to the *Voltage Output Mode* and *Current Output Mode* paragraphs in the *Analog Output Interface* chapter.	February 2021
1.0.3	Added chapter *Programming Hints* and sub-chapter *Global DAC Status Register Read*	April 2022

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1 Product Description

The TPMC542 is a standard single-wide PCI Mezzanine Card (PMC) compatible module providing 16 or 8 channels of simultaneous update single-ended 16bit analog output and 20 channels of tristate capable 5V-tolerant LVTTL/TTL digital input/output.

A 32 bit 33 MHz PCI interface is provided at the PMC P11 and P12 connectors.

The analog output signals and digital I/O signals are accessible via a 68 pin Mini D Ribbon (MDR68) type front I/O connector.

For each individual D/A channel, the following output ranges are configurable:

- 0V to 5V Voltage Range
- 0V to 10V Voltage Range
- ±5V Voltage Range
- ±10V Voltage Range
- 4mA to 20mA Current Range
- 0mA to 20mA Current Range
- 0mA to 24mA Current Range

Additionally, a 20% over-range may be enabled for each Voltage Range.

The TPMC542 provides a D/A Sequencer unit for periodic simultaneous digital to analog conversions at a configurable conversion rate. In sequencer mode, the D/A conversion data is fetched from buffers in host memory by PCI master DMA transfer and is temporarily stored in an on-board data buffer. The Sequencer provides a Frame Mode used for repetitive frames of simultaneous D/A conversions upon a frame trigger signal event.

Conversion clock (conversion rate) and frame trigger signals may be generated on-board for internal use and may also be driven out on P14 rear I/O if the card is operating as a master card in a Multi-Board configuration. The conversion clock (conversion rate) and frame trigger signals may also be sourced externally via the P14 rear I/O interface if the card is operating as a target card in a Multi-Board configuration.

Each TPMC542 is factory calibrated. The correction data is stored in an on-board serial EEPROM unique to each PMC module. These correction values may be used to perform a hardware correction for every D/A channel and output range.

The digital I/O lines are ESD protected. Each digital I/O line has a dedicated line transmitter with individual output enable control and a dedicated line receiver. The line receivers are always enabled, so the digital I/O line level can always be monitored. Each digital I/O line input is capable of generating an interrupt triggered on rising edge, falling edge or both. Additionally, a debounce filter can be configured to get rid of bouncing on the digital I/O inputs. Each digital I/O line has a 4.7kΩ pull resistor to a common reference. The common pull resistor reference is programmable by software (one setting for all digital I/O lines) to +3.3V, +5V or GND.

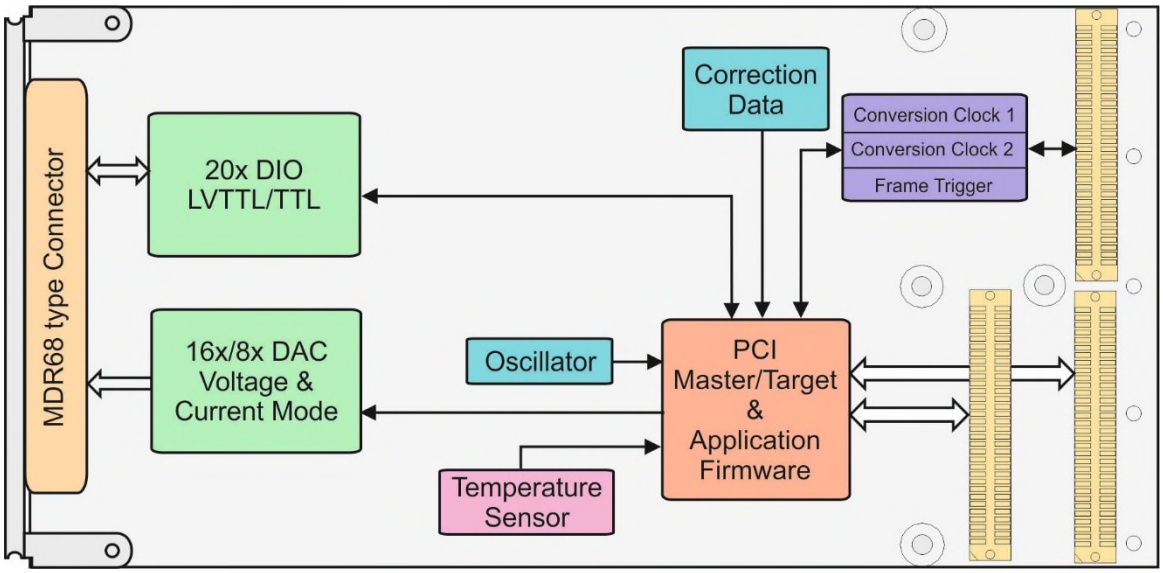


Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Standard single-wide
Electrical Interface	PCI Rev. 3.0 compatible 33MHz / 32bit PCI Initiator/Target 3.3V and 5V PCI Signaling Voltage compatible
On-Board Devices	
FPGA	XC6SLX25-2FTG256I (Xilinx)
DAC	AD5755-1ACPZ (Analog Devices)
Digital I/O	74LVT126PW (NXP)
Non-Volatile Memory	
FPGA Configuration Flash	32 Mbit Serial Flash W25Q32FVZPIG (Winbond)
Correction Data EEPROM	16 kbit Serial EEPROM M93C86-WMN6TP (ST)
I/O Interface	
D/A Channels	TPMC542-10R: 16 D/A Channels TPMC542-20R: 8 D/A Channels
D/A Channel Output	**Voltage Mode Ranges:** 0V … 5V, 0V … 10V, -5V … +5V, -10V … +10V Voltage Ranges available with 20% Overrange Mode: 0V … 6V, 0V … 12V, -6V … +6V, -12V … +12V Up to 10mA load current per D/A channel output D/A channel output slew rate 1.9V/us (typical) **Current Mode Ranges:** 4mA … 20mA, 0mA … 20mA, 0mA … 24mA External load resistor range per channel: up to 1K (with increased power dissipation and cooling requirements), recommended maximum load resistor value: 680Ω, recommended load resistor value: less than or equal to 390Ω
D/A Conversion Rate	Max. 38ksps Conversion Rate (all D/A Channels simultaneous)
Digital I/O Channels	20 TTL/LVTTL Digital I/O Lines 3.3V Driver, 5V tolerant Receiver, Individual Output Enable Control, Common Pull Resistor Reference Control (3.3V, 5V, GND) Up to 15mA Source Current and up to 6mA Sink Current per Digital I/O Line
I/O Connectors	
Front I/O	68 pin Mini D Ribbon (MDR) (3M N10268-52E2PC or compatible)
P14 Back I/O	64 pin Mezzanine Connector (Molex 71436-2864 or compatible)

Physical Data		
Power Requirements	Only the 5V PMC Power Supply is used Typically 0.25A @ +5V DC without I/O Load I/O Load Calculation: Add 0.010A per active DIO Output Line Add 0.070A per active D/A Voltage Output without Overrange Add 0.082A per active D/A Voltage Output with Overrange Add approx. ($I_{RANGE\_MAX}^2$ * R_{EXT}) / 2.25V ampere per active D/A Current Output	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	TPMC542-10R: 283000h TPMC542-20R: 356000h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	TPMC542-10R: 92g TPMC542-20R: 84g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

The PMC module is sensitive to static electricity. Packing, unpacking and all other module handling has to be done with the appropriate care.

3.2 Power Dissipation Limit

Please note that with multiple D/A channels operating in Current Mode, the PMC power consumption and dissipation may exceed the maximum values defined in IEEE Std. 1386-2001. This is largely depending on the resistance value of the external load resistors used for D/A channels in current mode. Although the DAC device supports external load resistor values of up to 1K Ohm in Current Mode, the value of the external load resistor should not exceed 680Ω. Load resistor values of less than (or equal to) 390Ω are recommended.

See also the *I/O Load Calculation* in the *Technical Specification* table. Normally the total current drawn from the PMC 5V power supply should not exceed 1.5A (7.5W).

3.3 Forced Air-Cooling Requirements

The TPMC542 requires forced air cooling.

Moderate air cooling is required when D/A channels are only used in Voltage Mode or when D/A channels are used in Current Mode with external load resistor values <= 390Ω.

Air cooling requirements increase with: Ambient Temperature, Number of Current Mode D/A Channels on the same DAC device, Resistance value of external Current Mode load resistors.

Firm air cooling is required when D/A channels are used in Current Mode with external load resistor values > 390Ω.

It is recommended to limit the number of D/A Current Mode channels with external resistor values > 390Ω and to spread these over the DAC devices (e.g. use D/A channels 1, 5, 9, 13).

4 PCI Interface

4.1 PCI Identifier & BAR Configuration

Vendor-ID	0x1498 (TEWS TECHNOLOGIES)
Device-ID	0x021E (TPMC542)
Class Code	0x118000 (Other data acquisition/signal processing controllers)
Subsystem Vendor-ID	0x1498 (TEWS TECHNOLOGIES)
Subsystem Device-ID	0x000A (TPMC542-10R) 0x0014 (TPMC542-20R)

Table 4-1 : PCI Identifier

The TPMC542 provides two spaces mapped in PCI Memory Space.

PCI Base Address Register (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	1024	32	Little	Register Space
1 (0x14)	MEM	2048	32	Little	Correction Data Space

Table 4-2 : PCI Base Address Register (BAR) Configuration

4.2 Register Space

PCI Base Address Register 0 (Offset 0x10 in PCI Configuration Space).

Offset to BAR0	Description	Size (Bit)
0x000 … 0x154	Reserved	-
DAC Global Registers		
0x158	Global DAC Control Register	32
0x15C	Global DAC Status Register	32
0x160	Reserved	-
0x164	Reserved	-
DAC Device Registers		
0x168	DAC1 Configuration Register	32
0x16C	DAC1 Reserved	-
0x170	DAC1 Correction Register A	32
0x174	DAC1 Correction Register B	32
0x178	DAC1 Correction Register C	32
0x17C	DAC1 Correction Register D	32
0x180	DAC1 Data Register A & B	32
0x184	DAC1 Data Register C & D	32
0x188	DAC1 Status Register	32
0x18C	DAC1 Mode Register	32
0x190	Reserved	-
0x194	Reserved	-
0x198	DAC2 Configuration Register	32
0x19C	DAC2 Reserved	-
0x1A0	DAC2 Correction Register A	32
0x1A4	DAC2 Correction Register B	32
0x1A8	DAC2 Correction Register C	32
0x1AC	DAC2 Correction Register D	32
0x1B0	DAC2 Data Register A & B	32
0x1B4	DAC2 Data Register C & D	32
0x1B8	DAC2 Status Register	32
0x1BC	DAC2 Mode Register	32
0x1C0	Reserved	-
0x1C4	Reserved	-
0x1C8	DAC3 Configuration Register	32
0x1CC	DAC3 Reserved	-
0x1D0	DAC3 Correction Register A	32

Offset to BAR0	Description	Size (Bit)
0x1D4	DAC3 Correction Register B	32
0x1D8	DAC3 Correction Register C	32
0x1DC	DAC3 Correction Register D	32
0x1E0	DAC3 Data Register A & B	32
0x1E4	DAC3 Data Register C & D	32
0x1E8	DAC3 Status Register	32
0x1EC	DAC3 Mode Register	32
0x1F0	Reserved	-
0x1F4	Reserved	-
0x1F8	DAC4 Configuration Register	32
0x1FC	DAC4 Reserved	-
0x200	DAC4 Correction Register A	32
0x204	DAC4 Correction Register B	32
0x208	DAC4 Correction Register C	32
0x20C	DAC4 Correction Register D	32
0x210	DAC4 Data Register A & B	32
0x214	DAC4 Data Register C & D	32
0x218	DAC4 Status Register	32
0x21C	DAC4 Mode Register	32
0x220 … 0x2E4	Reserved	-
DAC Sequencer Registers		
0x2E8	D/A Sequencer Control Register	32
0x2EC	D/A Sequencer Status Register	32
0x2F0	Reserved	-
0x2F4	D/A Sequencer Number of Conversions Register	32
0x2F8	D/A Sequencer Conversion Count Register	32
0x2FC	D/A Sequencer FIFO Level Register	32
0x300	Reserved	-
0x304	Reserved	-
0x308	D/A Sequencer DMA Buffer Base Address Register	32
0x30C	D/A Sequencer DMA Buffer Length Register	32
0x310	D/A Sequencer DMA Buffer Next Address Register	32
0x314	Reserved	-
0x318	Reserved	-
0x31C	Reserved	-
Conversion Signals Registers		
0x320	Conversion Clock 1 Generator Register	32
0x324	Conversion Clock 2 Generator Register	32

Offset to BAR0	Description	Size (Bit)
0x328	Reserved	-
0x32C	Frame Trigger Generator Configuration Register 1	32
0x330	Frame Trigger Generator Configuration Register 2	32
0x334	Reserved	-
0x338	Reserved	-
0x33C	Conversion Signal Generator Enable Register	32
0x340	Conversion Signal Generator Output Driver Register	32
0x344	Conversion Signal Source Selection Register	32
0x348	Frame Timer Register	32
0x34C	Reserved	-
0x350	Reserved	-
DIO Registers		
0x354	DIO Input Register	32
0x358	DIO Input Filter Register	32
0x35C	DIO Output Register	32
0x360	DIO Output Enable Register	32
0x364	Reserved	-
0x368	Reserved	-
Interrupt Registers		
0x36C	Interrupt Enable Register	32
0x370	Error Interrupt Enable Register	32
0x374	DIO Rising Edge Interrupt Enable Register	32
0x378	DIO Falling Edge Interrupt Enable Register	32
0x37C	Reserved	-
0x380	Reserved	-
0x384	Interrupt Status Register	32
0x388	Error Interrupt Status Register	32
0x38C	DIO Interrupt Status Register	32
0x390	Reserved	-
0x394	Reserved	-
Other Registers		
0x398	Global Configuration Register	32
0x39C	DIO Pull Resistors Register	32
0x3A0	P14 Back I/O Pull Resistors Register	32
0x3A4	Correction Data EEPROM Control/Status Register	32
0x3A8	Temperature Sensor Trigger Register	32
0x3AC	Temperature Sensor Data Register	32
0x3B0 … 0x3F8	Reserved	-

Offset to BAR0	Description	Size (Bit)
0x3FC	Firmware Version Register	32

Table 4-3 : Register Space

For the TPMC542-20R the registers for DAC3 and DAC4 are reserved.

Register Bit Access Type		Description
R	Read	The bit is readable by software.
R/W	Read/Write	The bit is readable and writeable by software.
R/C	Read/Clear	The bit is readable by software. The bit is set by the firmware. Software may clear the bit by writing a '1'.
R/S	Read/Set	The bit is readable by software. Software may set this bit to '1'. The bit is cleared by the firmware.

Table 4-4 : Register Bit Access Types

When reading reserved register bits, the value is undefined.

Reserved register bits shall be written as '0'.

4.2.1 D/A Global Registers

4.2.1.1 Global DAC Control Register (0x158)

This register provides control options for all on-board DAC devices.

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	-	-
19	DAC4_ RST_ REQ	DAC4 Reset Request See description for DAC1.	R/S	0
18	DAC3_ RST_ REQ	DAC3 Reset Request See description for DAC1.	R/S	0
17	DAC2_ RST_ REQ	DAC2 Reset Request See description for DAC1.	R/S	0
16	DAC1_ RST_ REQ	DAC1 Reset Request When set, performs a DAC reset via the DAC (AD5755-1) RESET# pin. After the actual reset phase, a post-reset DAC auto-configuration is performed. This bit is automatically cleared. The DAC Busy Bit in the Global DAC Status Register indicates the active DAC reset and post-reset auto-configuration phase (also see chapter *Programming Hints / Global DAC Status Register Read*!).	R/S	0
15:4	-	Reserved	-	-
3	DAC4_ CONV_ REQ	DAC4 Conversion Pulse Request See description for DAC1.	R/S	0
2	DAC3_ CONV_ REQ	DAC3 Conversion Pulse Request See description for DAC1.	R/S	0
1	DAC2_ CONV_ REQ	DAC2 Conversion Pulse Request See description for DAC1.	R/S	0
0	DAC1_ CONV_ REQ	DAC1 Conversion Pulse Request Manual Controlled Conversion Mode: When set, generates a DAC conversion pulse. Software should check the DAC Busy Bit to be clear in the Global DAC Status Register before (also see chapter *Programming Hints / Global DAC Status Register Read*!). This bit is automatically cleared. Sequencer Mode & Manual Immediate Mode: This bit has no effect and is cleared immediately.	R/S	0

Table 4-5 : Global DAC Control Register (0x158)

4.2.1.2 Global DAC Status Register (0x15C)

This read only register provides status information for all on-board DAC devices.

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	-	-
19	DAC4_ FAULT	DAC4 Fault Status See description for DAC1.	R	0
18	DAC3_ FAULT	DAC3 Fault Status See description for DAC1.	R	0
17	DAC2_ FAULT	DAC2 Fault Status See description for DAC1.	R	0
16	DAC1_ FAULT	DAC1 Fault Status This bit is set when the DAC (AD5755-1) FAULT# output pin is active (low).	R	0
15:12	-	Reserved	-	-
11	DAC4_SETL	DAC4 Settle Status See description for DAC1.	R	-
10	DAC3_SETL	DAC3 Settle Status See description for DAC1.	R	-
9	DAC2_SETL	DAC2 Settle Status See description for DAC1.	R	-
8	DAC1_SETL	DAC1 Settle Status Indicates a fix 24us passing time after a DAC conversion.	R	-
7:4	-	Reserved	-	-
3	DAC4_ BUSY	DAC4 Busy Status See description for DAC1.	R	0
2	DAC3_ BUSY	DAC3 Busy Status See description for DAC1.	R	0
1	DAC2_ BUSY	DAC2 Busy Status See description for DAC1.	R	0
0	DAC1_ BUSY	DAC1 Busy Status Set when: • a DAC transfer request is being processed (including any required recovery times) • A DAC reset request is processed (including post-reset auto-configuration time) Does not cover any analog output settling time.	R	0

Table 4-6 : Global DAC Status Register (0x15C)

Also see chapter *Programming Hints / Global DAC Status Register Read*!

4.2.2 D/A Device Registers

The registers described in this section are provided per on-board DAC device.

4.2.2.1 DAC Configuration Register(s) (0x168, 0x198, 0x1C8, 0x1F8)

This register is intended for initial DAC configuration.

Each DAC device must be configured before use.

DAC configuration should be performed while the DAC is configured for Manual Mode.

After writing the DAC Configuration Register, the DAC Busy Bit in the Global DAC Status Register should be monitored to become clear again. *Also see* chapter *Programming Hints / Global DAC Status Register Read*!

This register is available per DAC device.

A write to the DAC configuration register logs an internal request for writing the configuration data to the corresponding DAC device (via the DAC serial interface) as soon as possible. If not already set, the DAC Busy bit in the Global DAC Status Register is set and remains so, until the configuration data transfer to the DAC device is done.

This register may be accessed with 32 bit, 16 bit or 8 bit transfer size.

Bit	Symbol	Description	Access	Reset Value
DAC Channel D				
31	-	Reserved	-	-
30	OE_D	Output Enable DAC Channel D	R/W	0
29	PU_D	Power-Up DAC Channel D	R/W	0
28	OVR_D	Over Range DAC Channel D Enables 20% over-range for Voltage Ranges.	R/W	0
27:24	OR_D	Output Range DAC Channel D See description for DAC Channel A.	R/W	0
DAC Channel C				
23	-	Reserved	-	-
22	OE_C	Power-Up DAC Channel C	R/W	0
21	PU_C	Output Enable DAC Channel C	R/W	0
20	OVR_C	Over Range DAC Channel C Enables 20% over-range for Voltage Ranges.	R/W	0
19:16	OR_C	Output Range DAC Channel C See description for DAC Channel A.	R/W	0
DAC Channel B				
15	-	Reserved	-	-
14	OE_B	Power-Up DAC Channel B	R/W	0
13	PU_B	Output Enable DAC Channel B	R/W	0
12	OVR_B	Over Range DAC Channel B Enables 20% over-range for Voltage Ranges.	R/W	0

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>11:8</td><td>OR_B</td><td>Output Range DAC Channel B
See description for DAC Channel A.</td><td>R/W</td><td>0</td></tr>
<tr><td colspan="5">DAC Channel A</td></tr>
<tr><td>7</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>6</td><td>OE_A</td><td>Output Enable DAC Channel A</td><td>R/W</td><td>0</td></tr>
<tr><td>5</td><td>PU_A</td><td>Power-Up DAC Channel A</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>OVR_A</td><td>Over Range DAC Channel A
Enables 20% over-range for Voltage Ranges.</td><td>R/W</td><td>0</td></tr>
<tr><td>3:0</td><td>OR_A</td><td>Output Range DAC Channel A
<table>
<tr><th>3:0</th><th>Output Voltage Range</th></tr>
<tr><td>0000</td><td>0V to 5V Voltage Range</td></tr>
<tr><td>0001</td><td>0V to 10V Voltage Range</td></tr>
<tr><td>0010</td><td>Reserved</td></tr>
<tr><td>0011</td><td>±5V Voltage Range</td></tr>
<tr><td>0100</td><td>±10V Voltage Range</td></tr>
<tr><td>0101</td><td>Reserved</td></tr>
<tr><td>011x</td><td>Reserved</td></tr>
<tr><td>10xx</td><td>Reserved</td></tr>
<tr><td>1100</td><td>4mA to 20mA Current Range</td></tr>
<tr><td>1101</td><td>0mA to 20mA Current Range</td></tr>
<tr><td>1110</td><td>0mA to 24mA Current Range</td></tr>
<tr><td>1111</td><td>Reserved</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
</table>

Table 4-7 : DAC Configuration Register (0x168, 0x198, 0x1C8, 0x1F8)

Also see the *DAC (Re-) Configuration* chapter.

4.2.2.2 DAC Correction Registers (0x170, 0x174, 0x178, 0x17C, 0x1A0, …)

These registers are intended for performing a DAC correction.

If used, the DAC correction registers should be configured while the DAC is operating in Manual Mode.

Leaving the DAC Correction Registers unmodified at their Reset Value effectively disables DAC Correction.

These registers are available per DAC device. There is a register for each DAC channel.

To enable data correction for a D/A channel, the offset and gain correction values for the specific DAC device, DAC channel and Output Range must be read from the Correction Data Space at PCI Base Address Register 1 (BAR1) and written to the corresponding DAC Correction Register.

To disable data correction for a D/A channel, the corresponding DAC Correction Registers must be set to all 0.

These registers may be accessed with 32 bit or 16 bit transfer size.

Bit	Symbol	Description	Access	Reset Value
31:16	GAIN_A	Gain Correction Value D/A Channel A	R/W	0x0000
15:0	OFFS_A	Offset Correction Value D/A Channel A	R/W	0x0000

Table 4-8 : DAC Correction Register A (0x170, 0x1A0, 0x1D0, 0x200)

Bit	Symbol	Description	Access	Reset Value
31:16	GAIN_B	Gain Correction Value D/A Channel B	R/W	0x0000
15:0	OFFS_B	Offset Correction Value D/A Channel B	R/W	0x0000

Table 4-9 : DAC Correction Register B (0x174, 0x1A4, 0x1D4, 0x204)

Bit	Symbol	Description	Access	Reset Value
31:16	GAIN_C	Gain Correction Value D/A Channel C	R/W	0x0000
15:0	OFFS_C	Offset Correction Value D/A Channel C	R/W	0x0000

Table 4-10 : DAC Correction Register C (0x178, 0x1A8, 0x1D8, 0x208)

Bit	Symbol	Description	Access	Reset Value
31:16	GAIN_D	Gain Correction Value D/A Channel D	R/W	0x0000
15:0	OFFS_D	Offset Correction Value D/A Channel D	R/W	0x0000

Table 4-11 : DAC Correction Register D (0x17C, 0x1AC, 0x1DC, 0x20C)

Also see the *DAC Data Correction* chapter.

4.2.2.3 DAC Data Registers (0x180, 0x184, 0x1B0, 0x1B4, …)

These registers are available per DAC device.

These registers are intended to be used for DACs operating in manual mode (not for DACs operating in sequencer mode).

A write to a DAC data register logs an internal request for transferring the conversion data (via the DAC serial interface) to the corresponding DAC device and D/A channel as soon as possible. If not already set, the DAC Busy bit in the Global DAC Status Register is set and remains so, until the data transfer to the DAC device is done.

These registers may be accessed with 32 bit or 16 bit transfer size.

Bit	Symbol	Description	Access	Reset Value
31:16	DATA_B	Digital Data for DAC Channel B	R/W	0x0000
15:0	DATA_A	Digital Data for DAC Channel A	R/W	0x0000

Table 4-12 : DAC Data Register A & B (0x180, 0x1B0, 0x1E0, 0x210)

Bit	Symbol	Description	Access	Reset Value
31:16	DATA_D	Digital Data for DAC Channel D	R/W	0x0000
15:0	DATA_C	Digital Data for DAC Channel C	R/W	0x0000

Table 4-13 : DAC Data Register C & D (0x184, 0x1B4, 0x1E4, 0x214)

Also see the *DAC Data Coding* chapter.

Also see the *D/A Manual Mode Conversions* chapter.

4.2.2.4 DAC Status Register(s) (0x188, 0x1B8, 0x1E8, 0x218)

This register is available per DAC device.

Each AD5755-1 DAC device provides an internal status register accessible via the DAC serial interface.

Setting the STAT_REQ bit logs an internal request for reading the actual status from the corresponding DAC device (via the DAC serial interface) as soon as possible. If not already set, the DAC Busy bit in the Global DAC Status Register is set and remains so, until the status read transfer from the DAC device is done.

Bit	Symbol	Description	Access	Reset Value
31	STAT_ REQ	Status Read Request When set, clears the Status Valid bit and logs a request for updating the DAC Status Register with current status information from the DAC device. This bit clears immediately. This is the recommended DAC Status Read Mode for DACs operating in Manual Mode.	R/S	0
30	STAT_ VAL	Status Valid 0: Stale Status Information 1: Updated Status Information The bit is set, when the DAC Status Register has been updated with actual status data from the DAC device. The bit is cleared upon logging a Status Read Request. The bit may also be cleared by writing a '1'.	R/C	0
29	-	Reserved	-	-
28	STAT_ AUTO	Automatic DAC Status Read Mode 0: Automatic DAC Status Read Mode Disabled 1: Automatic DAC Status Read Mode Enabled In automatic mode, the DAC Status Register is automatically updated after each DAC register write (e.g. after a DAC Data Register write). This is the recommended DAC Status Read Mode for DACs operating in Sequencer Mode.	R/W	0
27:16	-	Reserved	-	-
15	DC_D Fault	In current mode, this bit is set if the channel D DC/DC converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In voltage output mode, this bit is set if the channel D DC/DC converter is unable to regulate to 15V as expected.	R	x
14	DC_C Fault	In current mode, this bit is set if the channel C DC/DC converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In voltage output mode, this bit is set if the channel C DC/DC converter is unable to regulate to 15V as expected.	R	x
13	DC_B Fault	In current mode, this bit is set if the channel B DC/DC converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In voltage output mode, this bit is set if the channel B DC/DC converter is unable to regulate to 15V as expected.	R	x

Bit	Symbol	Description	Access	Reset Value
12	DC_A Fault	In current mode, this bit is set if the channel A DC/DC converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In voltage output mode, this bit is set if the channel A DC/DC converter is unable to regulate to 15V as expected.	R	x
11:9	-	Reserved	-	-
8	OVER TEMP	This bit is set if the AD5755-1 core temperature exceeds approximately 150°C.	R	x
7	VOUT_D Fault	This bit is set if a fault is detected on the AD5755-1 V_{OUT}_D pin.	R	x
6	VOUT_C Fault	This bit is set if a fault is detected on the AD5755-1 V_{OUT}_C pin.	R	x
5	VOUT_B Fault	This bit is set if a fault is detected on the AD5755-1 V_{OUT}_B pin.	R	x
4	VOUT_A Fault	This bit is set if a fault is detected on the AD5755-1 V_{OUT}_A pin.	R	x
3	IOUT_D Fault	This bit is set if a fault is detected on the AD5755-1 I_{OUT}_D pin.	R	x
2	IOUT_C Fault	This bit is set if a fault is detected on the AD5755-1 I_{OUT}_C pin.	R	x
1	IOUT_B Fault	This bit is set if a fault is detected on the AD5755-1 I_{OUT}_B pin.	R	x
0	IOUT_A Fault	This bit is set if a fault is detected on the AD5755-1 I_{OUT}_A pin.	R	x

Table 4-14 : DAC Status Register (0x188, 0x1B8, 0x1E8, 0x218)

Note that a Status Read Request has an impact on the maximum D/A conversion rate when the DAC is operating in Sequencer Mode.

Note that the DAC devices also provide a FAULT# status pin readable in the Global DAC Status Register. The FAULT# pin event is interrupt capable.

4.2.2.5 DAC Mode Register(s) (0x18C, 0x1BC, 0x1EC, 0x21C)

This register is available per DAC device.

By default, the DAC devices are operating in Manual Mode. Alternatively, a DAC device may be set to Sequencer Mode for periodic D/A conversions at a configurable conversion rate.

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1	DAC_ MAN_ CNV_ MODE	DAC Manual Conversion Mode (Manual Mode) 0: Immediate Conversion Mode 1: Controlled Conversion Mode This bit controls the DAC conversion pulse (LDAC# signal) generation when the DAC is operating in Manual Mode. In immediate conversion mode, a DAC conversion pulse is generated automatically when DAC data transfers are done. SW should wait until the DAC Busy Bit is clear before writing data for the next conversion. In controlled conversion mode, a DAC conversion pulse is generated upon SW request. D/A channel data must be transferred before. SW should wait until the DAC Busy Bit is clear (Global DAC Status Register, also see chapter *Programming Hints / Global DAC Status Register Read*!) before setting the conversion pulse request (Global DAC Control Register). This mode may be used for simultaneous D/A conversions in Manual Mode.	R/W	0
0	DAC_ OP_ MODE	DAC Operating Mode 0: Manual Mode 1: Sequencer Mode This bit sets the general DAC operating mode. In Manual Mode, the analog outputs are updated via software control (there is no periodic conversion rate). In Sequencer Mode, the analog outputs are getting updated simultaneously & periodically at a configurable conversion rate. See the *D/A Sequencer Registers* section.	R/W	0

Table 4-15 : DAC Mode Register (0x18C, 0x1BC, 0x1EC, 0x21C)

Note that all four channels of a (Quad) DAC device are always operating in the same operating mode (Manual Mode or Sequencer Mode).

4.2.3 D/A Sequencer Register

The D/A Sequencer is used for periodic digital to analog conversions at a configurable conversion rate.

Each DAC device may be assigned to the D/A sequencer.

All DAC devices assigned to the D/A sequencer are operating in simultaneous conversion mode. For each conversion, the analog output update is performed for all channels of all DAC devices assigned to the D/A sequencer.

The D/A sequencer may operate in Normal Mode or Frame Mode.

Normal Mode is used for generating a single block of D/A conversions by software request.

Frame Mode is used for generating a frame of D/A conversions upon a frame trigger signal event. Frame Mode may also be used for repetitive frames of D/A conversions at a configurable frame interval rate and for Multi-Board synchronization.

4.2.3.1 Sequencer Control Register (0x2E8)

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved	-	-
Sequencer DMA Control				
23:18	-	Reserved	-	-
17	SEQ_ DMA_ RST	Sequencer DMA Reset Initiates a DMA Engine reset (except register values). This bit is self-clearing.	R/S	0
16	SEQ_ DMA_ ENA	Sequencer DMA Enable 0: DMA Engine Disabled 1: DMA Engine Enabled Enables the internal sequencer DMA Engine. When being disabled, any active DMA transfer is completed before the DMA Engine enters Idle or Error state. In case of a DMA Engine error the DMA Engine operation is stopped. Upon a DMA Engine error, software should read the Sequencer Status Register and disable the sequencer DMA Engine afterwards. The sequencer DMA Engine is reset when disabled.	R/W	0
Sequencer FIFO Control				
15:9	-	Reserved	-	-
8	SEQ_ FIFO_ CLR	FIFO Clear Clears the sequencer's internal FIFO when set. This bit is self-clearing.	R/S	0
Sequencer Output Unit Control				
7:6	-	Reserved	-	-
5	SEQ_ CONV_ CLK_ SRC	Sequencer Conversion Clock Source These bits are selecting the sequencer’s conversion clock signal source. The selected sequencer conversion clock signal defines the sequencer’s conversion rate. Note that in Frame Mode, the sequencer conversion clock signal must be phase locked to the frame trigger signal. 0: Conversion Clock 1 (Selected Source) 1: Conversion Clock 2 (Selected Source)	R/W	0

Bit	Symbol	Description	Access	Reset Value
4	SEQ_ OU_ CLR_ PRLD	Sequencer Output Unit Clear DAC Pre-Load Status Setting this bit marks the sequencer DAC devices as 'un-loaded'. The DAC devices are automatically pre-loaded again when data is/becomes available in the sequencer FIFO. This bit is self-clearing.	R/S	0
3	SEQ_ OU_ CONV_ START	Sequencer Output Unit Start Conversion (Normal Mode) Setting this bit starts the conversion process in Normal Mode. Note that the Sequencer Output Unit must be enabled before. The sequencer FIFO level may be checked before setting this bit. This bit is self-clearing.	R/S	0
2	SEQ_ OU_ MODE	Sequencer Output Unit Mode 0: Normal Mode 1: Frame Mode Normal Mode: In Normal Mode, the configured number of D/A conversions is generated starting with the next conversion clock event after the conversion process has been started by software. Frame Mode: In Frame Mode, the configured number of D/A conversions is generated starting with the next conversion clock event after a (each) frame trigger signal event.	R/W	0
1	SEQ_ OU_ RST	Sequencer Output Unit Reset Initiates a sequencer output unit reset (except register values). This bit is self-clearing.	R/S	0
0	SEQ_ OU_ ENA	Sequencer Output Unit Enable 0: Sequencer Output Unit Disable 1: Sequencer Output Enable Enables the sequencer output unit. The sequencer output unit handles the data transfer to the sequencer's DAC devices and the DAC conversion pulse (LDAC# signal) generation. When enabled and while the sequencer DAC devices are not completely pre-loaded, data in the sequencer FIFO is automatically transferred to the sequencer's DAC devices for pre-loading the DACs for the first/next conversion (except in an error case). In case of a sequencer output unit error the sequencer output unit operation is stopped. Upon a sequencer output unit error, software should read the Sequencer Status Register and disable the sequencer output unit afterwards. The sequencer output unit is reset when disabled.	R/W	0

Table 4-16 : Sequencer Control Register (0x2E8)

4.2.3.2 Sequencer Status Register (0x2EC)

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved	-	-
Sequencer DMA Status				
23:21	-	Reserved	-	-
20	SEQ_ DMA_ DONE	Sequencer DMA Buffer Done This bit indicates that all values have been read from the DMA buffer. The bit is automatically cleared when a new DMA Buffer is validated by writing to the DMA Buffer Length Register while the DMA Engine is in Idle State.	R	0
19	-	Reserved	-	-
18	SEQ_ DMA_ ERR	Sequencer DMA Engine State: DMA Error Indicates that the DMA Engine is in an Error State. Possible causes: • PCI Master Abort (the addressed PCI Target did not respond) • PCI Target Abort (the addressed PCI Target detected a fatal error) In case of an error, the DMA engine operation is stopped. This bit is automatically cleared when the sequencer DMA Engine is disabled.	R	0
17	SEQ_ DMA_ BSY	Sequencer DMA Engine State: DMA Busy Indicates that the DMA Engine is currently busy (active).	R	0
16	SEQ_ DMA_ IDLE	Sequencer DMA Engine State: DMA Idle Indicates that the DMA Engine is in Idle State. A DMA transfer may be started (a DMA buffer may be validated) by writing to the DMA Buffer Length Register.	R	0
Sequencer FIFO Status				
15:8	-	Reserved	-	-

Sequencer Output Unit Status				
7	-	Reserved	-	-
6	SEQ_OU_FRM_ERR	Sequencer Output Unit Frame Error A next frame trigger event occurs, but the configured number of conversions has not been processed so far. In case of an error, the conversion process is terminated and the sequencer output unit operation is stopped. This bit is automatically cleared when the sequencer output unit is disabled.	R	0
5	SEQ_OU_CONV_TIME_ERR	Sequencer Output Unit Conversion Timing Error A next conversion pulse is due, but would violate the DAC timing specification. Possible causes: Too high conversion clock frequency, etc. In case of an error, the conversion process is terminated and the sequencer output unit operation is stopped. This bit is automatically cleared when the sequencer output unit is disabled.	R	0
4	SEQ_OU_CONV_DATA_ERR	Sequencer Output Unit Conversion Data Error A next conversion pulse is due, but not all sequencer DAC devices are in a proper pre-loaded state. Possible causes: FIFO data underrun, too high conversion clock frequency, etc. In case of an error, the conversion process is terminated and the sequencer output unit operation is stopped. This bit is automatically cleared when the sequencer output unit is disabled.	R	0
3	-	Reserved	-	-
2	SEQ_OU_ACT	Sequencer Output Unit Conversion Process Active Normal Mode: This bit is set when the software starts the conversion process and the bit is cleared when the configured number of conversions has been performed. Frame Mode: This bit is set upon a (each) frame trigger event that starts a conversion process (except in a frame error case) and the bit is cleared when the configured number of conversions has been performed (for a frame).	R	0
1	SEQ_OU_PRLD	Sequencer Output Unit DACs in Pre-Loaded State Indicates that all sequencer DAC devices are pre-loaded with conversion data for all four DAC channels. This bit is automatically cleared upon a DAC conversion pulse or when the software clears the pre-load status manually.	R	0
0	SEQ_OU_IDLE	Sequencer Output Unit in Idle State Indicates that the Sequencer Output Unit is in Idle State.	R	0

Table 4-17 : Sequencer Status Register (0x2EC)

4.2.3.3 Number of Conversions Register (0x2F4)

This register sets the desired number of D/A conversions per software request (Normal Mode) or frame trigger event (Frame Mode).

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	NUM_ CONV	Number of Conversions to be performed Normal Mode: Number of D/A conversions per software request. Set to 0 for continuous D/A conversions. When the configured number of conversions has been performed, the conversion process is stopped (until the next software request) and the corresponding bit in the Sequencer Status Register is cleared. Frame Mode: Number of D/A conversions per frame trigger event. Set to 0 for continuous D/A conversions after a single frame event. When the configured number of conversions has been performed, the conversion process is stopped (until the next frame trigger event) and the corresponding bit in the Sequencer Status Register is cleared.	R/W	0

Table 4-18 : Number of Conversions Register (0x2F4)

Note that for each sequencer controlled conversion event, all four D/A channels of all DAC devices assigned to the sequencer are updated simultaneously. After each sequencer controlled conversion event, the sequencer DAC devices are pre-loaded with conversion data for the next conversion event (provided data is available in the sequencer FIFO).

The number of required D/A data values per sequencer controlled conversion event is:
Number_of_DAC_Devices_assigned_to_the_Sequencer x 4 (Channels per DAC Device)

4.2.3.4 Conversion Count Register (0x2F8)

This register shows the number of D/A conversions that have been performed.

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	CONV_ CNT	Number of Conversions that have been performed (per D/A conversion block or frame). Normal Mode: The value is automatically cleared when the software starts the (next) conversion process. Frame Mode: The value is automatically cleared at the next frame trigger event (except in a frame error case).	R	0

Table 4-19 : Conversion Count Register (0x2F8)

4.2.3.5 FIFO Level Register (0x2FC)

Bit	Symbol	Description	Access	Reset Value
31:0	SEQ_ FIFO_ LVL	Sequencer FIFO Level This value shows the current sequencer FIFO fill level in Number of Bytes (FIFO size 32KB). A conversion data value consists of two bytes.	R	0

Table 4-20 : FIFO Level Register (0x2FC)

4.2.3.6 DMA Buffer Base Address Register (0x308)

Bit	Symbol	Description	Access	Reset Value
31:0	DMA_ BUF_ ADDR	DMA Buffer Base Address PCI memory mapped base address of the DMA Buffer in Host memory that provides D/A conversion data. The DMA Buffer base address is latched when the DMA Buffer Length Register is written while the DMA Engine is in Idle State.	R/W	0

Table 4-21 : DMA Buffer Base Address Register (0x308)

4.2.3.7 DMA Buffer Length Register (0x30C)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	DMA_ BUF_ LEN	DMA Buffer Length Byte Length of the provided DMA Buffer in Host RAM. **A write to the DMA Buffer Length Register initiates the DMA transfer.** Only effective when the sequencer DMA Engine is in Idle State.	R/W	0

Table 4-22 : DMA Buffer Length Register (0x30C)

4.2.3.8 DMA Buffer Next Address Register (0x310)

Bit	Symbol	Description	Access	Reset Value
31:0	DMA_ NEXT_ ADDR	DMA Buffer Next Address This register holds the PCI address of the address location in Host RAM the next D/A conversion data is read from.	R	0

Table 4-23 : DMA Buffer Next Address Register (0x310)

4.2.4 Conversion Signal Registers

These registers apply for Sequencer Mode operation.

There are three conversion signals, available for a sequencer:

- Conversion Clock 1
- Conversion Clock 2
- Frame Trigger

Each of the two Conversion Clock signals may be selected as the D/A Sequencer Conversion Clock in the D/A Sequencer Control Register for setting the sequencer's conversion rate.

The Frame Trigger signal (along with a conversion clock signal) is used to start a frame of D/A conversions in sequencer Frame Mode.

For each of these signals, there is an on-board signal generator provided.

For each of these signals, the signal source is configurable to be either the output signal of the on-board signal generator or an input signal from the I/O interface.

The on-board signal generator output signals may optionally be driven out on the I/O interface.

4.2.4.1 Conversion Clock 1 Generator Register (0x320)

This register controls the conversion clock 1 signal generation.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>30:29</td><td>CLK1_
GEN_
SRC</td><td>Clock Source
<table><tr><th>30:29</th><th>Internal Clock Source</th></tr><tr><td>00</td><td>20 MHz</td></tr><tr><td>01</td><td>22.05 MHz</td></tr><tr><td>10</td><td>60 MHz</td></tr><tr><td>11</td><td>Reserved</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>28</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>27:0</td><td>CLK1_
GEN_
DIV</td><td>Clock Divider
These bits set the divider for the selected clock source.
The frequency of the clock generator output is: $\frac{SRC\_CLK}{DIV+1}$</td><td>R/W</td><td>0xFFF FFFF</td></tr>
</table>

Table 4-24 : Conversion Clock 1 Generator Register (0x320)

4.2.4.2 Conversion Clock 2 Generator Register (0x324)

This register controls the conversion clock 2 signal generation.

Bit	Symbol	Description	Access	Reset Value
31	-	Reserved	-	-
30:29	CLK2_ GEN_ SRC	Clock Source 30:29 = 00: 20 MHz 30:29 = 01: 22.05 MHz 30:29 = 10: 60 MHz 30:29 = 11: Reserved	R/W	00
28	-	Reserved	-	-
27:0	CLK2_ GEN_ DIV	Clock Divider These bits set the divider for the selected clock source. The frequency of the clock generator output is: $\frac{SRC\_CLK}{DIV+1}$	R/W	0xFFF FFFF

Table 4-25 : Conversion Clock 2 Generator Register (0x324)

4.2.4.3 Frame Trigger Generator Register 1 (0x32C)

This register configures the frame trigger signal generation.

Bit	Symbol	Description	Access	Reset Value
31:30	-	Reserved	-	-
29	FTRIG_ GEN_ CLK_ SRC	Frame Trigger Associated Conversion Clock 0: The Frame Trigger Signal is generated for the Conversion Clock 1 Generator output signal 1: The Frame Trigger Signal is generated for the Conversion Clock 2 Generator output signal	R/W	0
28	-	Reserved	-	-
27:0	FTRIG_ GEN_ IVAL	Frame Trigger Interval Sets the frame trigger pulse interval in number of cycles of the associated clock signal. Frame Trigger Interval = (FTRIG_GEN_IVAL + 1) clock cycles. The frame trigger interval does not apply if the configured number of frame trigger pulses is 1.	R/W	0xFFF FFFF

Table 4-26 : Frame Trigger Generator Register 1 (0x32C)

4.2.4.4 Frame Trigger Generator Register 2 (0x330)

This register configures the frame trigger signal generation.

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	FTRIG_ GEN_ NUM	Number of Frame Trigger Pulses Sets the number of frame trigger pulses to be generated. Value 0 is for continuous frame trigger pulses at the configured frame trigger interval rate. Frame trigger signal generation is started via the Conversion Signal Generator Enable Register.	R/W	0

Table 4-27 : Frame Trigger Generator Register 2 (0x330)

4.2.4.5 Conversion Signal Generator Enable Register (0x33C)

This register provides enable control for the on-board conversion clock and frame trigger signal generators.

Bit	Symbol	Description	Access	Reset Value
31:10	-	Reserved	-	-
8	FTRIG_ GEN_ ENA	Frame Trigger Generation Enable Enables/Disables the frame trigger signal generation. If enabled, the configured number of frame trigger pulses is generated, starting with the next rising edge of the associated conversion clock signal. The conversion clock generator associated with the frame trigger generation must also be enabled.	R/W	0
7:2	-	Reserved	-	-
1	CLK2_ GEN_ ENA	Conversion Clock 2 Generator Enable 0: Clock Generator Disabled 1: Clock Generator Enabled	R/W	0
0	CLK1_ GEN_ ENA	Conversion Clock 1 Generator Enable 0: Clock Generator Disabled 1: Clock Generator Enabled	R/W	0

Table 4-28 : Conversion Signal Generator Enable Register (0x33C)

Note that for generating synchronized Clock 1 and Clock 2 signals, both conversion clock generators must be configured for the same clock source. Furthermore, the target clock frequencies must be integer multiples.

4.2.4.6 Conversion Signal Generator Output Driver Register (0x340)

This register is used for configuring output drivers for the output signals of the on-board conversion signal generators.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5:4</td><td>FTRIG_ GEN_ OUT_ CFG</td><td>Frame Trigger Generator Signal Output Driver Configuration
<table><tr><th>5:4</th><th>Output Driver Configuration</th></tr><tr><td>0x</td><td>Output Driver Disabled</td></tr><tr><td>10</td><td>Output Driver Enabled
P14 Rear I/O FRAME_TRIG Pin</td></tr><tr><td>11</td><td>Output Driver Enabled
Front I/O DIO 5 Line</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>3:2</td><td>CLK2_ GEN_ OUT_ CFG</td><td>Conversion Clock 2 Generator Signal Output Driver Configuration
<table><tr><th>3:2</th><th>Output Driver Configuration</th></tr><tr><td>0x</td><td>Output Driver Disabled</td></tr><tr><td>10</td><td>Output Driver Enabled
P14 Rear I/O CONV_CLK2 Pin</td></tr><tr><td>11</td><td>Output Driver Enabled
Front I/O DIO 3 Line</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>1:0</td><td>CLK1_ GEN_ OUT_ CFG</td><td>Conversion Clock 1 Generator Signal Output Driver Configuration
<table><tr><th>1:0</th><th>Output Driver Configuration</th></tr><tr><td>0x</td><td>Output Driver Disabled</td></tr><tr><td>10</td><td>Output Driver Enabled
P14 Rear I/O CONV_CLK1 Pin</td></tr><tr><td>11</td><td>Output Driver Enabled
Front I/O DIO 1 Line</td></tr></table></td><td>R/W</td><td>00</td></tr>
</table>

Table 4-29 : Conversion Signal Generator Output Driver Register (0x340)

Note that for driving out a Conversion Clock and/or Frame Trigger generator signal on the corresponding DIO front I/O pin, the corresponding bit combination must be set in the Conversion Signal Generator Output Driver Register and the corresponding bit in the DIO Output Enable Register must be clear.

The regular DIO output operation dominates, thus if a bit is set in the DIO Output Enable Register, the corresponding value set in the DIO Output Register is driven out on the DIO front I/O pin (regardless of the Conversion Signal Generator Output Driver Register setting).

4.2.4.7 Conversion Signal Source Selection Register (0x344)

This register is used for the selecting the signal source of the conversion control signals used by the sequencer(s).

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5:4</td><td>FTRIG_ SRC</td><td>Frame Trigger Signal Source<table><tr><th>5:4</th><th>Signal Source</th></tr><tr><td>0x</td><td>Internal Frame Trigger Generator</td></tr><tr><td>10</td><td>P14 Rear I/O FRAME_TRIG Input</td></tr><tr><td>11</td><td>Front I/O DIO 5 Line Input</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>3:2</td><td>CLK2_ SRC</td><td>Conversion Clock 2 Signal Source<table><tr><th>3:2</th><th>Signal Source</th></tr><tr><td>0x</td><td>Internal Clock 2 Generator</td></tr><tr><td>10</td><td>P14 Rear I/O CONV_CLK2 Input</td></tr><tr><td>11</td><td>Front I/O DIO 3 Line Input</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>1:0</td><td>CLK1_ SRC</td><td>Conversion Clock 1 Signal Source<table><tr><th>1:0</th><th>Signal Source</th></tr><tr><td>0x</td><td>Internal Clock 1 Generator</td></tr><tr><td>10</td><td>P14 Rear I/O CONV_CLK1 Input</td></tr><tr><td>11</td><td>Front I/O DIO 1 Line Input</td></tr></table></td><td>R/W</td><td>00</td></tr>
</table>

Table 4-30 : Conversion Signal Source Selection Register (0x344)

The following table shows typical Conversion Signal Path configuration examples.

PMC Configuration Example	Internal Signal Generator Enabled	Conversion Signal Generator Output Driver Configuration	Conversion Signal Source Selection
Single Card Standalone	Yes	Output Driver Disabled	Internal Signal Generator
Single Card with External Signal Generators	No	Output Driver Disabled	I/O Input
Multi-Board Master Card	Yes	Output Driver Enabled	I/O Input
Multi-Board Target Card	No	Output Driver Disabled	I/O Input

Table 4-31 : Conversion Signal Path Configuration Examples

4.2.4.8 Frame Timer Register (0x348)

Bit	Symbol	Description	Access	Reset Value
31	FTIM_ ENA	Frame Timer Enable 0: Frame Timer Disabled 1: Frame Timer Enabled If enabled, a frame trigger signal event (selected signal source) resets the frame timer and (re-) starts the timer process.	R/W	0
30	FTIM_ SRC	Frame Timer Clock Source 0: Conversion Clock 1 (Selected Signal Source) 1: Conversion Clock 2 (Selected Signal Source)	R/W	0
29	FTIM_ STAT	Frame Timer Event Status A frame timer event is generated when the frame timer expires. This bit is automatically cleared upon a (the next) frame trigger signal event (selected source).	R	0
28	-	Reserved	-	-
27:0	FTIM_ VAL	Frame Timer Value If enabled, the Frame Timer expires FTIM_VAL + 1 clock cycles after a frame trigger signal event (selected signal source).	R/W	0xFFF_ FFFF

Table 4-32 : Frame Timer Register (0x348)

4.2.5 DIO Registers

These registers are handling the Digital I/O interface available at the front I/O connector.

4.2.5.1 DIO Input Register (0x354)

The Digital I/O receivers are always enabled, so each DIO level can always be monitored.

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	-	-
19	IN20	DIO20 Input (see description for DIO1)	R	-
18	IN19	DIO19 Input (see description for DIO1)	R	-
17	IN18	DIO18 Input (see description for DIO1)	R	-
16	IN17	DIO17 Input (see description for DIO1)	R	-
15	IN16	DIO16 Input (see description for DIO1)	R	-
14	IN15	DIO15 Input (see description for DIO1)	R	-
13	IN14	DIO14 Input (see description for DIO1)	R	-
12	IN13	DIO13 Input (see description for DIO1)	R	-
11	IN12	DIO12 Input (see description for DIO1)	R	-
10	IN11	DIO11 Input (see description for DIO1)	R	-
9	IN10	DIO10 Input (see description for DIO1)	R	-
8	IN9	DIO9 Input (see description for DIO1)	R	-
7	IN8	DIO8 Input (see description for DIO1)	R	-
6	IN7	DIO7 Input (see description for DIO1)	R	-
5	IN6	DIO6 Input (see description for DIO1)	R	-
4	IN5	DIO5 Input (see description for DIO1)	R	-
3	IN4	DIO4 Input (see description for DIO1)	R	-
2	IN3	DIO3 Input (see description for DIO1)	R	-
1	IN2	DIO2 Input (see description for DIO1)	R	-
0	IN1	DIO1 Input Always reflects the actual input state of Digital I/O 1 (even if the DIO1 output driver is enabled in the DIO Output Enable Register). 0: Digital I/O 1 Line is low. 1: Digital I/O 1 Line is high.	R	-

Table 4-33 : DIO Input Register (0x354)

4.2.5.2 DIO Input Filter Register (0x358)

A debounce filter can be configured to get rid of bouncing on the digital I/O inputs.

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	-	-
15:0	DEB	Digital I/O Input Debounce Configuration T_{REJECT} = ([DEB + 1] x 50ns) Pulses with a duration smaller than T_{REJECT} are filtered and are not passed on to the internal logic. T_{PASS} = ([DEB + 1] x 75ns) = 1.5 x T_{REJECT} Pulses with a duration greater than T_{PASS} are not filtered and are passed on to the internal logic. Please note that pulses with a duration between T_{PASS} and T_{REJECT} may or may not be filtered.	R/W	0x0000

Table 4-34 : DIO Input Filter Register (0x358)

4.2.5.3 DIO Output Register (0x35C)

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	-	-
19	OUT20	DIO20 Output (see description for DIO1)	R/W	0
18	OUT19	DIO19 Output (see description for DIO1)	R/W	0
17	OUT18	DIO18 Output (see description for DIO1)	R/W	0
16	OUT17	DIO17 Output (see description for DIO1)	R/W	0
15	OUT16	DIO16 Output (see description for DIO1)	R/W	0
14	OUT15	DIO15 Output (see description for DIO1)	R/W	0
13	OUT14	DIO14 Output (see description for DIO1)	R/W	0
12	OUT13	DIO13 Output (see description for DIO1)	R/W	0
11	OUT12	DIO12 Output (see description for DIO1)	R/W	0
10	OUT11	DIO11 Output (see description for DIO1)	R/W	0
9	OUT10	DIO10 Output (see description for DIO1)	R/W	0
8	OUT9	DIO9 Output (see description for DIO1)	R/W	0
7	OUT8	DIO8 Output (see description for DIO1)	R/W	0
6	OUT7	DIO7 Output (see description for DIO1)	R/W	0
5	OUT6	DIO6 Output (see description for DIO1)	R/W	0
4	OUT5	DIO5 Output (see description for DIO1)	R/W	0
3	OUT4	DIO4 Output (see description for DIO1)	R/W	0
2	OUT3	DIO3 Output (see description for DIO1)	R/W	0
1	OUT2	DIO2 Output (see description for DIO1)	R/W	0
0	OUT1	DIO1 Output Sets the output state of the Digital I/O 1 line when the corresponding output driver is enabled in the DIO Output Enable Register. 0: Digital I/O 1 Line is driven low. 1: Digital I/O 1 Line is driven high.	R/W	0

Table 4-35 : DIO Output Register (0x35C)

4.2.5.4 DIO Output Enable Register (0x360)

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	-	-
19	OE20	DIO20 Output Enable (see description for DIO1)	R/W	0
18	OE19	DIO19 Output Enable (see description for DIO1)	R/W	0
17	OE18	DIO18 Output Enable (see description for DIO1)	R/W	0
16	OE17	DIO17 Output Enable (see description for DIO1)	R/W	0
15	OE16	DIO16 Output Enable (see description for DIO1)	R/W	0
14	OE15	DIO15 Output Enable (see description for DIO1)	R/W	0
13	OE14	DIO14 Output Enable (see description for DIO1)	R/W	0
12	OE13	DIO13 Output Enable (see description for DIO1)	R/W	0
11	OE12	DIO12 Output Enable (see description for DIO1)	R/W	0
10	OE11	DIO11 Output Enable (see description for DIO1)	R/W	0
9	OE10	DIO10 Output Enable (see description for DIO1)	R/W	0
8	OE9	DIO9 Output Enable (see description for DIO1)	R/W	0
7	OE8	DIO8 Output Enable (see description for DIO1)	R/W	0
6	OE7	DIO7 Output Enable (see description for DIO1)	R/W	0
5	OE6	DIO6 Output Enable (see description for DIO1)	R/W	0
4	OE5	DIO5 Output Enable (see description for DIO1)	R/W	0
3	OE4	DIO4 Output Enable (see description for DIO1)	R/W	0
2	OE3	DIO3 Output Enable (see description for DIO1)	R/W	0
1	OE2	DIO2 Output Enable (see description for DIO1)	R/W	0
0	OE1	DIO1 Output Enable 0: Digital I/O 1 Output Driver is disabled 1: Digital I/O 1 Output Driver is enabled If enabled, the level of the Digital I/O line is set in the DIO Output Register. The Digital I/O line receivers are always enabled and the DIO line level is always readable in the DIO Input Register.	R/W	0

Table 4-36 : DIO Output Enable Register (0x360)

4.2.6 Interrupt Registers

4.2.6.1 Interrupt Enable Register (0x36C)

For an interrupt status bit to be set, the interrupt must be enabled prior to the interrupt event.

Bit	Symbol	Description	Access	Reset Value
31:30	-	Reserved	-	-
29	FTIM_ INT_EN	Frame Timer Event Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
28	FTRIG_ INT_EN	Frame Trigger Event Interrupt Status 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
27:24	-	Reserved (A/D)	-	-
23:20	-	Reserved (D/A)	-	-
19	DAC4_ CONV_ INT_EN	DAC 4 Convert Event Interrupt Enable See description for DAC 1	R/W	0
18	DAC3_ CONV_ INT_EN	DAC 3 Convert Event Interrupt Enable See description for DAC 1	R/W	0
17	DAC2_ CONV_ INT_EN	DAC 2 Convert Event Interrupt Enable See description for DAC 1	R/W	0
16	DAC1_ CONV_ INT_EN	DAC 1 Convert Event Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
15:8	-	Reserved (A/D)	-	-
7:5	-	Reserved (D/A)	-	-
4	DA_SEQ_ CONV_ DONE_ INT_EN	D/A Sequencer Block/Frame Conversions Done Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
3:1	-	Reserved (D/A)	-	-
0	DA_SEQ_ DMA_ DONE_ INT_EN	D/A Sequencer DMA Buffer Done Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0

Table 4-37 : Interrupt Enable Register (0x36C)

4.2.6.2 Error Interrupt Enable Register (0x370)

For an interrupt status bit to be set, the interrupt must be enabled prior to the interrupt event.

Bit	Symbol	Description	Access	Reset Value
Sequencer Error Interrupt Enable				
31:24	-	Reserved (A/D)	-	-
23:20	-	Reserved (D/A)	-	-
19	DA_SEQ_FRAME_ERR_INT_EN	D/A Sequencer Frame Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
18	DA_SEQ_CONV_TIME_ERR_INT_EN	D/A Sequencer Conversion Timing Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
17	DA_SEQ_CONV_DATA_ERR_INT_EN	D/A Sequencer Conversion Data Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
16	DA_SEQ_DMA_ERR_INT_EN	D/A Sequencer DMA Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
Device Error Interrupt Enable				
15:8	-	Reserved (A/D)	-	-
7:4	-	Reserved (D/A)	-	-
3	DAC4_ERR_INT_EN	DAC 4 Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
2	DAC3_ERR_INT_EN	DAC 3 Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
1	DAC2_ERR_INT_EN	DAC 2 Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
0	DAC1_ERR_INT_EN	DAC 1 Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0

Table 4-38 : Error Interrupt Enable Register (0x370)

4.2.6.3 DIO Rising Edge Interrupt Enable Register (0x374)

For an interrupt status bit to be set, the interrupt must be enabled prior to the interrupt event.

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	-	-
19	DIO20_ RISE_ INT_EN	DIO 20 Rising Edge Interrupt Enable See description for DIO1	R/W	0
18	DIO19_ RISE_ INT_EN	DIO 19 Rising Edge Interrupt Enable See description for DIO1	R/W	0
17	DIO18_ RISE_ INT_EN	DIO 18 Rising Edge Interrupt Enable See description for DIO1	R/W	0
16	DIO17_ RISE_ INT_EN	DIO 17 Rising Edge Interrupt Enable See description for DIO1	R/W	0
15	DIO16_ RISE_ INT_EN	DIO 16 Rising Edge Interrupt Enable See description for DIO1	R/W	0
14	DIO15_ RISE_ INT_EN	DIO 15 Rising Edge Interrupt Enable See description for DIO1	R/W	0
13	DIO14_ RISE_ INT_EN	DIO 14 Rising Edge Interrupt Enable See description for DIO1	R/W	0
12	DIO13_ RISE_ INT_EN	DIO 13 Rising Edge Interrupt Enable See description for DIO1	R/W	0
11	DIO12_ RISE_ INT_EN	DIO 12 Rising Edge Interrupt Enable See description for DIO1	R/W	0
10	DIO11_ RISE_ INT_EN	DIO 11 Rising Edge Interrupt Enable See description for DIO1	R/W	0
9	DIO10_ RISE_ INT_EN	DIO 10 Rising Edge Interrupt Enable See description for DIO1	R/W	0
8	DIO9_ RISE_ INT_EN	DIO 9 Rising Edge Interrupt Enable See description for DIO1	R/W	0
7	DIO8_ RISE_ INT_EN	DIO 8 Rising Edge Interrupt Enable See description for DIO1	R/W	0
6	DIO7_ RISE_ INT_EN	DIO 7 Rising Edge Interrupt Enable See description for DIO1	R/W	0
5	DIO6_ RISE_ INT_EN	DIO 6 Rising Edge Interrupt Enable See description for DIO1	R/W	0

Bit	Symbol	Description	Access	Reset Value
4	DIO5_ RISE_ INT_EN	DIO 5 Rising Edge Interrupt Enable See description for DIO1	R/W	0
3	DIO4_ RISE_ INT_EN	DIO 4 Rising Edge Interrupt Enable See description for DIO1	R/W	0
2	DIO3_ RISE_ INT_EN	DIO 3 Rising Edge Interrupt Enable See description for DIO1	R/W	0
1	DIO2_ RISE_ INT_EN	DIO 2 Rising Edge Interrupt Enable See description for DIO1	R/W	0
0	DIO1_ RISE_ INT_EN	DIO 1 Rising Edge Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See DIO Interrupt Status Register.	R/W	0

Table 4-39 : DIO Rising Edge Interrupt Enable Register (0x374)

4.2.6.4 DIO Falling Edge Interrupt Enable Register (0x378)

For an interrupt status bit to be set, the interrupt must be enabled prior to the interrupt event.

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	-	-
19	DIO20_FALL_INT_EN	DIO 20 Falling Edge Interrupt Enable See description for DIO1	R/W	0
18	DIO19_FALL_INT_EN	DIO 19 Falling Edge Interrupt Enable See description for DIO1	R/W	0
17	DIO18_FALL_INT_EN	DIO 18 Falling Edge Interrupt Enable See description for DIO1	R/W	0
16	DIO17_FALL_INT_EN	DIO 17 Falling Edge Interrupt Enable See description for DIO1	R/W	0
15	DIO16_FALL_INT_EN	DIO 16 Falling Edge Interrupt Enable See description for DIO1	R/W	0
14	DIO15_FALL_INT_EN	DIO 15 Falling Edge Interrupt Enable See description for DIO1	R/W	0
13	DIO14_FALL_INT_EN	DIO 14 Falling Edge Interrupt Enable See description for DIO1	R/W	0
12	DIO13_FALL_INT_EN	DIO 13 Falling Edge Interrupt Enable See description for DIO1	R/W	0
11	DIO12_FALL_INT_EN	DIO 12 Falling Edge Interrupt Enable See description for DIO1	R/W	0
10	DIO11_FALL_INT_EN	DIO 11 Falling Edge Interrupt Enable See description for DIO1	R/W	0
9	DIO10_FALL_INT_EN	DIO 10 Falling Edge Interrupt Enable See description for DIO1	R/W	0
8	DIO9_FALL_INT_EN	DIO 9 Falling Edge Interrupt Enable See description for DIO1	R/W	0
7	DIO8_FALL_INT_EN	DIO 8 Falling Edge Interrupt Enable See description for DIO1	R/W	0
6	DIO7_FALL_INT_EN	DIO 7 Falling Edge Interrupt Enable See description for DIO1	R/W	0
5	DIO6_FALL_INT_EN	DIO 6 Falling Edge Interrupt Enable See description for DIO1	R/W	0

Bit	Symbol	Description	Access	Reset Value
4	DIO5_ FALL_ INT_EN	DIO 5 Falling Edge Interrupt Enable See description for DIO1	R/W	0
3	DIO4_ FALL__ INT_EN	DIO 4 Falling Edge Interrupt Enable See description for DIO1	R/W	0
2	DIO3_ FALL_ INT_EN	DIO 3 Falling Edge Interrupt Enable See description for DIO1	R/W	0
1	DIO2_ FALL_ INT_EN	DIO 2 Falling Edge Interrupt Enable See description for DIO1	R/W	0
0	DIO1_ FALL_ INT_EN	DIO 1 Falling Edge Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See DIO Interrupt Status Register.	R/W	0

Table 4-40 : DIO Falling Edge Interrupt Enable Register (0x378)

4.2.6.5 Interrupt Status Register (0x384)

A PCI interrupt is asserted if any bit is set in the Interrupt Status Register.

For an interrupt status bit to be set, the interrupt must be enabled prior to the interrupt event.

The interrupt acknowledge process depends on the corresponding setting in the Global Configuration Register.

Bit	Symbol	Description	Access	Reset Value
31	DIO_INT	Digital I/O Interrupt Status This bit is set if there is any bit set in the DIO Interrupt Status Register.	R	0
30	ERR_ INT	Error Interrupt Status This bit is set if there is any bit set in the Error Interrupt Status Register	R	0
29	FTIM_ INT	Frame Timer Event Interrupt Status If enabled, this bit is set upon a frame timer event (frame timer has expired)	R/C	0
28	FTRIG _INT	Frame Trigger Event Interrupt Status If enabled, this bit is set upon a frame trigger signal event (selected signal source).	R/C	0
27:24	-	Reserved (A/D)	-	-
23:20	-	Reserved (D/A)	-	-
19	DAC4_ CONV_ INT	DAC 4 Convert Event Interrupt Status See description for DAC 1	R/C	0
18	DAC3_ CONV_ INT	DAC 3 Convert Event Interrupt Status See description for DAC 1	R/C	0
17	DAC2_ CONV_ INT	DAC 2 Convert Event Interrupt Status See description for DAC 1	R/C	0
16	DAC1_ CONV_ INT	DAC 1 Convert Event Interrupt Status If enabled, this bit is set upon a DAC conversion event (the DAC analog outputs have just been updated). Intended for Manual Mode (not Sequencer Mode).	R/C	0
15:8	-	Reserved (A/D)	-	-
7:5	-	Reserved (D/A)	-	-
4	DA_ SEQ_ CONV_ DONE_ INT	D/A Sequencer Block/Frame Conversions Done Interrupt Status If enabled, the interrupt status bit is set when the configured number of conversions has been performed per request (Normal Mode) or frame (Frame Mode).	R/C	0
3:1	-	Reserved (D/A)	-	-
0	DA_ SEQ_ DMA_ DONE_ INT	D/A Sequencer DMA Buffer Done Interrupt Status If enabled, the interrupt status bit is set upon a DMA Buffer Done event.	R/C	0

Table 4-41 : Interrupt Status Register (0x384)

4.2.6.6 Error Interrupt Status Register (0x388)

Bit	Symbol	Description	Access	Reset Value
Sequencer Error Interrupt Status				
31:20	-	Reserved (A/D)	-	-
23:20	-	Reserved (D/A)	-	-
19	DA_SEQ_FRAME_ERR_INT	D/A Sequencer Frame Error Interrupt Status If enabled, this bit is set upon a sequencer frame error event. In case of an error event, the sequencer operation is stopped. See Sequencer Status Register for status information.	R/C	0
18	DA_SEQ_CONV_TIME_ERR_INT	D/A Sequencer Conversion Timing Error Interrupt Status If enabled, this bit is set upon a sequencer conversion timing error event. In case of an error event, the sequencer operation is stopped. See Sequencer Status Register for status information.	R/C	0
17	DA_SEQ_CONV_DATA_ERR_INT	D/A Sequencer Conversion Data Error Interrupt Status If enabled, this bit is set upon a sequencer conversion data error event. In case of an error event, the sequencer operation is stopped. See Sequencer Status Register for status information.	R/C	0
16	DA_SEQ_DMA_ERR_INT	D/A Sequencer DMA Error Interrupt Status In case of a DMA error event, the sequencer's DMA engine operation is stopped. See DMA Status Register for status information.	R/C	0
Device Error Interrupt Status				
15:8	-	Reserved (A/D)	-	-
7:4	-	Reserved (D/A)	-	-
3	DAC4_ERR_INT	DAC 4 Error Interrupt Status See description for DAC 1	R/C	0
2	DAC3_ERR_INT	DAC 3 Error Interrupt Status See description for DAC 1	R/C	0
1	DAC2_ERR_INT	DAC 2 Error Interrupt Status See description for DAC 1	R/C	0
0	DAC1_ERR_INT	DAC 1 Error Interrupt Status If enabled, this bit is set upon a DAC FAULT# pin assertion event.	R/C	0

Table 4-42 : Error Interrupt Status Register (0x388)

4.2.6.7 DIO Interrupt Status Register (0x38C)

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	-	-
19	DIO20_INT	Digital I/O 20 Interrupt Status See description for Digital I/O 1	R/C	0
18	DIO19_INT	Digital I/O 19 Interrupt Status See description for Digital I/O 1	R/C	0
17	DIO18_INT	Digital I/O 18 Interrupt Status See description for Digital I/O 1	R/C	0
16	DIO17_INT	Digital I/O 17 Interrupt Status See description for Digital I/O 1	R/C	0
15	DIO16_INT	Digital I/O 16 Interrupt Status See description for Digital I/O 1	R/C	0
14	DIO15_INT	Digital I/O 15 Interrupt Status See description for Digital I/O 1	R/C	0
13	DIO14_INT	Digital I/O 14 Interrupt Status See description for Digital I/O 1	R/C	0
12	DIO13_INT	Digital I/O 13 Interrupt Status See description for Digital I/O 1	R/C	0
11	DIO12_INT	Digital I/O 12 Interrupt Status See description for Digital I/O 1	R/C	0
10	DIO11_INT	Digital I/O 11 Interrupt Status See description for Digital I/O 1	R/C	0
9	DIO10_INT	Digital I/O 10 Interrupt Status See description for Digital I/O 1	R/C	0
8	DIO9_INT	Digital I/O 9 Interrupt Status See description for Digital I/O 1	R/C	0
7	DIO8_INT	Digital I/O 8 Interrupt Status See description for Digital I/O 1	R/C	0
6	DIO7_INT	Digital I/O 7 Interrupt Status See description for Digital I/O 1	R/C	0
5	DIO6_INT	Digital I/O 6 Interrupt Status See description for Digital I/O 1	R/C	0
4	DIO5_INT	Digital I/O 5 Interrupt Status See description for Digital I/O 1	R/C	0
3	DIO4_INT	Digital I/O 4 Interrupt Status See description for Digital I/O 1	R/C	0
2	DIO3_INT	Digital I/O 3 Interrupt Status See description for Digital I/O 1	R/C	0
1	DIO2_INT	Digital I/O 2 Interrupt Status See description for Digital I/O 1	R/C	0
0	DIO1_INT	Digital I/O 1 Interrupt Status If enabled, the interrupt status bit is set upon a rising and/or falling edge of the Digital I/O input signal (depending on the configuration of the DIO Rising/Falling Edge Interrupt Enable Registers).	R/C	0

Table 4-43 : DIO Interrupt Status Register (0x38C)

4.2.7 Other Registers

4.2.7.1 Global Configuration Register (0x398)

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1	INT_ ACK_ MODE	Interrupt Acknowledge Mode Sets the Interrupt Acknowledge Mode. 0: Clear by Write Mode 1: Clear on Read Mode Clear by Write Mode: Interrupts are acknowledged by writing a '1' to the corresponding interrupt status register bit. Clear on Read Mode: Interrupts are cleared when the corresponding interrupt status register is read.	R/W	0
0	DMA_ ENDIAN_ MODE	DMA Endian Mode Sets the Endian Mode for DMA access to Host Memory. 0: Little Endian Mode 16 bit D/A digital value are stored in Little Endian format in Host Memory. 1: Big Endian Mode 16 bit D/A digital value are stored in Big Endian format in Host Memory.	R/W	0

Table 4-44 : Global Configuration Register (0x398)

4.2.7.2 DIO Pull Reference Register (0x39C)

Each of the 20 Digital I/O lines is connected to an on-board 4.7kΩ pull resistor.
The common reference voltage for the pull resistors is configurable to be +3.3V, +5V, GND or floating.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:2</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>1:0</td><td>DIO_
VPULL</td><td>Digital I/O Line Pull Resistor Reference Configuration

<table><tr><th>1:0</th><th>DIO Pull Resistor Reference</th></tr><tr><td>00</td><td>Floating</td></tr><tr><td>01</td><td>+5V (Pull-Ups)</td></tr><tr><td>10</td><td>+3.3V (Pull-Ups)</td></tr><tr><td>11</td><td>GND (Pull-Downs)</td></tr></table></td><td>R/W</td><td>00</td></tr>
</table>

Table 4-45 : DIO Pull Reference Register (0x39C)

Note that in the default case (Floating), the pull resistors are all connected to each other on the floating reference signal side.

4.2.7.3 P14 I/O Pull Reference Register (0x3A0)

Each P14 I/O signal (CONV_CLK1, CONV_CLK2 and FRAME_TRIG) has a 4K7 pull resistor to a common reference.
The common reference voltage for the pull resistors is configurable to be +3.3V, +5V, GND or floating.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:2</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>1:0</td><td>P14_
VPULL</td><td>P14 I/O Line Pull Resistor Reference Configuration

<table><tr><th>1:0</th><th>P14 Pull Resistor Reference</th></tr><tr><td>00</td><td>Floating</td></tr><tr><td>01</td><td>+5V (Pull-Ups)</td></tr><tr><td>10</td><td>+3.3V (Pull-Ups)</td></tr><tr><td>11</td><td>GND (Pull-Downs)</td></tr></table></td><td>R/W</td><td>00</td></tr>
</table>

Table 4-46 : P14 I/O Pull Reference Register (0x3A0)

Note that in the default case (Floating), the pull resistors are all connected to each other on the floating reference signal side.

4.2.7.4 Correction Data EEPROM Control/Status Register (0x3A4)

Bit	Symbol	Description	Access	Reset Value
31:17	-	Reserved	-	-
16	EEBSY	Read-only Activity Status of the on-board Correction Data EEPROM 0: Correction Data EEPROM Not Busy 1: Correction Data EEPROM Busy After power-up or PCI reset, the content of the Correction Data EEPROM is automatically copied to the Correction Data Space. During this process, the EEBSY is set. The EEBSY bit is also set when the EELOCK field is changed from 0xABCD to a different value while data is written to (or read from) the EEPROM. Software should check that the EEBSY bit is '0' before reading data from the Correction Data Space.	R	0
15:0	EELOCK	Correction Data EEPROM Lock This field must be set to the value 0xABCD to allow write accesses to the Correction Data Space. Writes to the Correction Data Space are ignored otherwise. When the value of this field is changed from 0xABCD to a different value, an automatic EEPROM update procedure is started: The content of the Correction Data Space is programmed to the on-board Correction Data EEPROM, and is immediately read back to the Correction Data Space. The EEBSY bit is set during this procedure. Before setting EELOCK to 0xABCD, software should check that the EEBSY bit is clear.	R/W	0x0000

Table 4-47 : Correction Data EEPROM Control/Status Register (0x3A4)

Note that writing this register is intended for factory use only!

Writing this register may overwrite the DAC data correction values stored in the on-board EEPROM!

4.2.7.5 Temperature Sensor Trigger Register (0x3A8)

This register is used to trigger a measurement of the on-board temperature sensor.

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1	TS_AUTO	Temperature Sensor Auto Acquire Mode If this bit is set, the Temperature Sensor Data Register is automatically updated every second. If this bit is clear, the Temperature Sensor Trigger bit must be set for an update of the Temperature Sensor Data Register.	R/W	0
0	TS_TRIG	Temperature Sensor Trigger Write '1' to start reading the data from the on-board temperature sensor. This bit is cleared automatically when the data is valid in the Temperature Sensor Data Register.	R/S	0

Table 4-48 : Temperature Sensor Trigger Register (0x3A8)

4.2.7.6 Temperature Sensor Data Register (0x3AC)

This register holds the measured 13bit two's complement data of the on-board temperature sensor.

Bit	Symbol	Description	Access	Reset Value
31:0	TEMP	Measured data of the on-board temperature sensor The read value of the temperature sensor is stored sign-extended as a 32 bit two's complement. To actually calculate the temperature from the two's complement data value, use the following formula: Temperature (°C) = TEMP/256	R	0

Table 4-49 : Temperature Sensor Data Register (0x3AC)

4.2.7.7 Firmware Version Register (0x3FC)

Bit	Symbol	Description	Access	Reset Value
31:0	FID	Major & minor version, revision and build number of the FPGA firmware.	R	x

Table 4-50 : Firmware Version Register (0x3FC)

4.3 Correction Data Space

PCI Base Address Register 1 (Offset 0x14 in PCI Configuration Space).

DAC data correction values are determined at factory and can be read from this space.

The correction values are loaded from a serial EEPROM after power-up or PCI reset and are available as indicated via the EEBSY bit in the Correction Data EEPROM Control/Status Register.

There is an Offset Correction Value and a Gain Correction Value for each D/A Channel and each output range.

For the on-board logic (firmware) to perform DAC data correction, the correction values must be read from the Correction Data Space and be written to the corresponding DAC Correction Registers.

Also see the *DAC Correction Registers* section (Register Space chapter) and the *DAC Data Correction* chapter.

BAR1 Offset	D/A Channel	DAC Device	DAC Device Channel	Description	Size (Bit)
Output Range 0V … 5V					
0x000	DA_1A	1	A	$Offset_{CORR}$	16
0x002				$Gain_{CORR}$	16
0x004	DA_1B		B	$Offset_{CORR}$	16
0x006				$Gain_{CORR}$	16
0x008	DA_1C		C	$Offset_{CORR}$	16
0x00A				$Gain_{CORR}$	16
0x00C	DA_1D		D	$Offset_{CORR}$	16
0x00E				$Gain_{CORR}$	16
0x010	DA_2A	2	A	$Offset_{CORR}$	16
0x012				$Gain_{CORR}$	16
0x014	DA_2B		B	$Offset_{CORR}$	16
0x016				$Gain_{CORR}$	16
0x018	DA_2C		C	$Offset_{CORR}$	16
0x01A				$Gain_{CORR}$	16
0x01C	DA_2D		D	$Offset_{CORR}$	16
0x01E				$Gain_{CORR}$	16
0x020	DA_3A	3	A	$Offset_{CORR}$	16
0x022				$Gain_{CORR}$	16
0x024	DA_3B		B	$Offset_{CORR}$	16
0x026				$Gain_{CORR}$	16
0x028	DA_3C		C	$Offset_{CORR}$	16
0x02A				$Gain_{CORR}$	16
0x02C	DA_3D		D	$Offset_{CORR}$	16
0x02E				$Gain_{CORR}$	16

BAR1 Offset	D/A Channel	DAC Device	DAC Device Channel	Description	Size (Bit)
0x030	DA_4A	4	A	$Offset_{CORR}$	16
0x032				$Gain_{CORR}$	16
0x034	DA_4B		B	$Offset_{CORR}$	16
0x036				$Gain_{CORR}$	16
0x038	DA_4C		C	$Offset_{CORR}$	16
0x03A				$Gain_{CORR}$	16
0x03C	DA_4D		D	$Offset_{CORR}$	16
0x03E				$Gain_{CORR}$	16
Output Range 0V … 6V					
0x040	DA_1A	1	A	$Offset_{CORR}$	16
0x042				$Gain_{CORR}$	16
0x044	DA_1B		B	$Offset_{CORR}$	16
0x046				$Gain_{CORR}$	16
0x048	DA_1C		C	$Offset_{CORR}$	16
0x04A				$Gain_{CORR}$	16
0x04C	DA_1D		D	$Offset_{CORR}$	16
0x04E				$Gain_{CORR}$	16
0x050	DA_2A	2	A	$Offset_{CORR}$	16
0x052				$Gain_{CORR}$	16
0x054	DA_2B		B	$Offset_{CORR}$	16
0x056				$Gain_{CORR}$	16
0x058	DA_2C		C	$Offset_{CORR}$	16
0x05A				$Gain_{CORR}$	16
0x05C	DA_2D		D	$Offset_{CORR}$	16
0x05E				$Gain_{CORR}$	16
0x060	DA_3A	3	A	$Offset_{CORR}$	16
0x062				$Gain_{CORR}$	16
0x064	DA_3B		B	$Offset_{CORR}$	16
0x066				$Gain_{CORR}$	16
0x068	DA_3C		C	$Offset_{CORR}$	16
0x06A				$Gain_{CORR}$	16
0x06C	DA_3D		D	$Offset_{CORR}$	16
0x06E				$Gain_{CORR}$	16
0x070	DA_4A	4	A	$Offset_{CORR}$	16
0x072				$Gain_{CORR}$	16
0x074	DA_4B		B	$Offset_{CORR}$	16
0x076				$Gain_{CORR}$	16
0x078	DA_4C		C	$Offset_{CORR}$	16
0x07A				$Gain_{CORR}$	16
0x07C	DA_4D		D	$Offset_{CORR}$	16
0x07E				$Gain_{CORR}$	16

Output Range 0V … 10V					
0x080	DA_1A	1	A	$Offset_{CORR}$	16
0x082				$Gain_{CORR}$	16
0x084	DA_1B		B	$Offset_{CORR}$	16
0x086				$Gain_{CORR}$	16
0x088	DA_1C		C	$Offset_{CORR}$	16
0x08A				$Gain_{CORR}$	16
0x08C	DA_1D		D	$Offset_{CORR}$	16
0x08E				$Gain_{CORR}$	16
0x090	DA_2A	2	A	$Offset_{CORR}$	16
0x092				$Gain_{CORR}$	16
0x094	DA_2B		B	$Offset_{CORR}$	16
0x096				$Gain_{CORR}$	16
0x098	DA_2C		C	$Offset_{CORR}$	16
0x09A				$Gain_{CORR}$	16
0x09C	DA_2D		D	$Offset_{CORR}$	16
0x09E				$Gain_{CORR}$	16
0x0A0	DA_3A	3	A	$Offset_{CORR}$	16
0x0A2				$Gain_{CORR}$	16
0x0A4	DA_3B		B	$Offset_{CORR}$	16
0x0A6				$Gain_{CORR}$	16
0x0A8	DA_3C		C	$Offset_{CORR}$	16
0x0AA				$Gain_{CORR}$	16
0x0AC	DA_3D		D	$Offset_{CORR}$	16
0x0AE				$Gain_{CORR}$	16
0x0B0	DA_4A	4	A	$Offset_{CORR}$	16
0x0B2				$Gain_{CORR}$	16
0x0B4	DA_4B		B	$Offset_{CORR}$	16
0x0B6				$Gain_{CORR}$	16
0x0B8	DA_4C		C	$Offset_{CORR}$	16
0x0BA				$Gain_{CORR}$	16
0x0BC	DA_4D		D	$Offset_{CORR}$	16
0x0BE				$Gain_{CORR}$	16
Output Range 0V … 12V					
0x0C0	DA_1A	1	A	$Offset_{CORR}$	16
0x0C2				$Gain_{CORR}$	16
0x0C4	DA_1B		B	$Offset_{CORR}$	16
0x0C6				$Gain_{CORR}$	16
0x0C8	DA_1C		C	$Offset_{CORR}$	16
0x0CA				$Gain_{CORR}$	16
0x0CC	DA_1D		D	$Offset_{CORR}$	16
0x0CE				$Gain_{CORR}$	16

0x0D0	DA_2A	2	A	$Offset_{CORR}$	16
0x0D2				$Gain_{CORR}$	16
0x0D4	DA_2B		B	$Offset_{CORR}$	16
0x0D6				$Gain_{CORR}$	16
0x0D8	DA_2C		C	$Offset_{CORR}$	16
0x0DA				$Gain_{CORR}$	16
0x0DC	DA_2D		D	$Offset_{CORR}$	16
0x0DE				$Gain_{CORR}$	16
0x0E0	DA_3A	3	A	$Offset_{CORR}$	16
0x0E2				$Gain_{CORR}$	16
0x0E4	DA_3B		B	$Offset_{CORR}$	16
0x0E6				$Gain_{CORR}$	16
0x0E8	DA_3C		C	$Offset_{CORR}$	16
0x0EA				$Gain_{CORR}$	16
0x0EC	DA_3D		D	$Offset_{CORR}$	16
0x0EE				$Gain_{CORR}$	16
0x0F0	DA_4A	4	A	$Offset_{CORR}$	16
0x0F2				$Gain_{CORR}$	16
0x0F4	DA_4B		B	$Offset_{CORR}$	16
0x0F6				$Gain_{CORR}$	16
0x0F8	DA_4C		C	$Offset_{CORR}$	16
0x0FA				$Gain_{CORR}$	16
0x0FC	DA_4D		D	$Offset_{CORR}$	16
0x0FE				$Gain_{CORR}$	16
Output Range -5V … +5V					
0x100	DA_1A	1	A	$Offset_{CORR}$	16
0x102				$Gain_{CORR}$	16
0x104	DA_1B		B	$Offset_{CORR}$	16
0x106				$Gain_{CORR}$	16
0x108	DA_1C		C	$Offset_{CORR}$	16
0x10A				$Gain_{CORR}$	16
0x10C	DA_1D		D	$Offset_{CORR}$	16
0x10E				$Gain_{CORR}$	16
0x110	DA_2A	2	A	$Offset_{CORR}$	16
0x112				$Gain_{CORR}$	16
0x114	DA_2B		B	$Offset_{CORR}$	16
0x116				$Gain_{CORR}$	16
0x118	DA_2C		C	$Offset_{CORR}$	16
0x11A				$Gain_{CORR}$	16
0x11C	DA_2D		D	$Offset_{CORR}$	16
0x11E				$Gain_{CORR}$	16

0x120	DA_3A	3	A	$Offset_{CORR}$	16
0x122				$Gain_{CORR}$	16
0x124	DA_3B		B	$Offset_{CORR}$	16
0x126				$Gain_{CORR}$	16
0x128	DA_3C		C	$Offset_{CORR}$	16
0x12A				$Gain_{CORR}$	16
0x12C	DA_3D		D	$Offset_{CORR}$	16
0x12E				$Gain_{CORR}$	16
0x130	DA_4A	4	A	$Offset_{CORR}$	16
0x132				$Gain_{CORR}$	16
0x134	DA_4B		B	$Offset_{CORR}$	16
0x136				$Gain_{CORR}$	16
0x138	DA_4C		C	$Offset_{CORR}$	16
0x13A				$Gain_{CORR}$	16
0x13C	DA_4D		D	$Offset_{CORR}$	16
0x13E				$Gain_{CORR}$	16
Output Range -6V … +6V					
0x140	DA_1A	1	A	$Offset_{CORR}$	16
0x142				$Gain_{CORR}$	16
0x144	DA_1B		B	$Offset_{CORR}$	16
0x146				$Gain_{CORR}$	16
0x148	DA_1C		C	$Offset_{CORR}$	16
0x14A				$Gain_{CORR}$	16
0x14C	DA_1D		D	$Offset_{CORR}$	16
0x14E				$Gain_{CORR}$	16
0x150	DA_2A	2	A	$Offset_{CORR}$	16
0x152				$Gain_{CORR}$	16
0x154	DA_2B		B	$Offset_{CORR}$	16
0x156				$Gain_{CORR}$	16
0x158	DA_2C		C	$Offset_{CORR}$	16
0x15A				$Gain_{CORR}$	16
0x15C	DA_2D		D	$Offset_{CORR}$	16
0x15E				$Gain_{CORR}$	16
0x160	DA_3A	3	A	$Offset_{CORR}$	16
0x162				$Gain_{CORR}$	16
0x164	DA_3B		B	$Offset_{CORR}$	16
0x166				$Gain_{CORR}$	16
0x168	DA_3C		C	$Offset_{CORR}$	16
0x16A				$Gain_{CORR}$	16
0x16C	DA_3D		D	$Offset_{CORR}$	16
0x16E				$Gain_{CORR}$	16

0x170	DA_4A	4	A	$Offset_{CORR}$	16
0x172				$Gain_{CORR}$	16
0x174	DA_4B		B	$Offset_{CORR}$	16
0x176				$Gain_{CORR}$	16
0x178	DA_4C		C	$Offset_{CORR}$	16
0x17A				$Gain_{CORR}$	16
0x17C	DA_4D		D	$Offset_{CORR}$	16
0x17E				$Gain_{CORR}$	16
Output Range -10V … +10V					
0x180	DA_1A	1	A	$Offset_{CORR}$	16
0x182				$Gain_{CORR}$	16
0x184	DA_1B		B	$Offset_{CORR}$	16
0x186				$Gain_{CORR}$	16
0x188	DA_1C		C	$Offset_{CORR}$	16
0x18A				$Gain_{CORR}$	16
0x18C	DA_1D		D	$Offset_{CORR}$	16
0x18E				$Gain_{CORR}$	16
0x190	DA_2A	2	A	$Offset_{CORR}$	16
0x192				$Gain_{CORR}$	16
0x194	DA_2B		B	$Offset_{CORR}$	16
0x196				$Gain_{CORR}$	16
0x198	DA_2C		C	$Offset_{CORR}$	16
0x19A				$Gain_{CORR}$	16
0x19C	DA_2D		D	$Offset_{CORR}$	16
0x19E				$Gain_{CORR}$	16
0x1A0	DA_3A	3	A	$Offset_{CORR}$	16
0x1A2				$Gain_{CORR}$	16
0x1A4	DA_3B		B	$Offset_{CORR}$	16
0x1A6				$Gain_{CORR}$	16
0x1A8	DA_3C		C	$Offset_{CORR}$	16
0x1AA				$Gain_{CORR}$	16
0x1AC	DA_3D		D	$Offset_{CORR}$	16
0x1AE				$Gain_{CORR}$	16
0x1B0	DA_4A	4	A	$Offset_{CORR}$	16
0x1B2				$Gain_{CORR}$	16
0x1B4	DA_4B		B	$Offset_{CORR}$	16
0x1B6				$Gain_{CORR}$	16
0x1B8	DA_4C		C	$Offset_{CORR}$	16
0x1BA				$Gain_{CORR}$	16
0x1BC	DA_4D		D	$Offset_{CORR}$	16
0x1BE				$Gain_{CORR}$	16

Output Range -12V … +12V					
0x1C0	DA_1A	1	A	$Offset_{CORR}$	16
0x1C2				$Gain_{CORR}$	16
0x1C4	DA_1B		B	$Offset_{CORR}$	16
0x1C6				$Gain_{CORR}$	16
0x1C8	DA_1C		C	$Offset_{CORR}$	16
0x1CA				$Gain_{CORR}$	16
0x1CC	DA_1D		D	$Offset_{CORR}$	16
0x1CE				$Gain_{CORR}$	16
0x1D0	DA_2A	2	A	$Offset_{CORR}$	16
0x1D2				$Gain_{CORR}$	16
0x1D4	DA_2B		B	$Offset_{CORR}$	16
0x1D6				$Gain_{CORR}$	16
0x1D8	DA_2C		C	$Offset_{CORR}$	16
0x1DA				$Gain_{CORR}$	16
0x1DC	DA_2D		D	$Offset_{CORR}$	16
0x1DE				$Gain_{CORR}$	16
0x1E0	DA_3A	3	A	$Offset_{CORR}$	16
0x1E2				$Gain_{CORR}$	16
0x1E4	DA_3B		B	$Offset_{CORR}$	16
0x1E6				$Gain_{CORR}$	16
0x1E8	DA_3C		C	$Offset_{CORR}$	16
0x1EA				$Gain_{CORR}$	16
0x1EC	DA_3D		D	$Offset_{CORR}$	16
0x1EE				$Gain_{CORR}$	16
0x1F0	DA_4A	4	A	$Offset_{CORR}$	16
0x1F2				$Gain_{CORR}$	16
0x1F4	DA_4B		B	$Offset_{CORR}$	16
0x1F6				$Gain_{CORR}$	16
0x1F8	DA_4C		C	$Offset_{CORR}$	16
0x1FA				$Gain_{CORR}$	16
0x1FC	DA_4D		D	$Offset_{CORR}$	16
0x1FE				$Gain_{CORR}$	16
Output Range 4mA … 20mA					
0x200	DA_1A	1	A	$Offset_{CORR}$	16
0x202				$Gain_{CORR}$	16
0x204	DA_1B		B	$Offset_{CORR}$	16
0x206				$Gain_{CORR}$	16
0x208	DA_1C		C	$Offset_{CORR}$	16
0x20A				$Gain_{CORR}$	16
0x20C	DA_1D		D	$Offset_{CORR}$	16
0x20E				$Gain_{CORR}$	16

0x210	DA_2A	2	A	$Offset_{CORR}$	16
0x212				$Gain_{CORR}$	16
0x214	DA_2B		B	$Offset_{CORR}$	16
0x216				$Gain_{CORR}$	16
0x218	DA_2C		C	$Offset_{CORR}$	16
0x21A				$Gain_{CORR}$	16
0x21C	DA_2D		D	$Offset_{CORR}$	16
0x21E				$Gain_{CORR}$	16
0x220	DA_3A	3	A	$Offset_{CORR}$	16
0x222				$Gain_{CORR}$	16
0x224	DA_3B		B	$Offset_{CORR}$	16
0x226				$Gain_{CORR}$	16
0x228	DA_3C		C	$Offset_{CORR}$	16
0x22A				$Gain_{CORR}$	16
0x22C	DA_3D		D	$Offset_{CORR}$	16
0x22E				$Gain_{CORR}$	16
0x230	DA_4A	4	A	$Offset_{CORR}$	16
0x232				$Gain_{CORR}$	16
0x234	DA_4B		B	$Offset_{CORR}$	16
0x236				$Gain_{CORR}$	16
0x238	DA_4C		C	$Offset_{CORR}$	16
0x23A				$Gain_{CORR}$	16
0x23C	DA_4D		D	$Offset_{CORR}$	16
0x23E				$Gain_{CORR}$	16
Output Range 0mA … 20mA					
0x240	DA_1A	1	A	$Offset_{CORR}$	16
0x242				$Gain_{CORR}$	16
0x244	DA_1B		B	$Offset_{CORR}$	16
0x246				$Gain_{CORR}$	16
0x248	DA_1C		C	$Offset_{CORR}$	16
0x24A				$Gain_{CORR}$	16
0x24C	DA_1D		D	$Offset_{CORR}$	16
0x24E				$Gain_{CORR}$	16
0x250	DA_2A	2	A	$Offset_{CORR}$	16
0x252				$Gain_{CORR}$	16
0x254	DA_2B		B	$Offset_{CORR}$	16
0x256				$Gain_{CORR}$	16
0x258	DA_2C		C	$Offset_{CORR}$	16
0x25A				$Gain_{CORR}$	16
0x25C	DA_2D		D	$Offset_{CORR}$	16
0x25E				$Gain_{CORR}$	16

0x260	DA_3A	3	A	$Offset_{CORR}$	16
0x262				$Gain_{CORR}$	16
0x264	DA_3B		B	$Offset_{CORR}$	16
0x266				$Gain_{CORR}$	16
0x268	DA_3C		C	$Offset_{CORR}$	16
0x26A				$Gain_{CORR}$	16
0x26C	DA_3D		D	$Offset_{CORR}$	16
0x26E				$Gain_{CORR}$	16
0x270	DA_4A	4	A	$Offset_{CORR}$	16
0x272				$Gain_{CORR}$	16
0x274	DA_4B		B	$Offset_{CORR}$	16
0x276				$Gain_{CORR}$	16
0x278	DA_4C		C	$Offset_{CORR}$	16
0x27A				$Gain_{CORR}$	16
0x27C	DA_4D		D	$Offset_{CORR}$	16
0x27E				$Gain_{CORR}$	16
Output Range 0mA … 24mA					
0x280	DA_1A	1	A	$Offset_{CORR}$	16
0x282				$Gain_{CORR}$	16
0x284	DA_1B		B	$Offset_{CORR}$	16
0x286				$Gain_{CORR}$	16
0x288	DA_1C		C	$Offset_{CORR}$	16
0x28A				$Gain_{CORR}$	16
0x28C	DA_1D		D	$Offset_{CORR}$	16
0x28E				$Gain_{CORR}$	16
0x290	DA_2A	2	A	$Offset_{CORR}$	16
0x292				$Gain_{CORR}$	16
0x294	DA_2B		B	$Offset_{CORR}$	16
0x296				$Gain_{CORR}$	16
0x298	DA_2C		C	$Offset_{CORR}$	16
0x29A				$Gain_{CORR}$	16
0x29C	DA_2D		D	$Offset_{CORR}$	16
0x29E				$Gain_{CORR}$	16
0x2A0	DA_3A	3	A	$Offset_{CORR}$	16
0x2A2				$Gain_{CORR}$	16
0x2A4	DA_3B		B	$Offset_{CORR}$	16
0x2A6				$Gain_{CORR}$	16
0x2A8	DA_3C		C	$Offset_{CORR}$	16
0x2AA				$Gain_{CORR}$	16
0x2AC	DA_3D		D	$Offset_{CORR}$	16
0x2AE				$Gain_{CORR}$	16

0x2B0	DA_4A	4	A	$Offset_{CORR}$	16
0x2B2				$Gain_{CORR}$	16
0x2B4	DA_4B		B	$Offset_{CORR}$	16
0x2B6				$Gain_{CORR}$	16
0x2B8	DA_4C		C	$Offset_{CORR}$	16
0x2BA				$Gain_{CORR}$	16
0x2BC	DA_4D		D	$Offset_{CORR}$	16
0x2BE				$Gain_{CORR}$	16
Reserved					
0x2C0 … 0x7FA	Reserved			Reserved	16
Serial Number					
0x7FC	Serial Number High Word				16
0x7FE	Serial Number Low Word				16

Table 4-51 : Correction Data Space

For the TPMC542-20R the correction values for DAC3 and DAC4 are reserved.

5 I/O Interface Description

5.1 Digital I/O Interface

The TPMC542 provides 20 Digital I/O lines available at the front I/O connector.

Each digital I/O line features a receiver, a driver with output enable control, a 47R series resistor, ESD protection diodes and a 4K7 pull resistor to a common reference voltage.

The driver level is LVTTL (3.3V). The receiver accepts LVTTL (3.3V) and TTL (5V) levels.

The common pull resistor reference is programmable. Options are Open | 3.3V | 5V | GND.

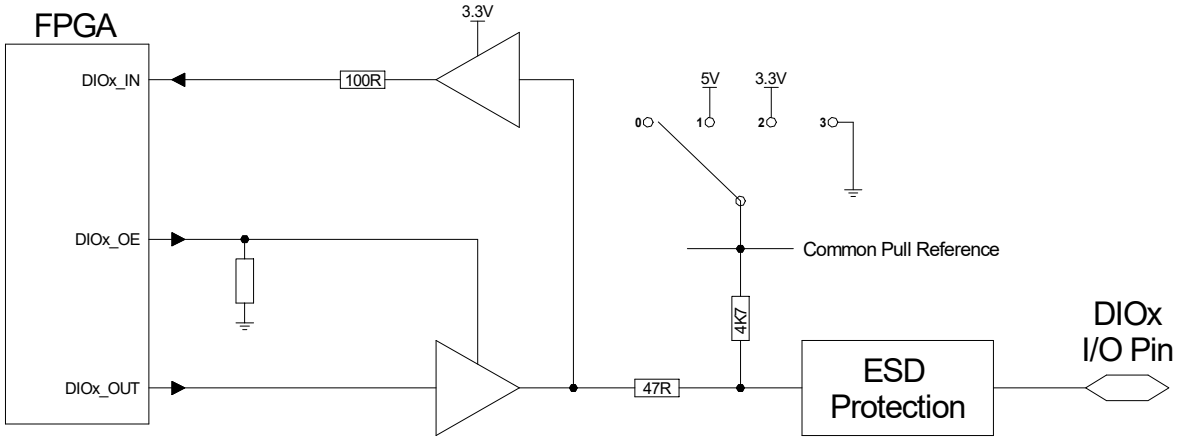


Figure 5-1 : Digital I/O Line Circuit

At power-up and/or after reset, all Digital I/O lines are configured as inputs. The pull resistor reference is floating and has to be configured by software whether to let the pull resistors operate as pull-down resistors to GND or as pull-up resistors to either +3.3V or +5V.

The receiver function is always enabled and may be used to monitor the I/O line level even when the I/O line is operating as an output.

Because of the series resistor, there is a reduced high-level voltage at the I/O pin when the output buffer sources a noticeable current to the external load while driving a high-level. To maintain a proper TTL high level, the recommended maximum I/O source current is 15 mA.

Also because of the series resistor, there is an increased low-level voltage at the I/O pin when the output buffer sinks a noticeable current from the external load while driving a low-level. To maintain a proper TTL low level, the recommended maximum I/O sink current is 6 mA.

For achieving a 5 V CMOS high-level output voltage (V_{OH} >= 3.5 V), the external load must be high impedance and the on-board common pull resistor reference must be set to 5V pull-up. The corresponding bit in the DIO Output Register must be set to 0 while the I/O output level is controlled via the corresponding bit in the DIO Output Enable Register with an inverted logic. To maintain a proper 5 V CMOS high level, the I/O load (leakage) current should not exceed 250 µA. A low impedance path to ground on the I/O load would result in a voltage divider with the on-board pull-up resistor, significantly reducing the high-level voltage at the I/O pin.

Each Digital I/O input is capable of generating an interrupt on either the rising edge or falling edge.

A common configurable debouncer setting may be applied to the Digital I/O inputs.

Pull Resistor Configuration	DIO Output Enable Register OEx Bit	DIO Output Register OUTx Bit	DIO Output Level
Open	0	x	Floating
	1	0	Active Low
	1	1	Active High (3.3V)
Pull-Up to 3.3V	0	x	Pulled High (3.3V)
	1	0	Active Low
	1	1	Active High (3.3V)
Pull-Up to 5V	0	x	Pulled High (5V)
	1	0	Active Low
	1	1	Active High (3.3V)
Pull-Down to GND	0	x	Pulled Low
	1	0	Active Low
	1	1	Active High (3.3V)

Table 5-1 : DIO Output Level Configuration

Note that the default configuration for the pull resistor reference is “Open”.

Note that in the “Open” case, the pull resistors are still connected to each other via the common reference rail.

5.2 Analog Output Interface

The TPMC542 provides up to 16 analog output channels (D/A channels) available at the front I/O connector.

Analog Devices AD5755-1 Quad-DAC devices are used for the analog outputs.

Each AD5755-1 device provides four 16 bit single-ended D/A channels (DAC Channels A-D).

The TPMC542-10R order option provides four AD5755-1 DAC devices (DACs 1 - 4), thus sixteen D/A channels.

The TPMC542-20R order option provides two AD5755-1 DAC devices (DACs 1 & 2), thus eight D/A channels.

For each D/A channel, the output mode/range is programmable with the following options:

- Voltage Range 0V to 5V
- Voltage Range 0V to 6V (by Overrange Option)
- Voltage Range 0V to 10V
- Voltage Range 0V to 12V (by Overrange Option)
- Voltage Range ±5V
- Voltage Range ±6V (by Overrange Option)
- Voltage Range ±10V
- Voltage Range ±12V (by Overrange Option)
- Current Range 4mA to 20mA
- Current Range 0mA to 20mA
- Current Range 0ma to 24mA

In Voltage Output Mode, each analog output channel is capable of driving up to 10mA load current with a capacitive load of up to 10nF. Output settling time depends on the voltage step size and the actual load. Settling time increases with capacitive load. Settling time figures for a test-load of 2K | 220pF are 11us (typ) for a 5V step in the 0V to 5V range and 18us (max) for a 10V step in the 0V to 10V range.

In Current Output Mode, an external load resistor (to ground) is required on the analog output. The AD5755-1 DAC supports external load resistor values of up to 1K per channel in current mode. However, for limiting the power consumption and dissipation, the maximum external load resistor value should not exceed 680R per channel. A load resistor value of 390 Ohm or less is recommended per channel. For reducing the on-board power consumption and dissipation, each channel's current output stage is operating with a dedicated on-board generated DC power supply that is dynamically adapted to the actual current load requirements. This feature allows a broad range of supported load resistor values (up to 1K) while keeping on-board power dissipation within limits when low load resistor values (e.g. down to 100R) are used. On the other hand, this feature implies that a large output current step requires an automatic adaption of the channel's current output stage supply voltage first, reducing the current output settling time. In Current Output Mode, the output settling may take about 1.2ms for a 0 mA to 24mA step into a 1K load.

The maximum rate for the sequencer controlled periodic simultaneous D/A conversions is 38ksps.

The AD5755-1 provides a FAULT# output pin for indicating error conditions. The fault pin status is readable in a status register and is also capable of generating an interrupt. The FAULT# pin is forced active by any of the following conditions:

- A short circuit or overcurrent is detected on a voltage output

- An open circuit or too high resistance value is detected on a current output (the AD5755-1 internal amplifier in the current mode output stage has less than approx. 1V remaining drive capability)
- The AD5755-1 chip temperature exceeds the maximum limit

Also see the notes in the *Handling and Operation Instructions* chapter!

6 DAC (Re-) Configuration

The DAC devices on the TPMC542 must be configured (power-up, output range, output enable) before use via the *DAC Configuration Register(s)*. The output range is configurable per D/A channel.

In general, a D/A channel should be configured for the desired output range and powered up first while the corresponding analog output is kept disabled. The D/A channel should then be loaded with the appropriate zero or mid-scale value (including a conversion to propagate the value right through to the DAC internal DAC Register) before the corresponding analog output is enabled.

Example Sequence for (re-) configuring a D/A channel:

- Set the DAC operating mode to Manual Immediate Conversion Mode (default after reset)
  → *DAC Mode Register*
- Disable the D/A channel output and power-down the D/A channel (default after reset)
  → *DAC Configuration Register*
- Wait until the DAC is no longer busy
  → *Global DAC Status Register*
- Configure the D/A channel output range and power-up the D/A channel (keep the D/A channel output disabled)
  → *DAC Configuration Register*
- Wait until the DAC is no longer busy
  → *Global DAC Status Register*
- Write 0x0001 to the D/A channel Data Register (also provides a trailing DAC conversion pulse)
  → *DAC Data Register*

  This step ensures that the following 0x0000 value will differ from the value stored in the DACs internal DAC Data Register and therefore provides that the 0x0000 value will propagate through the register stage inside the DAC device (the 0x0000 value may be ignored otherwise).
- Wait until the DAC is no longer busy
  → *Global DAC Status Register*
- Write 0x0000 to the D/A channel Data Register (also provides a trailing DAC conversion pulse)
  → *DAC Data Register*
- Wait until the DAC is no longer busy
  → *Global DAC Status Register*
- Enable the D/A channel output (while keeping the output range and power-up configuration)
  → *DAC Configuration Register*
- Wait until the DAC is no longer busy
  → *Global DAC Status Register*

See the *DAC Configuration Register(s)* section in the *Register Space* chapter.

7 DAC Data Coding

The TPMC542 provides Straight Binary Data Coding for the Unipolar Voltage Ranges and all Current Ranges, and Two's Complement Data Coding for the Bipolar Voltage Ranges.

Analog Output	Unipolar Voltage Output				Digital Code (Straight Binary)
Output Range	**+5V**	**+6V**	**+10V**	**+12V**	
LSB	76.29uV	91.55uV	152.59uV	183.11uV	
Full-Scale	4.999924V	5.999908V	9.999847V	11.999817V	0xFFFF
Full-Scale – 1 LSB	4.999847V	5.999817V	9.999695V	11.999634V	0xFFFE
Mid-Scale + 1 LSB	2.500076V	3.000092V	5.000153V	6.000183V	0x8001
Mid-Scale	2.5V	3V	5V	6V	0x8000
Mid-Scale – 1 LSB	2.499924V	2.999908V	4.999847v	5.999817V	0x7FFF
Zero-Scale + 1 LSB	76.29uV	91.55uV	152.59uV	183.11uV	0x0001
Zero-Scale	0V	0V	0V	0V	0x0000

Table 7-1 : DAC Data Coding - Unipolar Voltage Output Range

Analog Output	Bipolar Voltage Output				Digital Code (Two's Complement)
Output Range	**±5V**	**±6V**	**±10V**	**±12V**	
LSB	152.59uV	183.11uV	305.18uV	366.21uV	
Pos. Full-Scale	+4.999847V	+5.999817V	+9.999695V	+11.999634v	0x7FFF
Pos. Full Scale – 1 LSB	+4.999695V	+5.999634V	+9.999390V	+11.999268V	0x7FFE
Mid-Scale + 1 LSB	+152.59uV	+183.11uV	+305.18uV	+366.21uV	0x0001
Mid-Scale	0V	0V	0V	0V	0x0000
Mid-Scale – 1 LSB	-152.59uV	-183.11uV	-305.18uV	-366.21uV	0xFFFF
Neg. Full Scale + 1 LSB	-4.999847V	-5.999817V	-9.999695V	-11.999634v	0x8001
Neg. Full Scale	-5V	-6V	-10V	-12V	0x8000

Table 7-2 : DAC Data Coding - Bipolar Voltage Output Range

Analog Output	Current Output			Digital Code (Straight Binary)
Output Range	**4…20mA**	**0…20mA**	**0…24mA**	
LSB	244.141nA	305.176nA	366.211nA	
Full-Scale	19.999756mA	19.999695mA	23.999634mA	0xFFFF
Full-Scale – 1 LSB	19.999512mA	19.999390mA	23.999268mA	0xFFFE
Mid-Scale + 1 LSB	12.000244mA	10.000305mA	12.000366mA	0x8001
Mid-Scale	12mA	10mA	12mA	0x8000
Mid-Scale – 1 LSB	11.999756mA	9.999695mA	11.999634mA	0x7FFF
Zero-Scale + 1 LSB	4.000244mA	305.176nA	366.211nA	0x0001
Zero-Scale	4mA	0A	0A	0x0000

Table 7-3 : DAC Data Coding - Current Output Range

8 DAC Data Correction

The basic formula for correcting the DAC value with the corresponding correction values stored in the Correction Data Space is:

$$Data_{Corrected} = Data * \left(1 - \frac{Gain_{Corr}}{262144}\right) - \frac{Offset_{Corr}}{4}$$

Data is the digital DAC value that would be used with an ideal DAC.

Data_Corrected is the corrected digital DAC value that has to be used with the real DAC.

Gain_corr and Offset_corr are the DAC correction values from the Correction Data Space. They are stored separately for each D/A channel and output range.

The correction values are stored as two's complement 16 bit wide values in the range from –32768 to +32767. For higher accuracy they are scaled to ¼ LSB. No correction is performed for Gain_Corr = 0 and Offset_Corr = 0.

For effective D/A channel data correction performed by the TPMC542 firmware, the software must read the offset and gain correction values for the desired D/A channel and output range from the Correction Data Space and write the values to the corresponding *DAC Channel Correction Registers* (see Register Map).

Alternatively, software may modify the data values (according to the given formula) while keeping the *DAC Channel Correction Registers* clear (thus disabling any additional DAC value correction by the TPMC542 firmware).

Also see the ***DAC Correction Registers*** and ***Correction Data Space*** sections.

9 D/A Operating Modes

9.1 D/A Operating Modes Overview

9.1.1 DAC Operating Modes

The DAC operating mode is configurable per DAC device (i.e. for groups of four D/A channels, not for a single D/A channel) in the corresponding *DAC Mode Register*.

The TPMC542 provides the following operating modes for each DAC device.

- Manual Mode
    - Immediate Conversion Mode (Default)

      Manual Immediate Conversion Mode is used for generating simple single conversions. This is the default mode after power-up or reset.
    - Controlled Conversion Mode

      Manual Controlled Conversion Mode is used for generating simple simultaneous conversions.
- Sequencer Mode
    - Sequencer Mode is used for periodic equidistant simultaneous D/A conversions.

9.1.2 Sequencer Operating Modes

The sequencer operating mode is configured in the *Sequencer Control Register* and applies to all DAC devices assigned to the sequencer (i.e. to all DAC devices configured for Sequencer Mode).

The TPMC542 provides the following operating modes for the D/A sequencer.

- Sequencer Normal Mode (Default)

  Sequencer Normal Mode is used for generating a configurable number of equidistant simultaneous conversions upon software request.
- Sequencer Frame Mode

  Sequencer Frame Mode is used for generating a configurable number of equidistant simultaneous conversions (conversion frames) upon a frame trigger signal event. The frame trigger signal interval is programmable when using the internal frame trigger signal generator. Sequencer Frame Mode supports multi-board synchronization.

The various D/A operating modes are described in the following chapters.

9.2 D/A Manual Mode

The TPMC542 provides two different modes for performing manual D/A conversions (i.e. without any conversion clock rate).

The manual mode is configured in the *DAC Mode Register(s)*. Manual Immediate Conversion Mode is the default mode after power-up or reset.

9.2.1 Immediate Conversion Mode

In Immediate Conversion Mode, a DAC device convert pulse (LDAC#) is generated automatically after loading data to the DAC device. Writing to a *DAC Data Register* logs an internal request for transferring the conversion data to the DAC device as soon as possible. The DAC convert pulse is generated when all pending data has been loaded to the DAC device. The *DAC Busy* bit in the *Global DAC Status Register* may be used as an indication that the data transfer is done and the analog output update is being performed.

Immediate Conversion Mode is the most simple conversion mode. However, Immediate Conversion Mode is not suitable for simultaneous analog output updates.

Example Loop:

1. Write *DAC Data Register(s)*

   Write data for all DAC devices or for individual DAC devices configured for Manual Mode.
   For a DAC device, either write data for all four DAC channels or for individual DAC channels.

2. Wait until *DAC Busy* Status is Clear

   Keep reading the *Global DAC Status Register* until the corresponding *DAC Busy* bit(s) is (are) clear, indicating that the conversion data has been loaded to the DAC device(s) and that the conversion(s) is (are) just being performed or already has (have) been performed.

   Note: Also see chapter *Programming Hints / Global DAC Status Register Read*!

9.2.2 Controlled Conversion Mode

In Controlled Conversion Mode, data is transferred to the DAC devices by writing the *DAC Data Registers*. However, the analog outputs are not updated automatically after the data transfer(s) as in the Immediate Conversion Mode. The analog outputs are updated by issuing a DAC Convert Request by software.

Controlled Conversion Mode supports simultaneous analog output updates for multiple D/A channels.

Example Loop:

1. Write *DAC Data Register(s)*

   Write data for all DAC devices or for individual DAC devices configured for Manual Mode.
   For a DAC device, either write data for all four DAC channels or for individual DAC channels.

2. Wait until *DAC Busy* Status is Clear

   Keep reading the *Global DAC Status Register* until the corresponding *DAC Busy* bits are clear, indicating that the conversion data has been loaded to the DAC device(s).

   Note: Also see chapter *Programming Hints / Global DAC Status Register Read*!

3. Set *DAC Convert Request*

   Write the *Global DAC Control Register* and set the corresponding *DAC Convert Request* bit(s).
   The D/A conversion(s) is (are) performed immediately.

9.3 D/A Sequencer Mode

9.3.1 Sequencer Overview

The D/A sequencer is used for periodic simultaneous D/A conversions at a configurable conversion rate.

Each DAC device may be configured to operate in Sequencer Mode via the *DAC Mode Register(s)*.

All D/A output channels of all DAC devices assigned to the D/A sequencer are always operating in simultaneous conversion mode.

The D/A sequencer unit basically consists of:

- a DMA controller (for fetching the D/A conversion data from host memory)
- a FIFO (for buffering the D/A conversion data)
- a Data Output Unit (for transferring the D/A conversion data to the DAC devices)
- a DAC Convert Pulse Generator (for generating DAC convert pulses from a conversion clock signal)

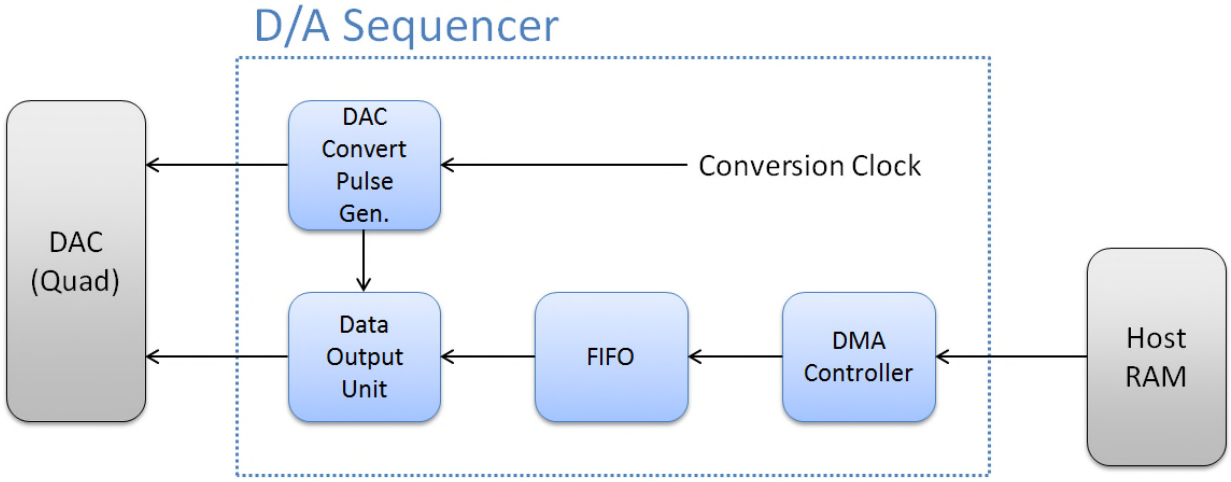


Figure 9-1 : D/A Sequencer Unit

The D/A conversion data (for all D/A channels of all DAC devices assigned to the D/A sequencer) is prepared in host memory data buffers.

The DMA Controller fetches the D/A conversion data from host memory by PCI Master DMA transfer upon SW request and stores the data in a FIFO buffer.

The Data Output Unit pre-loads the DAC devices with data for the first conversion, and (after a conversion) updates the DAC devices with data for the next conversion (when conversion data is available in the FIFO buffer)

The DAC Convert Pulse Generator generates the appropriate number of DAC convert pulses out of a configurable conversion clock signal.

9.3.2 Host Memory Data Buffers

Data buffers in host memory are used to pass/provide the D/A conversion data for the DAC devices operating in sequencer mode.

The D/A conversion data buffers must be mapped in 32 bit PCI Memory Space and must be accessible from the PCI bus.

The structure of a D/A conversion data buffer is a gapless list of D/A conversion data sets for the D/A sequencer.

A single D/A conversion data set consists of the conversion data for a single conversion event for all D/A channels (A-D) of all DAC devices (1-4) actually assigned to the sequencer, in ascending order.

Hence, the number of 16 Bit D/A words per D/A conversion data set is:
Number_of_DACs_assigned_to_the_Sequencer x 4 (DAC_Device_Channels)

Host Memory Data Buffer Example

For this example, DAC 2 and DAC 4 are configured to operate in Sequencer Mode while DAC 1 and DAC 3 are not configured for Sequencer Mode.

Conversion Data Set #	Memory Address	Data
1	Data Buffer Base Address	16 Bit Data for DAC 2 Channel A
	+2	16 Bit Data for DAC 2 Channel B
	+2	16 Bit Data for DAC 2 Channel C
	+2	16 Bit Data for DAC 2 Channel D
	+2	16 Bit Data for DAC 4 Channel A
	+2	16 Bit Data for DAC 4 Channel B
	+2	16 Bit Data for DAC 4 Channel C
	+2	16 Bit Data for DAC 4 Channel D
2	+2	16 Bit Data for DAC 2 Channel A
	+2	16 Bit Data for DAC 2 Channel B
	+2	16 Bit Data for DAC 2 Channel C
	+2	16 Bit Data for DAC 2 Channel D
	+2	16 Bit Data for DAC 4 Channel A
	+2	16 Bit Data for DAC 4 Channel B
	+2	16 Bit Data for DAC 4 Channel C
	+2	16 Bit Data for DAC 4 Channel D
3	+2	16 Bit Data for DAC 2 Channel A
	+2	…

Table 9-1 : Host Memory Data Buffer Example

9.3.3 Sequencer DMA Operation

The conversion data for the DAC devices assigned to the D/A sequencer is fetched from data buffers in host memory by the sequencer's DMA controller via PCI Master read access upon software request. The DMA read data is buffered in the on-board Sequencer FIFO. One data buffer is handled at a time.

There are two main PMC target registers for D/A sequencer DMA access control:

- *DMA Buffer Base Address Register*
- *DMA Buffer Length Register*

The (PCI Memory mapped) base address of the data buffer must be written to the *DMA Buffer Base Address Register*.

The DMA read transfer for the data buffer is started by writing to the *DMA Buffer Length Register* while the DMA Engine is in Idle state as indicated in the *Sequencer Status Register*. The same write access also sets the data amount provided by the data buffer (i.e. the number of data bytes to be fetched).

The current data buffer is reported as *Done* in the *Sequencer Status Register* when all data has been fetched from the data buffer.

For providing more conversion data, the software must prepare a next data buffer in host memory, write the base address of the new data buffer to the *DMA Buffer Base Address Register* and write the number of data bytes to the *DMA Buffer Length Register*, while the DMA Engine is in Idle state.

The base address of a next data buffer may be written immediately after starting the DMA process for the current data buffer. The *DMA Buffer Length Register* must only be written if the current/previous data buffer has been reported as *Done* and the DMA Engine is in Idle state again as indicated in the *Sequencer Status Register*.

9.3.4 Sequencer Conversion Control Signals

The D/A sequencer operates with an internal conversion clock signal, determining the D/A conversion rate for all DAC devices assigned to the sequencer. The D/A sequencer may operate with either the internal Conversion Clock Signal 1 or with the internal Conversion Clock Signal 2.

In Sequencer Frame Mode, the sequencer additionally operates with the internal frame trigger signal. In Sequencer Frame Mode, a frame trigger signal event starts a configurable number of equidistant simultaneous D/A conversions.

Both the sequencer's conversion clock signal selection and the sequencer operating mode are configured in the *Sequencer Control Register*.

See the ***Conversion Control Signals*** chapter for more information on the conversion control signals.

Note that in Sequencer Frame Mode, the selected Conversion Clock Signal source must be phase locked to the selected Frame Trigger Signal source.

9.3.5 Sequencer Operating Modes

The sequencer operating mode is configured in the *Sequencer Control Register*.

Available sequencer operating modes are:

- Sequencer Normal Mode
- Sequencer Frame Mode

Sequencer Normal Mode is used for generating a configurable number of equidistant simultaneous D/A conversions at a configurable conversion rate upon software request.

Sequencer Frame Mode is used for generating a configurable number of equidistant simultaneous D/A conversions at a configurable conversion rate upon a frame trigger signal event. Since the internal frame trigger signal generator provides a configurable frame trigger interval, the Sequencer Frame Mode supports generating frames of equidistant simultaneous D/A conversions at a configurable frame interval rate. Sequencer Frame Mode also supports Multi-Board synchronization.

Basically, the two sequencer modes only differ in the way a conversion process (a configurable number of equidistant simultaneous conversions) is started. In Sequencer Normal Mode the conversion process is started by software while in Sequencer Frame Mode the conversion process is started upon a frame trigger signal event.

The sequencer operating modes are described in the following chapters.

9.3.6 Sequencer Normal Mode

9.3.6.1 Sequencer Normal Mode Description

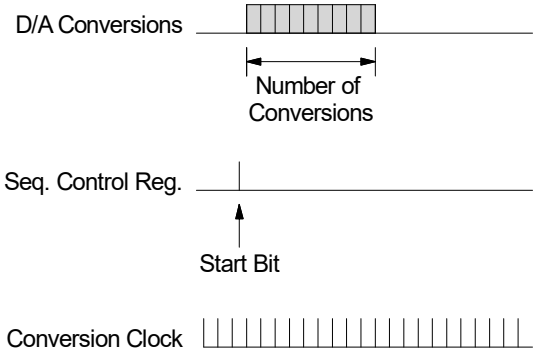


Figure 9-2 : Sequencer Normal Mode Diagram

In Sequencer Normal Mode, the sequencer operates with an internal conversion clock signal for generating the convert pulses for the DAC devices, thus defining the actual conversion rate for the simultaneous DAC output updates.

The software configures the desired number of conversions (*Number of Conversions Register*) for the next block of D/A conversions. Setting the number of conversions to 0 selects continuous conversion mode.

The conversion data is fetched via DMA read access and accumulates in the sequencer FIFO. The FIFO fill level is readable.

When data is/becomes available in the sequencer FIFO while the Sequencer Output Unit is enabled in the *Sequencer Control Register*, the sequencer DAC devices are automatically pre-loaded for the first conversion. The Sequencer DAC Pre-Load status is readable in the *Sequencer Status Register*.

No DAC convert pulses are generated until the software starts the conversion process.

The conversion process is started by setting the corresponding Start Bit in the *Sequencer Control Register*. When the Start Bit is set, starting with the next sequencer conversion clock event (after synchronization), the configured number of convert pulses is generated for the sequencer DAC devices at the sequencer's conversion clock rate. The active conversion phase is indicated by a corresponding bit in the *Sequencer Status Register*.

After each single DAC convert pulse event, the data set for the next conversion is transferred to the sequencer DAC devices when conversion data is/becomes available in the sequencer FIFO.

When the configured number of conversions has been performed, the corresponding bit in the *Sequencer Status Register* is cleared and no further convert pulses are generated for the sequencer DAC devices.

When data is/becomes available in the sequencer FIFO, the sequencer DAC devices are pre-loaded again for the next conversion block.

For a next block of data conversions, the software must re-trigger the conversion process by re-setting the corresponding Start Bit in the *Sequencer Control Register*.

The following error condition is monitored:

- A next convert pulse is due, but not all sequencer DAC devices are in a proper pre-loaded state or the convert pulse would violate the timing specification of at least one sequencer DAC device.

In an error case, the conversion process is stopped and the appropriate error flags are set in the *Sequencer Status Register*.

9.3.6.2 Sequencer Normal Mode Example

For the following example, only DAC 1 and DAC 3 are operating in Sequencer Normal Mode.

The example performs four simultaneous conversions at a 10 kHz conversion rate.

Participating D/A Channels in ascending order are: DAC 1 Channels A-D, DAC 3 Channels A-D

Number of Bytes per Conversion Data Set = 2 (DACs) x 4 (Channels per DAC) x 2 (Bytes per Data Word) = 16 Byte.

Total number of data bytes = 4 (Conversions) x 16 (Number of Bytes per Conversion Data Set) = 64 Byte.

Conversion data plan:

	D/A Channels							
Conv.	**DA_1A**	**DA_1B**	**DA_1C**	**DA_1D**	**DA_3A**	**DA_3B**	**DA_3C**	**DA_3D**
1st	0x011A	0x011B	0x011C	0x011D	0x013A	0x013B	0x013C	0x013D
2nd	0x021A	0x021B	0x021C	0x021D	0x023A	0x023B	0x023C	0x023D
3rd	0x031A	0x031B	0x031C	0x031D	0x033A	0x033B	0x033C	0x033D
4th	0x041A	0x041B	0x041C	0x041D	0x043A	0x043B	0x043C	0x043D

Table 9-2 : Simple Normal Mode Example: Conversion Data Plan

Prepare Conversion Data in Host Memory **(Little Endian Example)**:

Conversion Data Set	Memory Byte Address	D/A Channel	Data	Notes
1st	DMA Buffer Base Address	DA_1A	0x1A	LSB
	+1		0x01	MSB
	+1	DA_1B	0x1B	LSB
	+1		0x01	MSB
	+1	DA_1C	0x1C	LSB
	+1		0x01	MSB
	+1	DA_1D	0x1D	LSB
	+1		0x01	MSB
	+1	DA_3A	0x3A	LSB
	+1		0x01	MSB
	+1	DA_3B	0x3B	LSB
	+1		0x01	MSB
	+1	DA_3C	0x3C	LSB
	+1		0x01	MSB
	+1	DA_3D	0x3D	LSB
	+1		0x01	MSB
2nd	+1	DA_1A	0x1A	
	+1		0x02	
	+1	DA_1B	0x1B	
	+1		0x02	
	+1	DA_1C	0x1C	
	+1		0x02	
	+1	DA_1D	0x1D	

	+1		0x02	
	+1	DA_3A	0x3A	
	+1		0x02	
	+1	DA_3B	0x3B	
	+1		0x02	
	+1	DA_3C	0x3C	
	+1		0x02	
	+1	DA_3D	0x3D	
	+1		0x02	
3rd	+1	DA_1A	0x1A	
	+1		0x03	
	+1	DA_1B	0x1B	
	+1		0x03	
	+1	DA_1C	0x1C	
	+1		0x03	
	+1	DA_1D	0x1D	
	+1		0x03	
	+1	DA_3A	0x3A	
	+1		0x03	
	+1	DA_3B	0x3B	
	+1		0x03	
	+1	DA_3C	0x3C	
	+1		0x03	
	+1	DA_3D	0x3D	
	+1		0x03	
4th	+1	DA_1A	0x1A	
	+1		0x04	
	+1	DA_1B	0x1B	
	+1		0x04	
	+1	DA_1C	0x1C	
	+1		0x04	
	+1	DA_1D	0x1D	
	+1		0x04	
	+1	DA_3A	0x3A	
	+1		0x04	
	+1	DA_3B	0x3B	
	+1		0x04	
	+1	DA_3C	0x3C	
	+1		0x04	
	+1	DA_3D	0x3D	
	+1		0x04	

Table 9-3 : Simple Normal Mode Example: Data in Host Memory

The example assumes, that the DAC devices have already been properly configured (Power-Up, Output Range, Output Enable) after power-up or reset.

Conversion Clock Configuration

Step	Data	Register	Notes
Write	0x000007CF	*Conversion Clock 1 Register* (0x320)	Generate 10kHz out of 20MHz (Divider = 1999)
Write	0x00000001	*Conversion Signal Generator Enable Register* (0x33C)	Enable Clock 1 Generator

Conversion Data Fetch

Step	Data	Register	Notes
Read		*FIFO Level Register* (0x2FC)	Show FIFO is empty
Write	0x00010000	*Sequencer Control Register* (0x2E8)	Enable DMA Engine
Read		*Sequencer Status Register* (0x2EC)	Check that the DMA Engine Status is Idle
Write	DMA Buffer Base Address	*DMA Buffer Base Address Register* (0x308)	Set DMA Buffer Base Address
Write	0x00000040	*DMA Buffer Length Register* (0x30C)	Set DMA Buffer Length (64 Byte) and start DMA Transfer
Read		*Sequencer Status Register* (0x2EC)	Keep on reading until the DMA Buffer status is Done and the DMA Engine is Idle again
Read		*FIFO Level Register* (0x2FC)	FIFO Level indicates 64 Byte

Sequencer Configuration

Step	Data	Register	Notes
Write	0x00000001	*DAC 1 Mode Register* (0x18C)	Set DAC 1 to Sequencer Mode
Write	0x00000001	*DAC 3 Mode Register* (0x1EC)	Set DAC 3 to Sequencer Mode
Write	0x00000004	*Number of Conversions Register* (0x2F4)	Set Number of Conversions to perform

DAC Pre-Loading

Step	Data	Register	Notes
Write	0x00010001	*Sequencer Control Register* (0x2E8)	Enable Sequencer Output Unit
Read		*Sequencer Status Register* (0x2EC)	Keep on reading until the DACs are Preloaded for the first Conversion
Read		*FIFO Level Register* (0x2FC)	FIFO Level indicates 64 – 16 = 48 Byte now

Conversion Process

Step	Data	Register	Notes
Write	0x00010009	*Sequencer Control Register* (0x2E8)	Start the Conversion Process
Read		*Sequencer Status Register* (0x2EC)	Keep on reading until the conversion process is no longer active
Read		*Conversion Count Register* (0x2F8)	Conversion Count shows 4 Conversions
Read		*FIFO Level Register* (0x2FC)	FIFO Level is 0

Additional Notes

- When data is or becomes available in the FIFO while the Sequencer Output Unit is in Idle state, the Sequencer Output Unit leaves the Idle state and starts preloading the sequencer DAC devices with data for the next conversion. If all DACs assigned to the sequencer are finally preloaded, the Sequencer Output unit enters the Pre-Loaded state (see *Sequencer Status Register*).
- Before starting a conversion sequence (*Sequencer Control Register*), the sequencer DAC devices must be in a Pre-Loaded state (as indicated in the *Sequencer Status Register*).
- If a conversion sequence is done (i.e. the configured number of conversions have been performed), the Sequencer Output Unit enters the Idle state again (except in an error case).

9.3.6.3 Sequencer Normal Mode Start Synchronization

In Sequencer Normal Mode, the *Sequencer Output Unit Start Conversion bit* in the *Sequencer Control Register* is internally synchronized to the (free running) sequencer conversion clock signal.

The *Sequencer Output Unit Start Conversion bit* in the *Sequencer Control Register* may be set while the sequencer configuration clock is already running or before the sequencer conversion clock becomes active (provided that the sequencer configuration clock provides a stable level while being inactive).

The first falling sequencer conversion clock edge after the first rising sequencer conversion clock edge after the *Sequencer Output Unit Start Conversion bit* is set in the *Sequencer Control Register* triggers the first conversion event.

The total number of conversion events performed per start bit event is configured in the *Number Of Conversions Register*.

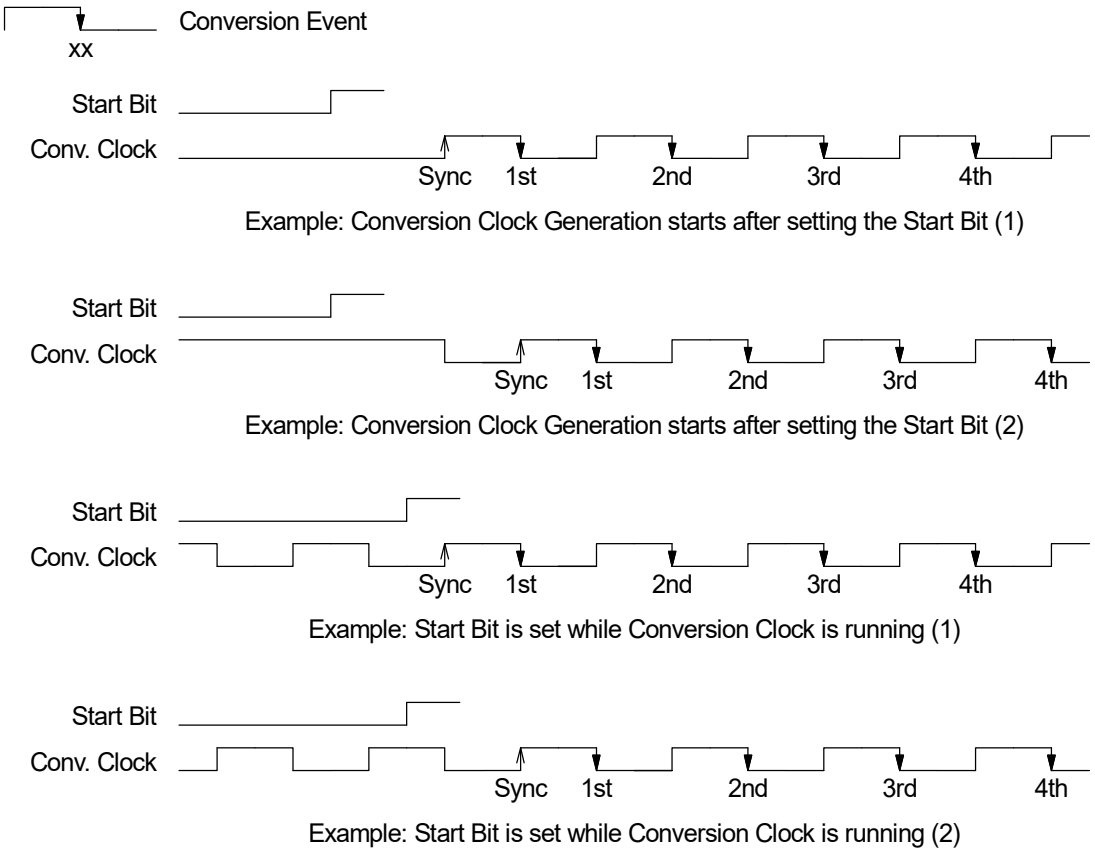


Figure 9-3 : Sequencer Normal Mode Start Synchronization

9.3.7 Sequencer Frame Mode

9.3.7.1 Sequencer Frame Mode Description

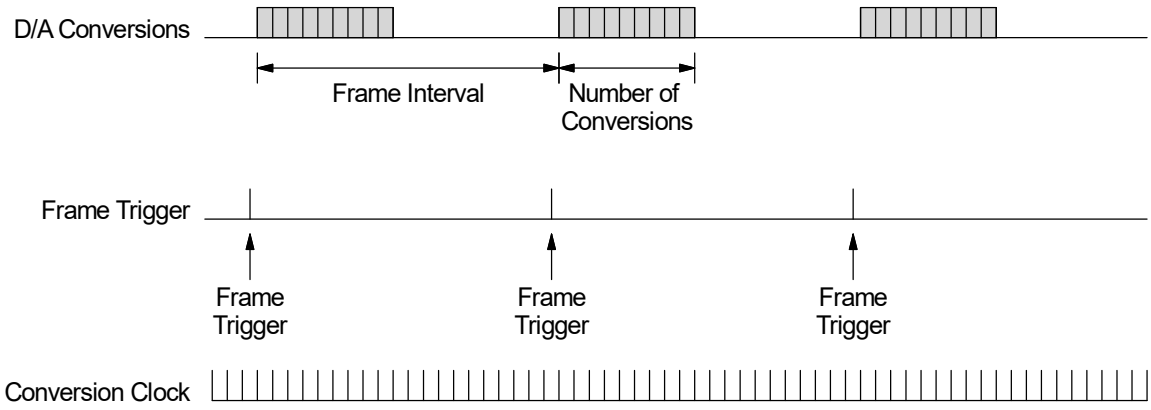


Figure 9-4 : Sequencer Frame Mode Diagram

In Sequencer Frame Mode, the sequencer operates with an internal conversion clock signal for generating the convert pulses for the DAC devices, thus defining the actual conversion rate for the simultaneous DAC output updates.

Additionally in Sequencer Frame Mode, the sequencer operates with the internal frame trigger signal for starting a configurable number of periodic equidistant simultaneous D/A conversions (a conversion frame).

Note that in sequencer frame mode, the selected conversion clock source must be phase locked to the selected frame trigger signal source.

The software configures the desired number of conversions per frame (*Number of Conversions Register*), the conversion clock rate (*Conversion Clock Generator Registers*), the frame interval (*Frame Trigger Generator Register 1*) and the number of frames (*Frame Trigger Generator Register 2*). For seamless conversion frames, the number of conversions per frame must match for the configured frame interval and conversion clock rate.

The conversion data is fetched via DMA read access and accumulates in the sequencer FIFO. The FIFO fill level is readable.

When data is/becomes available in the sequencer FIFO while the Sequencer Output Unit is enabled in the *Sequencer Control Register*, the sequencer DAC devices are automatically pre-loaded for the first conversion. The Sequencer DAC Pre-Load status is readable in the *Sequencer Status Register*.

Starting with the first conversion clock event after the first/next frame trigger signal event, the configured number of convert pulses is generated for the sequencer DAC devices at the sequencer's conversion clock rate. The active conversion frame phase is indicated by a corresponding bit in the *Sequencer Status Register*.

After each single DAC convert pulse event, the data set for the next conversion is transferred to the sequencer DAC devices when conversion data is/becomes available in the sequencer FIFO.

When the configured number of conversions per frame has been performed, the corresponding bit in the *Sequencer Status Register* is cleared and no further convert pulses are generated for the sequencer DAC devices until the next frame trigger signal event.

When data is/becomes available in the sequencer FIFO, the sequencer DAC devices are pre-loaded again for the first conversion of the next frame and the next frame trigger signal event triggers the next conversion process.

The following error conditions are monitored:

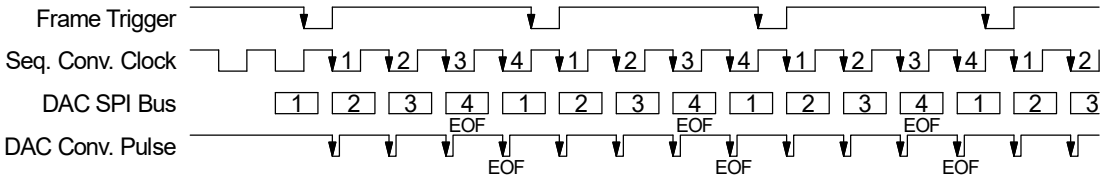
- A next convert pulse is due, but not all sequencer DAC devices are in a proper pre-loaded state or the convert pulse would violate the timing specification of at least one sequencer DAC device.
- A next frame trigger event occurs, but the configured number of conversions (per frame) has not been performed so far.

In an error case the conversion process is stopped and the appropriate error flags are set in the *Sequencer Status Register*.

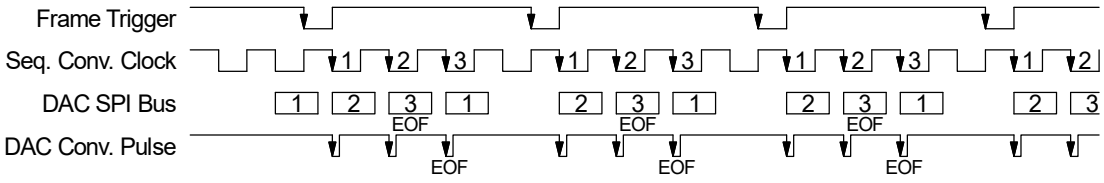
9.3.7.2 Sequencer Frame Mode Example Diagrams (D/A)

For the following diagrams, continuous frame trigger signal generation is assumed.

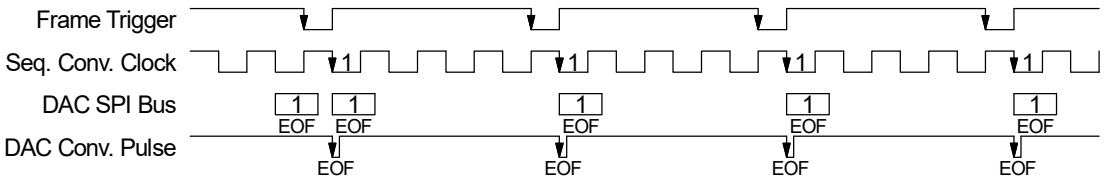
1 Conversion Clock Event
1 Conversion Data Set (for a single Conversion Event)
EOF End Of Frame (Conversion Data Set, Conversion Pulse)



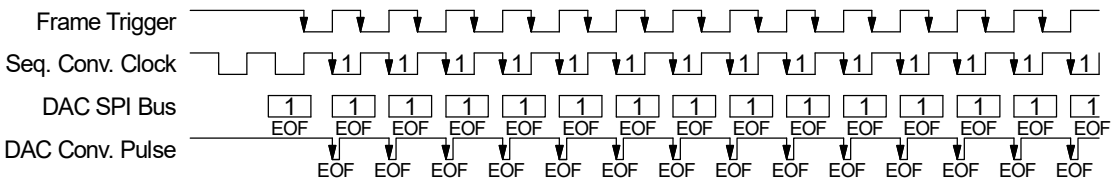
Example: Frame Interval = 4 Conversion Clocks, Conversions per Frame = 4



Example: Frame Interval = 4 Conversion Clocks, Conversions per Frame = 3



Example: Frame Interval = 4 Conversion Clocks, Conversions per Frame = 1



Example: Frame Interval = 1 Conversion Clock, Conversions per Frame = 1

Figure 9-5 : Frame Mode Example Diagrams (D/A)

9.3.7.3 Sequencer Frame Mode Notes

- In Sequencer Frame Mode, the sequencer additionally operates with a frame trigger signal that must be phase locked to the sequencer's conversion clock signal.
- All sequencers in Frame Mode must use the same frame trigger signal source and thus are operating with the same frame interval and the same number of frame trigger pulses
- The number of conversion events per frame is configurable but is the same for all frames
- In a Multi-Board scenario, the number of conversions per frame must be configured (register value) on all associated PMC cards
- (If sourced externally) The frame trigger signal must meet certain timing requirements

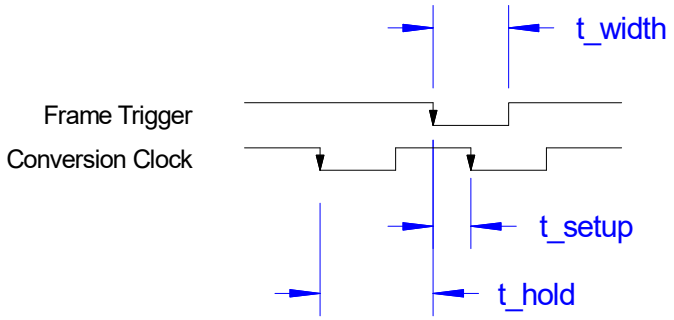


Figure 9-6 : Frame Trigger Timing Requirements

Timing Parameter	Description	Min	Max
t_width	Pulse Width	500ns	½ T_{CONV_CLK}
t_hold	Conversion Clock Event to next Frame Trigger Event	½ T_{CONV_CLK} - 250ns	-
t_setup	Frame Trigger Event to next Conversion Clock Event	250ns	-

Table 9-4 : Frame Trigger Timing Parameter

- In Sequencer Frame Mode, the first falling conversion clock edge after the frame trigger event triggers the first conversion event for the frame.

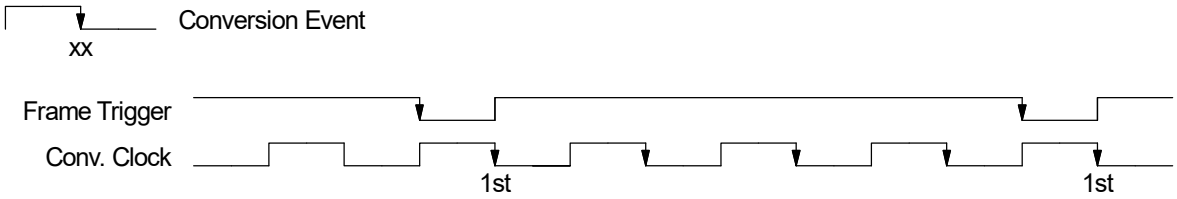


Figure 9-7 : Sequencer Frame Mode 1st Conversion Event

- The sequencer conversion clock may run continuously. The total number of conversions per frame is configured in the *Number Of Conversions Register*.

10 Conversion Control Signals

10.1 Internal Conversion Control Signals

The internal conversion control signals are used for controlling the D/A conversions in sequencer operation.

There are three internal conversion control signals:

- Conversion Clock 1
- Conversion Clock 2
- Frame Trigger

A conversion clock signal determines the conversion rate for the simultaneous D/A conversions performed in Sequencer Mode.

The frame trigger signal is only used in Sequencer Frame Mode. In Sequencer Frame Mode a frame trigger signal event starts a frame of equidistant simultaneous D/A conversions.

For each of the internal conversion control signals (Conversion Clock 1, Conversion Clock 2, Frame Trigger), the actual signal source is configurable in the *Conversion Signal Source Selection Register*.

The following signal source options are provided for each internal conversion control signal:

- Internal signal generator
- Input signal from the I/O interface

Typically, the signal source configuration for the internal frame trigger signal and the associated internal conversion clock signal is the same when using Sequencer Frame Mode.

Conversion Clock 1 ← Conversion Clock 1 Signal Generator | Conversion Clock 1 I/O Pin

Conversion Clock 2 ← Conversion Clock 1 Signal Generator | Conversion Clock 2 I/O Pin

Frame Trigger Signal ← Frame Trigger Generator Signal | Frame Trigger I/O Signal

10.2 Internal Signal Generators

There is a dedicated internal signal generator as a signal source option for each of the internal conversion control signals, thus the PMC provides the following internal signal generators:

- Conversion Clock 1 Signal Generator
- Conversion Clock 2 Signal Generator
- Frame Trigger Signal Generator

10.2.1 Conversion Clock Signal Generators

Conversion clock signal generation is configured in the *Conversion Clock 1* and *Conversion Clock 2 Generator Registers* and is enabled in the *Conversion Signal Generator Enable Register*.

Each conversion clock signal generator provides an on-board clock source selection and a configurable divider.

If enabled, the conversion clock signals are generated continuously with a 50% duty cycle and the configured rate.

A conversion clock generator output signal may be:

- selected as the source for the corresponding internal conversion clock signal (*Conversion Signal Source Selection Register*)
- driven out on a dedicated I/O pin (*Conversion Signal Generator Output Driver Register*)
- selected as the associated conversion clock generator signal for the Frame Trigger Signal Generator (*Frame Trigger Generator Register 1*)

10.2.2 Frame Trigger Signal Generator

Frame Trigger signal generation is configured in the *Frame Trigger Generator Registers 1 and 2* and is enabled in the *Conversion Signal Generator Enable Register*.

The frame trigger signal is always generated for one of the internal conversion clock generator signals, hence the frame trigger signal can be generated for either the conversion clock 1 generator signal or for the conversion clock 2 generator signal. Frame trigger signal generation requires that the associated conversion clock generator is also enabled.

The frame trigger signal is generated as a single active low pulse of the associated conversion clock generator signal (see figure below).

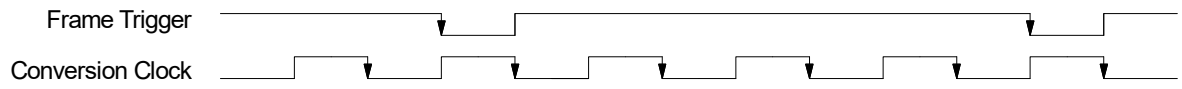


Figure 10-1 : Frame Trigger Signal Gen. Example (Frame Trigger Interval = 4)

The frame trigger interval is programmable in number of cycles of the associated conversion clock generator signal (*Frame Trigger Generator Register 1*). Frame trigger pulses may be generated continuously or in a configurable number (*Frame Trigger Generator Register 2*).

The frame trigger generator output signal may be:

- selected as the source of the internal frame trigger signal (*Conversion Signal Source Selection Register*)
- driven out on a dedicated I/O pin (*Conversion Signal Generator Output Driver Register*)

10.3 I/O Signals

The PMC features the following bi-directional PMC I/O pins carrying conversion control signals.

- Conversion Clock 1 I/O Pin
- Conversion Clock 2 I/O Pin
- Frame Trigger I/O Pin

Each of these I/O signals features a dedicated I/O line driver and a dedicated I/O line receiver (both connected to the same I/O pin). When enabled, the driver level is 3.3V LVTTL (TTL compatible). The receivers are accepting LVTTL and/or TTL levels and are always enabled.

Output Function

Each of the following internal signal generator output signals may be driven out on the corresponding PMC I/O pin (see *Conversion Signal Generator Output Driver Register*).

- Conversion Clock Generator 1 Signal → Conversion Clock 1 I/O Pin
- Conversion Clock Generator 2 Signal → Conversion Clock 2 I/O Pin
- Frame Trigger Generator Signal → Frame Trigger I/O Pin

Input Function

Each of the mentioned conversion control signal PMC I/O pins may be selected as being the source of the corresponding internal conversion control signal (see *Conversion Signal Source Selection Register*).

- Conversion Clock 1 Signal ← Conversion Clock 1 I/O Pin
- Conversion Clock 2 Signal ← Conversion Clock 2 I/O Pin
- Frame Trigger Signal ← Frame Trigger I/O Pin

Note that the input function is always available, even when the output function is active.

10.4 Conversion Control Signal Block Diagram

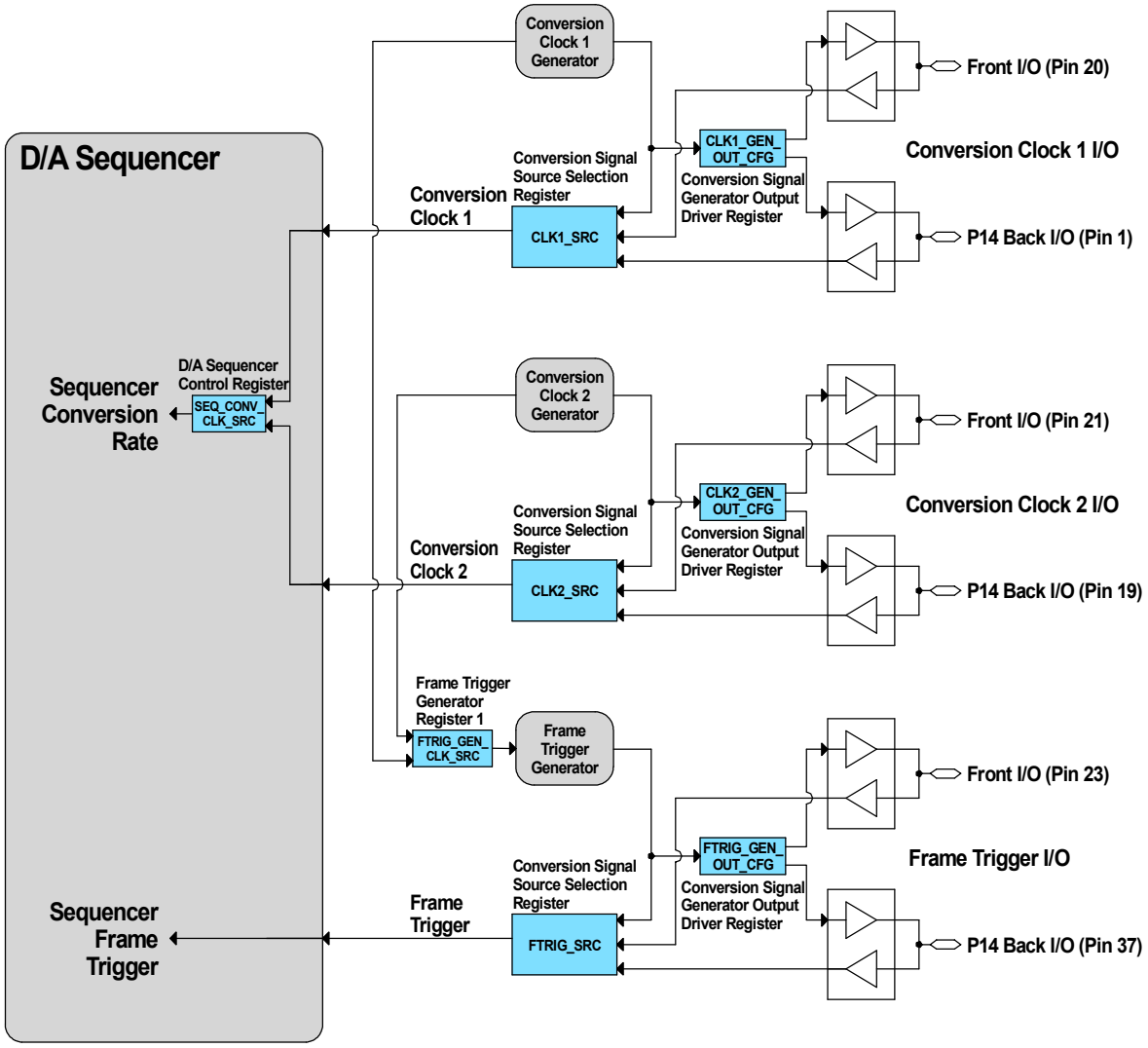


Figure 10-2 : Conversion Control Signal Block Diagram

Note that the TPMC542 provides one D/A sequencer.

10.5 Multi-Board Synchronization

The Sequencer Frame Mode supports Multi-Board synchronization.

In a Multi-Board application, one PMC is operating as the multi-board master card while the other cards are operating as multi-board target cards.

The multi-board master card generates the frame trigger and conversion clock signal to be used by all cards of the multi-board application and drives these signals out on the corresponding I/O pins.

The multi-board master's frame trigger and conversion clock I/O signals must be connected to the frame trigger and conversion clock I/O signals of all target cards in the multi-board application.

All cards associated with the multi-board application (including the master card) are using the corresponding I/O pin input signal as the signal source for both the internal frame trigger signal and the internal conversion clock signal.

All card's sequencer's operating in frame mode are waiting for a frame trigger signal event for starting the sequencer conversion process.

The frame trigger signal is generated on the master card (aligned to the associated conversion clock signal) and is distributed (along with the associated conversion clock signal) to all associated cards via the I/O interface. The software may check the DAC pre-load status and FIFO level on all associated cards before starting the frame trigger signal generation by enabling the signal generators on the master card.

The appropriate conversion signal path (*Conversion Signal Generator Output Driver Register* and *Conversion Signal Source Selection Register*) must be configured on all cards in the multi-board application.

The following table shows typical Conversion Signal Path configuration examples.

PMC Configuration Example	Internal Signal Generator Enabled	Conversion Signal Generator Output Driver Configuration	Conversion Signal Source Selection
Single Card Standalone	Yes	Output Driver Disabled	Internal Signal Generator
Single Card with External Signal Generators	No	Output Driver Disabled	I/O Input
Multi-Board Master Card	Yes	Output Driver Enabled	I/O Input
Multi-Board Target Card	No	Output Driver Disabled	I/O Input

Table 10-1 : Conversion Signal Path Configuration Examples

11 I/O Pin Assignment

11.1 Front I/O Connector

Pin-Count	68
Connector Type	Mini D Ribbon (MDR) Receptacle Connector
Source & Order Info	3M N10268-52E2PC or compatible

Table 11-1 : Front I/O Connector Type

Signal Group	Direction	Level
DAC x Channel x	Out	Voltage Mode max. ±12V Current Mode max. 24mA
Digital I/O x	In/Out	3.3V LVTTL Driver with Pull Resistor Reference Open, 5V, 3.3V or GND Input LVTTL/TTL (up to 5V)

Table 11-2 : Front I/O Signal Types

Note that the following Front I/O Signals are only provided on the TPMC542-10R order option (and not on the TPMC542-20R order option):

DAC 3 Channel A … D, DAC 4 Channel A … D

Note that typically, the following pin pairs are building a twisted pair inside the Front I/O cable:

Pins 1 & 35, Pins 2 & 36, …, Pins 34 & 68.

Signal	Pin		Pin	Signal
DAC 1 Channel D	1		35	Ground
DAC 1 Channel C	2		36	Ground
DAC 1 Channel B	3		37	Ground
DAC 1 Channel A	4		38	Ground
DAC 2 Channel D	5		39	Ground
DAC 2 Channel C	6		40	Ground
DAC 2 Channel B	7		41	Ground
DAC 2 Channel A	8		42	Ground
DAC 3 Channel D	9		43	Ground
DAC 3 Channel C	10		44	Ground
DAC 3 Channel B	11		45	Ground
DAC 3 Channel A	12		46	Ground
DAC 4 Channel D	13		47	Ground
DAC 4 Channel C	14		48	Ground
DAC 4 Channel B	15		49	Ground
DAC 4 Channel A	16		50	Ground
NC	17		51	NC
NC	18		52	NC
Ground	19		53	Ground
Digital I/O 1 (Conv. Clock 1)	20		54	Digital I/O 2
Digital I/O 3 (Conv. Clock 2)	21		55	Digital I/O 4
Ground	22		56	Ground
Digital I/O 5 (Frame Trigger)	23		57	Digital I/O 6
Digital I/O 7	24		58	Digital I/O 8
Ground	25		59	Ground
Digital I/O 9	26		60	Digital I/O 10
Digital I/O 11	27		61	Digital I/O 12
Ground	28		62	Ground
Digital I/O 13	29		63	Digital I/O 14
Digital I/O 15	30		64	Digital I/O 16
Ground	31		65	Ground
Digital I/O 17	32		66	Digital I/O 18
Digital I/O 19	33		67	Digital I/O 20
Ground	34		68	Ground

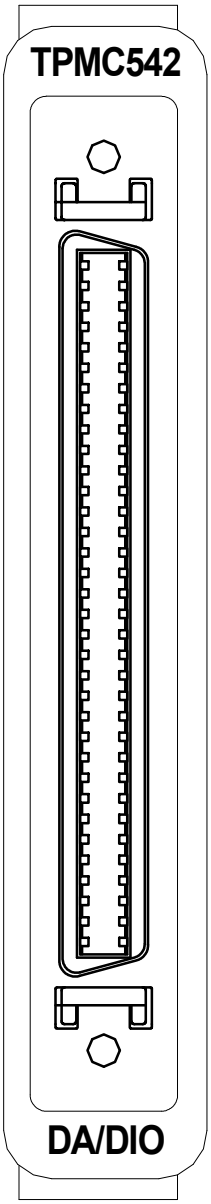


Table 11-3 : Front I/O Pin Assignment

11.2 P14 Rear I/O Connector

Pin-Count	64
Connector Type	CMC Plug Connector
Source & Order Info	Molex 71436-2864

Table 11-4 : P14 Rear I/O Connector Type

Pin	I/O Signal	Dir.	Level
1	Conv. Clock 1	In/Out	LVTTL, TTL
3	Ground		
5			
7			
9			
11			
13			
15			
17			
19	Conv. Clock 2	In/Out	LVTTL, TTL
21	Ground		
23			
25			
27			
29			
31			
33			
35			
37	Frame Trigger	In/Out	LVTTL, TTL
39	Ground		
41			
43			
45			
47			
49			
51			
53			
55	Reserved	In/Out	LVTTL, TTL
57	Ground		
59			
61			
63			

Pin	I/O Signal	Dir.	Level
2	Ground		
4			
6			
8			
10			
12			
14			
16			
18			
20	Ground		
22			
24			
26			
28			
30			
32			
34			
36			
38	Ground		
40			
42			
44			
46			
48			
50			
52			
54			
56	Ground		
58			
60			
62			
64			

Table 11-5 : P14 Rear I/O Pin Assignment

12 Programming Hints

12.1 Global DAC Status Register Read

Whenever the Global DAC Status Register is read right after a register write (e.g. to evaluated the DAC Busy Status right after a manual DAC Reset Request write, DAC Configuration Register write or DAC Data Register write) the read data of the first Global DAC Status Register read must be discarded.

In other words: Whenever the Global DAC Status Register is read right after a register write, a single leading dummy read of the Global DAC Status Register is required.