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TEWS TECHNOLOGIES

TPMC543

8 Analog Current Input Channels, 16/8 Analog High-Voltage Input Channels, 8 Analog Voltage/Current Output Channels and 8 Digital LVTTL/TTL I/O Channels

Version 1.0

User Manual

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TPMC543-10R

8 Analog Current Input Channels, 16/8 Analog High-Voltage Input Channels, 8 Analog Voltage / Current Output Channels, 8 Digital LVTTL/TTL I/O Channels

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	May 2021
1.0.1	Added Correction Data Space Description	July 2021
1.0.2	Changes in Handling and Operation Instructions chapter	March 2021
1.0.3	Added Absolute Maximum Ratings for the Analog Inputs to the Technical Specifications table Added D/*A channel output slew rate* to the Technical Specifications table Added Table for High-Voltage Analog Input Signal Range (Differential Mode) Unified that Forced Air Cooling is required at Ambient Temperatures exceeding +25°C Added chapter *Programming Hints* and sub-chapter *Global DAC Status Register Read* Clarified ADC Gain 0.16 is in fact 0.166… Tailored to the TPMC543-10R order option	February 2023

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1 Product Description

The TPMC543 is a standard single-wide PCI Mezzanine Card (PMC) compatible module providing:

- A PCI Master DMA capable 32 bit 33 MHz PCI interface
- 8x Differential 16 bit Analog Current Input Channels (Front I/O)
- 16x Single-Ended / 8x Differential 16 bit Analog High-Voltage Input Channels (Front I/O)
- 8x Single-Ended 16 bit Analog Output Channels. Each channel programmable to operate in bipolar or unipolar Voltage Mode or unipolar Current Mode (Front I/O).
- 8x Tristate-Capable bi-directional 5V-tolerant LVTTL/TTL compatible General Purpose Digital I/O Lines (Front I/O)
- 3x Tristate-Capable bi-directional 5V-tolerant LVTTL/TTL compatible Digital I/O Lines for Conversion Control Signals (Conversion Clock, Frame Trigger) (Rear-I/O)

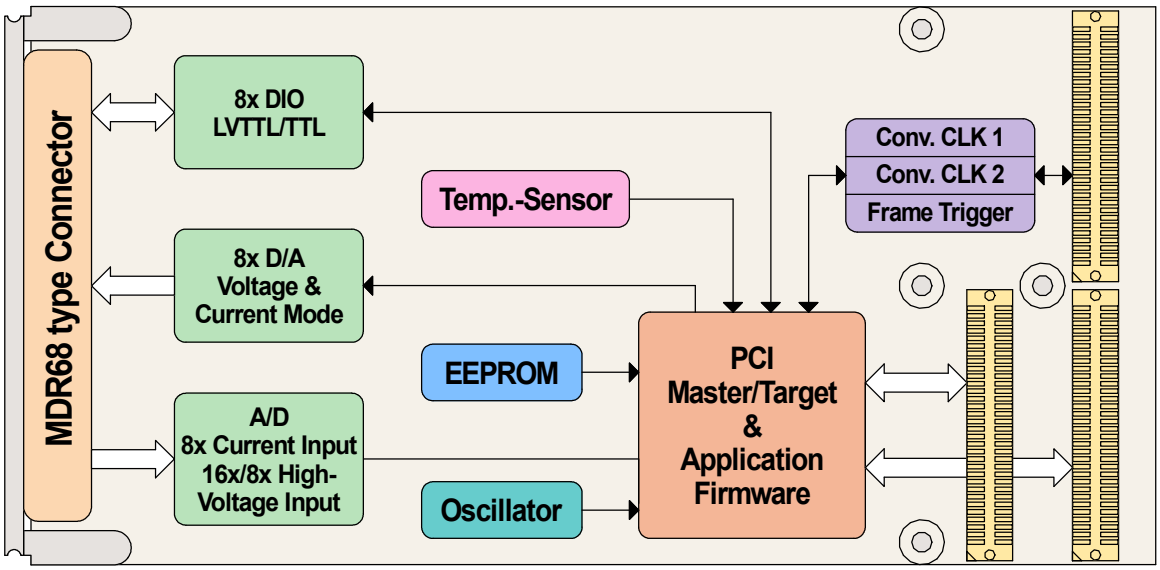


Figure 1-1 : TPMC543-10R Block Diagram

Analog Inputs

The TPMC543 utilizes the ADS3022 ADC device for the A/D analog input channels. The ADAS3022 is a 16 bit multi-channel ADC utilizing an embedded input channel multiplexer for connecting up to 8 single-ended (or up to 4 differential) analog input channels sequentially to a single integrated SAR ADC. Due to the multiplexed nature of the ADAS3022, an A/D conversion (when triggered) is being performed with a small delay between the (active) input channels of an ADAS3022 device (pseudo-simultaneous).

The analog inputs of the TPMC543 come in a certain hardware configuration (build-option), depending on the order option.

For the TPMC543-10R, the A/D channels of the ADC devices (groups of 8 SE or 4 DF channels) are hardware configured to provide:

- 8 Differential Bipolar Current Input Channels
    - Available Range: ±25mA
- 16 Single-Ended / 8 Differential Bipolar High-Voltage Input Channels
    - Single-Ended Ranges: ±10V, ±20V, ±40, ±48V (per channel)
    - Differential Ranges: ±10V, ±20V, ±40V, ±80V, ±96V (per channel)

The TPMC543 provides an A/D Sequencer unit for performing a sequence of periodic analog to digital conversions at a configurable conversion rate. In sequencer mode, the A/D conversion data is temporarily stored in an on-board data buffer and then written to buffers in host memory by PCI master DMA transfer. The A/D Sequencer also provides a Frame Mode for repetitive frames of A/D conversion sequences upon a frame trigger signal event or at a configurable frame rate.

Besides the Sequencer Mode, A/D channel data can also be processed directly via the register interface (Manual Mode).

Analog Outputs

The TPMC543 utilizes the AD5755-1 DAC device for the D/A analog output channels.

The AD5755-1 DAC device supports 4 single-ended 16bit D/A analog output channels configurable to operate in unipolar/bipolar voltage output mode or unipolar current output mode (per channel).

The TPMC543R-10R features 2 AD5755-1 DAC devices, thus providing 8 D/A analog output channels.

Each individual D/A channel can be configured to operate in any of the following output ranges:

- 0V to 5V Voltage Range
- 0V to 6V Voltage Range
- 0V to 10V Voltage Range
- 0V to 12V Voltage Range
- ±5V Voltage Range
- ±6V Voltage Range
- ±10V Voltage Range
- ±12V Voltage Range
- 4mA to 20mA Current Range
- 0mA to 20mA Current Range
- 0mA to 24mA Current Range

The TPMC543 provides a D/A Sequencer unit for performing a sequence of periodic simultaneous digital to analog conversions at a configurable conversion rate. In sequencer mode, the D/A conversion data is fetched from buffers in host memory via PCI Master DMA transfer and is temporarily stored in an on-board data buffer. The D/A Sequencer also provides a Frame Mode for repetitive frames of simultaneous D/A conversions upon a frame trigger signal event at a configurable frame rate

Besides the Sequencer Mode, D/A channel data can also be processed directly via the register interface (Manual Mode).

Digital I/O

The TPMC543 features 8 tristate-capable bi-directional general purpose digital I/O lines at the front I/O connector. Each digital I/O line has a dedicated line transmitter with individual output enable control and a dedicated line receiver. The line receivers are always enabled, so the digital I/O line level can be monitored even when used as an output. Each digital I/O line input is capable of generating an interrupt triggered on rising edge, falling edge or both edges. Additionally, a debounce filter can be configured to get rid of bouncing on the digital I/O inputs. Each digital I/O line is ESD protected and features a 4.7kΩ pull resistor to a common reference. The common pull resistor reference is programmable by software to +3.3V, +5V or GND.

Conversion Control Signals

Conversion clock (conversion rate) and frame trigger signals may be generated on-board for internal use and may also be driven out on P14 rear I/O if the card is operating as a master card in a Multi-Board configuration. The conversion clock (conversion rate) and frame trigger signals may also be sourced externally via the P14 rear I/O interface if the card is operating as a slave card in a Multi-Board configuration.

Conversion Correction Data

Each TPMC543 is factory calibrated. Conversion data correction values are determined during the factory acceptance test and are stored in an on-board serial EEPROM unique to each PMC module. These correction values may be used to perform a hardware correction for every individual D/A channel and output range and for every individual A/D channel and input range.

I/O Connector

The general purpose digital I/O signals, the analog output signals and the analog input signals are accessible on a 68 pos. Mini D Ribbon (MDR68) front connector.

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 ,Standard single-wide
Electrical Interface	PCI Rev. 3.0 compatible 33 MHz / 32 bit PCI Initiator/Target, 3.3V and 5V PCI Signaling Voltage compatible
On Board Devices	
FPGA	Xilinx Spartan-6, Industrial Temperature Range
Digital I/O	74LVT126 (NXP)
DAC	TPMC543-10R: 2x AD5755-1 (Analog Devices)
ADC	TPMC543-10R: 4x ADAS3022 (Analog Devices)
EEPROM	M93C86 (ST) 16kbit Serial EEPROM
FPGA Config. Memory	W25Q32 (Winbond) 32Mbit Serial SPI Flash
I/O Interface	
A/D Channels	Current Inputs: ±25mA (Differential) Max Operating Range is ±25mA per Input Absolute Maximum Rating is 28mA @70°C, 25.5mA @+85°C High-Voltage Inputs: Single-Ended ±10V, ±20V, ±40V, ±48V Differential ±10V, ±20V, ±40V, ±80V, ±96V Max Operating Range is ±48V per Input Pin to Ground Absolute Maximum Rating is ±66V per Input Pin to Ground Order Options: TPMC543-10R: • 8x Differential Current Inputs • 16x Single-Ended / 8x Differential High-Voltage Inputs
D/A Channels	Output range configurable per D/A channel. Simultaneous Conversion for all D/A Channels. Conversion Rate up to 38kSPS. Voltage Mode Ranges: 0V…5V, 0V…10V, -5V…+5V, -10V…+10V 0V…6V, 0V…12V, -6V…+6V, -12V…+12V Up to 10mA load current per Voltage Mode D/A Channel D/A channel output slew rate 1.9V/us (typical) Current Mode Ranges: 4mA…20mA, 0mA…20mA, 0mA…24mA Max 680Ω load resistance per Current Mode D/A Channel Order Options: TPMC543-10R: • 8x Single-Ended Voltage/Current Outputs

Digital I/O Channels	8 ESD Protected TTL/LVTTL Digital I/O Lines (Front I/O) 3.3V Driver, 5V tolerant Receiver, Individual Output Enable Control, Pull Resistor to common reference, Programmable common pull resistor reference (3.3V, 5V, GND) Up to 12mA Source Current and up to 6mA Sink Current per Digital I/O Line	
I/O Connectors		
Front I/O	68 pin Mini D Ribbon (MDR) (3M N10268-52E2PC or compatible)	
P14 Rear I/O	64 pin Mezzanine Connector (Molex 71436-2864 or compatible)	
Physical Data		
Power Requirements	Only the 5V PMC Power Supply is used TPMC543-10R: Typically 0.85A @ +5V DC without I/O Load Add 0.005A @ +5V per active DIO Output Line Add 0.070A @ +5V per active D/A Voltage Output w/o Overrange Add 0.082A @ +5V per active D/A Voltage Output w/ Overrange Add approx. ($I_{RANGE\_MAX}^2$ * R_{EXT}) / 3V ampere @ +5V per active D/A Current Output	
Temperature Range	Operating	-40°C to +85 °C **(Forced air cooling is mandatory)**
	Storage	-40°C to +85 °C
MTBF	TPMC543-10R: 165000h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	TPMC543-10R: 86g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.

Packing, unpacking and all other module handling has to be done with the appropriate care.

3.2 Forced Air Cooling

This PMC module generates noticeable heat and requires adequate forced air cooling!

Temperature Control is required!

Forced air cooling is mandatory at ambient temperatures exceeding 25°C!

3.3 High Voltage Potentials

For the High-Voltage Analog Input Configuration, care must be taken as there may be on-board voltage potentials of about twice the highest signal voltage level.

E.g. the voltage between A/D channel I/O connector pins is 96V when one A/D channel input voltage is +48V to ground while the other A/D channel input voltage is -48V to ground.

This may be extremely dangerous (especially for AC signals)!

Measures must be taken to prevent users from touching card contacts while external signal generators are in operation!

3.4 Analog Current Inputs

Care must be taken not to confuse the Analog Current Input I/O pins with the Analog High-Voltage Input I/O pins since the passive analog input circuit part is not protected!

Applying currents greater than |25mA| (or differential voltages greater than |6.25V|) to an analog current input may permanently damage the resistors in the analog current input path!

4 Address Map(s)

4.1 PCI Configuration Space

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				Initial Values (Hex Values)
	31 24	23 16	15 8	7 0	
0x00	Device ID		Vendor ID		021D 1498
0x04	Status		Command		0280 0000
0x08	Class Code			Revision ID	118000 00
0x0C	not supported	Header Type	PCI Latency Timer	not supported	00 00 00 00
0x10	Base Address Register 0 (BAR0)				FFFFFC00
0x14	Base Address Register 1 (BAR1)				FFFFF800
0x18	not supported				00000000
0x1C	not supported				00000000
0x20	not supported				00000000
0x24	not supported				00000000
0x28	PCI CardBus Information Structure Pointer				00000000
0x2C	Subsystem ID		Subsystem Vendor ID		s.b. 1498
0x30	not supported				00000000
0x34	Reserved			New Cap. Ptr.	000000 00
0x38	Reserved				00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	00 00 01 00
0x40-0xFF	Reserved				00000000

Table 4-1 : PCI Configuration Space Header

Vendor-ID:	0x1498	TEWS TECHNOLOGIES
Device-ID:	0x021F	TPMC543
Subsystem-ID:	0x000A	-10R Order Option
Subsystem Vendor-ID:	0x1498	TEWS TECHNOLOGIES

Table 4-2 : TPMC543 PCI IDs

4.2 PCI Memory Space

The TPMC543 application registers are mapped into PCI Memory Space.

Base Address Register (BAR)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	MEM	1024	32	Little	Register Space
1	MEM	2048	32	Little	Correction Data Space

Table 4-3 : PCI Memory Address Spaces

4.2.1 Register Space

The Register Space is accessible via PCI Base Address Register 0 (BAR0).

ADC3, ADC4 and DAC2 registers are not available for the TPMC543-20R order option.

PCI BAR 0 Offset	Description	Size (Bit)
A/D Global Registers		
0x000	Global ADC Control Register	32
0x004	Global ADC Status Register	32
0x008	Reserved	-
0x00C	Reserved	-
A/D Device Registers		
0x010	ADC1 Configuration Register	32
0x014	Reserved	-
0x018	ADC1 Correction Register Channel 0	32
0x01C	ADC1 Correction Register Channel 1	32
0x020	ADC1 Correction Register Channel 2	32
0x024	ADC1 Correction Register Channel 3	32
0x028	ADC1 Correction Register Channel 4	32
0x02C	ADC1 Correction Register Channel 5	32
0x030	ADC1 Correction Register Channel 6	32
0x034	ADC1 Correction Register Channel 7	32
0x038	ADC1 Data Register Channel 0/1	32
0x03C	ADC1 Data Register Channel 2/3	32
0x040	ADC1 Data Register Channel 4/5	32
0x044	ADC1 Data Register Channel 6/7	32
0x048	ADC1 Mode Register	32
0x04C	Reserved	-
0x050	Reserved	-
0x054	ADC2 Configuration Register	32
0x058	Reserved	-
0x05C	ADC2 Correction Register Channel 0	32
0x060	ADC2 Correction Register Channel 1	32
0x064	ADC2 Correction Register Channel 2	32

PCI BAR 0 Offset	Description	Size (Bit)
0x068	ADC2 Correction Register Channel 3	32
0x06C	ADC2 Correction Register Channel 4	32
0x070	ADC2 Correction Register Channel 5	32
0x074	ADC2 Correction Register Channel 6	32
0x078	ADC2 Correction Register Channel 7	32
0x07C	ADC2 Data Register Channel 0/1	32
0x080	ADC2 Data Register Channel 2/3	32
0x084	ADC2 Data Register Channel 4/5	32
0x088	ADC2 Data Register Channel 6/7	32
0x08C	ADC2 Mode Register	32
0x090	Reserved	-
0x094	Reserved	-
0x098	ADC3 Configuration Register	32
0x09C	Reserved	-
0x0A0	ADC3 Correction Register Channel 0	32
0x0A4	ADC3 Correction Register Channel 1	32
0x0A8	ADC3 Correction Register Channel 2	32
0x0AC	ADC3 Correction Register Channel 3	32
0x0B0	ADC3 Correction Register Channel 4	32
0x0B4	ADC3 Correction Register Channel 5	32
0x0B8	ADC3 Correction Register Channel 6	32
0x0BC	ADC3 Correction Register Channel 7	32
0x0C0	ADC3 Data Register Channel 0/1	32
0x0C4	ADC3 Data Register Channel 2/3	32
0x0C8	ADC3 Data Register Channel 4/5	32
0x0CC	ADC3 Data Register Channel 6/7	32
0x0D0	ADC3 Mode Register	32
0x0D4	Reserved	-
0x0D8	Reserved	-
0x0DC	ADC4 Configuration Register	32
0x0E0	Reserved	-
0x0E4	ADC4 Correction Register Channel 0	32
0x0E8	ADC4 Correction Register Channel 1	32
0x0EC	ADC4 Correction Register Channel 2	32
0x0F0	ADC4 Correction Register Channel 3	32
0x0F4	ADC4 Correction Register Channel 4	32
0x0F8	ADC4 Correction Register Channel 5	32
0x0FC	ADC4 Correction Register Channel 6	32
0x100	ADC4 Correction Register Channel 7	32
0x104	ADC4 Data Register Channel 0/1	32
0x108	ADC4 Data Register Channel 2/3	32
0x10C	ADC4 Data Register Channel 4/5	32

PCI BAR 0 Offset	Description	Size (Bit)
0x110	ADC4 Data Register Channel 6/7	32
0x114	ADC4 Mode Register	32
0x118	Reserved	-
0x11C	Reserved	-
A/D Sequencer Registers		
0x120	A/D Sequencer Control Register	32
0x124	A/D Sequencer Status Register	32
0x128	Reserved	-
0x12C	A/D Sequencer Number of Conversions Register	32
0x130	A/D Sequencer Conversion Count Register	32
0x134	A/D Sequencer FIFO Level Register	32
0x138	Reserved	-
0x13C	Reserved	-
0x140	A/D Sequencer DMA Buffer Base Address Register	32
0x144	A/D Sequencer DMA Buffer Length Register	32
0x148	A/D Sequencer DMA Buffer Next Address Register	32
0x14C	A/D Sequencer DMA Status Base Address Register	32
0x150	Reserved	-
0x154	Reserved	-
D/A Global Registers		
0x158	Global DAC Control Register	32
0x15C	Global DAC Status Register	32
0x160	Reserved	-
0x164	Reserved	-
D/A Device Registers		
0x168	DAC1 Configuration Register	32
0x16C	Reserved	-
0x170	DAC1 Correction Register A	32
0x174	DAC1 Correction Register B	32
0x178	DAC1 Correction Register C	32
0x17C	DAC1 Correction Register D	32
0x180	DAC1 Data Register A & B	32
0x184	DAC1 Data Register C & D	32
0x188	DAC1 Status Register	32
0x18C	DAC1 Mode Register	32
0x190	Reserved	-
0x194	Reserved	-
0x198	DAC2 Configuration Register	32
0x19C	Reserved	-
0x1A0	DAC2 Correction Register A	32
0x1A4	DAC2 Correction Register B	32
0x1A8	DAC2 Correction Register C	32

PCI BAR 0 Offset	Description	Size (Bit)
0x1AC	DAC2 Correction Register D	32
0x1B0	DAC2 Data Register A & B	32
0x1B4	DAC2 Data Register C & D	32
0x1B8	DAC2 Status Register	32
0x1BC	DAC2 Mode Register	32
0x1C0 … 0x2E4	Reserved	-
D/A Sequencer Registers		
0x2E8	D/A Sequencer Control Register	32
0x2EC	D/A Sequencer Status Register	32
0x2F0	Reserved	-
0x2F4	D/A Sequencer Number Of Conversions Register	32
0x2F8	D/A Sequencer Conversion Count Register	32
0x2FC	D/A Sequencer FIFO Level Register	32
0x300	Reserved	-
0x304	Reserved	-
0x308	D/A Sequencer DMA Buffer Base Address Register	32
0x30C	D/A Sequencer DMA Buffer Length Register	32
0x310	D/A Sequencer DMA Buffer Next Address Register	32
0x314	Reserved	-
0x318	Reserved	-
0x31C	Reserved	-
Conversion Signal Registers		
0x320	Conversion Clock 1 Generator Register	32
0x324	Conversion Clock 2 Generator Register	32
0x328	Reserved	-
0x32C	Frame Trigger Generator Configuration Register 1	32
0x330	Frame Trigger Generator Configuration Register 2	32
0x334	Reserved	-
0x338	Reserved	-
0x33C	Conversion Signal Generator Enable Register	32
0x340	Conversion Signal Generator Output Driver Register	32
0x344	Conversion Signal Source Selection Register	32
0x348	Frame Timer Register	32
0x34C	Reserved	-
0x350	Reserved	-
Digital I/O Registers		
0x354	DIO Input Register	32
0x358	DIO Input Filter Register	32
0x35C	DIO Output Register	32
0x360	DIO Output Enable Register	32
0x364	Reserved	-

PCI BAR 0 Offset	Description	Size (Bit)
0x368	Reserved	-
Interrupt Registers		
0x36C	Interrupt Enable Register	32
0x370	Error Interrupt Enable Register	32
0x374	DIO Rising Edge Interrupt Enable Register	32
0x378	DIO Falling Edge Interrupt Enable Register	32
0x37C	Reserved	-
0x380	Reserved	-
0x384	Interrupt Status Register	32
0x388	Error Interrupt Status Register	32
0x38C	DIO Interrupt Status Register	32
0x390	Reserved	-
0x394	Reserved	-
Other Registers		
0x398	Global Configuration Register	32
0x39C	DIO Pull Reference Register	32
0x3A0	P14 I/O Pull Reference Register	32
0x3A4	Correction EEPROM Control/Status Register	32
0x3A8	Temperature Sensor Trigger Register	32
0x3AC	Temperature Sensor Data Register	32
0x3B0 … 0x3F8	Reserved	-
0x3FC	Firmware Version Register	32

Table 4-4 : Register Space Address Map

4.2.2 Correction Data Space

The Correction Data space is accessible via PCI Base Address Register 1 (BAR1).

The Correction Data Space provides correction data values for the various analog channels. These values may optionally be used to activate data correction for each individual A/D and D/A I/O channel. To activate data correction for a certain A/D or D/A analog channel, the user must first determine the analog channel setup for the actual application (single-ended or differential, ADC gain, A/D range, D/A range), read the corresponding data correction values from the Correction Data Space ($Offset_{Corr}$ and $Gain_{Corr}$) and write these values to the corresponding Correction Data Register in the Register Space.

Regarding the A/D Range section of the Correction Data Space: The analog Inputs of the TPMC543 are hardware-configured (per ADC device) in a certain build-option (either for current input or high-voltage input). The A/D section of the Correction Data Space is ADC Gain based. However, both analog input hardware-configurations may support or use the same ADC Gain. Additionally, not every defined A/D Range section of the Correction Data Space is applicable for a certain TPMC543 order option. E.g. for ADC devices hardware-configured in the Current Input Range Build-Option, only the *ADC Gain 1.6 Differential* section of the Correction Data Space applies.

Use the following table to determine the A/D ranges (ADC gains) that are applicable for the ADC devices of a certain order option (SE = Single-Ended, DF = Differential).

TPMC543 ADC Device	TPMC543-10R	Applicable ADC Gains (to look for in the Correction Data Table)
ADC 1	Current Input	Gain 1.6 in DF (only) (for all channels)
ADC 2		
ADC 3	High-Voltage Input	Gains 0.166… / 0.2 / 0.4 / 0.8 / 1.6 in DF Gains 0.166… / 0.4 / 0.8 / 1.6 in SE (depending on user ADC channel configuration)
ADC 4		

Table 4-5 : ADC Analog Input Build-Option for Order Option (TPMC543-10R)

PCI BAR 0 Offset	Description	Size (Bit)
A/D Range ADC Gain 0.166.. Differential High-Voltage Input Range: ±96V Current Input Range: N/A		
0x000	ADC 1, Gain 0.166.., Differential Channel 0, $Offset_{Corr}$	16
0x002	ADC 1, Gain 0.166.., Differential Channel 0, $Gain_{Corr}$	16
0x004	ADC 1, Gain 0.166.., Differential Channel 1, $Offset_{Corr}$	16
0x006	ADC 1, Gain 0.166.., Differential Channel 1, $Gain_{Corr}$	16
0x008	ADC 1, Gain 0.166.., Differential Channel 2, $Offset_{Corr}$	16
0x00A	ADC 1, Gain 0.166.., Differential Channel 2, $Gain_{Corr}$	16
0x00C	ADC 1, Gain 0.166.., Differential Channel 3, $Offset_{Corr}$	16
0x00E	ADC 1, Gain 0.166.., Differential Channel 3, $Gain_{Corr}$	16
0x010	ADC 2, Gain 0.166.., Differential Channel 0, $Offset_{Corr}$	16
0x012	ADC 2, Gain 0.166.., Differential Channel 0, $Gain_{Corr}$	16
0x014	ADC 2, Gain 0.166.., Differential Channel 1, $Offset_{Corr}$	16
0x016	ADC 2, Gain 0.166.., Differential Channel 1, $Gain_{Corr}$	16
0x018	ADC 2, Gain 0.166.., Differential Channel 2, $Offset_{Corr}$	16
0x01A	ADC 2, Gain 0.166.., Differential Channel 2, $Gain_{Corr}$	16
0x01C	ADC 2, Gain 0.166.., Differential Channel 3, $Offset_{Corr}$	16
0x01E	ADC 2, Gain 0.166.., Differential Channel 3, $Gain_{Corr}$	16
0x020	ADC 3, Gain 0.166.., Differential Channel 0, $Offset_{Corr}$	16
0x022	ADC 3, Gain 0.166.., Differential Channel 0, $Gain_{Corr}$	16
0x024	ADC 3, Gain 0.166.., Differential Channel 1, $Offset_{Corr}$	16
0x026	ADC 3, Gain 0.166.., Differential Channel 1, $Gain_{Corr}$	16
0x028	ADC 3, Gain 0.166.., Differential Channel 2, $Offset_{Corr}$	16
0x02A	ADC 3, Gain 0.166.., Differential Channel 2, $Gain_{Corr}$	16
0x02C	ADC 3, Gain 0.166.., Differential Channel 3, $Offset_{Corr}$	16
0x02E	ADC 3, Gain 0.166.., Differential Channel 3, $Gain_{Corr}$	16
0x030	ADC 4, Gain 0.166.., Differential Channel 0, $Offset_{Corr}$	16
0x032	ADC 4, Gain 0.166.., Differential Channel 0, $Gain_{Corr}$	16
0x034	ADC 4, Gain 0.166.., Differential Channel 1, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x036	ADC 4, Gain 0.166.., Differential Channel 1, $Gain_{Corr}$	16
0x038	ADC 4, Gain 0.166.., Differential Channel 2, $Offset_{Corr}$	16
0x03A	ADC 4, Gain 0.166.., Differential Channel 2, $Gain_{Corr}$	16
0x03C	ADC 4, Gain 0.166.., Differential Channel 3, $Offset_{Corr}$	16
0x03E	ADC 4, Gain 0.166.., Differential Channel 3, $Gain_{Corr}$	16
0x040 … 0x07E	Reserved	16
A/D Range ADC Gain 0.2 Differential High-Voltage Input Range: ±80V Current Input Range: N/A		
0x080	ADC 1, Gain 0.2, Differential Channel 0, $Offset_{Corr}$	16
0x082	ADC 1, Gain 0.2, Differential Channel 0, $Gain_{Corr}$	16
0x084	ADC 1, Gain 0.2, Differential Channel 1, $Offset_{Corr}$	16
0x086	ADC 1, Gain 0.2, Differential Channel 1, $Gain_{Corr}$	16
0x088	ADC 1, Gain 0.2, Differential Channel 2, $Offset_{Corr}$	16
0x08A	ADC 1, Gain 0.2, Differential Channel 2, $Gain_{Corr}$	16
0x08C	ADC 1, Gain 0.2, Differential Channel 3, $Offset_{Corr}$	16
0x08E	ADC 1, Gain 0.2, Differential Channel 3, $Gain_{Corr}$	16
0x090	ADC 2, Gain 0.2, Differential Channel 0, $Offset_{Corr}$	16
0x092	ADC 2, Gain 0.2, Differential Channel 0, $Gain_{Corr}$	16
0x094	ADC 2, Gain 0.2, Differential Channel 1, $Offset_{Corr}$	16
0x096	ADC 2, Gain 0.2, Differential Channel 1, $Gain_{Corr}$	16
0x098	ADC 2, Gain 0.2, Differential Channel 2, $Offset_{Corr}$	16
0x09A	ADC 2, Gain 0.2, Differential Channel 2, $Gain_{Corr}$	16
0x09C	ADC 2, Gain 0.2, Differential Channel 3, $Offset_{Corr}$	16
0x09E	ADC 2, Gain 0.2, Differential Channel 3, $Gain_{Corr}$	16
0x0A0	ADC 3, Gain 0.2, Differential Channel 0, $Offset_{Corr}$	16
0x0A2	ADC 3, Gain 0.2, Differential Channel 0, $Gain_{Corr}$	16
0x0A4	ADC 3, Gain 0.2, Differential Channel 1, $Offset_{Corr}$	16
0x0A6	ADC 3, Gain 0.2, Differential Channel 1, $Gain_{Corr}$	16
0x0A8	ADC 3, Gain 0.2, Differential Channel 2, $Offset_{Corr}$	16
0x0AA	ADC 3, Gain 0.2, Differential Channel 2, $Gain_{Corr}$	16
0x0AC	ADC 3, Gain 0.2, Differential Channel 3, $Offset_{Corr}$	16
0x0AE	ADC 3, Gain 0.2, Differential Channel 3, $Gain_{Corr}$	16
0x0B0	ADC 4, Gain 0.2, Differential Channel 0, $Offset_{Corr}$	16
0x0B2	ADC 4, Gain 0.2, Differential Channel 0, $Gain_{Corr}$	16
0x0B4	ADC 4, Gain 0.2, Differential Channel 1, $Offset_{Corr}$	16
0x0B6	ADC 4, Gain 0.2, Differential Channel 1, $Gain_{Corr}$	16
0x0B8	ADC 4, Gain 0.2, Differential Channel 2, $Offset_{Corr}$	16
0x0BA	ADC 4, Gain 0.2, Differential Channel 2, $Gain_{Corr}$	16
0x0BC	ADC 4, Gain 0.2, Differential Channel 3, $Offset_{Corr}$	16
0x0BE	ADC 4, Gain 0.2, Differential Channel 3, $Gain_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x0C0 … 0x0FE	Reserved	16
A/D Range ADC Gain 0.4 Differential High-Voltage Input Range: ±40V Current Input Range: N/A		
0x100	ADC 1, Gain 0.4, Differential Channel 0, $Offset_{Corr}$	16
0x102	ADC 1, Gain 0.4, Differential Channel 0, $Gain_{Corr}$	16
0x104	ADC 1, Gain 0.4, Differential Channel 1, $Offset_{Corr}$	16
0x106	ADC 1, Gain 0.4, Differential Channel 1, $Gain_{Corr}$	16
0x108	ADC 1, Gain 0.4, Differential Channel 2, $Offset_{Corr}$	16
0x10A	ADC 1, Gain 0.4, Differential Channel 2, $Gain_{Corr}$	16
0x10C	ADC 1, Gain 0.4, Differential Channel 3, $Offset_{Corr}$	16
0x10E	ADC 1, Gain 0.4, Differential Channel 3, $Gain_{Corr}$	16
0x110	ADC 2, Gain 0.4, Differential Channel 0, $Offset_{Corr}$	16
0x112	ADC 2, Gain 0.4, Differential Channel 0, $Gain_{Corr}$	16
0x114	ADC 2, Gain 0.4, Differential Channel 1, $Offset_{Corr}$	16
0x116	ADC 2, Gain 0.4, Differential Channel 1, $Gain_{Corr}$	16
0x118	ADC 2, Gain 0.4, Differential Channel 2, $Offset_{Corr}$	16
0x11A	ADC 2, Gain 0.4, Differential Channel 2, $Gain_{Corr}$	16
0x11C	ADC 2, Gain 0.4, Differential Channel 3, $Offset_{Corr}$	16
0x11E	ADC 2, Gain 0.4, Differential Channel 3, $Gain_{Corr}$	16
0x120	ADC 3, Gain 0.4, Differential Channel 0, $Offset_{Corr}$	16
0x122	ADC 3, Gain 0.4, Differential Channel 0, $Gain_{Corr}$	16
0x124	ADC 3, Gain 0.4, Differential Channel 1, $Offset_{Corr}$	16
0x126	ADC 3, Gain 0.4, Differential Channel 1, $Gain_{Corr}$	16
0x128	ADC 3, Gain 0.4, Differential Channel 2, $Offset_{Corr}$	16
0x12A	ADC 3, Gain 0.4, Differential Channel 2, $Gain_{Corr}$	16
0x12C	ADC 3, Gain 0.4, Differential Channel 3, $Offset_{Corr}$	16
0x12E	ADC 3, Gain 0.4, Differential Channel 3, $Gain_{Corr}$	16
0x130	ADC 4, Gain 0.4, Differential Channel 0, $Offset_{Corr}$	16
0x132	ADC 4, Gain 0.4, Differential Channel 0, $Gain_{Corr}$	16
0x134	ADC 4, Gain 0.4, Differential Channel 1, $Offset_{Corr}$	16
0x136	ADC 4, Gain 0.4, Differential Channel 1, $Gain_{Corr}$	16
0x138	ADC 4, Gain 0.4, Differential Channel 2, $Offset_{Corr}$	16
0x13A	ADC 4, Gain 0.4, Differential Channel 2, $Gain_{Corr}$	16
0x13C	ADC 4, Gain 0.4, Differential Channel 3, $Offset_{Corr}$	16
0x13E	ADC 4, Gain 0.4, Differential Channel 3, $Gain_{Corr}$	16
0x140 … 0x17E	Reserved	16

PCI BAR 0 Offset	Description	Size (Bit)
A/D Range ADC Gain 0.8 Differential High-Voltage Input Range: ±20V Current Input Range: N/A		
0x180	ADC 1, Gain 0.8, Differential Channel 0, $Offset_{Corr}$	16
0x182	ADC 1, Gain 0.8, Differential Channel 0, $Gain_{Corr}$	16
0x184	ADC 1, Gain 0.8, Differential Channel 1, $Offset_{Corr}$	16
0x186	ADC 1, Gain 0.8, Differential Channel 1, $Gain_{Corr}$	16
0x188	ADC 1, Gain 0.8, Differential Channel 2, $Offset_{Corr}$	16
0x18A	ADC 1, Gain 0.8, Differential Channel 2, $Gain_{Corr}$	16
0x18C	ADC 1, Gain 0.8, Differential Channel 3, $Offset_{Corr}$	16
0x18E	ADC 1, Gain 0.8, Differential Channel 3, $Gain_{Corr}$	16
0x190	ADC 2, Gain 0.8, Differential Channel 0, $Offset_{Corr}$	16
0x192	ADC 2, Gain 0.8, Differential Channel 0, $Gain_{Corr}$	16
0x194	ADC 2, Gain 0.8, Differential Channel 1, $Offset_{Corr}$	16
0x196	ADC 2, Gain 0.8, Differential Channel 1, $Gain_{Corr}$	16
0x198	ADC 2, Gain 0.8, Differential Channel 2, $Offset_{Corr}$	16
0x19A	ADC 2, Gain 0.8, Differential Channel 2, $Gain_{Corr}$	16
0x19C	ADC 2, Gain 0.8, Differential Channel 3, $Offset_{Corr}$	16
0x19E	ADC 2, Gain 0.8, Differential Channel 3, $Gain_{Corr}$	16
0x1A0	ADC 3, Gain 0.8, Differential Channel 0, $Offset_{Corr}$	16
0x1A2	ADC 3, Gain 0.8, Differential Channel 0, $Gain_{Corr}$	16
0x1A4	ADC 3, Gain 0.8, Differential Channel 1, $Offset_{Corr}$	16
0x1A6	ADC 3, Gain 0.8, Differential Channel 1, $Gain_{Corr}$	16
0x1A8	ADC 3, Gain 0.8, Differential Channel 2, $Offset_{Corr}$	16
0x1AA	ADC 3, Gain 0.8, Differential Channel 2, $Gain_{Corr}$	16
0x1AC	ADC 3, Gain 0.8, Differential Channel 3, $Offset_{Corr}$	16
0x1AE	ADC 3, Gain 0.8, Differential Channel 3, $Gain_{Corr}$	16
0x1B0	ADC 4, Gain 0.8, Differential Channel 0, $Offset_{Corr}$	16
0x1B2	ADC 4, Gain 0.8, Differential Channel 0, $Gain_{Corr}$	16
0x1B4	ADC 4, Gain 0.8, Differential Channel 1, $Offset_{Corr}$	16
0x1B6	ADC 4, Gain 0.8, Differential Channel 1, $Gain_{Corr}$	16
0x1B8	ADC 4, Gain 0.8, Differential Channel 2, $Offset_{Corr}$	16
0x1BA	ADC 4, Gain 0.8, Differential Channel 2, $Gain_{Corr}$	16
0x1BC	ADC 4, Gain 0.8, Differential Channel 3, $Offset_{Corr}$	16
0x1BE	ADC 4, Gain 0.8, Differential Channel 3, $Gain_{Corr}$	16
0x1C0 … 0x1FE	Reserved	16
A/D Range ADC Gain 1.6 Differential High-Voltage Input Range: ±10V Current Input Range: ±25mA		
0x200	ADC 1, Gain 1.6, Differential Channel 0, $Offset_{Corr}$	16
0x202	ADC 1, Gain 1.6, Differential Channel 0, $Gain_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x204	ADC 1, Gain 1.6, Differential Channel 1, $Offset_{Corr}$	16
0x206	ADC 1, Gain 1.6, Differential Channel 1, $Gain_{Corr}$	16
0x208	ADC 1, Gain 1.6, Differential Channel 2, $Offset_{Corr}$	16
0x20A	ADC 1, Gain 1.6, Differential Channel 2, $Gain_{Corr}$	16
0x20C	ADC 1, Gain 1.6, Differential Channel 3, $Offset_{Corr}$	16
0x20E	ADC 1, Gain 1.6, Differential Channel 3, $Gain_{Corr}$	16
0x210	ADC 2, Gain 1.6, Differential Channel 0, $Offset_{Corr}$	16
0x212	ADC 2, Gain 1.6, Differential Channel 0, $Gain_{Corr}$	16
0x214	ADC 2, Gain 1.6, Differential Channel 1, $Offset_{Corr}$	16
0x216	ADC 2, Gain 1.6, Differential Channel 1, $Gain_{Corr}$	16
0x218	ADC 2, Gain 1.6, Differential Channel 2, $Offset_{Corr}$	16
0x21A	ADC 2, Gain 1.6, Differential Channel 2, $Gain_{Corr}$	16
0x21C	ADC 2, Gain 1.6, Differential Channel 3, $Offset_{Corr}$	16
0x21E	ADC 2, Gain 1.6, Differential Channel 3, $Gain_{Corr}$	16
0x220	ADC 3, Gain 1.6, Differential Channel 0, $Offset_{Corr}$	16
0x222	ADC 3, Gain 1.6, Differential Channel 0, $Gain_{Corr}$	16
0x224	ADC 3, Gain 1.6, Differential Channel 1, $Offset_{Corr}$	16
0x226	ADC 3, Gain 1.6, Differential Channel 1, $Gain_{Corr}$	16
0x228	ADC 3, Gain 1.6, Differential Channel 2, $Offset_{Corr}$	16
0x22A	ADC 3, Gain 1.6, Differential Channel 2, $Gain_{Corr}$	16
0x22C	ADC 3, Gain 1.6, Differential Channel 3, $Offset_{Corr}$	16
0x22E	ADC 3, Gain 1.6, Differential Channel 3, $Gain_{Corr}$	16
0x230	ADC 4, Gain 1.6, Differential Channel 0, $Offset_{Corr}$	16
0x232	ADC 4, Gain 1.6, Differential Channel 0, $Gain_{Corr}$	16
0x234	ADC 4, Gain 1.6, Differential Channel 1, $Offset_{Corr}$	16
0x236	ADC 4, Gain 1.6, Differential Channel 1, $Gain_{Corr}$	16
0x238	ADC 4, Gain 1.6, Differential Channel 2, $Offset_{Corr}$	16
0x23A	ADC 4, Gain 1.6, Differential Channel 2, $Gain_{Corr}$	16
0x23C	ADC 4, Gain 1.6, Differential Channel 3, $Offset_{Corr}$	16
0x23E	ADC 4, Gain 1.6, Differential Channel 3, $Gain_{Corr}$	16
0x240 … 0x27E	Reserved	16
A/D Range ADC Gain 3.2 Differential High-Voltage Input Range: N/A Current Input Range: N/A		
0x280	ADC 1, Gain 3.2, Differential Channel 0, $Offset_{Corr}$	16
0x282	ADC 1, Gain 3.2, Differential Channel 0, $Gain_{Corr}$	16
0x284	ADC 1, Gain 3.2, Differential Channel 1, $Offset_{Corr}$	16
0x286	ADC 1, Gain 3.2, Differential Channel 1, $Gain_{Corr}$	16
0x288	ADC 1, Gain 3.2, Differential Channel 2, $Offset_{Corr}$	16
0x28A	ADC 1, Gain 3.2, Differential Channel 2, $Gain_{Corr}$	16
0x28C	ADC 1, Gain 3.2, Differential Channel 3, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x28E	ADC 1, Gain 3.2, Differential Channel 3, $Gain_{Corr}$	16
0x290	ADC 2, Gain 3.2, Differential Channel 0, $Offset_{Corr}$	16
0x292	ADC 2, Gain 3.2, Differential Channel 0, $Gain_{Corr}$	16
0x294	ADC 2, Gain 3.2, Differential Channel 1, $Offset_{Corr}$	16
0x296	ADC 2, Gain 3.2, Differential Channel 1, $Gain_{Corr}$	16
0x298	ADC 2, Gain 3.2, Differential Channel 2, $Offset_{Corr}$	16
0x29A	ADC 2, Gain 3.2, Differential Channel 2, $Gain_{Corr}$	16
0x29C	ADC 2, Gain 3.2, Differential Channel 3, $Offset_{Corr}$	16
0x29E	ADC 2, Gain 3.2, Differential Channel 3, $Gain_{Corr}$	16
0x2A0	ADC 3, Gain 3.2, Differential Channel 0, $Offset_{Corr}$	16
0x2A2	ADC 3, Gain 3.2, Differential Channel 0, $Gain_{Corr}$	16
0x2A4	ADC 3, Gain 3.2, Differential Channel 1, $Offset_{Corr}$	16
0x2A6	ADC 3, Gain 3.2, Differential Channel 1, $Gain_{Corr}$	16
0x2A8	ADC 3, Gain 3.2, Differential Channel 2, $Offset_{Corr}$	16
0x2AA	ADC 3, Gain 3.2, Differential Channel 2, $Gain_{Corr}$	16
0x2AC	ADC 3, Gain 3.2, Differential Channel 3, $Offset_{Corr}$	16
0x2AE	ADC 3, Gain 3.2, Differential Channel 3, $Gain_{Corr}$	16
0x2B0	ADC 4, Gain 3.2, Differential Channel 0, $Offset_{Corr}$	16
0x2B2	ADC 4, Gain 3.2, Differential Channel 0, $Gain_{Corr}$	16
0x2B4	ADC 4, Gain 3.2, Differential Channel 1, $Offset_{Corr}$	16
0x2B6	ADC 4, Gain 3.2, Differential Channel 1, $Gain_{Corr}$	16
0x2B8	ADC 4, Gain 3.2, Differential Channel 2, $Offset_{Corr}$	16
0x2BA	ADC 4, Gain 3.2, Differential Channel 2, $Gain_{Corr}$	16
0x2BC	ADC 4, Gain 3.2, Differential Channel 3, $Offset_{Corr}$	16
0x2BE	ADC 4, Gain 3.2, Differential Channel 3, $Gain_{Corr}$	16
0x2C0 … 0x2FE	Reserved	16
A/D Range ADC Gain 6.4 Differential High-Voltage Input Range: N/A Current Input Range: N/A		
0x300	ADC 1, Gain 6.4, Differential Channel 0, $Offset_{Corr}$	16
0x302	ADC 1, Gain 6.4, Differential Channel 0, $Gain_{Corr}$	16
0x304	ADC 1, Gain 6.4, Differential Channel 1, $Offset_{Corr}$	16
0x306	ADC 1, Gain 6.4, Differential Channel 1, $Gain_{Corr}$	16
0x308	ADC 1, Gain 6.4, Differential Channel 2, $Offset_{Corr}$	16
0x30A	ADC 1, Gain 6.4, Differential Channel 2, $Gain_{Corr}$	16
0x30C	ADC 1, Gain 6.4, Differential Channel 3, $Offset_{Corr}$	16
0x30E	ADC 1, Gain 6.4, Differential Channel 3, $Gain_{Corr}$	16
0x310	ADC 2, Gain 6.4, Differential Channel 0, $Offset_{Corr}$	16
0x312	ADC 2, Gain 6.4, Differential Channel 0, $Gain_{Corr}$	16
0x314	ADC 2, Gain 6.4, Differential Channel 1, $Offset_{Corr}$	16
0x316	ADC 2, Gain 6.4, Differential Channel 1, $Gain_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x318	ADC 2, Gain 6.4, Differential Channel 2, $Offset_{Corr}$	16
0x31A	ADC 2, Gain 6.4, Differential Channel 2, $Gain_{Corr}$	16
0x31C	ADC 2, Gain 6.4, Differential Channel 3, $Offset_{Corr}$	16
0x31E	ADC 2, Gain 6.4, Differential Channel 3, $Gain_{Corr}$	16
0x320	ADC 3, Gain 6.4, Differential Channel 0, $Offset_{Corr}$	16
0x322	ADC 3, Gain 6.4, Differential Channel 0, $Gain_{Corr}$	16
0x324	ADC 3, Gain 6.4, Differential Channel 1, $Offset_{Corr}$	16
0x326	ADC 3, Gain 6.4, Differential Channel 1, $Gain_{Corr}$	16
0x328	ADC 3, Gain 6.4, Differential Channel 2, $Offset_{Corr}$	16
0x32A	ADC 3, Gain 6.4, Differential Channel 2, $Gain_{Corr}$	16
0x32C	ADC 3, Gain 6.4, Differential Channel 3, $Offset_{Corr}$	16
0x32E	ADC 3, Gain 6.4, Differential Channel 3, $Gain_{Corr}$	16
0x330	ADC 4, Gain 6.4, Differential Channel 0, $Offset_{Corr}$	16
0x332	ADC 4, Gain 6.4, Differential Channel 0, $Gain_{Corr}$	16
0x334	ADC 4, Gain 6.4, Differential Channel 1, $Offset_{Corr}$	16
0x336	ADC 4, Gain 6.4, Differential Channel 1, $Gain_{Corr}$	16
0x338	ADC 4, Gain 6.4, Differential Channel 2, $Offset_{Corr}$	16
0x33A	ADC 4, Gain 6.4, Differential Channel 2, $Gain_{Corr}$	16
0x33C	ADC 4, Gain 6.4, Differential Channel 3, $Offset_{Corr}$	16
0x33E	ADC 4, Gain 6.4, Differential Channel 3, $Gain_{Corr}$	16
0x340 … 0x37E	Reserved	16
A/D Range ADC Gain 0.166.. Single-Ended High-Voltage Input Range: ±48V Current Input Range: N/A		
0x380	ADC 1, Gain 0.166.., Single-Ended Channel 0, $Offset_{Corr}$	16
0x382	ADC 1, Gain 0.166.., Single-Ended Channel 0, $Gain_{Corr}$	16
0x384	ADC 1, Gain 0.166.., Single-Ended Channel 1, $Offset_{Corr}$	16
0x386	ADC 1, Gain 0.166.., Single-Ended Channel 1, $Gain_{Corr}$	16
0x388	ADC 1, Gain 0.166.., Single-Ended Channel 2, $Offset_{Corr}$	16
0x38A	ADC 1, Gain 0.166.., Single-Ended Channel 2, $Gain_{Corr}$	16
0x38C	ADC 1, Gain 0.166.., Single-Ended Channel 3, $Offset_{Corr}$	16
0x38E	ADC 1, Gain 0.166.., Single-Ended Channel 3, $Gain_{Corr}$	16
0x390	ADC 1, Gain 0.166.., Single-Ended Channel 4, $Offset_{Corr}$	16
0x392	ADC 1, Gain 0.166.., Single-Ended Channel 4, $Gain_{Corr}$	16
0x394	ADC 1, Gain 0.166.., Single-Ended Channel 5, $Offset_{Corr}$	16
0x396	ADC 1, Gain 0.166.., Single-Ended Channel 5, $Gain_{Corr}$	16
0x398	ADC 1, Gain 0.166.., Single-Ended Channel 6, $Offset_{Corr}$	16
0x39A	ADC 1, Gain 0.166.., Single-Ended Channel 6, $Gain_{Corr}$	16
0x39C	ADC 1, Gain 0.166.., Single-Ended Channel 7, $Offset_{Corr}$	16
0x39E	ADC 1, Gain 0.166.., Single-Ended Channel 7, $Gain_{Corr}$	16
0x3A0	ADC 2, Gain 0.166.., Single-Ended Channel 0, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x3A2	ADC 2, Gain 0.166.., Single-Ended Channel 0, $Gain_{Corr}$	16
0x3A4	ADC 2, Gain 0.166.., Single-Ended Channel 1, $Offset_{Corr}$	16
0x3A6	ADC 2, Gain 0.166.., Single-Ended Channel 1, $Gain_{Corr}$	16
0x3A8	ADC 2, Gain 0.166.., Single-Ended Channel 2, $Offset_{Corr}$	16
0x3AA	ADC 2, Gain 0.166.., Single-Ended Channel 2, $Gain_{Corr}$	16
0x3AC	ADC 2, Gain 0.166.., Single-Ended Channel 3, $Offset_{Corr}$	16
0x3AE	ADC 2, Gain 0.166.., Single-Ended Channel 3, $Gain_{Corr}$	16
0x3B0	ADC 2, Gain 0.166.., Single-Ended Channel 4, $Offset_{Corr}$	16
0x3B2	ADC 2, Gain 0.166.., Single-Ended Channel 4, $Gain_{Corr}$	16
0x3B4	ADC 2, Gain 0.166.., Single-Ended Channel 5, $Offset_{Corr}$	16
0x3B6	ADC 2, Gain 0.166.., Single-Ended Channel 5, $Gain_{Corr}$	16
0x3B8	ADC 2, Gain 0.166.., Single-Ended Channel 6, $Offset_{Corr}$	16
0x3BA	ADC 2, Gain 0.166.., Single-Ended Channel 6, $Gain_{Corr}$	16
0x3BC	ADC 2, Gain 0.166.., Single-Ended Channel 7, $Offset_{Corr}$	16
0x3BE	ADC 2, Gain 0.166.., Single-Ended Channel 7, $Gain_{Corr}$	16
0x3C0	ADC 3, Gain 0.166.., Single-Ended Channel 0, $Offset_{Corr}$	16
0x3C2	ADC 3, Gain 0.166.., Single-Ended Channel 0, $Gain_{Corr}$	16
0x3C4	ADC 3, Gain 0.166.., Single-Ended Channel 1, $Offset_{Corr}$	16
0x3C6	ADC 3, Gain 0.166.., Single-Ended Channel 1, $Gain_{Corr}$	16
0x3C8	ADC 3, Gain 0.166.., Single-Ended Channel 2, $Offset_{Corr}$	16
0x3CA	ADC 3, Gain 0.166.., Single-Ended Channel 2, $Gain_{Corr}$	16
0x3CC	ADC 3, Gain 0.166.., Single-Ended Channel 3, $Offset_{Corr}$	16
0x3CE	ADC 3, Gain 0.166.., Single-Ended Channel 3, $Gain_{Corr}$	16
0x3D0	ADC 3, Gain 0.166.., Single-Ended Channel 4, $Offset_{Corr}$	16
0x3D2	ADC 3, Gain 0.166.., Single-Ended Channel 4, $Gain_{Corr}$	16
0x3D4	ADC 3, Gain 0.166.., Single-Ended Channel 5, $Offset_{Corr}$	16
0x3D6	ADC 3, Gain 0.166.., Single-Ended Channel 5, $Gain_{Corr}$	16
0x3D8	ADC 3, Gain 0.166.., Single-Ended Channel 6, $Offset_{Corr}$	16
0x3DA	ADC 3, Gain 0.166.., Single-Ended Channel 6, $Gain_{Corr}$	16
0x3DC	ADC 3, Gain 0.166.., Single-Ended Channel 7, $Offset_{Corr}$	16
0x3DE	ADC 3, Gain 0.166.., Single-Ended Channel 7, $Gain_{Corr}$	16
0x3E0	ADC 4, Gain 0.166.., Single-Ended Channel 0, $Offset_{Corr}$	16
0x3E2	ADC 4, Gain 0.166.., Single-Ended Channel 0, $Gain_{Corr}$	16
0x3E4	ADC 4, Gain 0.166.., Single-Ended Channel 1, $Offset_{Corr}$	16
0x3E6	ADC 4, Gain 0.166.., Single-Ended Channel 1, $Gain_{Corr}$	16
0x3E8	ADC 4, Gain 0.166.., Single-Ended Channel 2, $Offset_{Corr}$	16
0x3EA	ADC 4, Gain 0.166.., Single-Ended Channel 2, $Gain_{Corr}$	16
0x3EC	ADC 4, Gain 0.166.., Single-Ended Channel 3, $Offset_{Corr}$	16
0x3EE	ADC 4, Gain 0.166.., Single-Ended Channel 3, $Gain_{Corr}$	16
0x3F0	ADC 4, Gain 0.166.., Single-Ended Channel 4, $Offset_{Corr}$	16
0x3F2	ADC 4, Gain 0.166.., Single-Ended Channel 4, $Gain_{Corr}$	16
0x3F4	ADC 4, Gain 0.166.., Single-Ended Channel 5, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x3F6	ADC 4, Gain 0.166.., Single-Ended Channel 5, $Gain_{Corr}$	16
0x3F8	ADC 4, Gain 0.166.., Single-Ended Channel 6, $Offset_{Corr}$	16
0x3FA	ADC 4, Gain 0.166.., Single-Ended Channel 6, $Gain_{Corr}$	16
0x3FC	ADC 4, Gain 0.166.., Single-Ended Channel 7, $Offset_{Corr}$	16
0x3FE	ADC 4, Gain 0.166.., Single-Ended Channel 7, $Gain_{Corr}$	16
A/D Range ADC Gain 0.4 Single-Ended High-Voltage Input Range: ±40V Current Input Range: N/A		
0x400	ADC 1, Gain 0.4, Single-Ended Channel 0, $Offset_{Corr}$	16
0x402	ADC 1, Gain 0.4, Single-Ended Channel 0, $Gain_{Corr}$	16
0x404	ADC 1, Gain 0.4, Single-Ended Channel 1, $Offset_{Corr}$	16
0x406	ADC 1, Gain 0.4, Single-Ended Channel 1, $Gain_{Corr}$	16
0x408	ADC 1, Gain 0.4, Single-Ended Channel 2, $Offset_{Corr}$	16
0x40A	ADC 1, Gain 0.4, Single-Ended Channel 2, $Gain_{Corr}$	16
0x40C	ADC 1, Gain 0.4, Single-Ended Channel 3, $Offset_{Corr}$	16
0x40E	ADC 1, Gain 0.4, Single-Ended Channel 3, $Gain_{Corr}$	16
0x410	ADC 1, Gain 0.4, Single-Ended Channel 4, $Offset_{Corr}$	16
0x412	ADC 1, Gain 0.4, Single-Ended Channel 4, $Gain_{Corr}$	16
0x414	ADC 1, Gain 0.4, Single-Ended Channel 5, $Offset_{Corr}$	16
0x416	ADC 1, Gain 0.4, Single-Ended Channel 5, $Gain_{Corr}$	16
0x418	ADC 1, Gain 0.4, Single-Ended Channel 6, $Offset_{Corr}$	16
0x41A	ADC 1, Gain 0.4, Single-Ended Channel 6, $Gain_{Corr}$	16
0x41C	ADC 1, Gain 0.4, Single-Ended Channel 7, $Offset_{Corr}$	16
0x41E	ADC 1, Gain 0.4, Single-Ended Channel 7, $Gain_{Corr}$	16
0x420	ADC 2, Gain 0.4, Single-Ended Channel 0, $Offset_{Corr}$	16
0x422	ADC 2, Gain 0.4, Single-Ended Channel 0, $Gain_{Corr}$	16
0x424	ADC 2, Gain 0.4, Single-Ended Channel 1, $Offset_{Corr}$	16
0x426	ADC 2, Gain 0.4, Single-Ended Channel 1, $Gain_{Corr}$	16
0x428	ADC 2, Gain 0.4, Single-Ended Channel 2, $Offset_{Corr}$	16
0x42A	ADC 2, Gain 0.4, Single-Ended Channel 2, $Gain_{Corr}$	16
0x42C	ADC 2, Gain 0.4, Single-Ended Channel 3, $Offset_{Corr}$	16
0x42E	ADC 2, Gain 0.4, Single-Ended Channel 3, $Gain_{Corr}$	16
0x430	ADC 2, Gain 0.4, Single-Ended Channel 4, $Offset_{Corr}$	16
0x432	ADC 2, Gain 0.4, Single-Ended Channel 4, $Gain_{Corr}$	16
0x434	ADC 2, Gain 0.4, Single-Ended Channel 5, $Offset_{Corr}$	16
0x436	ADC 2, Gain 0.4, Single-Ended Channel 5, $Gain_{Corr}$	16
0x438	ADC 2, Gain 0.4, Single-Ended Channel 6, $Offset_{Corr}$	16
0x43A	ADC 2, Gain 0.4, Single-Ended Channel 6, $Gain_{Corr}$	16
0x43C	ADC 2, Gain 0.4, Single-Ended Channel 7, $Offset_{Corr}$	16
0x43E	ADC 2, Gain 0.4, Single-Ended Channel 7, $Gain_{Corr}$	16
0x440	ADC 3, Gain 0.4, Single-Ended Channel 0, $Offset_{Corr}$	16
0x442	ADC 3, Gain 0.4, Single-Ended Channel 0, $Gain_{Corr}$	16
0x444	ADC 3, Gain 0.4, Single-Ended Channel 1, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x446	ADC 3, Gain 0.4, Single-Ended Channel 1, $Gain_{Corr}$	16
0x448	ADC 3, Gain 0.4, Single-Ended Channel 2, $Offset_{Corr}$	16
0x44A	ADC 3, Gain 0.4, Single-Ended Channel 2, $Gain_{Corr}$	16
0x44C	ADC 3, Gain 0.4, Single-Ended Channel 3, $Offset_{Corr}$	16
0x44E	ADC 3, Gain 0.4, Single-Ended Channel 3, $Gain_{Corr}$	16
0x450	ADC 3, Gain 0.4, Single-Ended Channel 4, $Offset_{Corr}$	16
0x452	ADC 3, Gain 0.4, Single-Ended Channel 4, $Gain_{Corr}$	16
0x454	ADC 3, Gain 0.4, Single-Ended Channel 5, $Offset_{Corr}$	16
0x456	ADC 3, Gain 0.4, Single-Ended Channel 5, $Gain_{Corr}$	16
0x458	ADC 3, Gain 0.4, Single-Ended Channel 6, $Offset_{Corr}$	16
0x45A	ADC 3, Gain 0.4, Single-Ended Channel 6, $Gain_{Corr}$	16
0x45C	ADC 3, Gain 0.4, Single-Ended Channel 7, $Offset_{Corr}$	16
0x45E	ADC 3, Gain 0.4, Single-Ended Channel 7, $Gain_{Corr}$	16
0x460	ADC 4, Gain 0.4, Single-Ended Channel 0, $Offset_{Corr}$	16
0x462	ADC 4, Gain 0.4, Single-Ended Channel 0, $Gain_{Corr}$	16
0x464	ADC 4, Gain 0.4, Single-Ended Channel 1, $Offset_{Corr}$	16
0x466	ADC 4, Gain 0.4, Single-Ended Channel 1, $Gain_{Corr}$	16
0x468	ADC 4, Gain 0.4, Single-Ended Channel 2, $Offset_{Corr}$	16
0x46A	ADC 4, Gain 0.4, Single-Ended Channel 2, $Gain_{Corr}$	16
0x46C	ADC 4, Gain 0.4, Single-Ended Channel 3, $Offset_{Corr}$	16
0x46E	ADC 4, Gain 0.4, Single-Ended Channel 3, $Gain_{Corr}$	16
0x470	ADC 4, Gain 0.4, Single-Ended Channel 4, $Offset_{Corr}$	16
0x472	ADC 4, Gain 0.4, Single-Ended Channel 4, $Gain_{Corr}$	16
0x474	ADC 4, Gain 0.4, Single-Ended Channel 5, $Offset_{Corr}$	16
0x476	ADC 4, Gain 0.4, Single-Ended Channel 5, $Gain_{Corr}$	16
0x478	ADC 4, Gain 0.4, Single-Ended Channel 6, $Offset_{Corr}$	16
0x47A	ADC 4, Gain 0.4, Single-Ended Channel 6, $Gain_{Corr}$	16
0x47C	ADC 4, Gain 0.4, Single-Ended Channel 7, $Offset_{Corr}$	16
0x47E	ADC 4, Gain 0.4, Single-Ended Channel 7, $Gain_{Corr}$	16
A/D Range ADC Gain 0.8 Single-Ended High-Voltage Input Range: ±20V Current Input Range: N/A		
0x480	ADC 1, Gain 0.8, Single-Ended Channel 0, $Offset_{Corr}$	16
0x482	ADC 1, Gain 0.8, Single-Ended Channel 0, $Gain_{Corr}$	16
0x484	ADC 1, Gain 0.8, Single-Ended Channel 1, $Offset_{Corr}$	16
0x486	ADC 1, Gain 0.8, Single-Ended Channel 1, $Gain_{Corr}$	16
0x488	ADC 1, Gain 0.8, Single-Ended Channel 2, $Offset_{Corr}$	16
0x48A	ADC 1, Gain 0.8, Single-Ended Channel 2, $Gain_{Corr}$	16
0x48C	ADC 1, Gain 0.8, Single-Ended Channel 3, $Offset_{Corr}$	16
0x48E	ADC 1, Gain 0.8, Single-Ended Channel 3, $Gain_{Corr}$	16
0x490	ADC 1, Gain 0.8, Single-Ended Channel 4, $Offset_{Corr}$	16
0x492	ADC 1, Gain 0.8, Single-Ended Channel 4, $Gain_{Corr}$	16
0x494	ADC 1, Gain 0.8, Single-Ended Channel 5, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x496	ADC 1, Gain 0.8, Single-Ended Channel 5, $Gain_{Corr}$	16
0x498	ADC 1, Gain 0.8, Single-Ended Channel 6, $Offset_{Corr}$	16
0x49A	ADC 1, Gain 0.8, Single-Ended Channel 6, $Gain_{Corr}$	16
0x49C	ADC 1, Gain 0.8, Single-Ended Channel 7, $Offset_{Corr}$	16
0x49E	ADC 1, Gain 0.8, Single-Ended Channel 7, $Gain_{Corr}$	16
0x4A0	ADC 2, Gain 0.8, Single-Ended Channel 0, $Offset_{Corr}$	16
0x4A2	ADC 2, Gain 0.8, Single-Ended Channel 0, $Gain_{Corr}$	16
0x4A4	ADC 2, Gain 0.8, Single-Ended Channel 1, $Offset_{Corr}$	16
0x4A6	ADC 2, Gain 0.8, Single-Ended Channel 1, $Gain_{Corr}$	16
0x4A8	ADC 2, Gain 0.8, Single-Ended Channel 2, $Offset_{Corr}$	16
0x4AA	ADC 2, Gain 0.8, Single-Ended Channel 2, $Gain_{Corr}$	16
0x4AC	ADC 2, Gain 0.8, Single-Ended Channel 3, $Offset_{Corr}$	16
0x4AE	ADC 2, Gain 0.8, Single-Ended Channel 3, $Gain_{Corr}$	16
0x4B0	ADC 2, Gain 0.8, Single-Ended Channel 4, $Offset_{Corr}$	16
0x4B2	ADC 2, Gain 0.8, Single-Ended Channel 4, $Gain_{Corr}$	16
0x4B4	ADC 2, Gain 0.8, Single-Ended Channel 5, $Offset_{Corr}$	16
0x4B6	ADC 2, Gain 0.8, Single-Ended Channel 5, $Gain_{Corr}$	16
0x4B8	ADC 2, Gain 0.8, Single-Ended Channel 6, $Offset_{Corr}$	16
0x4BA	ADC 2, Gain 0.8, Single-Ended Channel 6, $Gain_{Corr}$	16
0x4BC	ADC 2, Gain 0.8, Single-Ended Channel 7, $Offset_{Corr}$	16
0x4BE	ADC 2, Gain 0.8, Single-Ended Channel 7, $Gain_{Corr}$	16
0x4C0	ADC 3, Gain 0.8, Single-Ended Channel 0, $Offset_{Corr}$	16
0x4C2	ADC 3, Gain 0.8, Single-Ended Channel 0, $Gain_{Corr}$	16
0x4C4	ADC 3, Gain 0.8, Single-Ended Channel 1, $Offset_{Corr}$	16
0x4C6	ADC 3, Gain 0.8, Single-Ended Channel 1, $Gain_{Corr}$	16
0x4C8	ADC 3, Gain 0.8, Single-Ended Channel 2, $Offset_{Corr}$	16
0x4CA	ADC 3, Gain 0.8, Single-Ended Channel 2, $Gain_{Corr}$	16
0x4CC	ADC 3, Gain 0.8, Single-Ended Channel 3, $Offset_{Corr}$	16
0x4CE	ADC 3, Gain 0.8, Single-Ended Channel 3, $Gain_{Corr}$	16
0x4D0	ADC 3, Gain 0.8, Single-Ended Channel 4, $Offset_{Corr}$	16
0x4D2	ADC 3, Gain 0.8, Single-Ended Channel 4, $Gain_{Corr}$	16
0x4D4	ADC 3, Gain 0.8, Single-Ended Channel 5, $Offset_{Corr}$	16
0x4D6	ADC 3, Gain 0.8, Single-Ended Channel 5, $Gain_{Corr}$	16
0x4D8	ADC 3, Gain 0.8, Single-Ended Channel 6, $Offset_{Corr}$	16
0x4DA	ADC 3, Gain 0.8, Single-Ended Channel 6, $Gain_{Corr}$	16
0x4DC	ADC 3, Gain 0.8, Single-Ended Channel 7, $Offset_{Corr}$	16
0x4DE	ADC 3, Gain 0.8, Single-Ended Channel 7, $Gain_{Corr}$	16
0x4E0	ADC 4, Gain 0.8, Single-Ended Channel 0, $Offset_{Corr}$	16
0x4E2	ADC 4, Gain 0.8, Single-Ended Channel 0, $Gain_{Corr}$	16
0x4E4	ADC 4, Gain 0.8, Single-Ended Channel 1, $Offset_{Corr}$	16
0x4E6	ADC 4, Gain 0.8, Single-Ended Channel 1, $Gain_{Corr}$	16
0x4E8	ADC 4, Gain 0.8, Single-Ended Channel 2, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x4EA	ADC 4, Gain 0.8, Single-Ended Channel 2, $Gain_{Corr}$	16
0x4EC	ADC 4, Gain 0.8, Single-Ended Channel 3, $Offset_{Corr}$	16
0x4EE	ADC 4, Gain 0.8, Single-Ended Channel 3, $Gain_{Corr}$	16
0x4F0	ADC 4, Gain 0.8, Single-Ended Channel 4, $Offset_{Corr}$	16
0x4F2	ADC 4, Gain 0.8, Single-Ended Channel 4, $Gain_{Corr}$	16
0x4F4	ADC 4, Gain 0.8, Single-Ended Channel 5, $Offset_{Corr}$	16
0x4F6	ADC 4, Gain 0.8, Single-Ended Channel 5, $Gain_{Corr}$	16
0x4F8	ADC 4, Gain 0.8, Single-Ended Channel 6, $Offset_{Corr}$	16
0x4FA	ADC 4, Gain 0.8, Single-Ended Channel 6, $Gain_{Corr}$	16
0x4FC	ADC 4, Gain 0.8, Single-Ended Channel 7, $Offset_{Corr}$	16
0x4FE	ADC 4, Gain 0.8, Single-Ended Channel 7, $Gain_{Corr}$	16
A/D Range ADC Gain 1.6 Single-Ended High-Voltage Input Range: ±10V Current Input Range: N/A		
0x500	ADC 1, Gain 1.6, Single-Ended Channel 0, $Offset_{Corr}$	16
0x502	ADC 1, Gain 1.6, Single-Ended Channel 0, $Gain_{Corr}$	16
0x504	ADC 1, Gain 1.6, Single-Ended Channel 1, $Offset_{Corr}$	16
0x506	ADC 1, Gain 1.6, Single-Ended Channel 1, $Gain_{Corr}$	16
0x508	ADC 1, Gain 1.6, Single-Ended Channel 2, $Offset_{Corr}$	16
0x50A	ADC 1, Gain 1.6, Single-Ended Channel 2, $Gain_{Corr}$	16
0x50C	ADC 1, Gain 1.6, Single-Ended Channel 3, $Offset_{Corr}$	16
0x50E	ADC 1, Gain 1.6, Single-Ended Channel 3, $Gain_{Corr}$	16
0x510	ADC 1, Gain 1.6, Single-Ended Channel 4, $Offset_{Corr}$	16
0x512	ADC 1, Gain 1.6, Single-Ended Channel 4, $Gain_{Corr}$	16
0x514	ADC 1, Gain 1.6, Single-Ended Channel 5, $Offset_{Corr}$	16
0x516	ADC 1, Gain 1.6, Single-Ended Channel 5, $Gain_{Corr}$	16
0x518	ADC 1, Gain 1.6, Single-Ended Channel 6, $Offset_{Corr}$	16
0x51A	ADC 1, Gain 1.6, Single-Ended Channel 6, $Gain_{Corr}$	16
0x51C	ADC 1, Gain 1.6, Single-Ended Channel 7, $Offset_{Corr}$	16
0x51E	ADC 1, Gain 1.6, Single-Ended Channel 7, $Gain_{Corr}$	16
0x520	ADC 2, Gain 1.6, Single-Ended Channel 0, $Offset_{Corr}$	16
0x522	ADC 2, Gain 1.6, Single-Ended Channel 0, $Gain_{Corr}$	16
0x524	ADC 2, Gain 1.6, Single-Ended Channel 1, $Offset_{Corr}$	16
0x526	ADC 2, Gain 1.6, Single-Ended Channel 1, $Gain_{Corr}$	16
0x528	ADC 2, Gain 1.6, Single-Ended Channel 2, $Offset_{Corr}$	16
0x52A	ADC 2, Gain 1.6, Single-Ended Channel 2, $Gain_{Corr}$	16
0x52C	ADC 2, Gain 1.6, Single-Ended Channel 3, $Offset_{Corr}$	16
0x52E	ADC 2, Gain 1.6, Single-Ended Channel 3, $Gain_{Corr}$	16
0x530	ADC 2, Gain 1.6, Single-Ended Channel 4, $Offset_{Corr}$	16
0x532	ADC 2, Gain 1.6, Single-Ended Channel 4, $Gain_{Corr}$	16
0x534	ADC 2, Gain 1.6, Single-Ended Channel 5, $Offset_{Corr}$	16
0x536	ADC 2, Gain 1.6, Single-Ended Channel 5, $Gain_{Corr}$	16
0x538	ADC 2, Gain 1.6, Single-Ended Channel 6, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x53A	ADC 2, Gain 1.6, Single-Ended Channel 6, $Gain_{Corr}$	16
0x53C	ADC 2, Gain 1.6, Single-Ended Channel 7, $Offset_{Corr}$	16
0x53E	ADC 2, Gain 1.6, Single-Ended Channel 7, $Gain_{Corr}$	16
0x540	ADC 3, Gain 1.6, Single-Ended Channel 0, $Offset_{Corr}$	16
0x542	ADC 3, Gain 1.6, Single-Ended Channel 0, $Gain_{Corr}$	16
0x544	ADC 3, Gain 1.6, Single-Ended Channel 1, $Offset_{Corr}$	16
0x546	ADC 3, Gain 1.6, Single-Ended Channel 1, $Gain_{Corr}$	16
0x548	ADC 3, Gain 1.6, Single-Ended Channel 2, $Offset_{Corr}$	16
0x54A	ADC 3, Gain 1.6, Single-Ended Channel 2, $Gain_{Corr}$	16
0x54C	ADC 3, Gain 1.6, Single-Ended Channel 3, $Offset_{Corr}$	16
0x54E	ADC 3, Gain 1.6, Single-Ended Channel 3, $Gain_{Corr}$	16
0x550	ADC 3, Gain 1.6, Single-Ended Channel 4, $Offset_{Corr}$	16
0x552	ADC 3, Gain 1.6, Single-Ended Channel 4, $Gain_{Corr}$	16
0x554	ADC 3, Gain 1.6, Single-Ended Channel 5, $Offset_{Corr}$	16
0x556	ADC 3, Gain 1.6, Single-Ended Channel 5, $Gain_{Corr}$	16
0x558	ADC 3, Gain 1.6, Single-Ended Channel 6, $Offset_{Corr}$	16
0x55A	ADC 3, Gain 1.6, Single-Ended Channel 6, $Gain_{Corr}$	16
0x55C	ADC 3, Gain 1.6, Single-Ended Channel 7, $Offset_{Corr}$	16
0x55E	ADC 3, Gain 1.6, Single-Ended Channel 7, $Gain_{Corr}$	16
0x560	ADC 4, Gain 1.6, Single-Ended Channel 0, $Offset_{Corr}$	16
0x562	ADC 4, Gain 1.6, Single-Ended Channel 0, $Gain_{Corr}$	16
0x564	ADC 4, Gain 1.6, Single-Ended Channel 1, $Offset_{Corr}$	16
0x566	ADC 4, Gain 1.6, Single-Ended Channel 1, $Gain_{Corr}$	16
0x568	ADC 4, Gain 1.6, Single-Ended Channel 2, $Offset_{Corr}$	16
0x54A	ADC 4, Gain 1.6, Single-Ended Channel 2, $Gain_{Corr}$	16
0x56C	ADC 4, Gain 1.6, Single-Ended Channel 3, $Offset_{Corr}$	16
0x56E	ADC 4, Gain 1.6, Single-Ended Channel 3, $Gain_{Corr}$	16
0x570	ADC 4, Gain 1.6, Single-Ended Channel 4, $Offset_{Corr}$	16
0x572	ADC 4, Gain 1.6, Single-Ended Channel 4, $Gain_{Corr}$	16
0x574	ADC 4, Gain 1.6, Single-Ended Channel 5, $Offset_{Corr}$	16
0x576	ADC 4, Gain 1.6, Single-Ended Channel 5, $Gain_{Corr}$	16
0x578	ADC 4, Gain 1.6, Single-Ended Channel 6, $Offset_{Corr}$	16
0x57A	ADC 4, Gain 1.6, Single-Ended Channel 6, $Gain_{Corr}$	16
0x57C	ADC 4, Gain 1.6, Single-Ended Channel 7, $Offset_{Corr}$	16
0x57E	ADC 4, Gain 1.6, Single-Ended Channel 7, $Gain_{Corr}$	16
A/D Range ADC Gain 3.2 Single-Ended High-Voltage Input Range: N/A Current Input Range: N/A		
0x580	ADC 1, Gain 3.2, Single-Ended Channel 0, $Offset_{Corr}$	16
0x582	ADC 1, Gain 3.2, Single-Ended Channel 0, $Gain_{Corr}$	16
0x584	ADC 1, Gain 3.2, Single-Ended Channel 1, $Offset_{Corr}$	16
0x586	ADC 1, Gain 3.2, Single-Ended Channel 1, $Gain_{Corr}$	16
0x588	ADC 1, Gain 3.2, Single-Ended Channel 2, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x58A	ADC 1, Gain 3.2, Single-Ended Channel 2, $Gain_{Corr}$	16
0x58C	ADC 1, Gain 3.2, Single-Ended Channel 3, $Offset_{Corr}$	16
0x58E	ADC 1, Gain 3.2, Single-Ended Channel 3, $Gain_{Corr}$	16
0x590	ADC 1, Gain 3.2, Single-Ended Channel 4, $Offset_{Corr}$	16
0x592	ADC 1, Gain 3.2, Single-Ended Channel 4, $Gain_{Corr}$	16
0x594	ADC 1, Gain 3.2, Single-Ended Channel 5, $Offset_{Corr}$	16
0x596	ADC 1, Gain 3.2, Single-Ended Channel 5, $Gain_{Corr}$	16
0x598	ADC 1, Gain 3.2, Single-Ended Channel 6, $Offset_{Corr}$	16
0x59A	ADC 1, Gain 3.2, Single-Ended Channel 6, $Gain_{Corr}$	16
0x59C	ADC 1, Gain 3.2, Single-Ended Channel 7, $Offset_{Corr}$	16
0x59E	ADC 1, Gain 3.2, Single-Ended Channel 7, $Gain_{Corr}$	16
0x5A0	ADC 2, Gain 3.2, Single-Ended Channel 0, $Offset_{Corr}$	16
0x5A2	ADC 2, Gain 3.2, Single-Ended Channel 0, $Gain_{Corr}$	16
0x5A4	ADC 2, Gain 3.2, Single-Ended Channel 1, $Offset_{Corr}$	16
0x5A6	ADC 2, Gain 3.2, Single-Ended Channel 1, $Gain_{Corr}$	16
0x5A8	ADC 2, Gain 3.2, Single-Ended Channel 2, $Offset_{Corr}$	16
0x5AA	ADC 2, Gain 3.2, Single-Ended Channel 2, $Gain_{Corr}$	16
0x5AC	ADC 2, Gain 3.2, Single-Ended Channel 3, $Offset_{Corr}$	16
0x5AE	ADC 2, Gain 3.2, Single-Ended Channel 3, $Gain_{Corr}$	16
0x5B0	ADC 2, Gain 3.2, Single-Ended Channel 4, $Offset_{Corr}$	16
0x5B2	ADC 2, Gain 3.2, Single-Ended Channel 4, $Gain_{Corr}$	16
0x5B4	ADC 2, Gain 3.2, Single-Ended Channel 5, $Offset_{Corr}$	16
0x5B6	ADC 2, Gain 3.2, Single-Ended Channel 5, $Gain_{Corr}$	16
0x5B8	ADC 2, Gain 3.2, Single-Ended Channel 6, $Offset_{Corr}$	16
0x5BA	ADC 2, Gain 3.2, Single-Ended Channel 6, $Gain_{Corr}$	16
0x5BC	ADC 2, Gain 3.2, Single-Ended Channel 7, $Offset_{Corr}$	16
0x5BE	ADC 2, Gain 3.2, Single-Ended Channel 7, $Gain_{Corr}$	16
0x5C0	ADC 3, Gain 3.2, Single-Ended Channel 0, $Offset_{Corr}$	16
0x5C2	ADC 3, Gain 3.2, Single-Ended Channel 0, $Gain_{Corr}$	16
0x5C4	ADC 3, Gain 3.2, Single-Ended Channel 1, $Offset_{Corr}$	16
0x5C6	ADC 3, Gain 3.2, Single-Ended Channel 1, $Gain_{Corr}$	16
0x5C8	ADC 3, Gain 3.2, Single-Ended Channel 2, $Offset_{Corr}$	16
0x5CA	ADC 3, Gain 3.2, Single-Ended Channel 2, $Gain_{Corr}$	16
0x5CC	ADC 3, Gain 3.2, Single-Ended Channel 3, $Offset_{Corr}$	16
0x5CE	ADC 3, Gain 3.2, Single-Ended Channel 3, $Gain_{Corr}$	16
0x5D0	ADC 3, Gain 3.2, Single-Ended Channel 4, $Offset_{Corr}$	16
0x5D2	ADC 3, Gain 3.2, Single-Ended Channel 4, $Gain_{Corr}$	16
0x5D4	ADC 3, Gain 3.2, Single-Ended Channel 5, $Offset_{Corr}$	16
0x5D6	ADC 3, Gain 3.2, Single-Ended Channel 5, $Gain_{Corr}$	16
0x5D8	ADC 3, Gain 3.2, Single-Ended Channel 6, $Offset_{Corr}$	16
0x5DA	ADC 3, Gain 3.2, Single-Ended Channel 6, $Gain_{Corr}$	16
0x5DC	ADC 3, Gain 3.2, Single-Ended Channel 7, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x5DE	ADC 3, Gain 3.2, Single-Ended Channel 7, $Gain_{Corr}$	16
0x5E0	ADC 4, Gain 3.2, Single-Ended Channel 0, $Offset_{Corr}$	16
0x5E2	ADC 4, Gain 3.2, Single-Ended Channel 0, $Gain_{Corr}$	16
0x5E4	ADC 4, Gain 3.2, Single-Ended Channel 1, $Offset_{Corr}$	16
0x5E6	ADC 4, Gain 3.2, Single-Ended Channel 1, $Gain_{Corr}$	16
0x5E8	ADC 4, Gain 3.2, Single-Ended Channel 2, $Offset_{Corr}$	16
0x5EA	ADC 4, Gain 3.2, Single-Ended Channel 2, $Gain_{Corr}$	16
0x5EC	ADC 4, Gain 3.2, Single-Ended Channel 3, $Offset_{Corr}$	16
0x5EE	ADC 4, Gain 3.2, Single-Ended Channel 3, $Gain_{Corr}$	16
0x5F0	ADC 4, Gain 3.2, Single-Ended Channel 4, $Offset_{Corr}$	16
0x5F2	ADC 4, Gain 3.2, Single-Ended Channel 4, $Gain_{Corr}$	16
0x5F4	ADC 4, Gain 3.2, Single-Ended Channel 5, $Offset_{Corr}$	16
0x5F6	ADC 4, Gain 3.2, Single-Ended Channel 5, $Gain_{Corr}$	16
0x5F8	ADC 4, Gain 3.2, Single-Ended Channel 6, $Offset_{Corr}$	16
0x5FA	ADC 4, Gain 3.2, Single-Ended Channel 6, $Gain_{Corr}$	16
0x5FC	ADC 4, Gain 3.2, Single-Ended Channel 7, $Offset_{Corr}$	16
0x5FE	ADC 4, Gain 3.2, Single-Ended Channel 7, $Gain_{Corr}$	16
A/D Range ADC Gain 6.4 Single-Ended High-Voltage Input Range: N/A Current Input Range: N/A		
0x600	ADC 1, Gain 6.4, Single-Ended Channel 0, $Offset_{Corr}$	16
0x602	ADC 1, Gain 6.4, Single-Ended Channel 0, $Gain_{Corr}$	16
0x604	ADC 1, Gain 6.4, Single-Ended Channel 1, $Offset_{Corr}$	16
0x606	ADC 1, Gain 6.4, Single-Ended Channel 1, $Gain_{Corr}$	16
0x608	ADC 1, Gain 6.4, Single-Ended Channel 2, $Offset_{Corr}$	16
0x60A	ADC 1, Gain 6.4, Single-Ended Channel 2, $Gain_{Corr}$	16
0x60C	ADC 1, Gain 6.4, Single-Ended Channel 3, $Offset_{Corr}$	16
0x60E	ADC 1, Gain 6.4, Single-Ended Channel 3, $Gain_{Corr}$	16
0x610	ADC 1, Gain 6.4, Single-Ended Channel 4, $Offset_{Corr}$	16
0x612	ADC 1, Gain 6.4, Single-Ended Channel 4, $Gain_{Corr}$	16
0x614	ADC 1, Gain 6.4, Single-Ended Channel 5, $Offset_{Corr}$	16
0x616	ADC 1, Gain 6.4, Single-Ended Channel 5, $Gain_{Corr}$	16
0x618	ADC 1, Gain 6.4, Single-Ended Channel 6, $Offset_{Corr}$	16
0x61A	ADC 1, Gain 6.4, Single-Ended Channel 6, $Gain_{Corr}$	16
0x61C	ADC 1, Gain 6.4, Single-Ended Channel 7, $Offset_{Corr}$	16
0x61E	ADC 1, Gain 6.4, Single-Ended Channel 7, $Gain_{Corr}$	16
0x620	ADC 2, Gain 6.4, Single-Ended Channel 0, $Offset_{Corr}$	16
0x622	ADC 2, Gain 6.4, Single-Ended Channel 0, $Gain_{Corr}$	16
0x624	ADC 2, Gain 6.4, Single-Ended Channel 1, $Offset_{Corr}$	16
0x626	ADC 2, Gain 6.4, Single-Ended Channel 1, $Gain_{Corr}$	16
0x628	ADC 2, Gain 6.4, Single-Ended Channel 2, $Offset_{Corr}$	16
0x62A	ADC 2, Gain 6.4, Single-Ended Channel 2, $Gain_{Corr}$	16
0x62C	ADC 2, Gain 6.4, Single-Ended Channel 3, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x62E	ADC 2, Gain 6.4, Single-Ended Channel 3, $Gain_{Corr}$	16
0x630	ADC 2, Gain 6.4, Single-Ended Channel 4, $Offset_{Corr}$	16
0x632	ADC 2, Gain 6.4, Single-Ended Channel 4, $Gain_{Corr}$	16
0x634	ADC 2, Gain 6.4, Single-Ended Channel 5, $Offset_{Corr}$	16
0x636	ADC 2, Gain 6.4, Single-Ended Channel 5, $Gain_{Corr}$	16
0x638	ADC 2, Gain 6.4, Single-Ended Channel 6, $Offset_{Corr}$	16
0x63A	ADC 2, Gain 6.4, Single-Ended Channel 6, $Gain_{Corr}$	16
0x63C	ADC 2, Gain 6.4, Single-Ended Channel 7, $Offset_{Corr}$	16
0x63E	ADC 2, Gain 6.4, Single-Ended Channel 7, $Gain_{Corr}$	16
0x640	ADC 3, Gain 6.4, Single-Ended Channel 0, $Offset_{Corr}$	16
0x642	ADC 3, Gain 6.4, Single-Ended Channel 0, $Gain_{Corr}$	16
0x644	ADC 3, Gain 6.4, Single-Ended Channel 1, $Offset_{Corr}$	16
0x646	ADC 3, Gain 6.4, Single-Ended Channel 1, $Gain_{Corr}$	16
0x648	ADC 3, Gain 6.4, Single-Ended Channel 2, $Offset_{Corr}$	16
0x64A	ADC 3, Gain 6.4, Single-Ended Channel 2, $Gain_{Corr}$	16
0x64C	ADC 3, Gain 6.4, Single-Ended Channel 3, $Offset_{Corr}$	16
0x64E	ADC 3, Gain 6.4, Single-Ended Channel 3, $Gain_{Corr}$	16
0x650	ADC 3, Gain 6.4, Single-Ended Channel 4, $Offset_{Corr}$	16
0x652	ADC 3, Gain 6.4, Single-Ended Channel 4, $Gain_{Corr}$	16
0x654	ADC 3, Gain 6.4, Single-Ended Channel 5, $Offset_{Corr}$	16
0x656	ADC 3, Gain 6.4, Single-Ended Channel 5, $Gain_{Corr}$	16
0x658	ADC 3, Gain 6.4, Single-Ended Channel 6, $Offset_{Corr}$	16
0x65A	ADC 3, Gain 6.4, Single-Ended Channel 6, $Gain_{Corr}$	16
0x65C	ADC 3, Gain 6.4, Single-Ended Channel 7, $Offset_{Corr}$	16
0x65E	ADC 3, Gain 6.4, Single-Ended Channel 7, $Gain_{Corr}$	16
0x660	ADC 4, Gain 6.4, Single-Ended Channel 0, $Offset_{Corr}$	16
0x662	ADC 4, Gain 6.4, Single-Ended Channel 0, $Gain_{Corr}$	16
0x664	ADC 4, Gain 6.4, Single-Ended Channel 1, $Offset_{Corr}$	16
0x666	ADC 4, Gain 6.4, Single-Ended Channel 1, $Gain_{Corr}$	16
0x668	ADC 4, Gain 6.4, Single-Ended Channel 2, $Offset_{Corr}$	16
0x66A	ADC 4, Gain 6.4, Single-Ended Channel 2, $Gain_{Corr}$	16
0x66C	ADC 4, Gain 6.4, Single-Ended Channel 3, $Offset_{Corr}$	16
0x66E	ADC 4, Gain 6.4, Single-Ended Channel 3, $Gain_{Corr}$	16
0x670	ADC 4, Gain 6.4, Single-Ended Channel 4, $Offset_{Corr}$	16
0x672	ADC 4, Gain 6.4, Single-Ended Channel 4, $Gain_{Corr}$	16
0x674	ADC 4, Gain 6.4, Single-Ended Channel 5, $Offset_{Corr}$	16
0x676	ADC 4, Gain 6.4, Single-Ended Channel 5, $Gain_{Corr}$	16
0x678	ADC 4, Gain 6.4, Single-Ended Channel 6, $Offset_{Corr}$	16
0x67A	ADC 4, Gain 6.4, Single-Ended Channel 6, $Gain_{Corr}$	16
0x67C	ADC 4, Gain 6.4, Single-Ended Channel 7, $Offset_{Corr}$	16
0x67E	ADC 4, Gain 6.4, Single-Ended Channel 7, $Gain_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
D/A Range 0…+5V		
0x680	DAC 1 Channel A, 0V … 5V Range, $Offset_{Corr}$	16
0x682	DAC 1 Channel A, 0V … 5V Range, $Gain_{Corr}$	16
0x684	DAC 1 Channel B, 0V … 5V Range, $Offset_{Corr}$	16
0x686	DAC 1 Channel B, 0V … 5V Range, $Gain_{Corr}$	16
0x688	DAC 1 Channel C, 0V … 5V Range, $Offset_{Corr}$	16
0x68A	DAC 1 Channel C, 0V … 5V Range, $Gain_{Corr}$	16
0x68C	DAC 1 Channel D, 0V … 5V Range, $Offset_{Corr}$	16
0x68E	DAC 1 Channel D, 0V … 5V Range, $Gain_{Corr}$	16
0x690	DAC 2 Channel A, 0V … 5V Range, $Offset_{Corr}$	16
0x692	DAC 2 Channel A, 0V … 5V Range, $Gain_{Corr}$	16
0x694	DAC 2 Channel B, 0V … 5V Range, $Offset_{Corr}$	16
0x696	DAC 2 Channel B, 0V … 5V Range, $Gain_{Corr}$	16
0x698	DAC 2 Channel C, 0V … 5V Range, $Offset_{Corr}$	16
0x69A	DAC 2 Channel C, 0V … 5V Range, $Gain_{Corr}$	16
0x69C	DAC 2 Channel D, 0V … 5V Range, $Offset_{Corr}$	16
0x69E	DAC 2 Channel D, 0V … 5V Range, $Gain_{Corr}$	16
D/A Range 0…+6V		
0x6A0	DAC 1 Channel A, 0V … 6V Range, $Offset_{Corr}$	16
0x6A2	DAC 1 Channel A, 0V … 6V Range, $Gain_{Corr}$	16
0x6A4	DAC 1 Channel B, 0V … 6V Range, $Offset_{Corr}$	16
0x6A6	DAC 1 Channel B, 0V … 6V Range, $Gain_{Corr}$	16
0x6A8	DAC 1 Channel C, 0V … 6V Range, $Offset_{Corr}$	16
0x6AA	DAC 1 Channel C, 0V … 6V Range, $Gain_{Corr}$	16
0x6AC	DAC 1 Channel D, 0V … 6V Range, $Offset_{Corr}$	16
0x6AE	DAC 1 Channel D, 0V … 6V Range, $Gain_{Corr}$	16
0x6B0	DAC 2 Channel A, 0V … 6V Range, $Offset_{Corr}$	16
0x6B2	DAC 2 Channel A, 0V … 6V Range, $Gain_{Corr}$	16
0x6B4	DAC 2 Channel B, 0V … 6V Range, $Offset_{Corr}$	16
0x6B6	DAC 2 Channel B, 0V … 6V Range, $Gain_{Corr}$	16
0x6B8	DAC 2 Channel C, 0V … 6V Range, $Offset_{Corr}$	16
0x6BA	DAC 2 Channel C, 0V … 6V Range, $Gain_{Corr}$	16
0x6BC	DAC 2 Channel D, 0V … 6V Range, $Offset_{Corr}$	16
0x6BE	DAC 2 Channel D, 0V … 6V Range, $Gain_{Corr}$	16
D/A Range 0…+10V		
0x6C0	DAC 1 Channel A, 0V … 10V Range, $Offset_{Corr}$	16
0x6C2	DAC 1 Channel A, 0V … 10V Range, $Gain_{Corr}$	16
0x6C4	DAC 1 Channel B, 0V … 10V Range, $Offset_{Corr}$	16
0x6C6	DAC 1 Channel B, 0V … 10V Range, $Gain_{Corr}$	16
0x6C8	DAC 1 Channel C, 0V … 10V Range, $Offset_{Corr}$	16
0x6CA	DAC 1 Channel C, 0V … 10V Range, $Gain_{Corr}$	16
0x6CC	DAC 1 Channel D, 0V … 10V Range, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x6CE	DAC 1 Channel D, 0V … 10V Range, $Gain_{Corr}$	16
0x6D0	DAC 2 Channel A, 0V … 10V Range, $Offset_{Corr}$	16
0x6D2	DAC 2 Channel A, 0V … 10V Range, $Gain_{Corr}$	16
0x6D4	DAC 2 Channel B, 0V … 10V Range, $Offset_{Corr}$	16
0x6D6	DAC 2 Channel B, 0V … 10V Range, $Gain_{Corr}$	16
0x6D8	DAC 2 Channel C, 0V … 10V Range, $Offset_{Corr}$	16
0x6DA	DAC 2 Channel C, 0V … 10V Range, $Gain_{Corr}$	16
0x6DC	DAC 2 Channel D, 0V … 10V Range, $Offset_{Corr}$	16
0x6DE	DAC 2 Channel D, 0V … 10V Range, $Gain_{Corr}$	16
D/A Range 0…+12V		
0x6E0	DAC 1 Channel A, 0V … 12V Range, $Offset_{Corr}$	16
0x6E2	DAC 1 Channel A, 0V … 12V Range, $Gain_{Corr}$	16
0x6E4	DAC 1 Channel B, 0V … 12V Range, $Offset_{Corr}$	16
0x6E6	DAC 1 Channel B, 0V … 12V Range, $Gain_{Corr}$	16
0x6E8	DAC 1 Channel C, 0V … 12V Range, $Offset_{Corr}$	16
0x6EA	DAC 1 Channel C, 0V … 12V Range, $Gain_{Corr}$	16
0x6EC	DAC 1 Channel D, 0V … 12V Range, $Offset_{Corr}$	16
0x6EE	DAC 1 Channel D, 0V … 12V Range, $Gain_{Corr}$	16
0x6F0	DAC 2 Channel A, 0V … 12V Range, $Offset_{Corr}$	16
0x6F2	DAC 2 Channel A, 0V … 12V Range, $Gain_{Corr}$	16
0x6F4	DAC 2 Channel B, 0V … 12V Range, $Offset_{Corr}$	16
0x6F6	DAC 2 Channel B, 0V … 12V Range, $Gain_{Corr}$	16
0x6F8	DAC 2 Channel C, 0V … 12V Range, $Offset_{Corr}$	16
0x6FA	DAC 2 Channel C, 0V … 12V Range, $Gain_{Corr}$	16
0x6FC	DAC 2 Channel D, 0V … 12V Range, $Offset_{Corr}$	16
0x6FE	DAC 2 Channel D, 0V … 12V Range, $Gain_{Corr}$	16
D/A Range +/- 5V		
0x700	DAC 1 Channel A, -5V … +5V Range, $Offset_{Corr}$	16
0x702	DAC 1 Channel A, -5V … +5V Range, $Gain_{Corr}$	16
0x704	DAC 1 Channel B, -5V … +5V Range, $Offset_{Corr}$	16
0x706	DAC 1 Channel B, -5V … +5V Range, $Gain_{Corr}$	16
0x708	DAC 1 Channel C, -5V … +5V Range, $Offset_{Corr}$	16
0x70A	DAC 1 Channel C, -5V … +5V Range, $Gain_{Corr}$	16
0x70C	DAC 1 Channel D, -5V … +5V Range, $Offset_{Corr}$	16
0x70E	DAC 1 Channel D, -5V … +5V Range, $Gain_{Corr}$	16
0x710	DAC 2 Channel A, -5V … +5V Range, $Offset_{Corr}$	16
0x712	DAC 2 Channel A, -5V … +5V Range, $Gain_{Corr}$	16
0x714	DAC 2 Channel B, -5V … +5V Range, $Offset_{Corr}$	16
0x716	DAC 2 Channel B, -5V … +5V Range, $Gain_{Corr}$	16
0x718	DAC 2 Channel C, -5V … +5V Range, $Offset_{Corr}$	16
0x71A	DAC 2 Channel C, -5V … +5V Range, $Gain_{Corr}$	16
0x71C	DAC 2 Channel D, -5V … +5V Range, $Offset_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x71E	DAC 2 Channel D, -5V … +5V Range, $Gain_{Corr}$	16
D/A Range +/- 6V		
0x720	DAC 1 Channel A, -6V … +6V Range, $Offset_{Corr}$	16
0x722	DAC 1 Channel A, -6V … +6V Range, $Gain_{Corr}$	16
0x724	DAC 1 Channel B, -6V … +6V Range, $Offset_{Corr}$	16
0x726	DAC 1 Channel B, -6V … +6V Range, $Gain_{Corr}$	16
0x728	DAC 1 Channel C, -6V … +6V Range, $Offset_{Corr}$	16
0x72A	DAC 1 Channel C, -6V … +6V Range, $Gain_{Corr}$	16
0x72C	DAC 1 Channel D, -6V … +6V Range, $Offset_{Corr}$	16
0x72E	DAC 1 Channel D, -6V … +6V Range, $Gain_{Corr}$	16
0x730	DAC 2 Channel A, -6V … +6V Range, $Offset_{Corr}$	16
0x732	DAC 2 Channel A, -6V … +6V Range, $Gain_{Corr}$	16
0x734	DAC 2 Channel B, -6V … +6V Range, $Offset_{Corr}$	16
0x736	DAC 2 Channel B, -6V … +6V Range, $Gain_{Corr}$	16
0x738	DAC 2 Channel C, -6V … +6V Range, $Offset_{Corr}$	16
0x73A	DAC 2 Channel C, -6V … +6V Range, $Gain_{Corr}$	16
0x73C	DAC 2 Channel D, -6V … +6V Range, $Offset_{Corr}$	16
0x73E	DAC 2 Channel D, -6V … +6V Range, $Gain_{Corr}$	16
D/A Range +/- 10V		
0x740	DAC 1 Channel A, -10V … +10V Range, $Offset_{Corr}$	16
0x742	DAC 1 Channel A, -10V … +10V Range, $Gain_{Corr}$	16
0x744	DAC 1 Channel B, -10V … +10V Range, $Offset_{Corr}$	16
0x746	DAC 1 Channel B, -10V … +10V Range, $Gain_{Corr}$	16
0x748	DAC 1 Channel C, -10V … +10V Range, $Offset_{Corr}$	16
0x74A	DAC 1 Channel C, -10V … +10V Range, $Gain_{Corr}$	16
0x74C	DAC 1 Channel D, -10V … +10V Range, $Offset_{Corr}$	16
0x74E	DAC 1 Channel D, -10V … +10V Range, $Gain_{Corr}$	16
0x750	DAC 2 Channel A, -10V … +10V Range, $Offset_{Corr}$	16
0x752	DAC 2 Channel A, -10V … +10V Range, $Gain_{Corr}$	16
0x754	DAC 2 Channel B, -10V … +10V Range, $Offset_{Corr}$	16
0x756	DAC 2 Channel B, -10V … +10V Range, $Gain_{Corr}$	16
0x758	DAC 2 Channel C, -10V … +10V Range, $Offset_{Corr}$	16
0x75A	DAC 2 Channel C, -10V … +10V Range, $Gain_{Corr}$	16
0x75C	DAC 2 Channel D, -10V … +10V Range, $Offset_{Corr}$	16
0x75E	DAC 2 Channel D, -10V … +10V Range, $Gain_{Corr}$	16
D/A Range +/- 12V		
0x760	DAC 1 Channel A, -12V … +12V Range, $Offset_{Corr}$	16
0x762	DAC 1 Channel A, -12V … +12V Range, $Gain_{Corr}$	16
0x764	DAC 1 Channel B, -12V … +12V Range, $Offset_{Corr}$	16
0x766	DAC 1 Channel B, -12V … +12V Range, $Gain_{Corr}$	16
0x768	DAC 1 Channel C, -12V … +12V Range, $Offset_{Corr}$	16
0x76A	DAC 1 Channel C, -12V … +12V Range, $Gain_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x76C	DAC 1 Channel D, -12V … +12V Range, $Offset_{Corr}$	16
0x76E	DAC 1 Channel D, -12V … +12V Range, $Gain_{Corr}$	16
0x770	DAC 2 Channel A, -12V … +12V Range, $Offset_{Corr}$	16
0x772	DAC 2 Channel A, -12V … +12V Range, $Gain_{Corr}$	16
0x774	DAC 2 Channel B, -12V … +12V Range, $Offset_{Corr}$	16
0x776	DAC 2 Channel B, -12V … +12V Range, $Gain_{Corr}$	16
0x778	DAC 2 Channel C, -12V … +12V Range, $Offset_{Corr}$	16
0x77A	DAC 2 Channel C, -12V … +12V Range, $Gain_{Corr}$	16
0x77C	DAC 2 Channel D, -12V … +12V Range, $Offset_{Corr}$	16
0x77E	DAC 2 Channel D, -12V … +12V Range, $Gain_{Corr}$	16
D/A Range 4mA … 20mA		
0x780	DAC 1 Channel A, 4mA … 20mA Range, $Offset_{Corr}$	16
0x782	DAC 1 Channel A, 4mA … 20mA Range, $Gain_{Corr}$	16
0x784	DAC 1 Channel B, 4mA … 20mA Range, $Offset_{Corr}$	16
0x7	DAC 1 Channel B, 4mA … 20mA Range, $Gain_{Corr}$	16
0x7	DAC 1 Channel C, 4mA … 20mA Range, $Offset_{Corr}$	16
0x7	DAC 1 Channel C, 4mA … 20mA Range, $Gain_{Corr}$	16
0x7	DAC 1 Channel D, 4mA … 20mA Range, $Offset_{Corr}$	16
0x7	DAC 1 Channel D, 4mA … 20mA Range, $Gain_{Corr}$	16
0x7	DAC 2 Channel A, 4mA … 20mA Range, $Offset_{Corr}$	16
0x7	DAC 2 Channel A, 4mA … 20mA Range, $Gain_{Corr}$	16
0x7	DAC 2 Channel B, 4mA … 20mA Range, $Offset_{Corr}$	16
0x7	DAC 2 Channel B, 4mA … 20mA Range, $Gain_{Corr}$	16
0x7	DAC 2 Channel C, 4mA … 20mA Range, $Offset_{Corr}$	16
0x7	DAC 2 Channel C, 4mA … 20mA Range, $Gain_{Corr}$	16
0x7	DAC 2 Channel D, 4mA … 20mA Range, $Offset_{Corr}$	16
0x7	DAC 2 Channel D, 4mA … 20mA Range, $Gain_{Corr}$	16
D/A Range 0mA … 20mA		
0x7A0	DAC 1 Channel A, 0mA … 20mA Range, $Offset_{Corr}$	16
0x7A2	DAC 1 Channel A, 0mA … 20mA Range, $Gain_{Corr}$	16
0x7A4	DAC 1 Channel B, 0mA … 20mA Range, $Offset_{Corr}$	16
0x7A6	DAC 1 Channel B, 0mA … 20mA Range, $Gain_{Corr}$	16
0x7A8	DAC 1 Channel C, 0mA … 20mA Range, $Offset_{Corr}$	16
0x7AA	DAC 1 Channel C, 0mA … 20mA Range, $Gain_{Corr}$	16
0x7AC	DAC 1 Channel D, 0mA … 20mA Range, $Offset_{Corr}$	16
0x7AE	DAC 1 Channel D, 0mA … 20mA Range, $Gain_{Corr}$	16
0x7B0	DAC 2 Channel A, 0mA … 20mA Range, $Offset_{Corr}$	16
0x7B2	DAC 2 Channel A, 0mA … 20mA Range, $Gain_{Corr}$	16
0x7B4	DAC 2 Channel B, 0mA … 20mA Range, $Offset_{Corr}$	16
0x7B6	DAC 2 Channel B, 0mA … 20mA Range, $Gain_{Corr}$	16
0x7B8	DAC 2 Channel C, 0mA … 20mA Range, $Offset_{Corr}$	16
0x7BA	DAC 2 Channel C, 0mA … 20mA Range, $Gain_{Corr}$	16

PCI BAR 0 Offset	Description	Size (Bit)
0x7BC	DAC 2 Channel D, 0mA … 20mA Range, $Offset_{Corr}$	16
0x7BE	DAC 2 Channel D, 0mA … 20mA Range, $Gain_{Corr}$	16
D/A Range 0mA … 24mA		
0x7C0	DAC 1 Channel A, 0mA … 24mA Range, $Offset_{Corr}$	16
0x7C2	DAC 1 Channel A, 0mA … 24mA Range, $Gain_{Corr}$	16
0x7C4	DAC 1 Channel B, 0mA … 24mA Range, $Offset_{Corr}$	16
0x7C6	DAC 1 Channel B, 0mA … 24mA Range, $Gain_{Corr}$	16
0x7C8	DAC 1 Channel C, 0mA … 24mA Range, $Offset_{Corr}$	16
0x7CA	DAC 1 Channel C, 0mA … 24mA Range, $Gain_{Corr}$	16
0x7CC	DAC 1 Channel D, 0mA … 24mA Range, $Offset_{Corr}$	16
0x7CE	DAC 1 Channel D, 0mA … 24mA Range, $Gain_{Corr}$	16
0x7D0	DAC 2 Channel A, 0mA … 24mA Range, $Offset_{Corr}$	16
0x7D2	DAC 2 Channel A, 0mA … 24mA Range, $Gain_{Corr}$	16
0x7D4	DAC 2 Channel B, 0mA … 24mA Range, $Offset_{Corr}$	16
0x7D6	DAC 2 Channel B, 0mA … 24mA Range, $Gain_{Corr}$	16
0x7D8	DAC 2 Channel C, 0mA … 24mA Range, $Offset_{Corr}$	16
0x7DA	DAC 2 Channel C, 0mA … 24mA Range, $Gain_{Corr}$	16
0x7DC	DAC 2 Channel D, 0mA … 24mA Range, $Offset_{Corr}$	16
0x7DE	DAC 2 Channel D, 0mA … 24mA Range, $Gain_{Corr}$	16
Other		
0x7E0	Reference Value #0: Standard-Voltage = 4096 (max pos. FS value in mV is 4096/0.166… = 24576mV)	16
0x7E2	Reference Value #1: High-Voltage = 16430 (max pos. FS value in mV is 16430/0.166… = 98580mV)	16
0x7E4	Reference Value #2: Current = 40960 (max pos. FS value in mA is 40960/1.6 = 25600mA)	16
0x7E6	Reserved (Reference Value)	16
0x7E8	Analog Input Build-Option 2 Coding Bits for each group of 2 Differential Inputs (ADC4.DF[3:2], ADC4.DF[1:0], …, ADC1.DF[1:0]) 00: Standard-Voltage 01: High-Voltage 10: Current Input 11: Reserved TPMC543-10R: 0x55AA	16
0x7EA	Reserved (Build-Option)	
0x7EC … 0x7F8	Reserved	16
0x7FA	EEPROM Layout Version	16
0x7FC	Serial Number High Word	16
0x7FE	Serial Number Low Word	16

Table 4-6 : Correction Data Space Address Map

5 Register Description

Register Bit Access Type		Description
R	Read	The bit is readable by software.
R/W	Read/Write	The bit is readable and writeable by software.
R/C	Read/Clear	The bit is readable by software. The bit is set by firmware. Software may clear the bit by writing a '1'.
R/S	Read/Set	The bit is readable by software. Software may set this bit to '1'. The bit is cleared by firmware.

Table 5-1 : Register Bit Access Types

When reading reserved register bits, the read value is undefined.
For future software compatibility: For register write access, reserved bits shall be written '0'.

5.1 A/D Global Registers

5.1.1 Global ADC Control Register (0x000)

This register provides control options for all on-board ADC devices.

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved	-	-
19	ADC4_ RST_REQ	ADC 4 Reset Request See description for ADC1.	R/S	0
18	ADC3_ RST_REQ	ADC 3 Reset Request See description for ADC1.	R/S	0
17	ADC2_ RST_REQ	ADC 2 Reset Request See description for ADC1.	R/S	0
16	ADC1_ RST_REQ	ADC 1 Reset Request When set, performs an ADC device reset via the ADC (ADAS3022) RESET pin. After the actual reset phase, a post-reset ADC auto-configuration is performed. This bit is automatically cleared. The ADC Busy Bit in the Global ADC Status Register indicates whether the reset cycle (comprising the active ADC device reset and the post-reset-auto-configuration phase) is completed.	R/S	0
15:4	-	Reserved	-	-
3	ADC4_ CONV_REQ	ADC 4 Conversion Request See description for ADC1.	R/S	0
2	ADC3_ CONV_REQ	ADC 3 Conversion Request See description for ADC1.	R/S	0
1	ADC2_ CONV_REQ	ADC 2 Conversion Request See description for ADC1.	R/S	0
0	ADC1_ CONV_REQ	ADC 1 Conversion Request Manual Mode: Write ‘1’ to start a conversion for the active ADC Channels of ADC 1 (see ADC Configuration Register). Before requesting a conversion, the ADC 1 Busy Bit in the Global ADC Status Register should be checked to be clear. This bit is self-clearing. Sequencer Mode: This bit has no effect and is cleared immediately.	R/S	0

Table 5-2 : Global ADC Control Register (0x000)

For each manually controlled conversion event, a conversion is performed for the configured number of active channels on the ADC device. For each ADC device, channel conversion always starts with ADC channel 0 and automatically proceeds in ascending order (according to the configured number of active channels on the ADC device).

5.1.2 Global ADC Status Register (0x004)

This read only register provides status information for all on-board ADC devices.

Bit	Symbol	Description	Access	Reset Value
31:4	-	Reserved	-	-
3	ADC4_ BUSY	ADC 4 Busy See description for ADC1.	R	0
2	ADC3_ BUSY	ADC 3 Busy See description for ADC1.	R	0
1	ADC2_ BUSY	ADC 2 Busy See description for ADC1.	R	0
0	ADC1_ BUSY	ADC 1 Busy Set while • analog sampling is in progress • data is transferred from the ADC • an ADC reset and/or configuration process is in progress This bit must be read as '0' before conversion data can be read from the corresponding ADC Data Registers in manual mode.	R	0

Table 5-3 : Global ADC Status Register (0x004)

5.2 A/D Device Registers

The registers described in this section are provided per on-board ADC device.

5.2.1 ADC Configuration Register(s) (0x010, 0x054, 0x098 and 0x0DC)

There is a dedicated ADC Configuration Register for each physical ADC device.

A write to the ADC configuration register logs an internal request for writing the current configuration data to the appropriate ADC device (via the ADC serial interface) as soon as possible. If not already set, the ADC Busy bit in the Global ADC Status Register is set and remains so until the configuration data transfer to the ADC device is done.

The content of this register is also used for the post-reset ADC auto-configuration after a manual ADC reset via the Global ADC Control Register.

This register is intended for initial ADC device configuration.

Each ADC device must be configured before use.

ADC device configuration should be performed while the ADC is configured for Manual Mode and not busy.

After writing the ADC Configuration Register, the ADC Busy Bit in the Global ADC Status Register should be monitored until it is clear again.

Note that all channels of an ADC device are always operating in the same general input mode (Single-Ended or Differential). There is no per channel SE/DF configuration.

The number of active ADC channels has an impact on the maximum A/D conversion rate and on the host memory data buffer structure in Sequencer Mode.

5.2.1.1 TPMC543-10R

5.2.1.1.1 ADC1 (0x010), ADC2 (0x054)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27	ADCx_ IN_ MODE	ADC Input Mode 0: Differential Mode (4 Channels) This bit sets the general ADC device input mode. In Differential Mode the ADC device provides 4 differential input channels 0 to 3. **Must be cleared by software for TPMC543-10R ADC1 & ADC2!**	R/W	1
26:24	ADCx_ NUM_ ACT_ CH	Number of active ADC channels per Conversion Event The active channel set always begins with ADC channel 0 and proceeds in ascending order. The maximum number of active ADC channels in Differential Mode is 4. Differential Mode (DF): Bit 26 is Don't Care (-) -00 : 1 ADC Channel (ADC Channel 0) -01: 2 ADC Channels (ADC Channels 0-1) -10: 3 ADC Channels (ADC Channels 0-2) -11: 4 ADC Channels (ADC Channels 0-3)	R/W	111

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>23:21</td><td>ADCx_ IR_CH7</td><td>Not applicable for TPMC543-10R ADC1 & ADC2.</td><td>R/W</td><td>111</td></tr>
<tr><td>20:18</td><td>ADCx_ IR_CH6</td><td>Not applicable for TPMC543-10R ADC1 & ADC2.</td><td>R/W</td><td>111</td></tr>
<tr><td>17:15</td><td>ADCx_ IR_CH5</td><td>Not applicable for TPMC543-10R ADC1 & ADC2.</td><td>R/W</td><td>111</td></tr>
<tr><td>14:12</td><td>ADCx_ IR_CH4</td><td>Not applicable for TPMC543-10R ADC1 & ADC2.</td><td>R/W</td><td>111</td></tr>
<tr><td>11:9</td><td>ADCx_ IR_CH3</td><td>ADC Input Range Configuration Channel 3 (DF)
See description for ADC Channel 0.</td><td>R/W</td><td>111</td></tr>
<tr><td>8:6</td><td>ADCx_ IR_CH2</td><td>ADC Input Range Configuration Channel 2 (DF)
See description for ADC Channel 0.</td><td>R/W</td><td>111</td></tr>
<tr><td>5:3</td><td>ADCx_ IR_CH1</td><td>ADC Input Range Configuration Channel 1 (DF)
See description for ADC Channel 0.</td><td>R/W</td><td>111</td></tr>
<tr><td>2:0</td><td>ADCx_ IR_CH0</td><td>ADC Input Range Configuration Channel 0 (DF)
<table><tr><th>IR</th><th>ADC Internal Gain</th><th>DF</th><th>LSB</th></tr><tr><td>011</td><td>1.6</td><td>±25mA</td><td>$\frac{78.125uV}{100\Omega}$</td></tr></table>IR: Input Range Coding
DF: Differential Mode
Must be set to 011 by software for TPMC543-10R ADC1 & ADC2 channels 0-3!</td><td>R/W</td><td>111</td></tr>
</table>

Table 5-4 : TPMC543-10R ADC1 & ADC2 Configuration Register (0x010, 0x054)

5.2.1.1.2 ADC3 (0x098), ADC4 (0x0DC)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27	ADCx_ IN_ MODE	ADC Input Mode 0: Differential Mode (4 Channels) 1: Single-Ended Mode (8 Channels) This bit sets the general ADC device input mode. In Single-Ended Mode the ADC device provides 8 single-ended input channels 0 to 7. Each channel is referenced to ground. In Differential Mode the ADC device provides 4 differential input channels 0 to 3.	R/W	1

Bit	Symbol	Description	Access	Reset Value
26:24	ADCx_ NUM_ ACT_ CH	Number of active ADC channels per Conversion Event The active channel set always begins with ADC channel 0 and proceeds in ascending order. The maximum number of active ADC channels in Single-Ended Mode is 8. The maximum number of active ADC channels in Differential Mode is 4. Single-Ended Mode (SE): 000 : 1 ADC Channel (ADC Channel 0) 001: 2 ADC Channels (ADC Channels 0-1) 010: 3 ADC Channels (ADC Channels 0-2) … 111: 8 ADC Channels (ADC Channels 0-7) Differential Mode (DF): Bit 26 is Don't Care (-) -00 : 1 ADC Channel (ADC Channel 0) -01: 2 ADC Channels (ADC Channels 0-1) -10: 3 ADC Channels (ADC Channels 0-2) -11: 4 ADC Channels (ADC Channels 0-3)	R/W	111
23:21	ADCx_ IR_CH7	ADC Input Range Configuration Channel 7 (SE) See description for ADC Channel 0.	R/W	111
20:18	ADCx_ IR_CH6	ADC Input Range Configuration Channel 6 (SE) See description for ADC Channel 0.	R/W	111
17:15	ADCx_ IR_CH5	ADC Input Range Configuration Channel 5 (SE) See description for ADC Channel 0.	R/W	111
14:12	ADCx_ IR_CH4	ADC Input Range Configuration Channel 4 (SE) See description for ADC Channel 0.	R/W	111
11:9	ADCx_ IR_CH3	ADC Input Range Configuration Channel 3 (SE, DF) See description for ADC Channel 0.	R/W	111
8:6	ADCx_ IR_CH2	ADC Input Range Configuration Channel 2 (SE, DF) See description for ADC Channel 0.	R/W	111
5:3	ADCx_ IR_CH1	ADC Input Range Configuration Channel 1 (SE, DF) See description for ADC Channel 0.	R/W	111

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>2:0</td><td>ADCx_
IR_CH0</td><td>ADC Input Range Configuration Channel 0 (SE, DF)

<table>
<tr><th>IR</th><th>ADC Internal Gain</th><th>DF</th><th>SE</th><th>LSB</th></tr>
<tr><td>000</td><td>0.166..</td><td>±96V</td><td>±48V 1)</td><td>$\frac{999}{249} \times 750uV$</td></tr>
<tr><td>111</td><td>0.2</td><td>±80V</td><td>±40V 1)</td><td>$\frac{999}{249} \times 625uV$</td></tr>
<tr><td>001</td><td>0.4</td><td>±40V</td><td>±40V</td><td>$\frac{999}{249} \times 312.5uV$</td></tr>
<tr><td>010</td><td>0.8</td><td>±20V</td><td>±20V</td><td>$\frac{999}{249} \times 156.25uV$</td></tr>
<tr><td>011</td><td>1.6</td><td>±10V</td><td>±10V</td><td>$\frac{999}{249} \times 78.125uV$</td></tr>
</table>
IR: Input Range Coding (setting 0b110 is reserved)
DF: Differential Mode, SE: Single-Ended Mode
1) 15 bit Resolution</td><td>R/W</td><td>111</td></tr>
</table>

Table 5-5 : TPMC543-10R ADC3 & ADC4 Configuration Register (0x098, 0x0DC)

5.2.2 ADC Correction Register(s) (0x018-0x034, 0x05C-0x078, 0x0A0-0x0BC, 0x0E4-0x100)

These registers are intended for performing ADC data correction.

If used, the ADC correction registers should be configured while the ADC is operating in Manual Mode and is not busy.

Leaving the ADC Correction Registers at their Reset Value (or clearing the ADC Correction Registers) leaves the ADC data values unmodified (without any ADC data correction).

There is a dedicated ADC Correction Register Set for each physical ADC device.

There is a dedicated ADC Correction Register for each ADC device channel.

Note that for ADC devices hardware-configured for analog current input, the ADC channels 0-3 are always operating in differential mode and the ADC channels 4-7 are not applicable.

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_CH0_GAIN	Gain Correction Value for ADC Channel 0 (SE, DF)	R/W	0x0000
15:0	ADCx_CH0_OFFS	Offset Correction Value for ADC Channel 0 (SE, DF)	R/W	0x0000

Table 5-6 : ADC x Correction Register Channel 0 (SE, DF)

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_CH1_GAIN	Gain Correction Value for ADC Channel 1 (SE, DF)	R/W	0x0000
15:0	ADCx_CH1_OFFS	Offset Correction Value for ADC Channel 1 (SE, DF)	R/W	0x0000

Table 5-7 : ADC x Correction Register Channel 1 (SE, DF)

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_CH2_GAIN	Gain Correction Value for ADC Channel 2 (SE, DF)	R/W	0x0000
15:0	ADCx_CH2_OFFS	Offset Correction Value for ADC Channel 2 (SE, DF)	R/W	0x0000

Table 5-8 : ADC x Correction Register Channel 2 (SE, DF)

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_CH3_GAIN	Gain Correction Value for ADC Channel 3 (SE, DF)	R/W	0x0000
15:0	ADCx_CH3_OFFS	Offset Correction Value for ADC Channel 3 (SE, DF)	R/W	0x0000

Table 5-9 : ADC x Correction Register Channel 3 (SE, DF)

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_CH4_GAIN	Gain Correction Value for ADC Channel 4 (SE)	R/W	0x0000
15:0	ADCx_CH4_OFFS	Offset Correction Value for ADC Channel 4 (SE)	R/W	0x0000

Table 5-10 : ADC x Correction Register Channel 4 (SE)

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_CH5_GAIN	Gain Correction Value for ADC Channel 5 (SE)	R/W	0x0000
15:0	ADCx_CH5_OFFS	Offset Correction Value for ADC Channel 5 (SE)	R/W	0x0000

Table 5-11 : ADC x Correction Register Channel 5 (SE)

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_CH6_GAIN	Gain Correction Value for ADC Channel 6 (SE)	R/W	0x0000
15:0	ADCx_CH6_OFFS	Offset Correction Value for ADC Channel 6 (SE)	R/W	0x0000

Table 5-12 : ADC x Correction Register Channel 6 (SE)

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_CH7_GAIN	Gain Correction Value for ADC Channel 7 (SE)	R/W	0x0000
15:0	ADCx_CH7_OFFS	Offset Correction Value for ADC Channel 7 (SE)	R/W	0x0000

Table 5-13 : ADC x Correction Register Channel 7 (SE)

To perform A/D data value hardware correction (based on factory determined correction values), the correction values corresponding to the actual ADC & channel configuration must be read from the correction data space and written to the appropriate ADC Channel Correction Registers.

Clearing a Correction Register effectively disables hardware correction for the corresponding ADC device channel (default).

5.2.3 ADC Data Register(s) (0x038-0x044, 0x07C-0x088, 0x0C0-0x0CC, 0x104-0x110)

There is a dedicated ADC Data Register Set for each physical ADC device.

These registers are used to pass the A/D conversion data in Manual Mode (these registers are also valid in Sequencer Mode, however these registers are not intended to be used in sequencer mode).

Triggering a manual conversion for an ADC device automatically gathers conversion data for all active ADC device channels (successively at a fast rate, pseudo-simultaneous). The ADC busy bit indicates the active conversion process. The conversion data is available when the ADC busy bit becomes clear again.
In Single-Ended Input Mode (SE) channels 0-7 are available. In Differential Input Mode (DF) channels 0-3 are available.

The ADC is configured via the ADC Configuration Register. A manual conversion is triggered in the Global ADC Control Register. The ADC Busy status is available in the Global ADC Status Register.

Data coding is Binary Two's Complement.

Note that for ADC devices hardware configured for analog current input function, the ADC channels 0-3 are always operating in differential mode and the ADC channels 4-7 are not applicable.

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_1_DATA	ADC Data ADC Channel 1 (SE, DF)	R	0x0000
15:0	ADCx_0_DATA	ADC Data ADC Channel 0 (SE, DF)	R	0x0000

Table 5-14 : ADC x Data Register Channel 0/1 (SE, DF)

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_3_DATA	ADC Data ADC Channel 3 (SE, DF)	R	0x0000
15:0	ADCx_2_DATA	ADC Data ADC Channel 2 (SE, DF)	R	0x0000

Table 5-15 : ADC x Data Register Channel 2/3 (SE, DF)

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_5_DATA	ADC Data ADC Channel 5 (SE)	R	0x0000
15:0	ADCx_4_DATA	ADC Data ADC Channel 4 (SE)	R	0x0000

Table 5-16 : ADC x Data Register Channel 4/5 (SE)

Bit	Symbol	Description	Access	Reset Value
31:16	ADCx_7_DATA	ADC Data ADC Channel 7 (SE)	R	0x0000
15:0	ADCx_6_DATA	ADC Data ADC Channel 6 (SE)	R	0x0000

Table 5-17 : ADC x Data Register Channel 6/7 (SE)

See the *Manual Mode A/D Conversions* sub-chapter more information.

See the *Analog Inputs* chapter for the A/D data coding.

5.2.4 ADC Mode Register(s) (0x048, 0x08C, 0x0D0, 0x114)

There is a dedicated ADC Mode Register for each physical ADC device.

Bit	Symbol	Description	Access	Reset Value
31:1	-	Reserved	-	-
0	ADCx_ OP_ MODE	ADC Operating Mode 0: Manual Mode 1: Sequencer Mode This bit sets the general ADC Operating Mode. In Manual Mode, an A/D conversion process is requested via Global ADC Control Register command (there is no periodic conversion rate). In Sequencer Mode, analog inputs are sampled periodically at a configurable conversion clock rate.	R/W	0

Table 5-18 : ADC x Mode Register (0x048, 0x08C, 0x0D0, 0x114)

Note that all channels of an ADC device are always operating in the same operating mode (Manual Mode or Sequencer Mode). The operating mode (Manual Mode or Sequencer Mode) is configurable per ADC device (not per A/D channel).

5.3 A/D Sequencer Register

The A/D Sequencer is used for periodic analog to digital conversions at a configurable conversion rate.

Each ADC device may be assigned to the A/D sequencer.

For each Sequencer Conversion Event, the analog input conversion is performed for all active channels of all ADC devices assigned to the A/D sequencer (always starting with ADC device channel 0). Active channels of the same ADC device are sampled pseudo-simultaneous (successively at a fast rate). ADC devices are processed synchronously (e.g. the channels 0 of all participating ADC devise are sampled synchronously and so forth).

The A/D sequencer may operate in Normal Mode or Frame Mode.

Normal Mode is used for generating a single block/sequence of equidistant A/D conversions by register command.

Frame Mode is used for generating a frame/sequence of A/D conversions upon a frame trigger signal event. Frame Mode may also be used for repetitive frames of A/D conversion sequences at a configurable frame interval rate and for Multi-Board synchronization.

5.3.1 A/D Sequencer Control Register (0x120)

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved	-	-
Sequencer DMA Control				
23:19	-	Reserved	-	-
18	AD_SEQ_ DMA_STAT_ ENA	A/D Sequencer DMA Status Enable 0: DMA Status Word Transfer Disabled 1: DMA Status Word Transfer Enabled If enabled, an additional DMA Status word is transferred to the Host RAM location configured via the DMA Status Base Address Register after a DMA Buffer termination event.	R/W	0
17	AD_SEQ_ DMA_RST	A/D Sequencer DMA Reset Writing '1' to this bit resets the DMA Controller. This bit is self-clearing	R/S	0
16	AD_SEQ_ DMA_ENA	A/D Sequencer DMA Enable 0: DMA Controller Disabled 1: DMA Controller Enabled Enables the Sequencer's DMA Controller to allow the initiation of DMA transfers by writing to the DMA Buffer Length Register. When being disabled, any active DMA transfer is completed before the DMA Engine enters Idle or Error state. The DMA Controller operation is stopped in case of a DMA Error. In this case the ADC Sequencer Status Register should be read and the DMA Controller should be disabled by software. The DMA Controller is reset when disabled.	R/W	0
Sequencer FIFO Control				
15:9	-	Reserved	-	-
8	AD_SEQ_ FIFO_CLR	A/D Sequencer FIFO Clear When set to 1, the ADC Sequencer's internal FIFO is cleared. This bit is self-clearing	R/S	0

<table>
<tr><th colspan="5">Sequencer Input Unit Control</th></tr>
<tr><td>7:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5</td><td>AD_SEQ_
IU_CLK_
SRC</td><td>A/D Sequencer Input Unit Conversion Clock Source
These bits select the Input Unit Conversion Clock signal source. The Input Unit Conversion Clock signal defines the ADC Sequencer’s Conversion Rate.
Note that in Frame Mode, the Input Unit Conversion Clock signal must be phase locked and aligned to the Frame Trigger signal. See chapters Frame Mode Notes and Frame Trigger Generator.
<table><tr><th>IU_CLK_SRC</th><th>Conversion Clock Source</th></tr><tr><td>0</td><td>Conversion Clock 1</td></tr><tr><td>1</td><td>Conversion Clock 2</td></tr></table>
If the Input Unit is still busy in collecting ADC data while the next conversion event is due, the conversion process is stopped and the AD_SEQ_
CNV_ERR bit in the ADC Sequencer Status Register is set.</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>3</td><td>AD_SEQ_
IU_CONV_
START</td><td>A/D Sequencer Input Unit Start Conversion (Normal Mode)
Set this bit to start a conversion process in Normal Mode.
The FIFO Level may be checked before setting this bit.
This bit is self-clearing</td><td>R/S</td><td>0</td></tr>
<tr><td>2</td><td>AD_SEQ_
IU_MODE</td><td>A/D Sequencer Input Unit Mode
0: Normal Mode
1: Frame Mode
In Normal Mode, the configured Number of A/D Conversions is performed right after the next conversion clock pulse (rising edge and falling edge) after the IU_CONV_START bit has been set.
In Frame Mode, the configured Number of Conversions is performed starting with the next conversion clock (falling edge) event after a frame trigger event.</td><td>R/W</td><td>0</td></tr>
<tr><td>1</td><td>AD_SEQ_
IU_RST</td><td>A/D Sequencer Input Unit Reset
Writing '1' to this bit resets the Input Unit.
This bit is self-clearing</td><td>R/S</td><td>0</td></tr>
<tr><td>0</td><td>AD_SEQ_
IU_ENA</td><td>A/D Sequencer Input Unit Enable
0: Input Unit Disabled
1: Input Unit Enabled
Enables the Input Unit.
The Input Unit handles the ADC Data transfer from the ADCs to the Sequencer's internal FIFO (and also controls the ADC Sequencer's Conversion Rate generation).
The Input Unit operation is stopped in case of an Input Unit Error. In this case the ADC Sequencer Status Register should be read and the Input Unit should be disabled.
The Input Unit is reset when disabled.</td><td>R/W</td><td>0</td></tr>
</table>

Table 5-19 : A/D Sequencer Control Register (0x120)

5.3.2 A/D Sequencer Status Register (0x124)

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved	-	-
Sequencer DMA Status				
23	-	Reserved	-	-
22:20	AD_SEQ_ DMA_TERM	A/D Sequencer DMA Buffer Termination These bits indicate the reason for the termination of the current DMA Buffer. These bits are automatically cleared when a new DMA Buffer is provided by writing to the DMA Buffer Length Register and are set when the DMA Buffer is terminated. Bit 22: Error / Buffer Abort The Sequencer Input Unit operation has been stopped before the desired Number of Conversions has been performed because of a Sequencer Input Unit Error. Bit 21: Block/Frame End in Buffer Normal Mode: The desired number of conversions (configured in the Number of Conversions Register) has been written to DMA Buffers (does not apply in Continuous Mode). Frame Mode: Number Of Conversions > 0: The desired number of conversions (configured in the Number of Conversions Register) has been written to DMA Buffers. Number of Conversions = 0 (Continuous Mode): Frame End due to next Frame Trigger event. Bit 20: Buffer End The end of the current DMA Buffer has been reached (the provided DMA Buffer space is exhausted). A new DMA Buffer must be provided.	R	000
19	-	Reserved	-	-
18	AD_SEQ_ DMA_ERR	A/D Sequencer DMA Error A PCI Master Abort occurred because the addressed PCI Target did not respond or a PCI Target Abort occurred because the addressed PCI Target detected a fatal error. In case of an error, the DMA Controller operation is automatically stopped. This bit is cleared when the DMA Controller is disabled.	R	0
17	AD_SEQ_ DMA_BSY	A/D Sequencer DMA Busy Indicates whether the DMA Controller is currently busy (active).	R	0
16	AD_SEQ_ DMA_IDLE	A/D Sequencer DMA Idle Indicates whether the DMA Controller is currently in Idle State. This bit is cleared when the DMA Controller is disabled. When in Idle state, a DMA transfer may be started (a DMA buffer may be assigned) by writing to the DMA Buffer Length Register.	R	0
Sequencer FIFO Status				
15:8	-	Reserved	-	-

Sequencer Input Unit Status				
7	-	Reserved	-	-
6	AD_SEQ_ IU_FRAME_ERR	A/D Sequencer Input Unit Frame Error A Frame Trigger event occurs, but the configured Number of Conversions for the current frame has not been processed so far (does not apply in Continuous Mode). In case of this error, the conversion process is terminated (no more conversion pulses are generated) and the Input Unit operation is stopped. This bit is automatically cleared when the Input Unit is disabled.	R	0
5	AD_SEQ_ CNV_ERR	A/D Sequencer Input Unit Conversion Error The Sequencer Conversion Clock requests the next conversion too fast while the current conversion process is still in progress. In case of this error, the conversion process is terminated (no more conversion pulses are generated) and the Input Unit operation is stopped. This bit is automatically cleared when the Input Unit is disabled.	R	0
4	AD_SEQ_ FIFO_OF	A/D Sequencer Input Unit FIFO Overflow Error The Input Unit needs to write ADC conversion data to the FIFO but the FIFO is full (e.g. because the FIFO data is not written to Host RAM fast enough). In case of this error, the conversion process is terminated (no more conversion pulses are generated) and the Input Unit operation is stopped. This bit is automatically cleared when the Input Unit is disabled.	R	0
3	-	Reserved	-	-
2	AD_SEQ_ IU_CNV_ACT	A/D Sequencer Input Unit Conversion Process Active Indicates that the conversion process is active. In Normal Mode, this bit is set when the Input Unit Start Conversion bit is set by software. This bit is cleared when the configured Number of Conversions has been performed. In Frame Mode, this bit is set when a Frame Trigger starts the conversion process (except in a frame error case). This bit is cleared when the configured Number of Conversions has been performed for a frame (this bit is never cleared for an active continuous mode conversion process).	R	0
1	-	Reserved	-	-
0	AD_SEQ_ IU_IDLE	A/D Sequencer Input Unit Idle Indicates whether the Input Unit is currently in Idle State. This bit is cleared when the Input Unit is disabled.	R	0

Table 5-20 : A/D Sequencer Status Register (0x124)

5.3.3 A/D Sequencer Number of Conversions Register (0x12C)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	AD_SEQ_ NUM_CONV	A/D Sequencer Number of Conversions to be performed Each Sequencer controlled conversion generates a conversion on all active ADC channels of all ADC devices operating in Sequencer Mode. Normal Mode: Number of A/D conversions per software request. Set to 0 for continuous A/D conversions. When the configured number of conversions has been performed, the conversion process is stopped (until the next request) and the appropriate busy bit in the Sequencer Status Register is cleared. Frame Mode: Number of A/D conversions per frame trigger event. Set to 0 for continuous A/D conversions after a frame trigger event. When the configured number of conversions has been performed, the conversion process is stopped (until the next frame trigger event) and the appropriate busy bit in the Sequencer Status Register is cleared.	R/W	0

Table 5-21 : A/D Sequencer Number of Conversions Register (0x12C)

For each sequencer controlled conversion event, a conversion is performed for the configured number of active channels on all ADC devices operating in sequencer mode.

For each ADC device, channel conversion always starts with ADC channel 0 and proceeds sequentially in ascending order. The participating ADC devices are processed in parallel. For example, ADC #1 channels 0 to 7 are processed successively at a fast rate (pseudo-simultaneous) while ADC#1 channel 0 is processed at the same time as ADC#2 channel 0 and ADC#1 channel 1 is processed at the same time as ADC#2 channel 1 and so forth.

The total number of A/D data values that are obtained per sequencer controlled conversion event corresponds to the total number of active channels of all the ADC devices operating in Sequencer Mode.

Example:

ADC 1, ADC 2 and ADC 4 are operating in Sequencer Mode.
The number of active ADC 1 channels is set to 2, the number of active ADC 2 channels is set to 4 and the number of active ADC 4 channels is set to 6 (Single-Ended Mode).
For this example, for each sequencer controlled conversion event, A/D values are taken for ADC 1 channels 0 to 1, ADC 2 channels 0 to 3 and ADC 4 channels 0 to 5. The total number of A/D data values taken for the sequencer controlled conversion event is 12.

When the Number of Conversions is set to 10, 10 sequencer controlled conversion events are performed, resulting in a total number of 120 A/D values.

Note that the ADAS3022 ADC device is a multiplexed ADC design with an internal channel multiplexer at the analog front end, selecting the actual analog signal path to the single integrated SAR ADC.

In consequence of the ADC device structure, a conversion on multiple ADAS3022 channels requires a corresponding number of ADAS3022 conversions (and conversion pulses). The TPMC543 control logic translates a single sequencer conversion clock event into an appropriate number of fast sequential ADAS3022 conversions (corresponding to the configured number of active ADC channels), hence emulating a pseudo-simultaneous sampling per ADC device. This is processed in parallel (synchronously) for each ADAS3022 ADC device.

5.3.4 A/D Sequencer Conversion Count Register (0x130)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	AD_SEQ_ CONV_CNT	A/D Sequencer Number of Sequencer Conversion Events that have been performed (per A/D conversion block or frame). The counter automatically turns over after 2^{28}-1 counts. Normal Mode: The value is automatically cleared when the software starts the (next) conversion process. Frame Mode: The value is automatically cleared at the next frame trigger event (except in a frame error case).	R	0

Table 5-22 : A/D Sequencer Conversion Count Register (0x130)

5.3.5 A/D Sequencer FIFO Level Register (0x134)

Bit	Symbol	Description	Access	Reset Value
31:0	ADC_SEQ_ FIFO_LEVEL	A/D Sequencer FIFO Level This value shows the current fill level of the sequencer's internal FIFO in number of bytes. The FIFO size is 64kByte. A single A/D data value consists of two bytes.	R	0x0000 0000

Table 5-23 : A/D Sequencer FIFO Level Register (0x134)

5.3.6 A/D Sequencer DMA Buffer Base Address Register (0x140)

Bit	Symbol	Description	Access	Reset Value
31:0	AD_SEQ_ DMA_BUF_ ADDR	A/D Sequencer DMA Buffer Base Address PCI memory mapped base address of the DMA Buffer in Host RAM where sampled ADC Data should be written to. The DMA Buffer Base Address is latched internally when the DMA Buffer Length Register is written (i.e. after writing the DMA Buffer Length Register, the next DMA Buffer Base Address may be entered here to save time).	R/W	0x0000 0000

Table 5-24 : A/D Sequencer DMA Buffer Base Address Register (0x140)

5.3.7 A/D Sequencer DMA Buffer Length Register (0x144)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	AD_SEQ_ DMA_BUF_ LEN	A/D Sequencer DMA Buffer Length Byte Length of the DMA Buffer provided in Host RAM. **A write to the DMA Buffer Length Register initiates a DMA transfer.** The Initiation of DMA transfers is only possible when the DMA Controller is in Idle state (and DMA Buffer Length is not zero).	R/W	0x0000 0000

Table 5-25 : A/D Sequencer DMA Buffer Length Register (0x144)

5.3.8 A/D Sequencer DMA Buffer Next Address Register (0x148)

Bit	Symbol	Description	Access	Reset Value
31:0	AD_SEQ_ DMA_NEXT_ ADDR	A/D Sequencer DMA Buffer Next Address This register shows the PCI address of the address location in Host RAM the next ADC Data is written to. It may be used to determine how much space is left in the provided DMA Buffer.	R	0x0000 0000

Table 5-26 : A/D Sequencer DMA Buffer Next Address Register (0x148)

5.3.9 A/D Sequencer DMA Buffer Status Base Address Register (0x14C)

Bit	Symbol	Description	Access	Reset Value
31:0	AD_SEQ_ DMA_STAT_ ADDR	A/D Sequencer DMA Buffer Status Word Base Address PCI memory mapped base address of the address location in Host RAM where the optional DMA Buffer Status Word information is written to (if enabled) when the processing of a DMA Buffer has been terminated.	R/W	0x0000 0000

Table 5-27 : A/D Sequencer DMA Buffer Status Base Address Register (0x14C)

Bit	Symbol	Description
31	-	Reserved
30:28	AD_SEQ_ DMA_TERM_ STAT	A/D Sequencer DMA Buffer Termination Status These bits indicate the reason for the termination of the current DMA Buffer. See A/D Sequencer Status Register for Bit description. Bit 30: Error / Buffer Abort Bit 29: Block/Frame End in Buffer Bit 28: Buffer End
27:0	AD_SEQ_ DMA_NUM_ BYTES	Number of Transferred Bytes Number of A/D data bytes that have been written to the DMA Buffer.

Table 5-28 : A/D Sequencer DMA Buffer Status Word (Host RAM)

The DMA Buffer Status Word in Host RAM is provided in Little Endian format.

5.4 D/A Global Registers

5.4.1 Global DAC Control Register (0x158)

This register provides control options for all on-board DAC devices.

Bit	Symbol	Description	Access	Reset Value
31:18	-	Reserved	-	-
17	DAC2_ RST_ REQ	DAC 2 Reset Request See description for DAC1.	R/S	0
16	DAC1_ RST_ REQ	DAC 1 Reset Request When set, performs a DAC device reset via the DAC (AD5755-1) RESET# pin. After the actual reset phase, a post-reset DAC auto-configuration is performed. This bit is automatically cleared. The DAC Busy Bit in the Global DAC Status Register indicates whether the reset cycle (comprising the active DAC reset & post-reset auto-configuration phase) is completed (also see chapter *Programming Hints / Global DAC Status Register Read*!).	R/S	0
15:2	-	Reserved	-	-
1	DAC2_ CONV_ REQ	DAC 2 Conversion Pulse Request See description for DAC1.	R/S	0
0	DAC1_ CONV_ REQ	DAC 1 Conversion Pulse Request Manual Controlled Conversion Mode: When set, generates a DAC conversion pulse. The DAC Busy Bit in the Global DAC Status Register should be checked to be clear before (also see chapter *Programming Hints / Global DAC Status Register Read*!). This bit is automatically cleared. Sequencer Mode & Manual Immediate Mode: This bit has no effect and is cleared immediately.	R/S	0

Table 5-29 : Global DAC Control Register (0x158)

5.4.2 Global DAC Status Register (0x15C)

This read only register provides status information for all on-board DAC devices.

Bit	Symbol	Description	Access	Reset Value
31:18	-	Reserved	-	-
17	DAC2_ FAULT	DAC 2 Fault Status See description for DAC1.	R	0
16	DAC1_ FAULT	DAC 1 Fault Status This bit is set when the DAC device (AD5755-1) FAULT# output pin is active (low).	R	0
15:10	-	Reserved	-	-
9	DAC2_ SETL	DAC 2 Settle Status See description for DAC1.	R	-
8	DAC1_ SETL	DAC 1 Settle Status Indicates a fix 24us passing time after a DAC conversion (worst case duration, actual output settling may vary due to voltage/current output magnitude changes)	R	-
7:2	-	Reserved	-	-
1	DAC2_ BUSY	DAC 2 Busy Status See description for DAC1.	R	0
0	DAC1_ BUSY	DAC 1 Busy Status Set when: • a DAC transfer request (conversion or configuration data) is being processed (including any required recovery times) (does not include any D/A output settling time) • A DAC reset request is processed (including post-reset auto-configuration time) Does not cover any analog output settling time.	R	0

Table 5-30 : Global DAC Status Register (0x15C)

Also see chapter *Programming Hints / Global DAC Status Register Read*!

5.5 D/A Device Registers

The registers described in this section are provided per on-board DAC device.

5.5.1 DAC Configuration Register(s) (0x168, 0x198)

This register is intended for initial DAC configuration.

Each DAC device must be configured before use.

DAC configuration should be performed while the DAC is configured for Manual Mode and not busy.

After writing the DAC Configuration Register, the DAC Busy Bit in the Global DAC Status Register is set and should be monitored to become clear again. Also see chapter *Programming Hints / Global DAC Status Register Read*!

This register is available per DAC device and may be accessed with 32 bit, 16 bit or 8 bit transfer size.

A write to the DAC configuration register logs an internal request for writing the (currently programmed) configuration data to the appropriate DAC device (via the DAC serial interface) as soon as possible. If not already set, the DAC Busy bit in the Global DAC Status Register is set and remains so, until the configuration data transfer to the DAC device is done.

Bit	Symbol	Description	Access	Reset Value
DAC Channel D				
31	-	Reserved	-	-
30	DACx_D_OE	Output Enable DAC Channel D	R/W	0
29	DACx_D_PU	Power-Up DAC Channel D	R/W	0
28	DACx_D_OV	Over Range DAC Channel D Enables 20% over-range for Voltage Ranges.	R/W	0
27:24	DACx_D_OR	Output Range DAC Channel D See description for DAC Channel A.	R/W	0
DAC Channel C				
23	-	Reserved	-	-
22	DACx_C_OE	Power-Up DAC Channel C	R/W	0
21	DACx_C_PU	Output Enable DAC Channel C	R/W	0
20	DACx_C_OV	Over Range DAC Channel C Enables 20% over-range for Voltage Ranges.	R/W	0
19:16	DACx_C_OR	Output Range DAC Channel C See description for DAC Channel A.	R/W	0
DAC Channel B				
15	-	Reserved	-	-
14	DACx_B_OE	Power-Up DAC Channel B	R/W	0
13	DACx_B_PU	Output Enable DAC Channel B	R/W	0
12	DACx_B_OV	Over Range DAC Channel B Enables 20% over-range for Voltage Ranges.	R/W	0

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>11:8</td><td>DACx_B_OR</td><td>Output Range DAC Channel B
See description for DAC Channel A.</td><td>R/W</td><td>0</td></tr>
<tr><td colspan="5">DAC Channel A</td></tr>
<tr><td>7</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>6</td><td>DACx_A_OE</td><td>Output Enable DAC Channel A</td><td>R/W</td><td>0</td></tr>
<tr><td>5</td><td>DACx_A_PU</td><td>Power-Up DAC Channel A</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>DACx_A_OV</td><td>Over Range DAC Channel A
Enables 20% over-range for Voltage Ranges.</td><td>R/W</td><td>0</td></tr>
<tr><td>3:0</td><td>DACx_A_OR</td><td>Output Range DAC Channel A
<table>
<tr><th>3:0</th><th>Output Voltage Range</th></tr>
<tr><td>0000</td><td>0V to 5V Voltage Range</td></tr>
<tr><td>0001</td><td>0V to 10V Voltage Range</td></tr>
<tr><td>0010</td><td>Reserved</td></tr>
<tr><td>0011</td><td>±5V Voltage Range</td></tr>
<tr><td>0100</td><td>±10V Voltage Range</td></tr>
<tr><td>0101</td><td>Reserved</td></tr>
<tr><td>011x</td><td>Reserved</td></tr>
<tr><td>10xx</td><td>Reserved</td></tr>
<tr><td>1100</td><td>4mA to 20mA Current Range</td></tr>
<tr><td>1101</td><td>0mA to 20mA Current Range</td></tr>
<tr><td>1110</td><td>0mA to 24mA Current Range</td></tr>
<tr><td>1111</td><td>Reserved</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
</table>

Table 5-31 : DAC x Configuration Register (0x168, 0x198)

See the *DAC (Re-) Configuration* chapter for avoiding analog output effects when changing the output range.

5.5.2 DAC Correction Register(s) (0x170 – 0x17C, 0x1A0 – 0x1AC)

These registers are intended for performing DAC data correction.

If used, the DAC correction registers should be configured while the DAC is operating in Manual Mode and not busy.

Leaving the DAC Correction Registers at their Reset Value (or clearing the DAC Corrections Registers) leaves the DAC data values unmodified (without any DAC data correction).

These registers are available per DAC device. There is a register for each DAC channel.

To perform D/A data value hardware correction (based on factory determined correction values), the D/A channel offset and gain correction values for the specific DAC device, DAC channel and Output Range must be read from the Correction Data Space at PCI Base Address Register 1 (BAR1) and written to the appropriate correction register.

Clearing a Correction Register effectively disables hardware correction for the corresponding DAC device channel.

These registers may be accessed with 32 bit or 16 bit transfer size (for data coherency during the DAC data correction).

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_A_GAIN	Gain Correction Value D/A Channel A	R/W	0x0000
15:0	DACx_A_OFFS	Offset Correction Value D/A Channel A	R/W	0x0000

Table 5-32 : DAC x Correction Register A (0x170, 0x1A0)

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_B_GAIN	Gain Correction Value D/A Channel B	R/W	0x0000
15:0	DACx_B_OFFS	Offset Correction Value D/A Channel B	R/W	0x0000

Table 5-33 : DAC x Correction Register B (0x174, 0x1A4)

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_C_GAIN	Gain Correction Value D/A Channel C	R/W	0x0000
15:0	DACx_C_OFFS	Offset Correction Value D/A Channel C	R/W	0x0000

Table 5-34 : DAC x Correction Register C (0x178, 0x1A8)

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_D_GAIN	Gain Correction Value D/A Channel D	R/W	0x0000
15:0	DACx_D_OFFS	Offset Correction Value D/A Channel D	R/W	0x0000

Table 5-35 : DAC x Correction Register D (0x17C, 0x1AC)

See the *D/A Data Correction* sub-chapter for more information.

5.5.3 DAC Data Register(s) (0x180, 0x184, 0x1B0, 0x1B4)

These registers are available per DAC device.

These registers are intended to be used for DACs operating in manual mode (not for DACs operating in sequencer mode). Writes to these registers are not processed when the DAC device is not in Manual Mode.

A write to a DAC data register logs an internal request for writing the channel data to the appropriate DAC device (via the DAC serial interface) as soon as possible. If not already set, the DAC Busy bit in the Global DAC Status Register is set and remains so, until the data transfer to the DAC device is done.

These registers may be accessed with 32 bit or 16 bit transfer size (for data coherency in the data transfer to the DAC devices)..

Data coding for unipolar ranges is Unipolar Straight Binary. Data coding for bipolar ranges is Binary Two's Complement.

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_B_DATA	Digital Data for DAC Channel B	R/W	0x0000
15:0	DACx_A_DATA	Digital Data for DAC Channel A	R/W	0x0000

Table 5-36 : DAC x Data Register A & B (0x180, 0x1B0)

Bit	Symbol	Description	Access	Reset Value
31:16	DACx_D_DATA	Digital Data for DAC Channel D	R/W	0x0000
15:0	DACx_C_DATA	Digital Data for DAC Channel C	R/W	0x0000

Table 5-37 : DAC x Data Register C & D (0x184, 0x1B4)

See the *Manual Mode D/A Conversions* sub-chapter more information.

See the *Analog Outputs* chapter for the D/A data coding.

5.5.4 DAC Status Register(s) (0x188, 0x1B8)

This register is available per DAC device.

Each AD5755-1 DAC device provides an internal status register, accessible via the DAC serial interface.

Setting the STAT_REQ bit logs an internal request for reading the actual status from the appropriate DAC device (via the DAC serial interface) as soon as possible. If not already set, the DAC Busy bit in the Global DAC Status Register is set and remains so, until the status read transfer from the DAC device is done and the status register bits have been updated.

Note that a Status Read Request has an impact on the maximum D/A conversion rate, especially when the DAC is operating in Sequencer Mode.

Bit	Symbol	Description	Access	Reset Value
31	DACx_ STAT_ REQ	Status Read Request When set, clears the Status Valid bit and logs a request for updating the DAC Status Register with current status information from the DAC device. This bit clears immediately. This is the recommended DAC Status Read Mode for DACs operating in Manual Mode.	R/S	0
30	DACx_ STAT_ VAL	Status Valid 0: Stale/Obsolete Status Information 1: Updated Status Information The bit is set, when the DAC Status Register has been updated with actual status data from the DAC device. The bit is cleared upon logging a Status Read Request. The bit may also be cleared by writing a '1'.	R/C	0
29	-	Reserved	-	-
28	DACx_ STAT_ AUTO	Automatic DAC Status Read Mode 0: Automatic DAC Status Read Mode Disabled 1: Automatic DAC Status Read Mode Enabled In automatic mode, the DAC Status Register is automatically updated after each DAC register write (e.g. after a DAC Data Register write). This is the recommended DAC Status Read Mode for DACs operating in Sequencer Mode.	R/W	0
27:16	-	Reserved	-	-
15	DACx_D_ DC_FAULT	In current mode, this bit is set if the channel D DC/DC converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In voltage output mode, this bit is set if the channel D DC/DC converter is unable to regulate to 15V as expected.	R	x
14	DACx_C_ DC_FAULT	In current mode, this bit is set if the channel C DC/DC converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In voltage output mode, this bit is set if the channel C DC/DC converter is unable to regulate to 15V as expected.	R	x

Bit	Symbol	Description	Access	Reset Value
13	DACx_B_ DC_FAULT	In current mode, this bit is set if the channel B DC/DC converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In voltage output mode, this bit is set if the channel B DC/DC converter is unable to regulate to 15V as expected.	R	x
12	DACx_A_ DC_FAULT	In current mode, this bit is set if the channel A DC/DC converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In voltage output mode, this bit is set if the channel A DC/DC converter is unable to regulate to 15V as expected.	R	x
11:9	-	Reserved	-	-
8	DACx_ OVER_ TEMP	This bit is set if the AD5755-1 core temperature exceeds approximately 150°C.	R	x
7	DACx_D_ VOUT_FAULT	This bit is set if a fault is detected on the AD5755-1 V_{OUT}_D pin (e.g. a short circuit).	R	x
6	DACx_C_ VOUT_FAULT	This bit is set if a fault is detected on the AD5755-1 V_{OUT}_C pin (e.g. a short circuit).	R	x
5	DACx_B_ VOUT_FAULT	This bit is set if a fault is detected on the AD5755-1 V_{OUT}_B pin (e.g. a short circuit).	R	x
4	DACx_A_ VOUT_FAULT	This bit is set if a fault is detected on the AD5755-1 V_{OUT}_A pin (e.g. a short circuit).	R	x
3	DACx_D_ IOUT_FAULT	This bit is set if a fault is detected on the AD5755-1 I_{OUT}_D pin (e.g. an open circuit).	R	x
2	DACx_C_ IOUT_FAULT	This bit is set if a fault is detected on the AD5755-1 I_{OUT}_C pin (e.g. an open circuit).	R	x
1	DACx_B_ IOUT_FAULT	This bit is set if a fault is detected on the AD5755-1 I_{OUT}_B pin (e.g. an open circuit).	R	x
0	DACx_A_ IOUT_FAULT	This bit is set if a fault is detected on the AD5755-1 I_{OUT}_A pin (e.g. an open circuit).	R	x

Table 5-38 : DAC x Status Register (0x188, 0x1B8)

5.5.5 DAC Mode Register(s) (0x18C, 0x1BC)

This register is available per DAC device.

By default, the DAC devices are operating in Manual Mode.

Alternatively, a DAC device may be set to Sequencer Mode for periodic D/A conversions at a configurable conversion rate.

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1	DACx_ MAN_ CNV_ MODE	DAC Manual Conversion Mode (Manual Mode) 0: Immediate Conversion Mode 1: Controlled Conversion Mode This bit controls the DAC output update when the DAC is operating in Manual Mode. In immediate conversion mode, a DAC output update is generated automatically when all pending DAC data transfers are done. The DAC Busy Bit should be checked to be clear before writing data for the next conversion. In controlled conversion mode, a DAC output update is generated (immediately) upon request (by register write). D/A channel data must be transferred before. The DAC Busy Bit should be checked to be clear (Global DAC Status Register, also see chapter *Programming Hints / Global DAC Status Register Read*!)) before setting the conversion pulse request (Global DAC Control Register).	R/W	0
0	DACx_ OP_ MODE	DAC Operating Mode 0: Manual Mode 1: Sequencer Mode This bit sets the general DAC operating mode. In Manual Mode, the analog outputs are updated via register access (there is no periodic conversion rate). In Sequencer Mode, the analog outputs are getting updated simultaneously & periodically at a configurable conversion rate. See the *D/A Sequencer Registers* chapter.	R/W	0

Table 5-39 : DAC x Mode Register (0x18C, 0x1BC)

Note that all four channels of a (Quad) DAC device are always operating in the same operating mode (Manual Mode or Sequencer Mode). There is no per channel operating mode configuration.

5.6 D/A Sequencer Register

The D/A Sequencer is used for periodic digital to analog conversions at a configurable conversion rate.

Each DAC device may be assigned to the D/A sequencer.

All DAC devices assigned to the D/A sequencer are operating in simultaneous conversion mode. For each Sequencer Conversion Event, the analog output update is performed for all channels of all DAC devices assigned to the D/A sequencer.

The D/A sequencer may operate in Normal Mode or Frame Mode.

Normal Mode is used for generating a single block of simultaneous D/A conversions by request (register write).

Frame Mode is used for generating a frame of simultaneous D/A conversions upon an internal or external frame trigger signal event. Frame Mode may also be used for repetitive frames of simultaneous D/A conversions at a configurable frame interval rate and for Multi-Board synchronization.

5.6.1 D/A Sequencer Control Register (0x2E8)

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved	-	-
Sequencer DMA Control				
23:18	-	Reserved	-	-
17	DA_SEQ_ DMA_RST	D/A Sequencer DMA Reset Initiates a DMA Engine reset (except register values). This bit is self-clearing.	R/S	0
16	DA_SEQ_ DMA_ENA	D/A Sequencer DMA Enable 0: DMA Engine Disabled 1: DMA Engine Enabled Enables the internal sequencer DMA Engine. When being disabled, any active DMA transfer is completed before the DMA Engine enters Idle or Error state. In case of a DMA Engine error the DMA Engine operation is stopped. Upon a DMA Engine error, software should read the DAC Sequencer Status Register and disable the sequencer DMA Engine afterwards. The sequencer DMA Engine is reset when disabled.	R/W	0
Sequencer FIFO Control				
15:9	-	Reserved	-	-
8	DA_SEQ_ FIFO_CLR	D/A Sequencer FIFO Clear Clears the sequencer's internal FIFO when set. This bit is self-clearing.	R/S	0

Sequencer Output Unit Control				
7:6	-	Reserved	-	-
5	DA_SEQ_ CONV_ CLK_SRC	D/A Sequencer Conversion Clock Source These bits are selecting the sequencer's conversion clock signal source. The selected sequencer conversion clock signal defines the sequencer's conversion rate. Note that in Frame Mode, the sequencer conversion clock signal must be phase locked to the frame trigger signal. See chapters *Frame Mode Notes* and *Frame Trigger Generator*. 0: Conversion Clock 1 (Selected Source) 1: Conversion Clock 2 (Selected Source)	R/W	0
4	DA_SEQ_ OU_CLR_ PRLD	D/A Sequencer Output Unit Clear DAC Pre-Load Status Setting this bit marks the sequencer DAC devices as 'un-loaded' (invalidating any performed preload). The DAC devices are automatically pre-loaded again when data is/becomes available in the sequencer FIFO. This bit is self-clearing.	R/S	0
3	DA_SEQ_ OU_CONV_ START	D/A Sequencer Output Unit Start Conversion (Normal Mode) Set this bit to start a conversion process in Normal Mode (the Sequencer Output Unit must be enabled before). The sequencer FIFO level may be checked before setting this bit. This bit is self-clearing.	R/S	0
2	DA_SEQ_ OU_MODE	D/A Sequencer Output Unit Mode 0: Normal Mode 1: Frame Mode Normal Mode: In Normal Mode, D /A conversions are generated starting with the next synchronized conversion clock event after the conversion process start command.. Frame Mode: In Frame Mode, D/A conversions are generated starting with the next conversion clock event after a (each) frame trigger signal event.	R/W	0
1	DA_SEQ_ OU_RST	D/A Sequencer Output Unit Reset Initiates a sequencer output unit reset (except register values). This bit is self-clearing.	R/S	0

0	DA_SEQ_ OU_ENA	D/A Sequencer Output Unit Enable 0: Sequencer Output Unit Disable 1: Sequencer Output Enable Enables the sequencer output unit. The sequencer output unit handles the data transfer from the sequencer's internal data FIFO to the sequencer's DAC devices. When enabled and while the sequencer DAC devices are not completely pre-loaded, data in the sequencer FIFO is automatically transferred to the sequencer's DAC devices for pre-loading the DACs for the first/next conversion (except in an error case). In case of a sequencer output unit error the sequencer output unit operation is stopped. Upon a sequencer output unit error, the Sequencer Status Register should be read and the sequencer output unit should be disabled afterwards. The sequencer output unit is reset when disabled.	R/W	0

Table 5-40 : D/A Sequencer Control Register (0x2E8)

5.6.2 D/A Sequencer Status Register (0x2EC)

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved	-	-
Sequencer DMA Status				
23:21	-	Reserved	-	-
20	DA_SEQ_ DMA_ DONE	D/A Sequencer DMA Buffer Done This bit indicates that all values have been read from the DMA buffer in H0ost memory. The bit is automatically cleared when a new DMA Buffer is validated by writing to the DMA Buffer Length Register while the DMA Engine is in Idle State.	R	0
19	-	Reserved	-	-
18	DA_SEQ_ DMA_ERR	D/A Sequencer DMA Engine State: DMA Error Indicates that the DMA Engine is in an Error State. Possible causes: • PCI Master Abort (the addressed PCI Target did not respond) • PCI Target Abort (the addressed PCI Target detected a fatal error) In case of an error, the DMA engine operation is stopped. This bit is automatically cleared when the sequencer DMA Engine is disabled.	R	0
17	DA_SEQ_ DMA_BSY	D/A Sequencer DMA Engine State: DMA Busy Indicates that the DMA Engine is currently busy (active).	R	0
16	DA_SEQ_ DMA_IDLE	D/A Sequencer DMA Engine State: DMA Idle Indicates that the DMA Engine is in Idle State. A DMA transfer may be started (a DMA buffer may be validated) by writing to the DMA Buffer Length Register.	R	0
Sequencer FIFO Status				
15:8	-	Reserved	-	-

Sequencer Output Unit Status				
7	-	Reserved	-	-
6	DA_SEQ_OU_FRM_ERR	D/A Sequencer Output Unit Frame Error A next frame trigger event occurs, but the configured number of conversions has not been processed so far (does not apply in Continuous Mode) In case of an error, the conversion process is terminated and the sequencer output unit operation is stopped. This bit is automatically cleared when the sequencer output unit is disabled.	R	0
5	DA_SEQ_OU_CNV_TIME_ERR	D/A Sequencer Output Unit Conversion Timing Error A next conversion pulse is due, but would violate the DAC timing specification. Possible causes: Too high conversion clock frequency, etc. In case of an error, the conversion process is terminated and the sequencer output unit operation is stopped. This bit is automatically cleared when the sequencer output unit is disabled.	R	0
4	DA_SEQ_OU_CNV_DATA_ERR	D/A Sequencer Output Unit Conversion Data Error A next conversion pulse is due, but not all sequencer DAC devices are in a proper pre-loaded state. Possible causes: FIFO data underrun, too high conversion clock frequency, etc. In case of an error, the conversion process is terminated and the sequencer output unit operation is stopped. This bit is automatically cleared when the sequencer output unit is disabled.	R	0
3	-	Reserved	-	-
2	DA_SEQ_OU_CNV_ACT	D/A Sequencer Output Unit Conversion Process Active Normal Mode: This bit is set when the conversion process is started and the bit is cleared when the configured number of conversions has been performed. Frame Mode: This bit is set upon a (each) frame trigger event that starts a conversion process (except in a frame error case) and the bit is cleared when the configured number of conversions has been performed for a frame (this bit is never cleared for an active continuous mode conversion process).	R	0
1	DA_SEQ_OU_PRLD	D/A Sequencer Output Unit DACs in Pre-Loaded State Indicates that all sequencer DAC devices are pre-loaded with conversion data for all four DAC channels. This bit is automatically cleared upon a DAC conversion pulse or when the pre-load status is cleared manually.	R	0
0	DA_SEQ_OU_IDLE	D/A Sequencer Output Unit in Idle State Indicates that the Sequencer Output Unit is in Idle State.	R	0

Table 5-41 : D/A Sequencer Status Register (0x2EC)

5.6.3 D/A Number of Conversions Register (0x2F4)

This register sets the desired number of D/A conversions per manual request (Normal Mode) or frame trigger event (Frame Mode).

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	DA_SEQ_ NUM_CONV	D/A Sequencer Number of Conversions to be performed Normal Mode: Number of D/A conversions per manual request. Set to 0 for continuous D/A conversions. When the configured number of conversions has been performed, the conversion process is stopped (until the next software request) and the appropriate bit in the Sequencer Status Register is cleared. Frame Mode: Number of D/A conversions per frame trigger event. Set to 0 for continuous D/A conversions after a frame trigger event. When the configured number of conversions has been performed, the conversion process is stopped (until the next frame trigger event) and the appropriate bit in the Sequencer Status Register is cleared.	R/W	0

Table 5-42 : D/A Sequencer Number of Conversions Register (0x2F4)

Note that for each sequencer controlled conversion event, all four D/A channels of all DAC devices assigned to the sequencer are updated simultaneously. After each sequencer controlled conversion event, the sequencer DAC devices are pre-loaded with conversion data for the next conversion event (when data is available in the sequencer FIFO). The automatic pre-load process is started even if the data set for the next conversion is not yet completely available in the FIFO), so in case of a following error event, some D/A channels may already have new data while others have not.

The number of required D/A data values per sequencer controlled conversion event is:
Number_of_DAC_Devices_assigned_to_the_Sequencer x 4 (Channels per DAC Device)

5.6.4 D/A Sequencer Conversion Count Register (0x2F8)

This register shows the number of D/A conversions that have been performed.

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	DA_SEQ_ CONV_CNT	D/A Sequencer Number of Conversions that have been performed (per D/A conversion block or frame). The counter automatically turns over after 2^{28}-1 counts. Normal Mode: The value is automatically cleared when the (next) conversion process is started. Frame Mode: The value is automatically cleared at the next frame trigger event (except in a frame error case).	R	0

Table 5-43 : D/A Sequencer Conversion Count Register (0x2F8)

5.6.5 D/A Sequencer FIFO Level Register (0x2FC)

Bit	Symbol	Description	Access	Reset Value
31:0	DA_SEQ_ FIFO_LVL	D/A Sequencer FIFO Level This value shows the current sequencer FIFO fill level in Number of Bytes. A single D/A data value consists of two bytes. FIFO size is 32kByte.	R	0

Table 5-44 : D/A Sequencer FIFO Level Register (0x2FC)

5.6.6 D/A Sequencer DMA Buffer Base Address Register (0x308)

Bit	Symbol	Description	Access	Reset Value
31:0	DA_SEQ_ DMA_BUF_ ADDR	D/A Sequencer DMA Buffer Base Address PCI memory mapped base address of the DMA Buffer in Host memory where D/A conversion data can be read from. The DMA Buffer base address is latched when the DMA Buffer Length Register is written (i.e. after writing the DMA Buffer Length Register, the next DMA Buffer Base Address may be entered here to save time).	R/W	0

Table 5-45 : D/A Sequencer DMA Buffer Base Address Register (0x308)

5.6.7 D/A Sequencer DMA Buffer Length Register (0x30C)

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	DA_SEQ_ DMA_BUF_ LEN	D/A Sequencer DMA Buffer Length Byte Length of the provided DMA Buffer in Host RAM. **A write to the DMA Buffer Length Register initiates a DMA transfer.** Only effective when the sequencer DMA Engine is in Idle State (and DMA Buffer Length is not zero).	R/W	0

Table 5-46 : D/A Sequencer DMA Buffer Length Register (0x30C)

5.6.8 D/A Sequencer DMA Buffer Next Address Register (0x310)

Bit	Symbol	Description	Access	Reset Value
31:0	DA_SEQ_ DMA_ NEXT_ ADDR	D/A Sequencer DMA Buffer Next Address This register holds the PCI address of the address location in Host RAM the next D/A conversion data is read from.	R	0

Table 5-47 : D/A Sequencer DMA Buffer Next Address Register (0x310)

5.7 Conversion Signal Registers

These registers apply for Sequencer Mode operation and/or external synchronization.

There are three conversion signals, available for a sequencer:

- Conversion Clock 1
- Conversion Clock 2
- Frame Trigger

Each of the two Conversion Clock signals may be selected as the Sequencer Conversion Clock in the Sequencer Control Registers, determining the sequencer's conversion rate.

The Frame Trigger signal (along with a conversion clock signal) is used to start a frame of conversions in sequencer Frame Mode.

For each of these signals, the signal source is configurable to be either the output signal of the corresponding on-board signal generator or an input signal from the I/O interface.

The on-board signal generator output signals may optionally be driven out on the I/O interface.

5.7.1 Conversion Clock 1 Generator Register (0x320)

This register controls the conversion clock 1 signal generation.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>30:29</td><td>CLK1_
GEN_
SRC</td><td>Conversion Clock 1 Clock Source
<table><tr><th>30:29</th><th>Internal Clock Source</th></tr><tr><td>00</td><td>20 MHz</td></tr><tr><td>01</td><td>22.05 MHz</td></tr><tr><td>10</td><td>60 MHz</td></tr><tr><td>11</td><td>Reserved</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>28</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>27:0</td><td>CLK1_
GEN_
DIV</td><td>Conversion Clock 1 Clock Divider
These bits set the divider for the selected clock source.
The frequency of the clock generator output is: $\frac{SRC\_CLK}{DIV+1}$</td><td>R/W</td><td>0xFFF FFFF</td></tr>
</table>

Table 5-48 : Conversion Clock 1 Generator Register (0x320)

5.7.2 Conversion Clock 2 Generator Register (0x324)

This register controls the conversion clock 2 signal generation.

Bit	Symbol	Description	Access	Reset Value
31	-	Reserved	-	-
30:29	CLK2_GEN_SRC	Conversion Clock 2 Clock Source 30:29 = 00: 20 MHz 30:29 = 01: 22.05 MHz 30:29 = 10: 60 MHz 30:29 = 11: Reserved	R/W	00
28	-	Reserved	-	-
27:0	CLK2_GEN_DIV	Conversion Clock Divider These bits set the divider for the selected clock source. The frequency of the clock generator output is: $\frac{SRC\_CLK}{DIV+1}$	R/W	0xFFFFFFF

Table 5-49 : Conversion Clock 2 Generator Register (0x324)

5.7.3 Frame Trigger Generator Register 1 (0x32C)

This register configures the frame trigger signal generation.

Bit	Symbol	Description	Access	Reset Value
31:30	-	Reserved	-	-
29	FTRIG_GEN_CLK	Frame Trigger Associated Conversion Clock 0: The Frame Trigger Signal is generated for the Conversion Clock 1 Generator output signal 1: The Frame Trigger Signal is generated for the Conversion Clock 2 Generator output signal	R/W	0
28	-	Reserved	-	-
27:0	FTRIG_GEN_IVAL	Frame Trigger Interval Sets the frame trigger pulse interval in number of cycles of the associated conversion clock signal. Frame Trigger Interval = (FTRIG_GEN_IVAL + 1) conversion clock cycles. The frame trigger interval does not apply if the configured number of frame trigger pulses is 1.	R/W	0xFFFFFFF

Table 5-50 : Frame Trigger Generator Register (0x32C)

5.7.4 Frame Trigger Generator Register 2 (0x330)

This register configures the frame trigger signal generation.

Bit	Symbol	Description	Access	Reset Value
31:28	-	Reserved	-	-
27:0	FTRIG_ GEN_ NUM	Number of Frames (Frame Trigger Pulses) Sets the number of frame trigger pulses (i.e. frames) to be generated. Value 0 is for continuous frame trigger pulses at the configured frame trigger interval rate. Frame trigger signal generation is started via the Conversion Signal Generator Enable Register.	R/W	0

Table 5-51 : Frame Trigger Generator Register 2 (0x330)

5.7.5 Conversion Signal Generator Enable Register (0x33C)

This register provides synchronous enable control for the on-board conversion clock and frame trigger signal generators.

Bit	Symbol	Description	Access	Reset Value
31:10	-	Reserved	-	-
8	FTRIG_ GEN_ ENA	Frame Trigger Generation Enable 0: Frame Trigger Generator Disabled 1: Frame Trigger Generator Enabled If enabled, the configured number of frame trigger pulses is generated, starting with the next rising edge of the associated conversion clock signal. The conversion clock generator associated with the frame trigger generation must also be enabled.	R/W	0
7:2	-	Reserved	-	-
1	CLK2_ GEN_ ENA	Conversion Clock 2 Generator Enable 0: Conversion Clock Generator Disabled 1: Conversion Clock Generator Enabled	R/W	0
0	CLK1_ GEN_ ENA	Conversion Clock 1 Generator Enable 0: Conversion Clock Generator Disabled 1: Conversion Clock Generator Enabled	R/W	0

Table 5-52 : Conversion Signal Generator Enable Register (0x33C)

Note that for generating phase aligned Clock 1 and Clock 2 signals, both conversion clock generators must be configured for the same clock source. Furthermore, the target clock frequencies must be integer multiples of another.

5.7.6 Conversion Signal Generator Output Driver Register (0x340)

This register is used for configuring output drivers for the output signals of the on-board conversion signal generators.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5:4</td><td>FTRIG_ GEN_ OUT_ CFG</td><td>Frame Trigger Generator Signal
Output Driver Configuration
<table><tr><th>5:4</th><th>Output Driver Configuration</th></tr><tr><td>0x</td><td>Output Driver Disabled</td></tr><tr><td>10</td><td>Output Driver Enabled
P14 Rear I/O FRAME_TRIG Pin</td></tr><tr><td>11</td><td>Output Driver Enabled
Front I/O DIO 5 Line</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>3:2</td><td>CLK2_ GEN_ OUT_ CFG</td><td>Conversion Clock 2 Generator Signal
Output Driver Configuration
<table><tr><th>3:2</th><th>Output Driver Configuration</th></tr><tr><td>0x</td><td>Output Driver Disabled</td></tr><tr><td>10</td><td>Output Driver Enabled
P14 Rear I/O CONV_CLK2 Pin</td></tr><tr><td>11</td><td>Output Driver Enabled
Front I/O DIO 3 Line</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>1:0</td><td>CLK1_ GEN_ OUT_ CFG</td><td>Conversion Clock 1 Generator Signal
Output Driver Configuration
<table><tr><th>1:0</th><th>Output Driver Configuration</th></tr><tr><td>0x</td><td>Output Driver Disabled</td></tr><tr><td>10</td><td>Output Driver Enabled
P14 Rear I/O CONV_CLK1 Pin</td></tr><tr><td>11</td><td>Output Driver Enabled
Front I/O DIO 1 Line</td></tr></table></td><td>R/W</td><td>00</td></tr>
</table>

Table 5-53 : Conversion Signal Generator Output Driver Register (0x340)

Note that for driving out a Conversion Clock and/or Frame Trigger generator signal on the appropriate DIO front I/O pin, the corresponding bit combination must be set in the Conversion Signal Generator Output Driver Register AND the corresponding DIO_OE# bit in the DIO Output Enable Register must be cleared.

The regular DIO output operation dominates, thus if a bit is set in the DIO Output Enable Register, the corresponding value set in the DIO Output Register is driven out on the DIO front I/O pin (regardless of the Conversion Signal Generator Output Driver Register setting).

Note that it is not recommended to use the conversion clock and frame trigger signal Front I/O option for the final user application since these digital signals with permanent activity would run in the same I/O cable as the analog I/O signals and would generate noticeable noise in the analog input and output signals. The Front I/O option for the conversion clock signals is merely intended to be used for testing.

5.7.7 Conversion Signal Source Selection Register (0x344)

This register is used for the selecting the signal source of the internal conversion control signals that are used by the sequencer(s).

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:6</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>5:4</td><td>FTRIG_ SRC</td><td>Frame Trigger Signal Source<table><tr><th>5:4</th><th>Signal Source</th></tr><tr><td>0x</td><td>FRAME_TRIG Generator</td></tr><tr><td>10</td><td>P14 Rear I/O FRAME_TRIG Input</td></tr><tr><td>11</td><td>Front I/O DIO 5 Line Input</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>3:2</td><td>CLK2_ SRC</td><td>Conversion Clock 2 Signal Source<table><tr><th>3:2</th><th>Signal Source</th></tr><tr><td>0x</td><td>CONV_CLK2 Generator</td></tr><tr><td>10</td><td>P14 Rear I/O CONV_CLK2 Input</td></tr><tr><td>11</td><td>Front I/O DIO 3 Line Input</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>1:0</td><td>CLK1_ SRC</td><td>Conversion Clock 1 Signal Source<table><tr><th>1:0</th><th>Signal Source</th></tr><tr><td>0x</td><td>CONV_CLK1 Generator</td></tr><tr><td>10</td><td>P14 Rear I/O CONV_CLK1 Input</td></tr><tr><td>11</td><td>Front I/O DIO 1 Line Input</td></tr></table></td><td>R/W</td><td>00</td></tr>
</table>

Table 5-54 : Conversion Signal Source Selection Register (0x344)

Note that it is not recommended to use the conversion clock and frame trigger signal Front I/O option for the final user application since these digital signals with permanent activity would run in the same I/O cable as the analog I/O signals and would generate noticeable noise in the analog input and output signals. The Front I/O option for the conversion clock signals is merely intended to be used for testing.

The following table shows typical Conversion Signal Path configuration examples.

PMC Configuration Example	Internal Conversion Signal Generator	Conversion Signal Output Driver	Conversion Signal Source Selection
Single Card	Enabled	Disabled	Internal Conversion Signal Generator
Multi-Board Master Card	Enabled	Enabled (P14 Rear I/O)	I/O Input
Multi-Board Slave Card or External Signal Generators	Disabled	Disabled	I/O Input

Table 5-55 : Conversion Signal Path Configuration Examples

5.7.8 Frame Timer Register (0x348)

Bit	Symbol	Description	Access	Reset Value
31	FTIM_ ENA	Frame Timer Enable 0: Frame Timer Disabled 1: Frame Timer Enabled If enabled, a frame trigger signal event (selected signal source) resets the frame timer and (re-) starts the timer process.	R/W	0
30	FTIM_ SRC	Frame Timer Clock Source 0: Conversion Clock 1 (Selected Signal Source) 1: Conversion Clock 2 (Selected Signal Source)	R/W	0
29	FTIM_ STAT	Frame Timer Event Status A frame timer event is generated when the frame timer expires. This bit is automatically cleared upon a frame trigger signal event (selected source).	R	0
28	-	Reserved	-	-
27:0	FTIM_ VAL	Frame Timer Value After a frame trigger signal event (selected signal source), the Frame Timer expires after FTIM_VAL + 1 cycles of the corresponding conversion clock signal.	R/W	0xFFF_ FFFF

Table 5-56 : Frame Timer Register (0x348)

5.8 DIO Registers

These registers are dealing with the Digital I/O interface available at the front I/O connector.

Note that the digital I/O lines are merely intended to be used in a static way. Since the digital I/O lines are running in the same I/O cable as the sensitive analog input and output lines, any activity on the digital I/O lines will generate noticeable noise in the analog signals.

5.8.1 DIO Input Register (0x354)

The Digital I/O receivers are always enabled, so each DIO line level can always be monitored.

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	DIO_IN8	DIO8 Input See description for DIO1.	R	0
6	DIO_IN7	DIO7 Input See description for DIO1.	R	0
5	DIO_IN6	DIO6 Input See description for DIO1.	R	0
4	DIO_IN5	DIO5 Input See description for DIO1.	R	0
3	DIO_IN4	DIO4 Input See description for DIO1.	R	0
2	DIO_IN3	DIO3 Input See description for DIO1.	R	0
1	DIO_IN2	DIO2 Input See description for DIO1.	R	0
0	DIO_IN1	DIO1 Input Shows the state of the Digital I/O 1 line (regardless if the corresponding output driver is enabled in the DIO Output Enable Register or not). 0: Digital I/O 1 Line State is low. 1: Digital I/O 1 Line State is high.	R	0

Table 5-57 : DIO Input Register (0x354)

5.8.2 DIO Input Filter Register (0x358)

A debounce filter can be configured to get rid of bouncing on the digital I/O inputs.

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	-	-
15:0	DIO_DEB	Digital I/O Input Debounce Configuration T_{REJECT} = ([DEB + 1] x 50ns) Pulses with a duration smaller than T_{REJECT} are filtered and are not passed on to the internal logic. T_{PASS} = ([DEB + 1] x 75ns) = 1.5 x T_{REJECT} Pulses with a duration greater than T_{PASS} are not filtered and are passed on to the internal logic. Please note that pulses with a duration between T_{PASS} and T_{REJECT} may or may not be filtered (uncertainty).	R/W	0x0000

Table 5-58 : DIO Input Filter Register (0x358)

5.8.3 DIO Output Register (0x35C)

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	DIO_OUT8	DIO8 Output See description for DIO1.	R/W	0
6	DIO_OUT7	DIO7 Output See description for DIO1.	R/W	0
5	DIO_OUT6	DIO6 Output See description for DIO1.	R/W	0
4	DIO_OUT5	DIO5 Output See description for DIO1.	R/W	0
3	DIO_OUT4	DIO4 Output See description for DIO1.	R/W	0
2	DIO_OUT3	DIO3 Output See description for DIO1.	R/W	0
1	DIO_OUT2	DIO2 Output See description for DIO1.	R/W	0
0	DIO_OUT1	DIO1 Output Sets the output state of the Digital I/O 1 line when the corresponding output driver is enabled in the DIO Output Enable Register. 0: Digital I/O 1 Line is driven low. 1: Digital I/O 1 Line is driven high.	R/W	0

Table 5-59 : DIO Output Register (0x35C)

5.8.4 DIO Output Enable Register (0x360)

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	DIO_OE8	DIO8 Output Enable See description for DIO1.	R/W	0
6	DIO_OE7	DIO7 Output Enable See description for DIO1.	R/W	0
5	DIO_OE6	DIO6 Output Enable See description for DIO1.	R/W	0
4	DIO_OE5	DIO5 Output Enable See description for DIO1.	R/W	0
3	DIO_OE4	DIO4 Output Enable See description for DIO1.	R/W	0
2	DIO_OE3	DIO3 Output Enable See description for DIO1.	R/W	0
1	DIO_OE2	DIO2 Output Enable See description for DIO1.	R/W	0
0	DIO_OE1	DIO1 Output Enable 0: Digital I/O 1 Output Driver is disabled 1: Digital I/O 1 Output Driver is enabled If enabled, the level of the Digital I/O line is adjusted in the DIO Output Register. The Digital I/O line receivers are always enabled and the DIO line level is always readable in the DIO Input Register.	R/W	0

Table 5-60 : DIO Output Enable Register (0x360)

5.9 Interrupt Registers

5.9.1 Interrupt Enable Register

For an interrupt status bit to be set, the interrupt must be enabled prior to the interrupt event.

Disabling an interrupt does not clear an already registered/pending interrupt (it only prevents subsequent events from generating an interrupt).

5.9.1.1 Interrupt Enable Register (0x36C)

Bit	Symbol	Description	Access	Reset Value
31:30	-	Reserved	-	-
29	FTIM_ INT_EN	Frame Timer Event Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
28	FTRIG_ INT_EN	Frame Trigger Event Interrupt Status 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
27	ADC4_ CONV_ INT_EN	ADC 4 Conversion Done Interrupt Enable See description for ADC 1.	R/W	0
26	ADC3_ CONV_ INT_EN	ADC 3 Conversion Done Interrupt Enable See description for ADC 1.	R/W	0
25	ADC2_ CONV_ INT_EN	ADC 2 Conversion Done Interrupt Enable See description for ADC 1.	R/W	0
24	ADC1_ CONV_ INT_EN	ADC 1 Conversion Done Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
23:18	-	Reserved (D/A)	-	-
17	DAC2_ CONV_ INT_EN	DAC 2 Convert Event Interrupt Enable See description for DAC 1.	R/W	0
16	DAC1_ CONV_ INT_EN	DAC 1 Convert Event Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
15:3	-	Reserved (A/D)	-	-
12	AD_SEQ_ CONV_ DONE_ INT_EN	A/D Sequencer Block/Frame Conversions Done Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
11-9	-	Reserved (A/D)	-	-

Bit	Symbol	Description	Access	Reset Value
8	AD_SEQ_DMA_TERM_INT_EN	A/D Sequencer DMA Buffer Termination Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
7:5	-	Reserved (D/A)	-	-
4	DA_SEQ_CONV_DONE_INT_EN	D/A Sequencer Block/Frame Conversions Done Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
3:1	-	Reserved (D/A)	-	-
0	DA_SEQ_DMA_DONE_INT_EN	D/A Sequencer DMA Buffer Done Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0

Table 5-61 : Interrupt Enable Register (0x36C)

5.9.1.2 Error Interrupt Enable Register (0x370)

Bit	Symbol	Description	Access	Reset Value
Sequencer Error Interrupt Enable				
31:28	-	Reserved (A/D)	-	-
27	AD_SEQ_FRAME_ERR_INT_EN	A/D Sequencer Frame Error Interrupt Status 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
26	AD_SEQ_CONV_TIME_ERR_INT_EN	A/D Sequencer Conversion Timing Error Interrupt Status 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
25	AD_SEQ_CONV_DATA_ERR_INT_EN	A/D Sequencer Conversion Data Error Interrupt Status 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
24	AD_SEQ_DMA_ERR_INT_EN	A/D Sequencer DMA Error Interrupt Status 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
23:20	-	Reserved (D/A)	-	-
19	DA_SEQ_FRAME_ERR_INT_EN	D/A Sequencer Frame Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0

Bit	Symbol	Description	Access	Reset Value
18	DA_SEQ_ CONV_ TIME_ ERR_ INT_EN	D/A Sequencer Conversion Timing Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
17	DA_SEQ_ CONV_ DATA_ ERR_ INT_EN	D/A Sequencer Conversion Data Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
16	DA_SEQ_ DMA_ ERR_ INT_EN	D/A Sequencer DMA Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
Device Error Interrupt Enable				
15:8	-	Reserved (A/D)	-	-
7:2	-	Reserved (D/A)	-	-
1	DAC2_ ERR_ INT_EN	DAC 2 Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0
0	DAC1_ ERR_ INT_EN	DAC 1 Error Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See Interrupt Status Register for Description.	R/W	0

Table 5-62 : Error Interrupt Enable Register (0x370)

5.9.1.3 DIO Rising Edge Interrupt Enable Register (0x374)

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	DIO8_ RISE_ INT_EN	DIO 8 Rising Edge Interrupt Enable See description for DIO1.	R/W	0
6	DIO7_ RISE_ INT_EN	DIO 7 Rising Edge Interrupt Enable See description for DIO1.	R/W	0
5	DIO6_ RISE_ INT_EN	DIO 6 Rising Edge Interrupt Enable See description for DIO1.	R/W	0
4	DIO5_ RISE_ INT_EN	DIO 5 Rising Edge Interrupt Enable See description for DIO1.	R/W	0
3	DIO4_ RISE_ INT_EN	DIO 4 Rising Edge Interrupt Enable See description for DIO1.	R/W	0
2	DIO3_ RISE_ INT_EN	DIO 3 Rising Edge Interrupt Enable See description for DIO1.	R/W	0
1	DIO2_ RISE_ INT_EN	DIO 2 Rising Edge Interrupt Enable See description for DIO1.	R/W	0
0	DIO1_ RISE_ INT_EN	DIO 1 Rising Edge Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See DIO Interrupt Status Register.	R/W	0

Table 5-63 : DIO Rising Edge Interrupt Enable Register (0x374)

5.9.1.4 DIO Falling Edge Interrupt Enable Register (0x378)

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	DIO8_ FALL_ INT_EN	DIO 8 Falling Edge Interrupt Enable See description for DIO1.	R/W	0
6	DIO7_ FALL_ INT_EN	DIO 7 Falling Edge Interrupt Enable See description for DIO1.	R/W	0
5	DIO6_ FALL_ INT_EN	DIO 6 Falling Edge Interrupt Enable See description for DIO1.	R/W	0
4	DIO5_ FALL_ INT_EN	DIO 5 Falling Edge Interrupt Enable See description for DIO1.	R/W	0
3	DIO4_ FALL__ INT_EN	DIO 4 Falling Edge Interrupt Enable See description for DIO1.	R/W	0
2	DIO3_ FALL_ INT_EN	DIO 3 Falling Edge Interrupt Enable See description for DIO1.	R/W	0
1	DIO2_ FALL_ INT_EN	DIO 2 Falling Edge Interrupt Enable See description for DIO1.	R/W	0
0	DIO1_ FALL_ INT_EN	DIO 1 Falling Edge Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled See DIO Interrupt Status Register.	R/W	0

Table 5-64 : DIO Falling Edge Interrupt Enable Register (0x378)

5.9.2 Interrupt Status Register

For an interrupt status bit to be set, the interrupt must be enabled prior to the interrupt event.

Active interrupts can only be cleared by an interrupt acknowledge process (not by disabling the interrupt).

The actual interrupt acknowledge process depends on the appropriate setting in the Global Configuration Register (either clear-by-status-write or clear-by-status-read).

5.9.2.1 Interrupt Status Register (0x384)

A PCI interrupt is asserted if any bit is set in the Interrupt Status Register.

Bit	Symbol	Description	Access	Reset Value
31	DIO_INT	Digital I/O Interrupt This bit is set if there is any bit set in the DIO Interrupt Status Register.	R	0
30	ERR_ INT	Error Interrupt This bit is set if there is any bit set in the Error Interrupt Status Register.	R	0
29	FTIM_ INT	Frame Timer Event Interrupt If enabled, this bit is set upon a frame timer event (frame timer has expired)	R/C	0
28	FTRIG _INT	Frame Trigger Event Interrupt If enabled, this bit is set upon a frame trigger signal event (selected signal source).	R/C	0
27	ADC4_ CONV_ INT	ADC 4 Conversion Done Interrupt (mainly for Manual Mode) See description for ADC 1.	R/C	0
26	ADC3_ CONV_ INT	ADC 3 Conversion Done Interrupt (mainly for Manual Mode) See description for ADC 1.	R/C	0
25	ADC2_ CONV_ INT	ADC 2 Conversion Done Interrupt (mainly for Manual Mode) See description for ADC 1.	R/C	0
24	ADC1_ CONV_ INT	ADC 1 Conversion Done Interrupt (mainly for Manual Mode) If enabled, this bit is set after a conversion on ADC 1 when all ADC conversion data becomes available in the ADC Data Registers.	R/C	0
23:18	-	Reserved (D/A)	-	-
17	DAC2_ CONV_ INT	DAC 2 Conversion Done Interrupt (mainly for Manual Mode) See description for DAC 1.	R/C	0
16	DAC1_ CONV_ INT	DAC 1 Conversion Done Interrupt (mainly for Manual Mode) If enabled, this bit is set upon a DAC conversion event (the DAC analog outputs have just been updated).	R/C	0
15:13	-	Reserved (A/D)	-	-
12	AD_ SEQ_ CONV_ DONE_ INT	A/D Sequencer Block/Frame Conversions Done Interrupt If enabled, the interrupt status bit is set when the configured number of conversions has been performed per request (Normal Mode) or frame (Frame Mode) or in case of an error (Frame Error, Conversion Error or Underflow Error).	R/C	0

Bit	Symbol	Description	Access	Reset Value
11	-	Reserved (D/A)	-	-
10:8	AD_ SEQ_ DMA_ TERM_ INT	A/D Sequencer DMA Buffer Termination Interrupt If enabled, the interrupt status bit is set upon a DMA Buffer termination event. Bit 10: DMA Buffer terminated because of an error. Bit 9: DMA Buffer terminated because all requested data has been transferred to the DMA Buffer. Bit 8: DMA Buffer terminated because the buffer is completely filled with data. See also A/D Sequencer Status Register.	R/C	000
7:5	-	Reserved (D/A)	-	-
4	DA_ SEQ_ CONV_ DONE_ INT	D/A Sequencer Block/Frame Conversions Done Interrupt If enabled, the interrupt status bit is set when the configured number of conversions has been performed per request (Normal Mode) or frame (Frame Mode) or in case of an error (Frame Error, Conversion Error or Underflow Error).	R/C	0
3:1	-	Reserved (D/A)	-	-
0	DA_ SEQ_ DMA_ DONE_ INT	D/A Sequencer DMA Buffer Done Interrupt If enabled, the interrupt status bit is set when all requested data has been fetched from the DMA Buffer.	R/C	0

Table 5-65 : Interrupt Status Register (0x384)

5.9.2.2 Error Interrupt Status Register (0x388)

Bit	Symbol	Description	Access	Reset Value
Sequencer Error Interrupt Status				
31:28	-	Reserved (A/D)	-	-
27	AD_SEQ_FRAME_ERR_INT	A/D Sequencer Frame Error Interrupt If enabled, this bit is set upon a sequencer frame error event (e.g. the start of the next frame has been detected but the configured number of conversions for the current frame has not been processed so far). In case of an error event, the sequencer operation is stopped. See Sequencer Status Register for status information.	R/C	0
26	AD_SEQ_CONV_TIME_ERR_INT	A/D Sequencer Conversion Timing Error Interrupt If enabled, this bit is set upon a sequencer conversion timing error event (e.g. the next conversion is due while a conversion process is still in progress). In case of an error event, the sequencer operation is stopped. See Sequencer Status Register for status information.	R/C	0
25	AD_SEQ_CONV_DATA_ERR_INT	A/D Sequencer Conversion Data Error Interrupt If enabled, this bit is set upon a sequencer conversion data error event (e.g. FIFO data overflow). In case of an error event, the sequencer operation is stopped. See Sequencer Status Register for status information.	R/C	0
24	AD_SEQ_DMA_ERR_INT	A/D Sequencer DMA Error Interrupt If enabled, this bit is set upon a DMA engine error event (e.g. PCI Target Abort). In case of a DMA error event, the sequencer's DMA engine operation is stopped. See Sequencer Status Register for status information.	R/C	0
23:20	-	Reserved (D/A)	-	-
19	DA_SEQ_FRAME_ERR_INT	D/A Sequencer Frame Error Interrupt If enabled, this bit is set upon a sequencer frame error event (e.g. the start of the next frame is has been detected but the configured number of conversions for the current frame has not been processed so far). In case of an error event, the sequencer operation is stopped. See Sequencer Status Register for status information.	R/C	0
18	DA_SEQ_CONV_TIME_ERR_INT	D/A Sequencer Conversion Timing Error Interrupt If enabled, this bit is set upon a sequencer conversion timing error event (e.g. the next conversion is due while a conversion process is still in progress). In case of an error event, the sequencer operation is stopped. See Sequencer Status Register for status information.	R/C	0

Bit	Symbol	Description	Access	Reset Value
17	DA_SEQ_ CONV_ DATA_ ERR_INT	D/A Sequencer Conversion Data Error Interrupt If enabled, this bit is set upon a sequencer conversion data error event (e.g. a next conversion is due but the associated DAC devices are not completely pre-loaded with data for the next conversion). In case of an error event, the sequencer operation is stopped. See Sequencer Status Register for status information.	R/C	0
16	DA_SEQ_ DMA_ ERR_INT	D/A Sequencer DMA Error Interrupt If enabled, this bit is set upon a DMA engine error event (e.g. PCI Target Abort). In case of a DMA error event, the sequencer's DMA engine operation is stopped. See Sequencer Status Register for status information.	R/C	0
Device Error Interrupt Status				
15:8	-	Reserved (A/D)	-	-
7:2	-	Reserved (D/A)	-	-
1	DAC2_ ERR_ INT	DAC 2 Error Interrupt See description for DAC 1.	R/C	0
0	DAC1_ ERR_ INT	DAC 1 Error Interrupt If enabled, this bit is set upon a DAC FAULT event. See Global DAC Status Register.	R/C	0

Table 5-66 : Error Interrupt Status Register (0x388)

5.9.2.3 DIO Interrupt Status Register (0x38C)

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	-
7	DIO8_INT	Digital I/O 8 Interrupt Status See description for Digital I/O 1.	R/C	0
6	DIO7_INT	Digital I/O 7 Interrupt Status See description for Digital I/O 1.	R/C	0
5	DIO6_INT	Digital I/O 6 Interrupt Status See description for Digital I/O 1.	R/C	0
4	DIO5_INT	Digital I/O 4 Interrupt Status See description for Digital I/O 1.	R/C	0
3	DIO4_INT	Digital I/O 4 Interrupt Status See description for Digital I/O 1.	R/C	0
2	DIO3_INT	Digital I/O 3 Interrupt Status See description for Digital I/O 1.	R/C	0
1	DIO2_INT	Digital I/O 2 Interrupt Status See description for Digital I/O 1.	R/C	0
0	DIO1_INT	Digital I/O 1 Interrupt Status If enabled, the interrupt status bit is set upon a rising and/or falling edge of the Digital I/O input signal (depending on the configuration of the DIO Rising/Falling Edge Interrupt Enable Registers).	R/C	0

Table 5-67 : DIO Interrupt Status Register (0x38C)

5.10 Other Registers

5.10.1 Global Configuration Register (0x398)

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1	INT_ ACK_ MODE	Interrupt Acknowledge Mode Sets the Interrupt Acknowledge Mode. 0: Clear by Write Mode 1: Clear on Read Mode Clear by Write Mode: Interrupts are acknowledged by writing a '1' to the appropriate interrupt status register bit. Clear on Read Mode: Interrupts are cleared when the appropriate interrupt status register is read. (Hint: clearing granularity is 8 bit, byte-enable based)	R/W	0
0	DMA_ ENDIAN_ MODE	DMA Endian Mode Sets the Endian Mode for DMA access from/to Host Memory in Sequencer Mode. Common for A/D and D/A sequencer operation. 0: Little Endian Mode 16 bit digital A/D and D/A values are stored in Little Endian format in Host Memory. 1: Big Endian Mode 16 bit digital A/D and D/A values are stored in Big Endian format in Host Memory.	R/W	0

Table 5-68 : Global Configuration Register (0x398)

5.10.2 DIO Pull Reference Register (0x39C)

Each of the Digital Front I/O lines is connected to an on-board 4.7kΩ pull resistor.

The common reference voltage for all the pull resistors is configurable to be either +3.3V, +5V, GND or floating.

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1:0	DIO_ VPULL	Digital I/O Pull Resistor Reference Configuration 1:0 — DIO Pull Resistor Reference 00 — Floating 01 — +5V (Pull-Ups) 10 — +3.3V (Pull-Ups) 11 — GND (Pull-Downs)	R/W	00

Table 5-69 : DIO Pull Reference Register (0x39C)

Note that in the default case (Floating), the pull resistors are all connected to each other on the floating reference signal side. Hence, the digital I/O lines are connected to each other through the pull-resistors.

5.10.3 P14 I/O Pull Reference Register (0x3A0)

Each digital P14 I/O signal (CONV_CLK1, CONV_CLK2 and FRAME_TRIG) has a 4K7 pull resistor to a common reference.

The common reference voltage for all the pull resistors is configurable to be either +3.3V, +5V, GND or floating.

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1:0	P14_ VPULL	P14 I/O Pull Resistor Reference Configuration 1:0 — P14 Pull Resistor Reference 00 — Floating 01 — +5V (Pull-Ups) 10 — +3.3V (Pull-Ups) 11 — GND (Pull-Downs)	R/W	00

Table 5-70 : P14 I/O Pull Reference Register (0x3A0)

Note that in the default case (Floating), the pull resistors are all connected to each other on the floating reference signal side. Hence, the digital I/O lines are connected to each other through the pull-resistors.

5.10.4 Correction Data EEPROM Control/Status Register (0x3A4)

Bit	Symbol	Description	Access	Reset Value
31:17	-	Reserved	-	-
16	EEBSY	Read-only Activity Status of the onboard Correction Data EEPROM 0: Correction Data EEPROM Not Busy 1: Correction Data EEPROM Busy After power-up or PCI reset, the content of the Correction Data EEPROM is automatically copied to the Correction Data Space. During this process, the EEBSY is set. The EEBSY bit is also set during an EEPROM update procedure (see EELOCK bit). Software should check that the EEBSY bit is '0' before reading data from the Correction Data Space (data valid indication).	R	0
15:0	EELOCK	Correction Data EEPROM Lock This field must be set to the value 0xABCD to allow write access to the Correction Data Space. Writes to the Correction Data Space are ignored otherwise. When the value of this field is changed from 0xABCD to a different value, an automatic EEPROM update procedure is started: The content of the Correction Data Space is programmed to the onboard Correction Data EEPROM, and is immediately read back to the Correction Data Space. The EEBSY bit is set during this procedure. Before setting EELOCK to 0xABCD, software should check that the EEBSY bit is clear.	R/W	0x0000

Table 5-71 : Correction Data EEPROM Control/Status Register (0x3A4)

5.10.5 Temperature Sensor Trigger Register (0x3A8)

This register is used to trigger a measurement of the onboard temperature sensor.

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1	TS_AUTO	Temperature Sensor Auto Acquire Mode If this bit is set, the Temperature Sensor Data Register is automatically updated every second. If this bit is cleared, the Temperature Sensor Trigger bit must be set for an update of the Temperature Sensor Data Register.	R/W	0
0	TS_TRIG	Temperature Sensor Trigger Write ‘1’ to start reading the data from the onboard temperature sensor. This bit is cleared automatically when the data is valid in the Temperature Sensor Data Register.	R/S	0

Table 5-72 : Temperature Sensor Trigger Register (0x3A8)

5.10.6 Temperature Sensor Data Register (0x3AC)

This register holds the measured 13bit two's complement data of the onboard temperature sensor.

Bit	Symbol	Description	Access	Reset Value
31:0	TEMP	Measured data of the onboard temperature sensor The read value of the temperature sensor is stored sign-extended as a 32 bit two's complement. To actually calculate the temperature from the two's complement data value, use the following formula: Temperature (°C) = TEMP/256	R	0

Table 5-73 : Temperature Sensor Data Register (0x3AC)

5.10.7 Firmware Version Register (0x3FC)

Bit	Symbol	Description	Access	Reset Value
31:0	FID	Major version, minor version, revision and build number of the installed FPGA firmware.	R	x

Table 5-74 : Firmware Version Register (0x3FC)

6 Analog Inputs

6.1 ADC Device

The Analog Devices ADAS3022 ADC device is used for the analog inputs.

The ADAS3022 is a multi-channel ADC device that consists of an integrated channel multiplexer to the select the active channel for the internal programmable gain amplifier and SAR ADC. Each ADAS3022 device provides eight (8) analog input signals that may be either used in a differential manner (up to 4 differential channels IN[0:3] per device) or in a single-ended manner (up to 8 single-ended channels IN[0:7] per device).

On the TPMC534, all channels of an ADC device are always operating in the same general input mode (either differential or single ended). The general input mode (differential or single-ended) may be different for each of the on-board ADC devices.

The TPMC543-10R features 4 ADAS3022 ADC devices.

6.2 Analog Input Hardware Configurations

On the TPMC543, the analog input channels of an ADC device are hardware-configured (build-option) for either analog current input or analog high-voltage input operation.

The ADC devices (and the corresponding analog input channels) can only be used with input ranges according to their analog input hardware configuration (e.g. ADC devices that are hardware configured to provide analog current input channels cannot be used to provide analog voltage input channels) and must be software configured accordingly. The analog input hardware configuration may be different for each of the on-board ADC devices.

Available Analog Input Hardware Configurations are:

- Current input
  - ±25mA in differential mode
- High-Voltage input:
  - ±10V, ±20V, ±40, ±48V in single-ended mode
  - ±20V, ±40V, ±80, ±96V in differential mode

Per se each ADC device may have a dedicated analog input hardware configuration. The actual analog input hardware configuration is fix and depends on the order option.

The following table shows the provided number of analog input channels for the TPMC543-10R (SE: Single-Ended, DF: Differential).

Analog Input Configuration	A/D Channels
	TPMC543-10R
Current Input Channels	8 (DF)
High-Voltage Input Channels	16 (SE) / 8 (DF)

Table 6-1 : Number of Analog Input Channels per Configuration (TPMC543-10R)

The following table shows the analog input hardware configuration of each ADC device for the TPMC543-10R (SE: Single-Ended, DF: Differential, CUR: Current Input, HV: High-Voltage Input).

TPMC543 ADC Device	TPMC543-10R
ADC#1	4x CUR (DF)
ADC#2	4x CUR (DF)
ADC#3	8x/4x HV (SE/DF)
ADC#4	8x/4x HV (SE/DF)

Table 6-2 : ADC Device Hardware Configuration (TPMC543-10R)

The on-board ADC devices of a given order option must be software configured according to the designated Analog Input Hardware Configuration shown in the table above. See the ADC Configuration Register description and the following sub-chapters for additional configuration hints.

6.2.1 Current Inputs

The Current Analog Input Configuration supports currents in the range -25mA … +25mA.

6.2.1.1 Analog Input Circuit

The Current Analog Input Circuit is a modified version of the Standard Analog Voltage Input Circuit.

For the (differential) analog current inputs, the passive part of the analog input circuit represents a 75Ω + 100Ω + 75Ω resistor chain, representing a total input resistance of 250Ω. The high-precision 100Ω resistor is used for the actual current/voltage conversion. The 75Ω resistors are also part of a 1st order low pass noise filter.

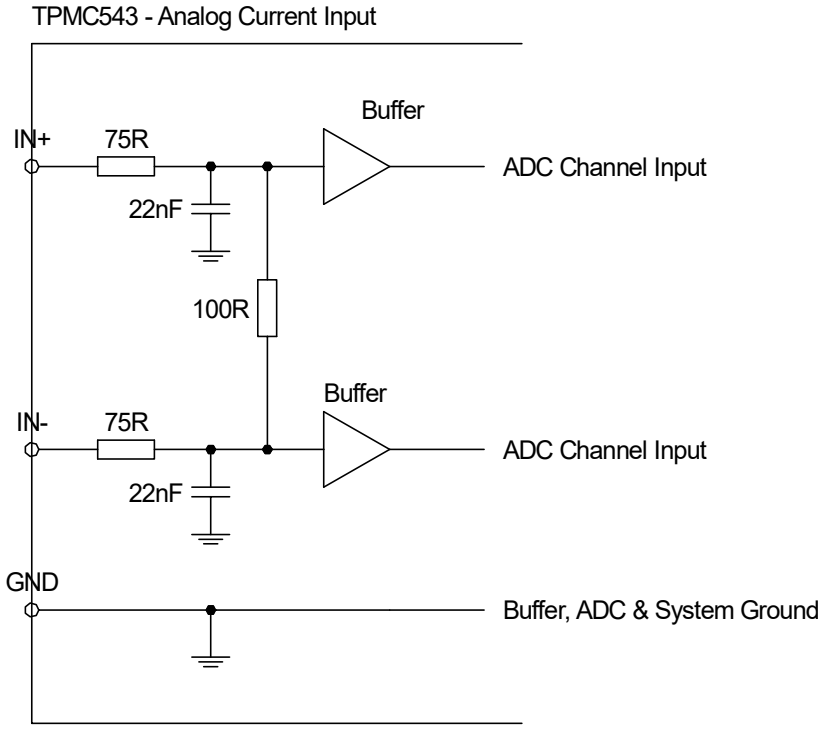


Figure 6-1 : Analog Current Input Circuit

6.2.1.2 Analog Input Mode

The analog current inputs are only used in a differential manner, so there is an IN+ input and an IN- input for each current input.

For each ADC device operating in differential mode, the differential A/D channels 0 …3 are available (I/O signals ADC#_IN[0:3]+ and ADC#_IN[0:3]-).

6.2.1.3 Analog Input Range

With the modification in the passive part of the analog input circuit, a certain input current range can be applied by using an existing ADC gain (voltage range) as described in the table below.

ADC Analog Voltage Input Range (DF = Differential)				I/O Interface Analog Current Input Range (DF = Differential)				
Gain	LSB	Input Range (DF)	#Bits	LSB* $= \frac{LSB}{100\Omega}$	Input Range (DF)	Digital +FS Value	Input Range (DF)	Digital +FS Value
1.6	78.125uV	±2.56V	16	**781.25nA**	±25.6mA	32767	**±25mA**	32000

Table 6-3 : Analog Current Input Range A/D Channel Gain Configuration (DF)

For using the analog inputs in the ±25mA analog input hardware configuration, the corresponding A/D channels must be software configured to operate with Gain 1.6 (respectively in the ADC ±2.56V differential input voltage range) as shown in the table above.

For the full positive input current of 25mA, the total current input resistance of 250Ω generates a voltage drop of up to 6.25VDC (which must be delivered by the external current transmitter/supply).

Note that even for the analog current inputs, the active part of the TPMC543 analog input circuit is still operating as a non-isolated analog voltage input circuit.

Care must be taken regarding the allowed voltage levels on the analog IN+ and IN- inputs referenced to the PMC system ground. The voltage levels on the IN+ and IN- inputs must not exceed ±10.24V per pin relative to ground! Otherwise the TPMC543 ADC common mode voltage ratings would be violated!

Care must be taken regarding the allowed maximum current and maximum differential voltage applied to a current input. The input current must be within the range of -25mA … +25mA! The differential input voltage applied to a current input must not exceed the range -6.25V … +6.25V! Otherwise the power ratings of the resistors in the current input stage would be exceeded and the resistors may get damaged!

6.2.1.4 A/D Data Coding (Current Input Configuration)

The A/D data coding is always Two's Complement.

See ADC Configuration Register(s) for the actual GAIN value.

Digital Code	Analog Input Current (V_{REF} = 4.096V)	Description
0x7FFF	(32767/32768) x (V_{REF}/GAIN) / 100Ω	Pos. Full Scale – 1 LSB
0x0001	(1/32768) x V_{REF}/GAIN / 100Ω	Mid-Scale + 1 LSB
0x0000	0V / 100Ω	Mid-Scale
0xFFFF	– (1/32768) x V_{REF}/GAIN / 100Ω	Mid-Scale – 1 LSB
0x8001	– (32767/32768) x V_{REF}/GAIN / 100Ω	Neg. Full-Scale + 1 LSB
0x8000	– V_{REF}/GAIN / 100Ω	Neg. Full-Scale

Table 6-4 : A/D Data Coding (Current Input Configuration)

6.2.1.5 Current Input External Wiring Hints

With the analog current inputs, special care must be taken regarding the external wiring for the various current transmitter types and configurations.

The list below summarizes some points to keep in mind:

- The TPMC543 current loop receiver (or analog current input) is not floating or isolated!

  The TPMC543 current loop receiver is non-isolated and operates in relation to the TPMC543 system ground (which equals the PMC carrier system's earth/protection ground for typical DC systems).

- On the TPMC543 the input current is passed through an on-board precision sense resistor for current-to-voltage conversion. The resulting sense voltage is fed to a differential ADC voltage input.

- The ADC input common mode voltage range must not be violated!

  The voltage levels on the IN+ and IN- I/O pins must not exceed ±10.24 relative to the TPMC543 ground!

- The analog input current must be kept within the defined current range!

  The differential voltage occurring at the differential current input must not exceed the range -6.25V … +6.25V. With the given input resistance of 250Ω this is equivalent to a current input range of -25mA … +25mA.

  The ±25mA current range covers typical loop current ranges of 0…20mA, 4…20mA or 0…24mA.

The following sub-chapters provide some example configurations and appropriate external wiring hints for the ±25mA current range.

6.2.1.5.1 2-Wire Transmitter, Non-Isolated Power Supply

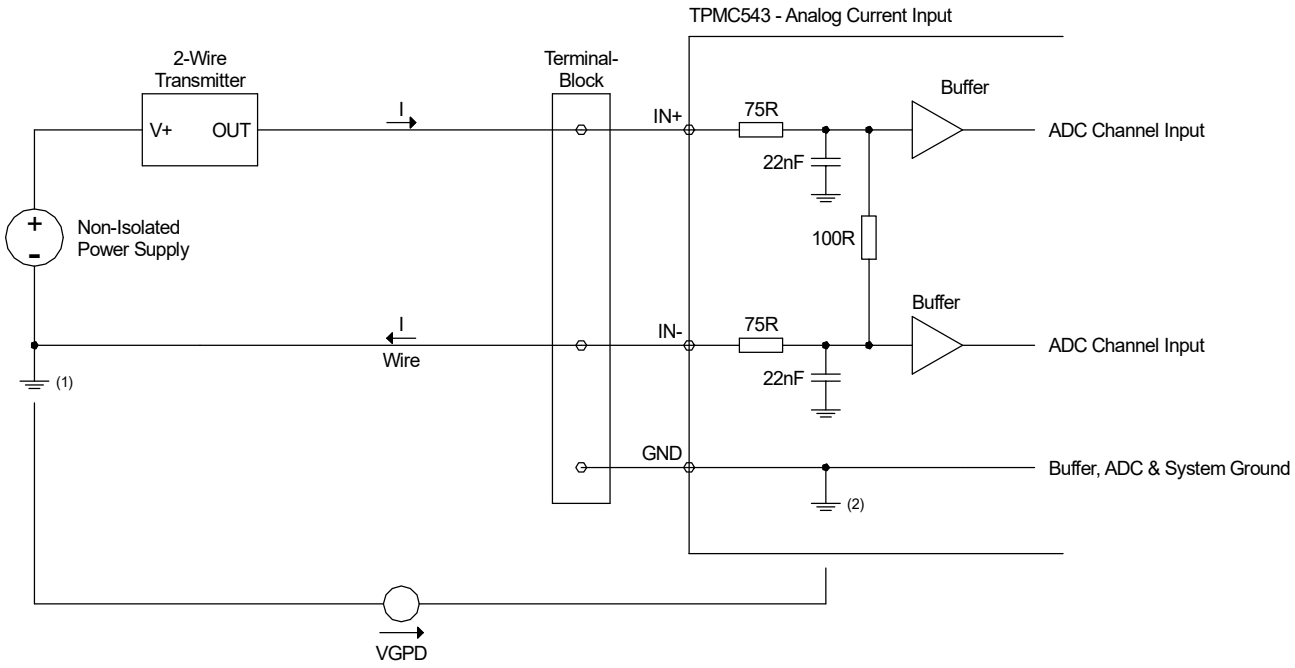


Figure 6-2 : 2-Wire Transmitter, Non-Isolated Power Supply, Low-Side Sensing

The external wiring scheme shown above requires keeping the (earth/protection) ground potential difference (GPD) between the Sensor/Transmitter system and the TPMC543 system under control, since this voltage adds (or might add) to the voltage level on the TPMC543 analog input pin. Measures must be taken to ensure that V_{GPD} does not exceed a couple of volts!

$$V_{IN+(max)} = I \times (75\Omega + 100\Omega + 75\Omega + R_{Wire}) + V_{GPD} \leq 10.24V$$

$$R_{Wire} \leq \frac{10.24V - V_{GPD}}{I} - (75\Omega + 100\Omega + 75\Omega)$$

The current is sourced by the external power supply positive terminal and returns to the power supply negative terminal.

Note that an additional I/O wire connection between the TPMC543 IN- and GND pins right at or close to the TPMC543 I/O connector might cause a part of the loop return current to take a path along the site's earth/protection ground wire installation (instead of flowing only in the IN- I/O wire connection as intended).

Note that an additional I/O ground wire connection between the TPMC543 GND pin and the loop power supply ground would provide an additional path for GPD currents already present in the site's electrical installation. As a result, such an I/O ground wire connection might have to carry unrelated GPD currents of unknown size.

The DC power supply must be capable to provide the minimum voltage drop required by the transmitter plus two-times the voltage drop on a wire connection plus the voltage drop on the TPMC543 analog current input circuit (6.25V @ 25mA).

A sinking current transmitter configuration (High-Side Sensing) as shown below must be avoided since this would most likely violate the TPMC543 ADC input common mode voltage rating because the external power supply voltage directly connects to the TPMC543 I/O pin (without being regulated by the current transmitter).

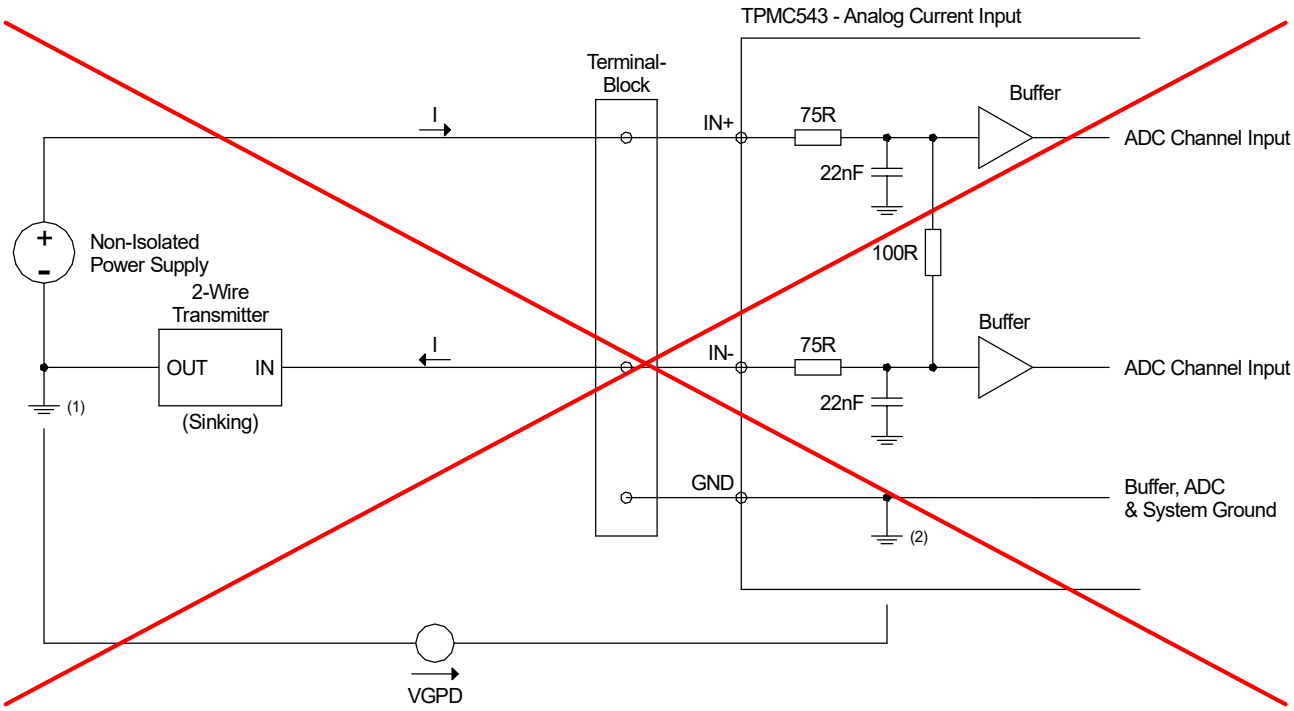


Figure 4 4 : 2-Wire Transmitter, Non-Isolated Power Supply, High-Side Sensing

$$V\_(IN+(max))=V\_(DC\ SUPPLY) + V\_GPD - I \times R\_Wire \leq 10.24V$$

6.2.1.5.2 2-Wire Transmitter, Isolated Power Supply

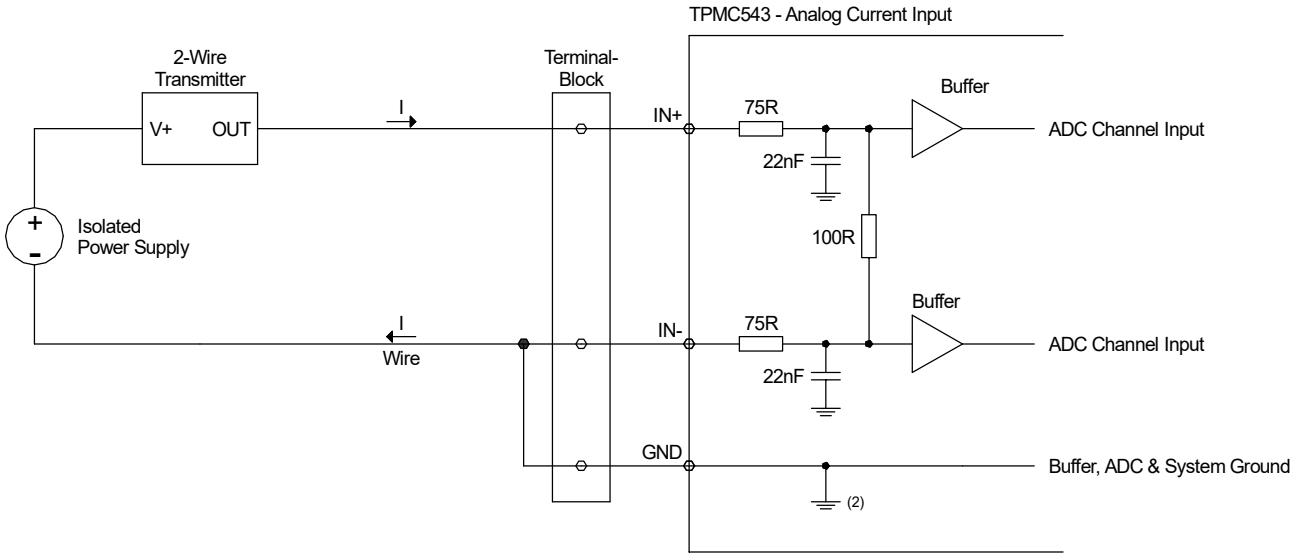


Figure 6-3 : 2-Wire Transmitter, Isolated Power Supply

The external wiring scheme shown above requires an additional external connection between the IN- pin and the GND pin (at close range, i.e. at the first terminal block).

The current is sourced by the isolated power supply positive terminal and returns to the isolated power supply negative terminal.

The DC power supply must be capable to provide the minimum voltage drop required by the transmitter plus two-times the voltage drop of a wire connection plus the voltage drop on the TPMC543 analog current input circuit (6.25V @ 25mA).

6.2.1.5.3 3-Wire Transmitter, Non-Isolated Power Supply

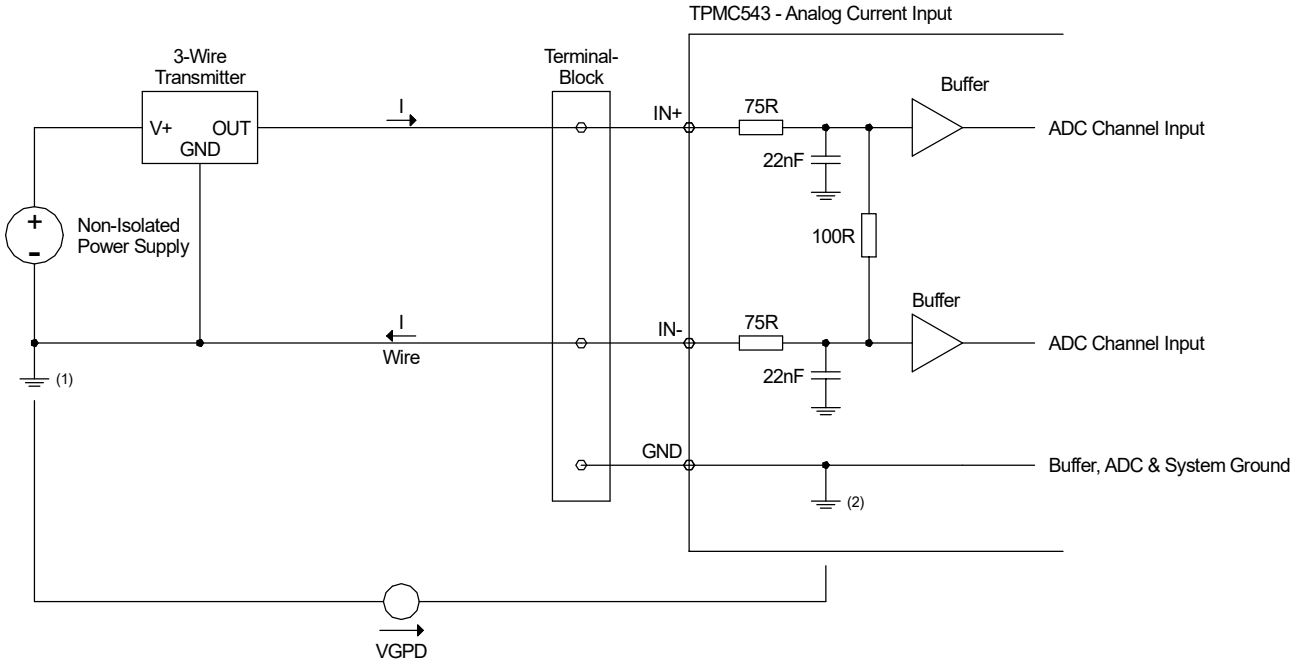


Figure 6-4 : 3-Wire Transmitter, Non-Isolated Power Supply

The external wiring scheme shown above requires keeping the (earth/protection) ground potential difference (GPD) between the Sensor/Transmitter system and the TPMC543 system under control, since this voltage adds (or might add) to the voltage level on the TPMC543 analog input pin. Measures must be taken to ensure that V_{GPD} does not exceed a couple of volts!

$$V_{IN+(max)} = I \times (75\Omega + 100\Omega + 75\Omega + R_{Wire}) + V_{GPD} \leq 10.24V$$

$$R_{Wire} \leq \frac{10.24V - V_{GPD}}{I} - (75\Omega + 100\Omega + 75\Omega)$$

The current is sourced by the external power supply positive terminal and returns to the power supply negative terminal.

Note that an additional I/O wire connection between the TPMC543 IN- and GND pins right at or close to the TPMC543 I/O connector might cause a part of the loop return current to take a path along the site's earth/protection ground wire installation (instead of flowing only in the IN- I/O wire connection as intended).

Note that an additional I/O ground wire connection between the TPMC543 GND pin and the loop power supply ground would provide an additional path for GPD currents already present in the site's electrical installation. As a result, such an I/O ground wire connection might have to carry unrelated GPD currents of unknown size.

The DC power supply must be capable to provide the minimum voltage drop required by the transmitter plus two-times the voltage drop on a wire connection plus the voltage drop on the TPMC543 analog current input circuit (6.25V @ 25mA).

6.2.1.5.4 4-Wire Transmitter, Isolated Transmitter

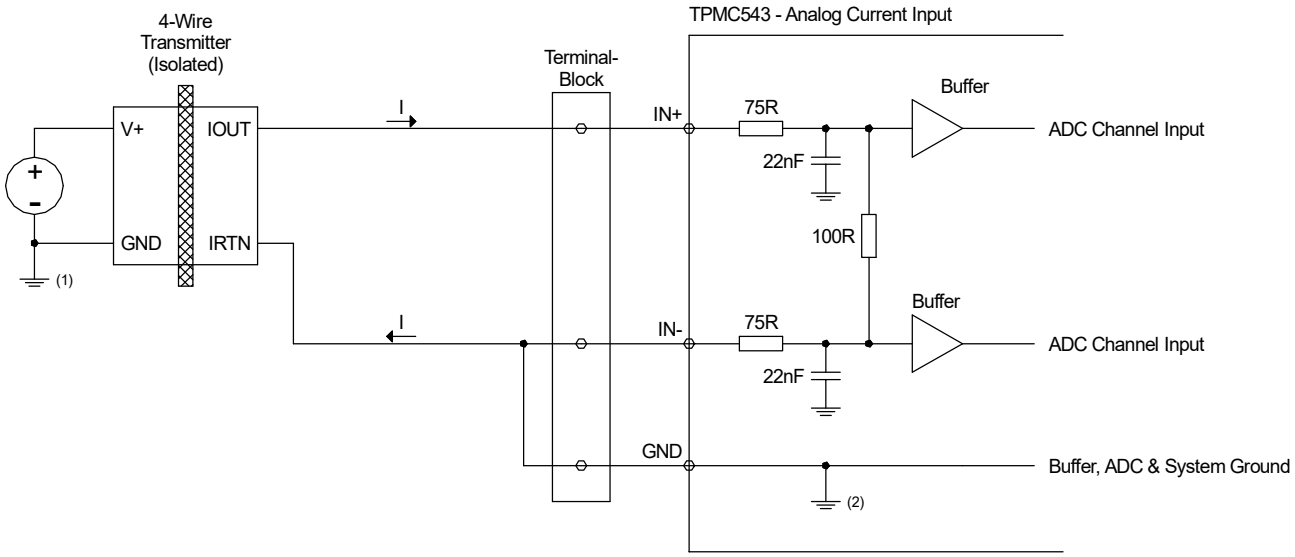


Figure 6-5 : 4-Wire Transmitter, Isolated Transmitter

The external wiring scheme shown above requires an additional external connection between the TPMC543 IN- pin and GND pin (at close range, i.e. at the first terminal block).

The current is sourced by the isolated transmitter I_{OUT} terminal and returns to the isolated transmitter I_{RTN} terminal.

The isolated transmitter must be capable to provide the voltage drop on the TPMC543 analog current input circuit (6.25V @ 25mA) plus two-times the voltage drop of a wire connection.

6.2.2 High-Voltage Inputs

The High-Voltage Analog Input Configuration supports single-ended voltages of up to ±48V (and symmetrical differential voltages of up to ±96V).

6.2.2.1 Analog Input Circuit

The High-Voltage Analog Input Circuit is a modified version of the Standard-Voltage Analog Input Circuit.

For the (single-ended) analog high-voltage inputs, the passive part of the analog input circuit represents an input voltage resistor divider that acts (approximately) as a divide-by-4 stage (249/999).

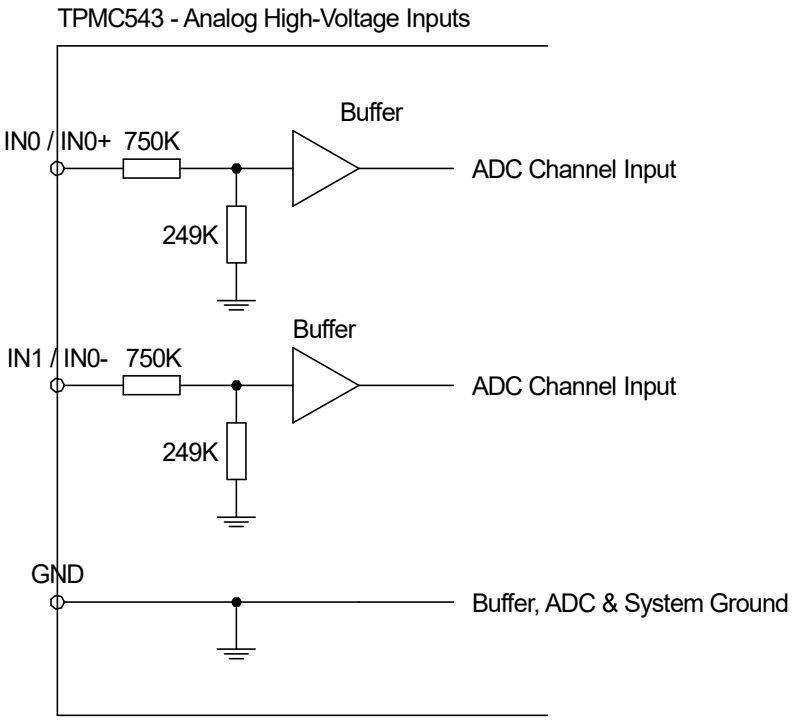


Figure 6-6 : High-Voltage Analog Input Circuit

The single-ended analog input DC resistance is approximately 1MΩ (999K).

6.2.2.2 Analog Input Mode

The analog high-voltage inputs are intended to be used in a single-ended manner, referenced to ground (though they may also be used in a differential manner).

For each ADC device operating in single-ended mode, the single-ended A/D channels 0 …7 are available (I/O signals ADC#_IN[0:7] and GND).

Care must be taken as there may be on-board voltage potentials of about twice the highest voltage (e.g. the voltage between the IN0 and IN1 I/O pins is 96V when the IN0 voltage is at +48V while the IN1 voltage is at -48V referenced to ground).

6.2.2.3 Analog Input Ranges

With the added resistor divider in the passive part of the analog input circuit, higher external I/O voltages can be applied by using the existing ADC gains and ranges (of the Standard-Voltage Input option) as described in the table below.

ADC Device Analog Voltage Input Ranges (SE = Single-Ended)				I/O Interface Analog High-Voltage Input Ranges (SE = Single-Ended)				
Gain	LSB	Input Range (SE)	#Bits	LSB* $= \frac{999}{249} \times LSB$	Input Range (SE)	Digital +FS Value	Input Range (SE)	Digital +FS Value
0.166..	750uV	±12.288V	15	**3.009..mV**	±49.300V	16383	**±48V**	15952
0.4	312.5uV	±10.24V	16	**1.253..mV**	±41.083V	32767	**±40V**	31903
0.8	156.25uV	±5.12V	16	**0.626..mV**	±20.542V	32767	**±20V**	31903
1.6	78.125uV	±2.56V	16	**0.313..mV**	±10.271V	32767	**±10V**	31903

Table 6-5 : High-Voltage Analog Input Range A/D Channel Gain Configuration (SE)

For Single-Ended (SE) High-Voltage application, the input signal range (to Ground) must be within the selected Single-Ended High-Voltage Input Range.

ADC Device Analog Voltage Input Ranges (DF = Differential)				I/O Interface Analog High-Voltage Input Ranges (DF = Differential)				
Gain	LSB	Input Range (DF)	#Bits	LSB* $= \frac{999}{249} \times LSB$	Input Range (DF)	Digital +FS Value	Input Range (DF)	Digital +FS Value
0.166..	750uV	±24.576V	16	**3.009..mV**	±98.600..V	32767	**±96V**	31903
0.2	625uV	±20.48V	16	**2.507..mV**	±82.166..V	32767	**±80V**	31903
0.4	312.5uV	±10.24V	16	**1.253..mV**	±41.083..V	32767	**±40V**	31903
0.8	156.25uV	±5.12V	16	**0.626..mV**	±20.541..V	32767	**±20V**	31903
1.6	78.125uV	±2.56V	16	**0.313..mV**	±10.270..V	32767	**±10V**	31903

Table 6-6 : High-Voltage Analog Input Range A/D Channel Gain Configuration (DF)

For using the analog inputs with the High-Voltage Analog Input (Hardware) Configuration, the corresponding A/D channels must be configured to operate with the appropriate ADC gain or input range as shown in the tables above.

Gain	Input Range (DF)	Input Range (DF)	Input Signal Range (IN+, IN-) to Ground	Additional Common DC Offset Voltage Range for Input Signals	Input Signal Range (IN+, IN-) to Ground Max Positive DC Shifted
0.166..	±24.576V	**±96V**	**-48V … +48V**	**±0V**	-48V … +48V
0.2	±20.48V	**±80V**	**-40V … +40V**	**±0V**	-40V … +40V
0.4	±10.24V	**±40V**	**-20V … +20V**	**±20V**	0V … +40V
0.8	±5.12V	**±20V**	**-10V … +10V**	**±30V**	+20V … +40V
1.6	±2.56V	**±10V**	**-5V … +5V**	**±35V**	+30V … +40V

Table 6-7 : High-Voltage Analog Input Signal Range (DF)

For Differential (DF) High-Voltage application, the Input Signal Range (to Ground) is Half of the Differential High-Voltage Input Range. The signals may additionally be shifted/offset by a Common DC Offset Voltage within the stated Range.

The signal level on any I/O connector Analog Input Pin in High-Voltage Hardware Configuration must not exceed the range -48V … +48V (referenced to ground)!

Care must be taken as there may be on-board voltage potentials of about twice the highest input voltage (e.g. the voltage between the IN0 and IN1 I/O pins is 96V(!) when the IN0 voltage is at +48V while the IN1 voltage is at -48V referenced to ground)!

6.2.2.4 A/D Data Coding (High-Voltage Input Configuration)

The A/D data coding is always Two's Complement.

See ADC Configuration Register(s) for the actual GAIN value.

Digital Code	Analog Input Voltage (V_{REF} = 4.096V)	Description
0x7FFF	(32767/32768) x (V_{REF}/GAIN) x (999/249)	Pos. Full Scale – 1 LSB
0x0001	(1/32768) x V_{REF}/GAIN x (999/249)	Mid-Scale + 1 LSB
0x0000	0V	Mid-Scale
0xFFFF	– (1/32768) x V_{REF}/GAIN x (999/249)	Mid-Scale – 1 LSB
0x8001	– (32767/32768) x V_{REF}/GAIN x (999/249)	Neg. Full-Scale + 1 LSB
0x8000	– V_{REF}/GAIN x (999/249)	Neg. Full-Scale

Table 6-8 : A/D Data Coding (High-Voltage Input Configuration)

6.3 Analog Input Sampling Scheme

On the TPMC543, for each A/D conversion event (software/register controlled conversion request in manual mode or conversion clock event in sequencer mode) all (active) A/D channels of all (active) ADC devices are sampled in a fast auto-sequence (pseudo-simultaneous).

A/D channels of the ADC devices are processed at a fast rate one after the other in ascending order (starting with channel 0). ADC devices are processed parallel-in-time (e.g. channel 0 of ADC#1 and ADC#2 are processed synchronously).

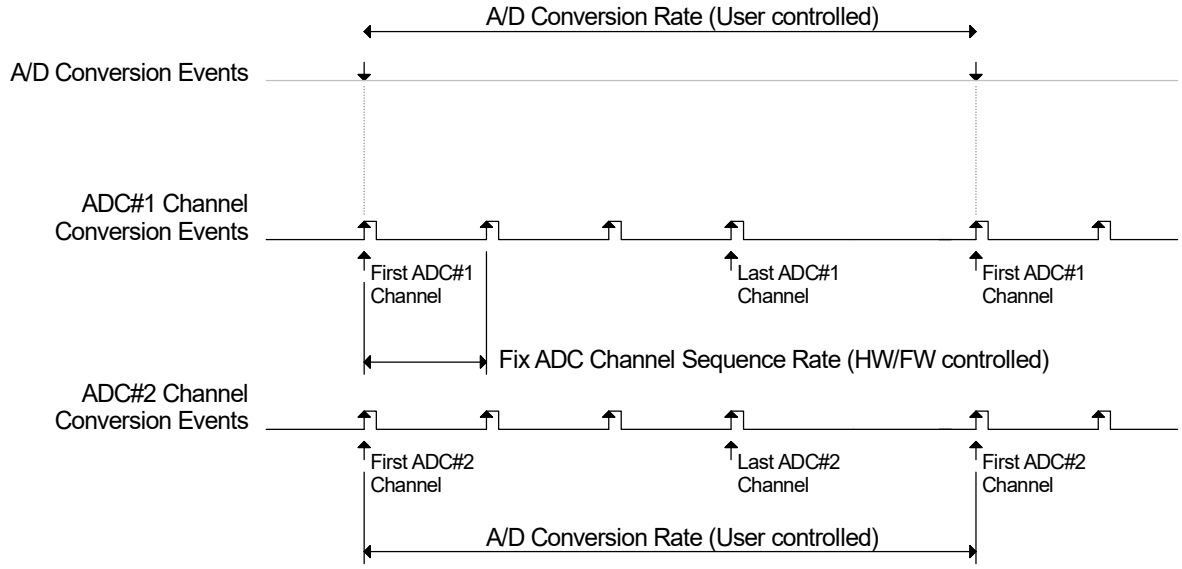


Figure 6-7 : Analog Input Sampling Scheme

6.4 A/D Data Correction

The basic formula for correcting the ADC value is:

$$Data\_Corrected = Data \cdot \left(1 - \frac{Gain_{corr}}{262144}\right) - \frac{Offset_{corr}}{4}$$

Data is the (uncorrected) digital value coming from the ADC.

Data_Corrected is the corrected digital ADC value that is stored in the ADC data registers in Manual Mode or written to Host RAM in Sequencer Mode.

Gain_corr and Offset_corr are the ADC correction values from the appropriate Correction Register.

The factory determined correction values for all A/D channels and ranges are accessible via the Correction Data Space. The correction values are stored as two's complement 16 bit wide values in the range from -32768 to +32767. For higher accuracy they are scaled to ¼ LSB.

For effective A/D channel data correction, the software must read the appropriate offset and gain correction values from the Correction Data Space (depending on the actual input mode & range) and write the values to the appropriate ADC Correction Registers (see Register Map).

No data correction/modification is performed when the ADC Correction Registers are cleared.

See ADC Correction Registers.

6.5 ADC Configuration

The following options are programmable per ADC device in the dedicated ADC Configuration Register.

- Analog Input Mode (individually per ADC device)

  For ADC devices hardware configured to provide high-voltage input channels, the general Analog Input Mode (Single-Ended or Differential) is configurable per ADC device (not per A/D channel).

  For ADC devices hardware configured to provide analog current input channels, the general Analog Input Mode (Single-Ended or Differential) must be configured for Differential Mode.

- Number of active A/D channels (individually per ADC device)

  The number of active Analog Input Channels is configurable for each ADC device and applies for both manual mode and sequencer operating mode.

  Note that for each ADC device, the range of active analog input channels always begins with ADC device channel 0 and proceeds in ascending order.

  The maximum number of active A/D channels per ADC device is 4 (four) for differential input mode and 8 (eight) for single-ended input mode.

  The number of active A/D channels has an impact on the maximum user A/D conversion rate (as implied in the *Analog Input Sampling Scheme* figure.

- A/D Channel Input Range (individually per A/D channel)

  Basically, the analog input voltage range (or ADC Gain) is configurable for each individual A/D channel. However, for ADC devices operating in an Analog Current Input hardware configuration, only ADC Gain 1.6 is applicable for all A/D channels of the ADC device.

  See the Analog Input Range tables (High-Voltage Inputs, Current Inputs) for applicable options.

6.6 ADC Operating Mode

Each configured ADC device is either operating in manual mode (default) or sequencer mode. The ADC device operating mode is configurable in the dedicated ADC Mode Register.

- Manual Mode

  A/D conversion events are triggered by register command.

- Sequencer Mode

  A/D conversion events are triggered by a sequencer conversion clock signal. Each sequencer conversion clock event automatically generates an A/D conversion for each active A/D channel of all ADC devices operating in sequencer mode.

Note that A/D each conversion event automatically generates a conversion on all active channels of the appropriate ADC device(s).

6.6.1 Manual Mode A/D Conversions

The following software sequence may be used for A/D conversions in Manual Mode.

Example Loop:

1. Generate ADC Conversion Request

   Set the appropriate bit(s) in the Global ADC Control Register.

2. Wait until ADC Busy is clear

   Read the appropriate bit(s) in the Global ADC Status Register.

   Please also see *Programming Hints* chapter!

3. Read ADC Data Register(s)

   Read the conversion data from the ADC Data Registers.

See Global ADC Control and Status Registers.

6.6.2 Sequencer Mode A/D Conversions

See the *Sequencer Operation* chapter for sequencer operating mode.

7 Analog Outputs

7.1 DAC Devices and D/A Channels

The Analog Devices AD5755-1 Quad-DAC device is used for the TPMC543 analog outputs.

Each AD5755-1 DAC device provides four 16 Bit D/A channels (D/A channels A-D).

The AD5755-1 DAC device provides a voltage output and a current output for each D/A channel. The voltage and current mode output signals of each AD5755-1 D/A channel are connected and mapped to a common TPMC543 I/O pin (per D/A channel) and so the TPMC543 D/A channels are configurable (programmable) to operate in either voltage or current output mode.

The TPMC543-10R order option provides two AD5755-1 DAC devices and therefore 8 (eight) 16-bit single-ended D/A channels (DAC1 Channels A-D and DAC2 Channels A-D).

7.2 Analog Output Ranges

Each TPMC543 D/A channel is programmable to operate in any of the following output modes / ranges:

- Voltage Range 0V to 5V
- Voltage Range 0V to 6V (over-range option enabled)
- Voltage Range 0V to 10V
- Voltage Range 0V to 12V (over-range option enabled)
- Voltage Range ±5V
- Voltage Range ±6V (over-range option enabled)
- Voltage Range ±10V
- Voltage Range ±12V (over-range option enabled)
- Current Range 4mA to 20mA
- Current Range 0mA to 20mA
- Current Range 0ma to 24mA

7.2.1 Voltage Output Ranges

7.2.1.1 Unipolar Voltage Output Ranges

Analog Output	Unipolar Voltage Output Range				Digital Code
	+5V	+6V	+10V	+12V	
LSB	76.29uV	91.55uV	152.59uV	183.11uV	
Full-Scale – 1 LSB	4.999924V	5.999908V	9.999847V	11.999817V	0xFFFF
Mid-Scale + 1 LSB	2.500076V	3.000092V	5.000153V	6.000183V	0x8001
Mid-Scale	2.5V	3V	5V	6V	0x8000
Mid-Scale – 1 LSB	2.499924V	2.999908V	4.999847v	5.999817V	0x7FFF
Zero-Scale + 1 LSB	76.29uV	91.55uV	152.59uV	183.11uV	0x0001
Zero-Scale	0V	0V	0V	0V	0x0000

Table 7-1 : Unipolar Voltage Output Ranges

7.2.1.2 Bipolar Voltage Output Ranges

Analog Output	Bipolar Voltage Output Range				Digital Code
	±5V	±6V	±10V	±12V	
LSB	152.59uV	183.11uV	305.18uV	366.21uV	
Pos. Full-Scale – 1 LSB	+4.999847V	+5.999817V	+9.999695V	+11.999634v	0x7FFF
Mid-Scale + 1 LSB	+152.59uV	+183.11uV	+305.18uV	+366.21uV	0x0001
Mid-Scale	0V	0V	0V	0V	0x0000
Mid-Scale – 1 LSB	-152.59uV	-183.11uV	-305.18uV	-366.21uV	0xFFFF
Neg. Full Scale + 1 LSB	-4.999847V	-5.999817V	-9.999695V	-11.999634v	0x8001
Neg. Full Scale	-5V	-6V	-10V	-12V	0x8000

Table 7-2 : Bipolar Voltage Output Ranges

7.2.2 Current Output Ranges

Analog Output	Current Output Range			Digital Code
	4…20mA	0…20mA	0…24mA	
LSB	244.141nA	305.176nA	366.211nA	
Full-Scale – 1 LSB	19.999756mA	19.999695mA	23.999634mA	0xFFFF
Mid-Scale + 1 LSB	12.000244mA	10.000305mA	12.000366mA	0x8001
Mid-Scale	12mA	10mA	12mA	0x8000
Mid-Scale – 1 LSB	11.999756mA	9.999695mA	11.999634mA	0x7FFF
Zero-Scale + 1 LSB	4.000244mA	305.176nA	366.211nA	0x0001
Zero-Scale	4mA	0A	0A	0x0000

Table 7-3 : Current Output Ranges

7.3 D/A Data Coding

Data coding for unipolar ranges is Unipolar Straight Binary.
Data coding for bipolar ranges is Binary Two's Complement.

Output Range	Analog Output Transfer Function	Digital Value Range	
		Decimal	Hex
+5V	5V x D / 65536	D = 0 … +65535	D = 0 … FFFF
+6V	6V x D / 65536		
+10V	10V x D / 65536		
+12V	12V x D / 65536		
±5V	5V x D / 32768	D = -32768 … -1, 0, +1, … +32767	D = 8000 … FFFF, 0000, 0001, …, 7FFF
±6V	6V x D / 32768		
±10V	10V x D / 32768		
±12V	12V x D / 32768		
4mA … 20mA	4mA + 16mA x D / 65536	D = 0 … +65535	D = 0 … FFFF
20mA	20mA x D / 65536		
24mA	24mA x D / 65536		

Table 7-4 : Analog Output Transfer Function

7.4 D/A Data Correction

The basic formula for correcting the DAC value is:

$$Data\_Corrected = Data \cdot \left(1 - \frac{Gain_{corr}}{262144}\right) - \frac{Offset_{corr}}{4}$$

Data is the (uncorrected) digital DAC value that would be used with an ideal DAC.

Data_Corrected is the corrected digital DAC value that is written to the real DAC.

Gain_corr and Offset_corr are the DAC correction values from the appropriate Correction Register.

The factory determined correction values for all D/A channels and ranges are accessible via the Correction Data Space. The correction values are stored as two's complement 16 bit wide values in the range from -32768 to +32767. For higher accuracy they are scaled to ¼ LSB.

For effective D/A channel data correction, the software must read the appropriate offset and gain correction values from the Correction Data Space (depending on the actual output range) and write the values to the appropriate DAC Correction Registers (see Register Map).

No data correction/modification is performed when the DAC Correction Registers are cleared.

7.5 D/A Channel Range (Re-) Configuration

The DAC devices on the TPMC543 must be configured (power-up, output range, output enable) before use via the *DAC Configuration Register(s)*. The output range is configurable per D/A channel.

In general, a D/A channel should be configured for the desired output range and powered up first while the corresponding analog output is kept disabled. The D/A channel should then be loaded with the appropriate zero or mid-scale value (including a conversion to propagate the value right through to the DAC internal DAC Register) before the corresponding analog output is enabled.

The following example sequence should be used to avoid analog output effects when D/A channels are being (re-) configured.

Example Sequence for (re-) configuring a D/A channel:

- Set the DAC operating mode to Manual Immediate Conversion Mode (default after reset)
  → *DAC Mode Register*
- Disable the D/A channel output and power-down the D/A channel (default after reset)
  → *DAC Configuration Register*
- Wait until the DAC is no longer busy
  → *Global DAC Status Register*
- Configure the D/A channel output range and power-up the D/A channel (keep the D/A channel output disabled)
  → *DAC Configuration Register*
- Wait until the DAC is no longer busy
  → *Global DAC Status Register*
- Write 0x0001 to the D/A channel Data Register (also provides a trailing DAC conversion pulse)
  → *DAC Data Register*

  This step ensures that the following 0x0000 value will differ from the value stored in the DACs internal DAC Data Register and therefore provides that the 0x0000 value will propagate through the register stage inside the DAC device (the 0x0000 value may be ignored by the DAC device otherwise).
- Wait until the DAC is no longer busy
  → *Global DAC Status Register*
- Write 0x0000 to the D/A channel Data Register (also provides a trailing DAC conversion pulse)
  → *DAC Data Register*
- Wait until the DAC is no longer busy
  → *Global DAC Status Register*
- Enable the D/A channel output (while keeping the output range and power-up configuration)
  → *DAC Configuration Register*
- Wait until the DAC is no longer busy
  → *Global DAC Status Register*

See the *DAC Configuration Register(s)* section in the *Register Description* chapter.

7.6 DAC Operating Mode

On the TPMC543, each configured DAC device is either operating in manual mode (default) or sequencer mode. The DAC device operating mode is configurable in the dedicated DAC Mode Registers.

- Manual Mode

  D/A conversion events are triggered by register writes

  - Immediate Conversion Mode (automatic D/A output update after conversion data transfer)
  - Controlled Conversion Mode (simultaneous D/A output updates by command bit)

- Sequencer Mode

  D/A conversion events are triggered by a sequencer conversion clock signal. A sequencer conversion clock event automatically generates a D/A conversion for each D/A channel of all DAC devices operating in sequencer mode (simultaneous D/A conversions).

7.6.1 Manual Mode D/A Conversions

In Manual Mode, the TPMC543 supports immediate D/A conversions for single D/A channels as well as controlled simultaneous D/A conversions for all on-board D/A channels.

The general Manual Conversion Mode (Immediate vs. Controlled) is configured in the DAC Mode Registers.

The following software sequence examples may be used for D/A conversions in Manual Mode.

7.6.1.1 Immediate Conversion Mode

In Immediate Conversion Mode, a DAC conversion pulse (LDAC#) is generated automatically after loading all pending data to a DAC device (the DAC Busy Status is clear in the Global DAC Status Register). Hence writing to the DAC Data Registers transfers the data to the DAC device and also initiates the analog output update afterwards. The DAC Busy bit in the Global DAC Status Register may be used as an indication for the analog output update.

Example Loop:

1. Write DAC Data Register(s)

   Write channel output data for all DAC devices or for individual DAC devices configured for Manual Mode.
   For a DAC device, either write output data for all four DAC channels or for individual DAC channels.

2. Wait until DAC Busy is clear

   Keep reading the Global DAC Status Register until the appropriate DAC Busy bits are clear, indicating that the conversion data has been loaded to the DAC device(s).

   Note: Also see chapter *Programming Hints / Global DAC Status Register Read*!

7.6.1.2 Controlled Conversion Mode

In Controlled Conversion Mode, data is transferred to the DAC devices by writing the DAC Data Registers. The analog outputs are updated by issuing a DAC Convert Request by register command. This mode supports simultaneous analog output updates for multiple channels.

Example Loop:

1. Write DAC Data Register(s)

   Write channel output data for all DAC devices or for individual DAC devices configured for Manual Mode.
   For a DAC device, either write data for all four DAC channels or for individual DAC channels.

2. Wait until DAC Busy is Clear

   Keep reading the Global DAC Status Register until the appropriate DAC Busy bits are clear, indicating that the channel output data has been loaded to the DAC device(s).

   Note: Also see chapter *Programming Hints / Global DAC Status Register Read*!

3. Write DAC Convert Request

   Write the Global DAC Control Register and set the appropriate DAC Convert Request bits.
   The D/A conversion is performed immediately.

7.6.2 Sequencer Mode D/A Conversions

See the *Sequencer Operation* chapter for sequencer operating mode.

8 Digital I/O

8.1 General Purpose Digital I/O (Front I/O)

The TPMC543 features eight general purpose Digital I/O lines available at the front I/O connector.

Each digital I/O line features a receiver, a driver with individual output enable control, a series resistor, ESD protection and a 4K7 pull resistor to a common reference voltage. The common pull resistor reference is programmable to be 5V (pull-up), 3.3V (pull-up) or GND (pull-down).

The receiver accepts LVTTL (3.3V) and 5V TTL / 5V CMOS signal levels. The driver signal level is LVTTL (3.3V). Provided that the output load is high impedance, a 5V CMOS output level may be generated with the 5V pull-up configuration while controlling the output via output enable control while the output is set to low.

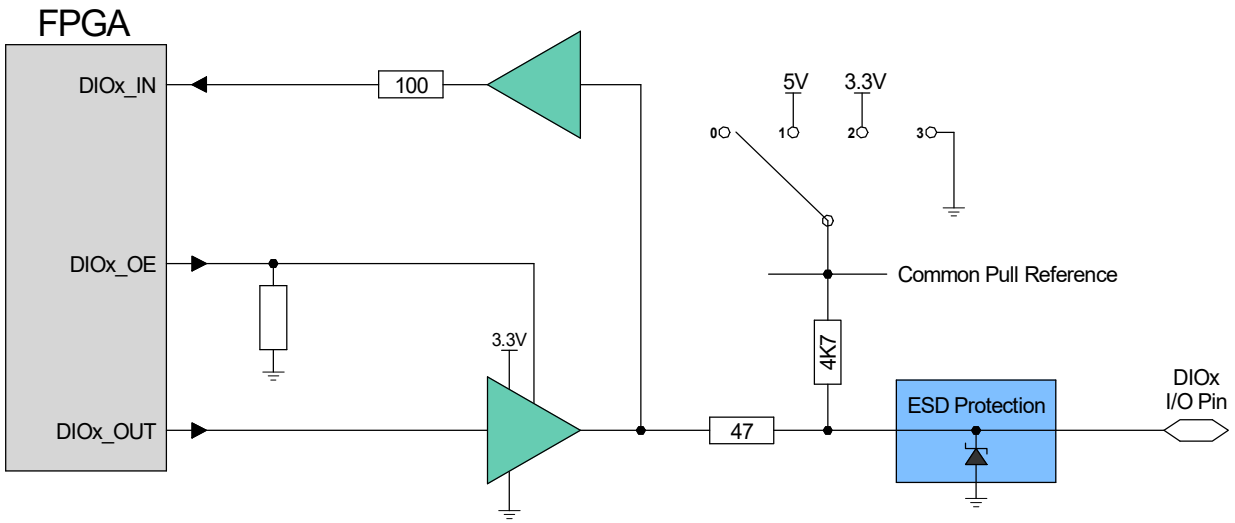


Figure 8-1 : Digital I/O Line Circuit

At power-up and/or after reset, all Digital I/O lines are configured as inputs (i.e. the output drivers are disabled). The pull resistor reference is open and has to be configured by software to let the pull resistors operate as pull-downs to GND or as pull-ups to +3.3V or +5V.

The receiver function is always active and may be used to monitor the I/O line level even when the I/O line is operating as an output.

Note that the default configuration for the pull resistor reference is "Open" and all the pull resistors are connected to each other via the common reference rail (and hence the digital I/O signals are connected to each other through the pull resistors).

Note that the digital I/O lines are merely intended to be used is a static way. Since the digital I/O lines are running in the same I/O cable as the analog input and output lines, any dynamic activity on the digital I/O lines will generate noticeable noise in the analog signals.

8.2 Conversion Control Digital I/O (Rear I/O)

The TPMC543 also features a couple of Digital I/O lines available at the P14 rear I/O connector.

These Digital Rear I/O lines are built in the same way as the general purpose Digital Front I/O lines. However, there is a dedicated common pull reference for the Digital Rear I/O signals.

While the Digital Front I/O lines are for general purpose, the Digital Rear I/O lines are intended for a dedicated function in the A/D and/or D/A sequencer modes (Conversion Clock Signals 1 & 2 and Frame Trigger Signal).

9 Sequencer Operation

Sequencer operation is used for periodic D/A and/or A/D conversions, based on an internal configurable or external conversion clock signal.

There is a dedicated sequencer for D/A operation and a dedicated sequencer for A/D operation.

9.1 A/D Sequencer Operation

9.1.1 Overview

The TPMC543 provides an A/D sequencer unit.

The A/D sequencer is used for periodic pseudo-simultaneous A/D conversions on all active A/D channels of the ADC devices operating in sequencer mode.

The A/D sequencer unit basically consists of:

- an ADC Convert Pulse Generator
- Data Input Unit (for gathering the A/D conversion data from the ADC devices)
- a FIFO (for buffering the A/D conversion data)
- a DMA controller (for writing the A/D conversion data to host memory)

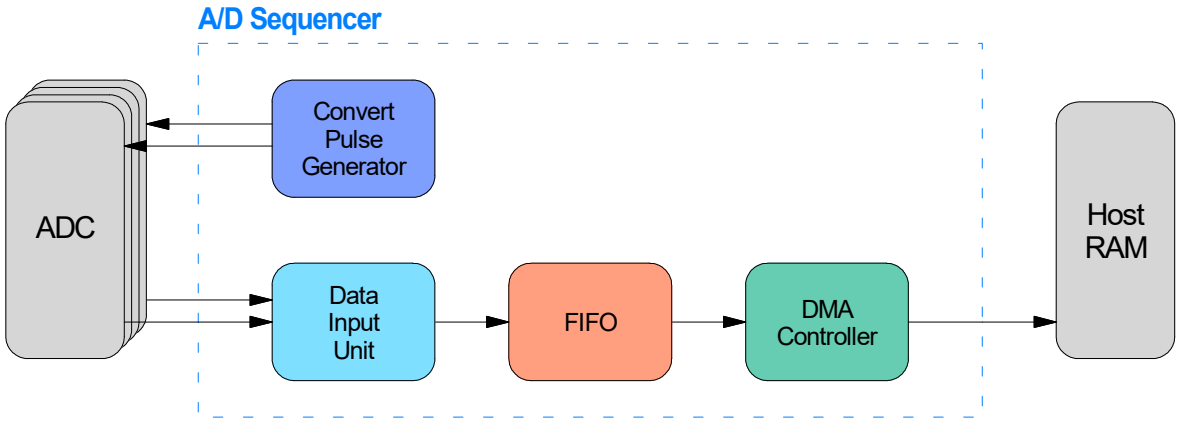


Figure 9-1 : A/D Sequencer Unit

Each ADC device may be assigned to the A/D sequencer (i.e. may be configured to operate in Sequencer Mode).

All active A/D input channels of the ADC devices assigned to the A/D sequencer are operating in pseudo-simultaneous conversion mode. Input channels on the same ADC device are processed sequentially in ascending order at a fast rate. This is processed in-parallel for all participating ADC devices.

Per sequencer conversion clock event, the A/D conversion data for all active A/D channels of all ADC devices assigned to the A/D sequencer is gathered from the ADC devices and temporary stored in an on-board/chip FIFO. The A/D conversion data is written to data buffers in host memory via DMA PCI Master Write access. While the sequence conversion clock is running continuously, the number of conversions to be performed is configurable.

9.1.2 Sequencer A/D Conversion

9.1.2.1 General Notes

Within the ADAS3022 ADC device, the analog inputs are internally multiplexed to a single SAR ADC unit. Therefore the TPMC543 A/D function cannot be classified as real „simultaneous sampling“.

For ADAS3022 ADC devices operating in sequencer mode, an A/D sequencer conversion clock event triggers a sequence of internally generated ADC conversion pulses, sampling all the active A/D channels of all ADC devices assigned to the sequencer as fast as possible. A/D *channels on the same ADC device* are sampled sequentially (one after the other) in ascending order at a fast rate. *ADC devices* are processed in-parallel.

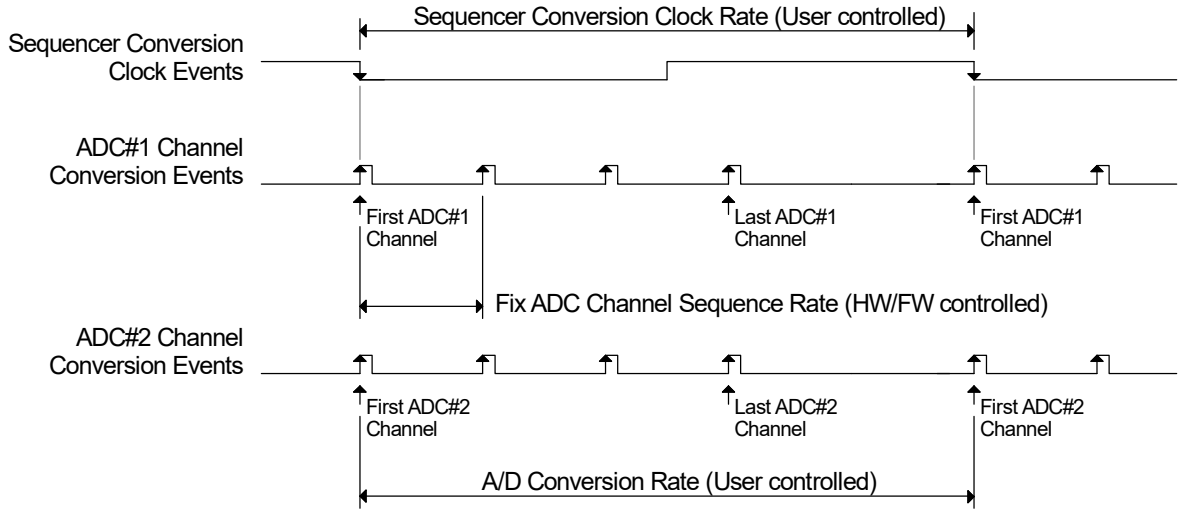


Figure 9-2 : A/D Sequencer Sampling Scheme

As shown above, the A/D (channel) conversion rate corresponds to the A/D sequencer conversion clock rate.

After a sequencer conversion clock event, the data of all active A/D channels of all ADC devices assigned to the sequencer is transferred from the ADC devices to the sequencer data FIFO (and this operation needs to be done before the next sequencer conversion clock event).

The maximum A/D conversion rate (= sequencer conversion clock rate) depends on the highest number of active A/D channels per ADC device (of all the ADC devices operating in Sequencer Mode).

Highest Number of Active A/D Channels per ADC Device	Max A/D Conversion Rate
1	800ksps[2)]
2	400ksps[3)]
4	200ksps
8[1)]	100ksps

[1)] Single-Ended Input Mode only, [2)] Noise may be higher above 600ksps, [3)] Noise may be higher above 350ksps

Table 9-1 : Max. A/D Conversion Rate

Brief functional description:

- Each on-board (multi-channel) ADC device may be assigned to the A/D sequencer
- Each ADC device is configurable to operate either in Single-Ended Input Mode (Input Channels 0 to 7) or in Differential Input Mode (Input Channels 0+/- to 3+/-)
    - ADC devices operating in an analog current input HW configuration must be configured to operate in differential input mode
- For each ADC device, the number of active A/D channels is programmable (always starting with input channel 0 and continuing in ascending order)
- The maximum A/D conversion rate (= A/D sequencer conversion clock rate) depends on the number of active A/D channels per ADC device
- For each A/D Sequencer Conversion Clock Event, an A/D conversion is generated for all active A/D channels of all ADC devices operating in sequencer mode, resulting in an A/D conversion data set that is gathered and stored in an internal FIFO. A/D channels on the same ADC device are sampled sequentially (one after the other) in ascending order at a fast rate. The participating ADC devices are processed in-parallel (e.g. all channels 0 of the participating ADC devices are sampled at the same time and so on).
- A/D conversion data sets are written to data buffers in host memory via DMA PCI Master Write access
- An A/D conversion data set data is written to the current host memory data buffer in the following order:
    - Lowest order ADC device operating in Sequencer Mode
        - ADC Channel 0 to Last active A/D Channel of ADC device
    - Next order ADC device operating in Sequencer Mode
        - ADC Channel 0 to Last active A/D Channel of ADC device
    - Highest order ADC device operating in Sequencer Mode
        - ADC Channel 0 to Last active A/D Channel of ADC device

9.1.2.2 Normal Mode

In **Sequencer Normal Mode**, the desired number of conversions (register value) for the next block of A/D conversions is configured. Setting the number of conversions to 0 selects continuous conversion mode.

No ADC conversion pulses are generated until the software starts the conversion process.

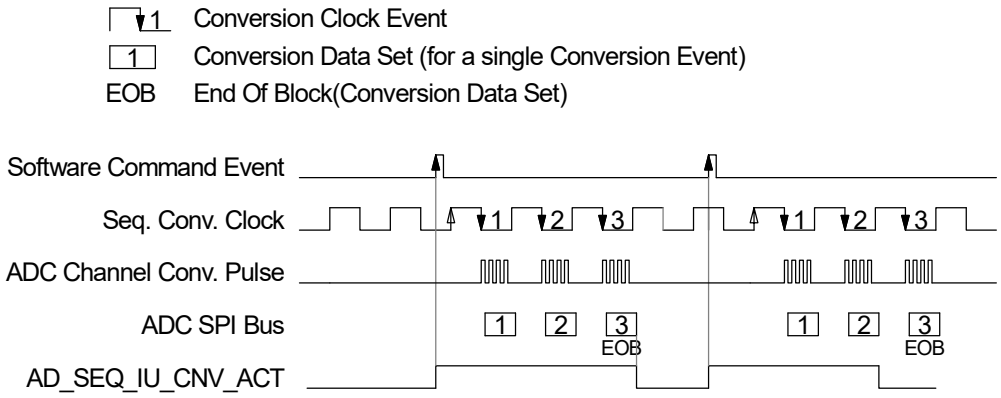
When the conversion process is started (by setting the appropriate register bit), first a rising edge of the sequencer conversion clock is required (due to the asynchronous character of the register bit start condition). Then starting with the next sequencer conversion clock falling edge event, the appropriate number of conversion pulses are generated for the sequencer ADC devices (at the sequencer conversion clock rate) in accordance with the configured number of conversions.

The active conversion phase is indicated by an appropriate bit in the Sequencer Status Register.

After each ADC conversion pulse event, the conversion data set is transferred to the sequencer FIFO.

When the configured number of conversions is done (when not operating in continuous mode), the appropriate bit in the Sequencer Status Register is cleared and no further conversion pulses are generated for the sequencer ADC devices.

For starting a next block of data conversions, the conversion process must re-started (by setting the appropriate register bit).



Example: Number Of Conversions = 3

Figure 9-3 : Normal Mode Example Diagram (A/D)

The following error conditions are monitored:

- Conversion Error

  The Sequencer Conversion Clock requests the next conversion too fast while the current conversion process is still in progress.

- FIFO Overflow Error

  The Input Unit needs to write ADC conversion data to the FIFO but the FIFO is full (e.g. because the FIFO data is not written to Host RAM fast enough).

In an error case the conversion process (sequencer operation) is stopped.

9.1.2.3 Frame Mode

In **Sequencer Frame Mode**, the desired number of conversions per frame and the frame interval (length) in number of conversion clock cycles is configured (register value). For seamless conversions, the number of conversions per frame must match for the configured frame interval and conversion clock rate (alternatively, the number of conversions may also be set to 0 for Continuous Mode).

No ADC conversion pulses are generated until a frame trigger signal event occurs.

Starting with the first conversion clock event after the first/next frame trigger event, the appropriate number of conversion pulses are generated for the sequencer ADC devices (at the sequencer conversion clock rate) in accordance with the configured number of conversions per frame.

The active conversion phase is indicated by an appropriate bit in the Sequencer Status Register and the A/D conversion data is automatically transferred to the A/D sequencer FIFO.

When the configured number of conversions per frame is done, the appropriate bit in the Sequencer Status Register is cleared and no further conversion pulses are generated for the sequencer ADC devices until the next frame trigger signal event.

After the next frame trigger event the frame conversion process automatically starts again (or continuous in continuous Mode).

The following error conditions are monitored:

- Frame Error

  A Frame Trigger event occurs, but the configured Number of Conversions for the current frame has not been processed so far (does not apply in Continuous Mode).

- Conversion Error

  The Sequencer Conversion Clock requests the next conversion too fast while the current conversion process is still in progress.

- FIFO Overflow Error

  The Input Unit needs to write ADC conversion data to the FIFO but the FIFO is full (e.g. because the FIFO data is not written to Host RAM fast enough).

In an error case the conversion process (sequencer operation) is stopped.

9.1.2.4 Frame Mode Example Diagrams (A/D)

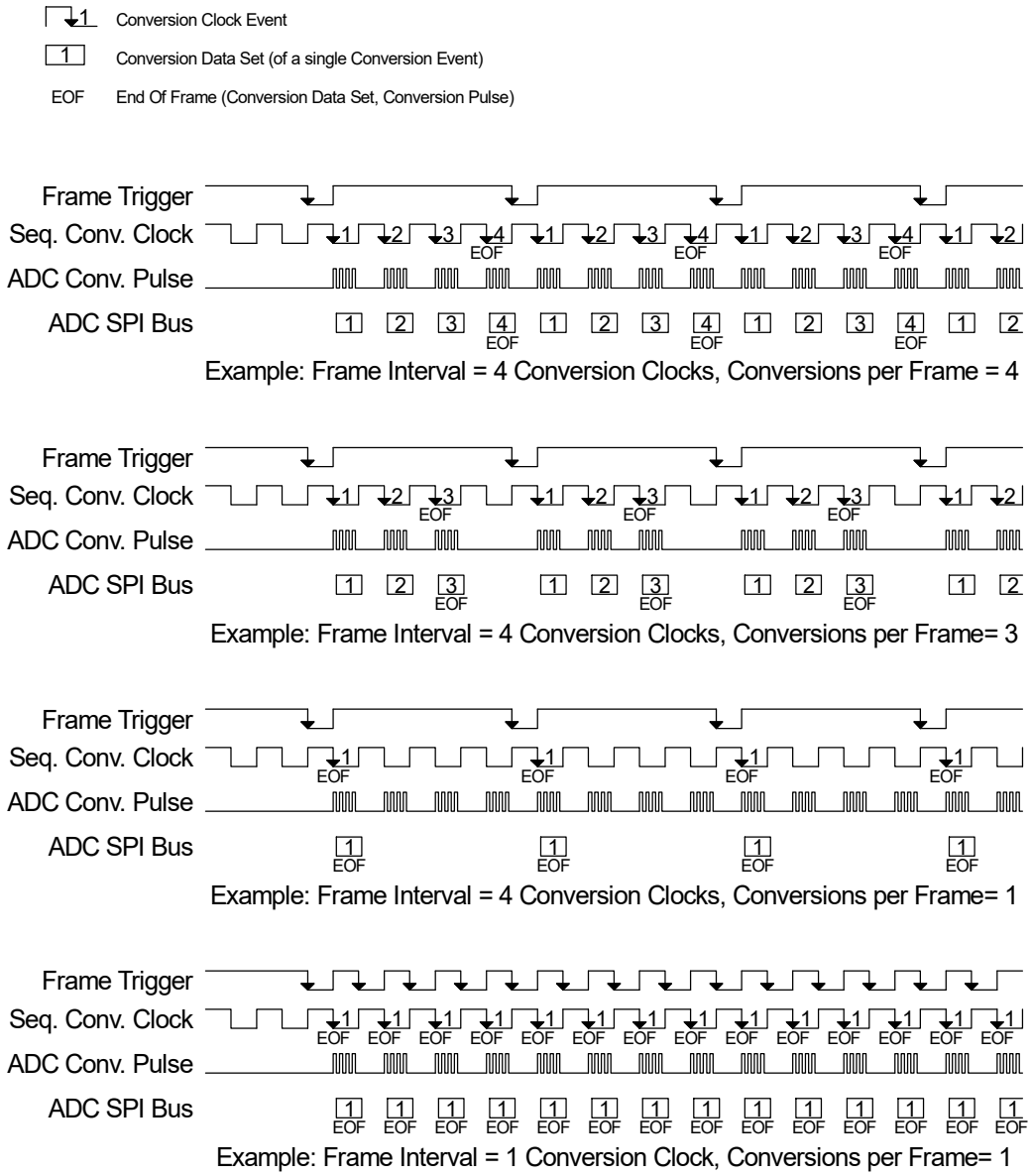


Figure 9-4 : Frame Mode Example Diagrams (A/D)

Seamless A/D conversions are achievable either by a matching Frame Interval / Conversions per Frame configuration or by using continuous conversions.

9.1.3 DMA Operation

The conversion data from the ADC devices assigned to the A/D sequencer is buffered in an on-board/chip FIFO. There also is a sideband information stored, indicating the last A/D data value for the last conversion event (according to the configured number of conversions per block/frame).

A/D conversion data accumulates in the FIFO and is then written to a data buffer in host memory by the sequencer's DMA controller via PCI Master Write access.

There are two main PMC target registers for A/D sequencer DMA to Host Memory control:

- DMA Buffer Base Address Register
- DMA Buffer Length Register

The (PCI Memory mapped) base address of the data buffer must be written to the DMA Buffer Base Address Register. The number of bytes to be read must be written to the DMA Buffer Length Register. Writing the DMA Buffer Length Register also validates the data buffer and initiates the DMA transfer to the host memory data buffer (if length is not zero).

The sequencer DMA controller fetches the A/D conversion data from the internal FIFO and writes the data to the configured host memory data buffer until any of the following events applies:

- The data buffer in Host memory is full
- The configured number of conversions (per block/frame) has been transferred
- An error has occurred

The base address of a next data buffer may be written immediately after a write to the DMA Buffer Length Register. The DMA Buffer Length Register must only be written if the previous data buffer has been reported as complete (and the DMA controller is in Idle state).

9.1.4 Host Memory Data Buffers

A/D sequencer conversion data is written to host memory data buffers per DMA PCI Master Write access.

The A/D conversion data buffers must be mapped in 32 bit PCI Memory Space and must be accessible from the PMC card PCI bus.

The structure of an A/D conversion data buffer is a gapless list of A/D sequencer conversion data sets.

An A/D sequencer conversion data set consists of the conversion data for a single sequencer conversion event comprising all ADC devices operating in sequencer mode with all active A/D channels, in ascending order.

The following Example configuration illustrates the host memory data organization:

- ADC 1 → Manual Mode
- ADC 2 → Sequencer Mode, Single-Ended Input Mode, Number of active channels = 4 (0-3)
- ADC 3 → Manual Mode
- ADC 4 → Sequencer Mode, Differential Input Mode, Number of active channels = 2 (0-1)

Conversion Data Set	Memory Address	Data
1 (1st A/D Conversion)	Data Buffer Base Address	16 Bit Data of ADC 2 Channel 0
	+2	16 Bit Data of ADC 2 Channel 1
	+2	16 Bit Data of ADC 2 Channel 2
	+2	16 Bit Data of ADC 2 Channel 3
	+2	16 Bit Data of ADC 4 Channel 0
	+2	16 Bit Data of ADC 4 Channel 1
2 (2nd A/D Conversion)	+2	16 Bit Data of ADC 2 Channel 0
	+2	16 Bit Data of ADC 2 Channel 1
	+2	16 Bit Data of ADC 2 Channel 2
	+2	16 Bit Data of ADC 2 Channel 3
	+2	16 Bit Data of ADC 4 Channel 0
	+2	16 Bit Data of ADC 4 Channel 1
3 (3rd A/D Conversion)	…	…

Table 9-2 : A/D Host Memory Data Buffer Example

9.2 D/A Sequencer Operation

9.2.1 Overview

The TPMC543 provides a D/A sequencer unit.

The D/A sequencer is used for periodic simultaneous D/A output conversions on all DAC devices assigned to the sequencer.

The D/A sequencer unit basically consists of:

- a DMA controller (for fetching the D/A output data from host memory)
- a FIFO (for buffering the D/A conversion data)
- Data Output Unit (for transferring the D/A conversion data to a DAC device)
- a DAC Convert Pulse Generator

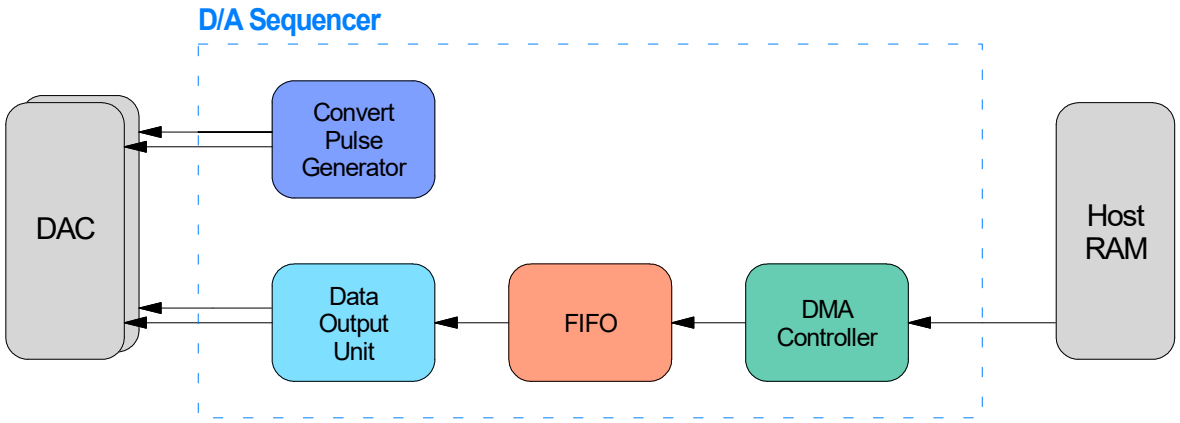


Figure 9-5 : D/A Sequencer Unit

Each DAC device may be assigned to the D/A sequencer (i.e. may be configured to operate in Sequencer Mode).

The D/A conversion data (for all D/A channels of all DAC devices assigned to the D/A sequencer) is prepared in host memory data buffers. The PMC fetches the D/A conversion data from host memory by PCI Master DMA transfer upon request and preloads the participating DAC devices with D/A channel output data.

Per sequencer conversion clock event, all D/A channel outputs on all participating DAC devices are updated simultaneously. While the sequencer conversion clock is running continuously, the number of simultaneous conversions to be performed is configurable. After each conversion event, the participating DAC devices are pre-loaded with D/A channel output data for the next conversion event.

9.2.2 Host Memory Data Buffers

Data buffers in host memory are used to pass/provide the D/A conversion data for the DAC devices which are operating in sequencer mode.

The D/A conversion data buffers must be mapped in 32 bit PCI Memory Space and must be accessible from the PCI bus.

The structure of a D/A conversion data buffer is a gapless list of D/A conversion data sets for the D/A sequencer.

A D/A conversion data set consists of the conversion data required for a single sequencer conversion event, covering all DAC devices assigned to the sequencer and all the device D/A channels, in ascending order.

The number of 16 Bit D/A words required per D/A conversion data set is:
Number_of_DACs_assigned_to_the_Sequencer x 4

The following Example configuration illustrates the host memory data organization:

- Both DAC 1 and DAC 2 are assigned to the D/A sequencer (i.e. are operating in sequence mode).

Conversion Data Set	Memory Address	Data
1 (1st D/A Conversion)	Data Buffer Base Address	16 Bit Data for DAC 1 Channel A
	+2	16 Bit Data for DAC 1 Channel B
	+2	16 Bit Data for DAC 1 Channel C
	+2	16 Bit Data for DAC 1 Channel D
	+2	16 Bit Data for DAC 2 Channel A
	+2	16 Bit Data for DAC 2 Channel B
	+2	16 Bit Data for DAC 2 Channel C
	+2	16 Bit Data for DAC 2 Channel D
2 (2nd D/A Conversion)	+2	16 Bit Data for DAC 1 Channel A
	+2	16 Bit Data for DAC 1 Channel B
	+2	16 Bit Data for DAC 1 Channel C
	+2	16 Bit Data for DAC 1 Channel D
	+2	16 Bit Data for DAC 2 Channel A
	+2	16 Bit Data for DAC 2 Channel B
	+2	16 Bit Data for DAC 2 Channel C
	+2	16 Bit Data for DAC 2 Channel D
3 (3rd D/A Conversion)	+2	16 Bit Data for DAC 1 Channel A
	+2	…

Table 9-3 : D/A Host Memory Data Buffer Example

9.2.3 DMA Operation

The conversion data for the DAC devices assigned to the D/A sequencer is fetched from data buffers in host memory by the sequencer's DMA controller via PCI Master read access. The conversion data is buffered in the sequencer FIFO.

There are two main PMC target registers for D/A sequencer DMA to Host Memory control:

- DMA Buffer Base Address Register
- DMA Buffer Length Register

The (PCI Memory mapped) base address of the data buffer must be written to the DMA Buffer Base Address Register.

The DMA read transfer (for a data buffer) is started by a (non-zero) write to the DMA Buffer Length register while the DMA Engine is in Idle state. The same write access also defines the data amount to be read from the data buffer.

The sequencer DMA controller fetches the D/A conversion data from the host memory data buffer and writes the data to the on-board sequencer FIFO.

A data buffer is reported as complete by status interrupt when all data (defined length) has been fetched

The base address of a next data buffer may be written immediately after a write to the DMA Buffer Length Register. The DMA Buffer Length Register must only be written if the previous data buffer has been reported as complete (and the DMA controller is in idle state).

9.2.4 Sequencer D/A Conversion

9.2.4.1 Normal Mode

In **Sequencer Normal Mode**, the desired number of conversions (register value) for the next block of D/A conversions is configured. Setting the number of conversions to 0 selects continuous conversion mode.

Conversion data accumulates in the sequencer FIFO after the DMA transfer has been initiated. The FIFO fill level is readable.

When data is/becomes available in the sequencer FIFO, the sequencer DAC devices are automatically pre-loaded for the first conversion.

No DAC conversion pulses are generated until the conversion process is started.

When the conversion process is started (by setting the appropriate register bit), first a rising edge of the sequencer conversion clock is required (due to the asynchronous character of the register bit start condition). Then starting with the next sequencer conversion clock falling edge event, the appropriate number of conversion pulses are generated for the sequencer DAC devices (at the sequencer conversion clock rate) in accordance with the configured number of conversions.

The active conversion phase is indicated by an appropriate bit in the Sequencer Status Register.

After each DAC conversion pulse event, the data set for the next conversion is transferred to the DAC devices operating in sequencer mode, when conversion data is or becomes available in the sequencer FIFO.

When the configured number of conversions is done (when not operating in continuous mode), the appropriate active bit in the Sequencer Status Register is cleared and no further conversion pulses are generated for the sequencer DAC devices.

When data is or becomes available in the sequencer FIFO, the sequencer DAC devices are being pre-loaded again for the next conversion block.

For starting a next block of data conversions, the software must re-start the conversion process (by setting the appropriate register bit).

The following error conditions are monitored:

- Conversion Timing Error

  A next conversion pulse is due, but would violate the DAC timing specification.

- Conversion Data Error

  A next conversion pulse is due, but not all sequencer DAC devices are in a proper pre-loaded state.

In an error case the conversion process (sequencer operation) is stopped.

The example diagram below shows that the (DAC device) preload status is set every time a data set has been transferred to the DAC device and is cleared upon the DAC conversion event. After detecting the preload condition, the conversion is initiated by software command. The activity bit is set with the register command and is cleared with the last conversion (according to the configurable number of conversions). It is also indicated that the DACs are automatically (pre-) loaded after a conversion event (provided that data is available in the FIFO).

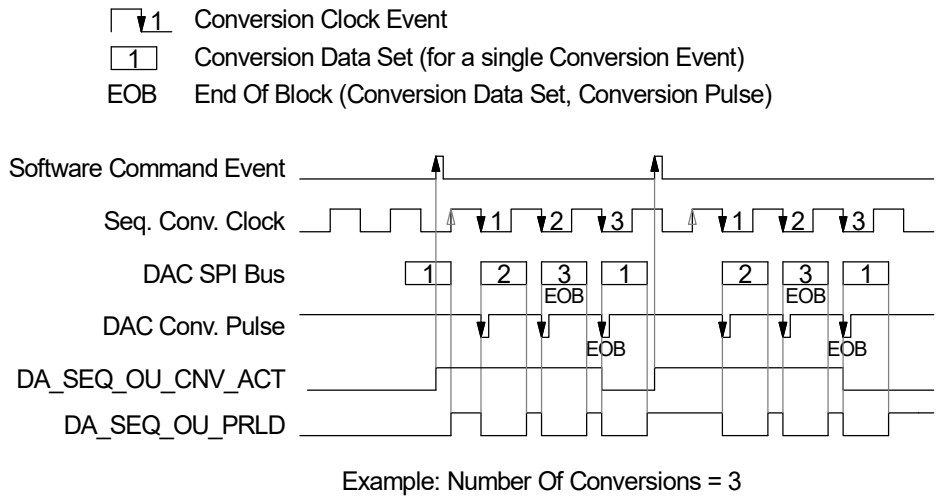


Figure 9-6 : Normal Mode Example Diagram (D/A)

9.2.4.2 Frame Mode

In **Sequencer Frame Mode**, the desired number of conversions per frame and the frame interval (length) in number of conversion clock cycles is configured (register value). For seamless conversions, the number of conversions per frame must match for the configured frame interval and conversion clock rate (alternatively, the number of conversions may also be set to 0 for Continuous Mode).

When data is/becomes available in the sequencer FIFO, the sequencer DAC devices are pre-loaded for the first conversion.

No DAC conversion pulses are generated until a frame trigger signal event happens.

Starting with the first conversion clock event after the first/next frame trigger event, the appropriate number of conversion pulses are generated for the sequencer DAC devices (at the sequencer conversion clock rate) in accordance with the configured number of conversions per frame.

The active conversion phase is indicated by an appropriate bit in the Sequencer Status Register.

After each DAC conversion pulse event, the data set for the next conversion is automatically transferred to the sequencer DAC devices (operating in Sequencer Mode) when conversion data is or becomes available in the sequencer FIFO.

When the configured number of conversions per frame is done, the appropriate bit in the Sequencer Status Register is cleared and no further conversion pulses are generated for the sequencer DAC devices until the next frame trigger signal event.

When data is or becomes available in the sequencer FIFO, the sequencer DAC devices are being pre-loaded again for the first conversion of the next frame.

After the next frame trigger event the frame conversion process automatically starts again.

The following error conditions are monitored:

- Frame Error

  A next frame trigger event occurs, but the configured number of conversions has not been processed so far (does not apply in Continuous Mode)

- Conversion Timing Error

  A next conversion pulse is due, but would violate the DAC timing specification.

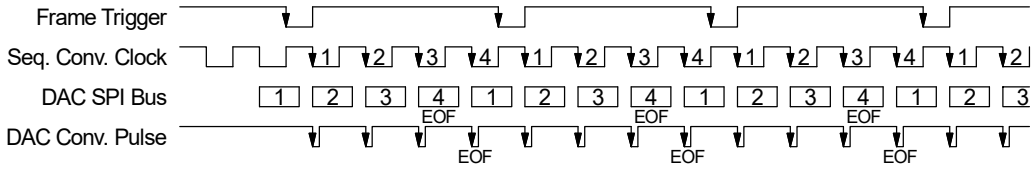
- Conversion Data Error

  A next conversion pulse is due, but not all sequencer DAC devices are in a proper pre-loaded state.

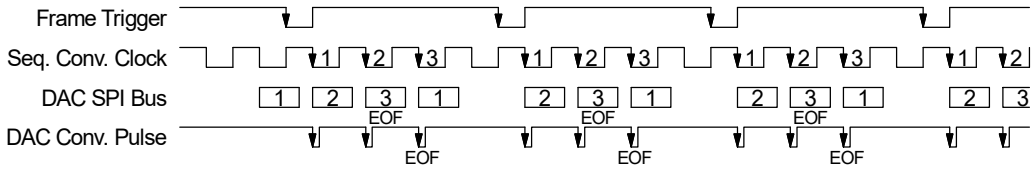
In an error case the conversion process (sequencer operation) is stopped.

9.2.4.3 Frame Mode Example Diagrams (D/A)

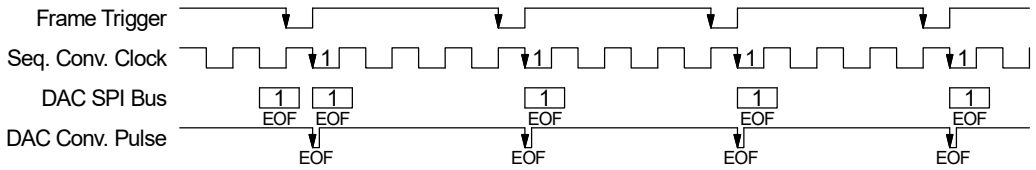
1 Conversion Clock Event
1 Conversion Data Set (for a single Conversion Event)
EOF End Of Frame (Conversion Data Set, Conversion Pulse)



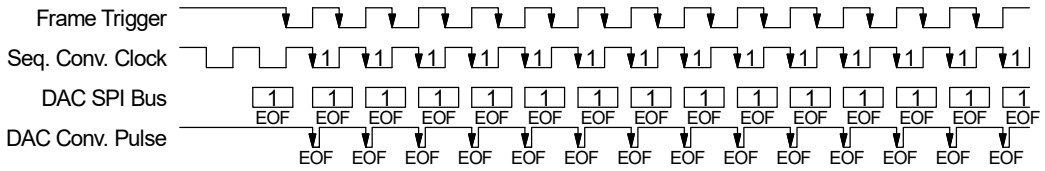
Example: Frame Interval = 4 Conversion Clocks, Conversions per Frame = 4



Example: Frame Interval = 4 Conversion Clocks, Conversions per Frame = 3



Example: Frame Interval = 4 Conversion Clocks, Conversions per Frame = 1



Example: Frame Interval = 1 Conversion Clock, Conversions per Frame = 1

Figure 9-7 : Frame Mode Example Diagrams (D/A)

Seamless equidistant DAC conversion pulses (simultaneous D/A conversions) are achievable either by a matching Frame Interval / Conversions per Frame configuration or by using continuous conversions.

9.2.5 Expected Maximum D/A Conversion Rate

The D/A conversion rate is mainly limited by the AD5755-1 DAC timing parameters. Between two DAC conversion events, conversion data for the next conversion event must be transferred to all DACs for all D/A channels. This takes approx. 25us (plus a small setup and hold time). The expected maximum D/A conversion rate is 38ksps.

9.3 Combined D/A and A/D Sequencer Operation

In D/A sequencer mode, a D/A sequencer conversion clock event triggers a conversion pulse on all participating DAC devices, generating a simultaneous D/A output update on all D/A channels of the participating DAC devices.

In A/D sequencer mode, an A/D sequencer conversion clock event triggers a sequence of internally generated ADC conversion pulses, sampling all the active A/D channels of all participating ADC devices. The A/D channels of an ADC device are processed sequentially (one after the other) in ascending order at a fast rate. The participating ADC devices are processed in-parallel (e.g. all channels 0 of the participating ADC devices are sampled at the same time and so on).

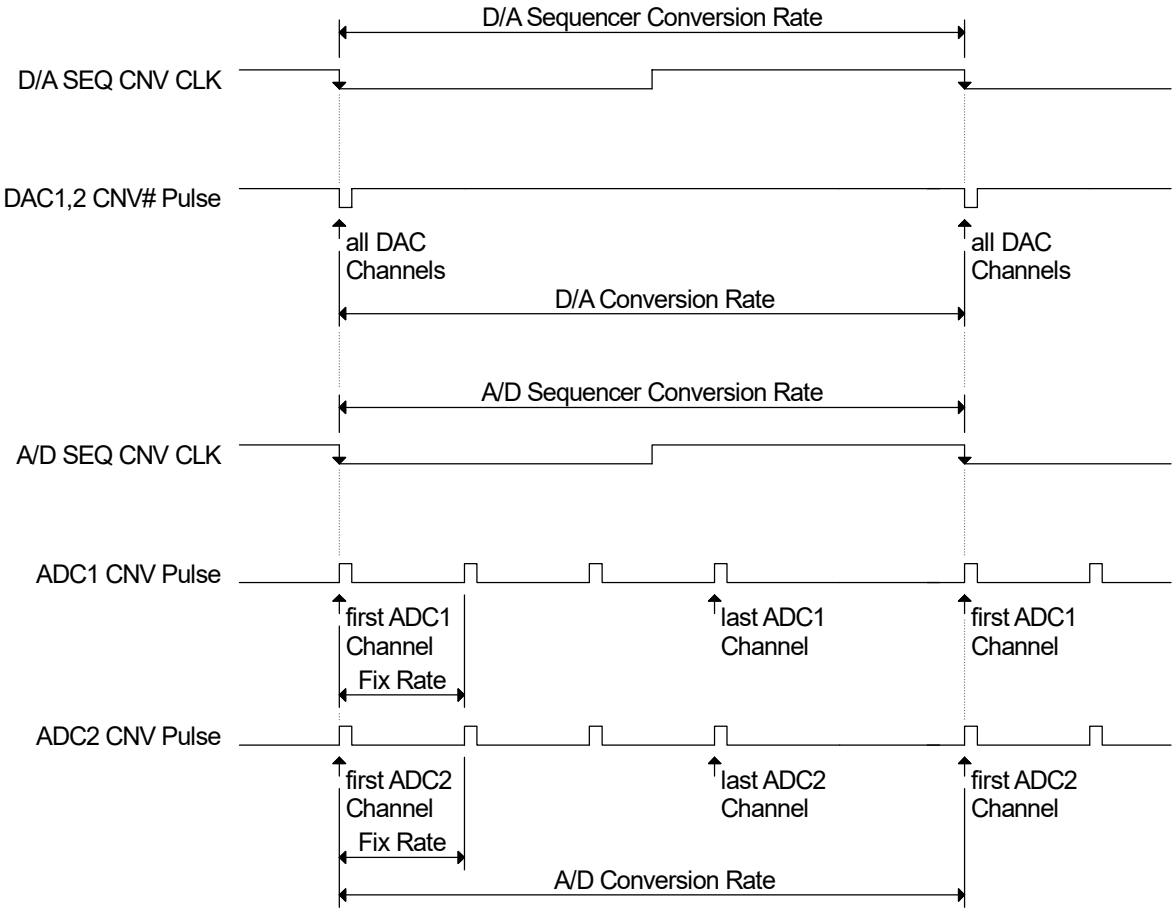


Figure 9-8 : D/A + A/D Sequencer Operation

For combined D/A and A/D sequencer operation, the conversion clock signals (and hence the conversion events) for the A/D and D/A sequencers may be generated synchronously and with the same rate. However, in this case the maximum sequencer conversion rate is limited to approximately 38ksps by the DAC device type. When using the internal signal generators for this purpose, it would be sufficient to use only one of the clock signal generators and select the same chosen conversion clock signal in both sequencers.

For combined D/A and A/D sequencer operation with different conversion rates for the D/A and A/D sequencers, the conversion clock signal rates must be integer multiples of another and the conversion clock signals must also be generated synchronously from the same clock source. When using the internal signal generators for this purpose, both conversion clock signal generators must be enabled with the same register write (Conversion Signal Generator Enable Register).

Note that in Sequencer Frame Mode, there only is a single frame trigger signal for both the A/D and D/A sequencer and the conversion clock signal for each sequencer must be phase aligned & locked to the frame trigger signal.

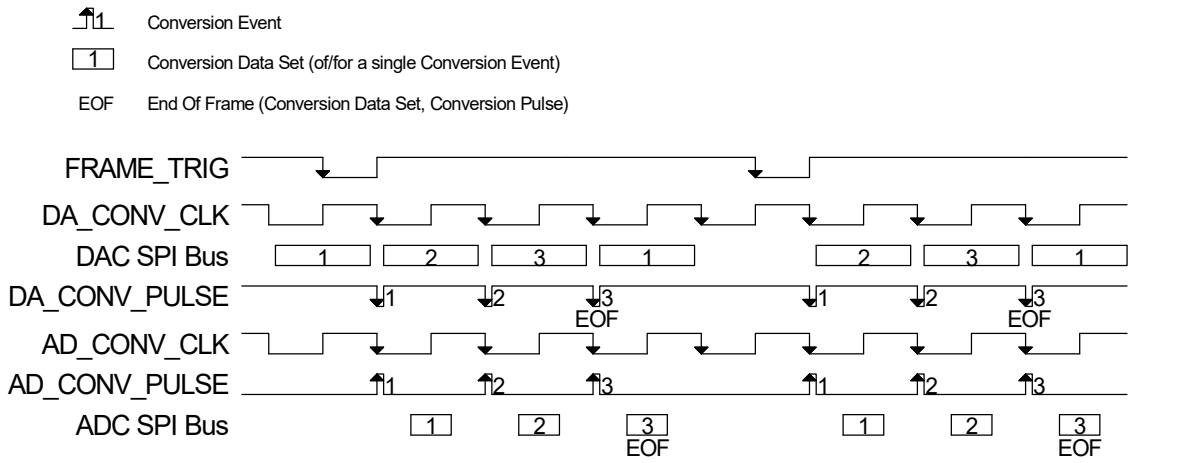


Figure 9-9 : Combined D/A & A/D Sequencer Operation in Frame Mode

9.4 Multi-Board Synchronization

The Sequencer Frame Mode supports Multi-Board synchronization.

In a Multi-Board application, one PMC may be operating as the multi-board master card while the other cards are operating as multi-board slave cards.

The multi-board master PMC generates the phase aligned frame trigger and conversion clock signals to be used by all cards of the multi-board application and drives these signals out on the appropriate Rear-I/O pins.

The multi-board master's frame trigger and conversion clock I/O signals must be connected to the frame trigger and conversion clock I/O signals of all slave cards in the multi-board application.

All cards participating in the multi-board application (including the master card) must use (configure) the I/O pin input signals as the signal source for both the frame trigger signal and the conversion clock signal.

The desired Number of Conversions (per Frame) must be configured on all participating cards.

All card's sequencers operating in frame mode are waiting for a frame trigger signal event for starting the sequencer conversion process. The frame trigger signal is generated on the master card (aligned to the associated conversion clock signal) and is distributed (along with the associated conversion clock signal) to all associated cards via the I/O interface. The DAC pre-load status and FIFO level may be checked on all associated cards before starting the frame trigger signal generation.

9.5 Frame Mode Notes

- A sequencer in Frame Mode must use the global frame trigger signal (thus when both sequencers are operating in Frame Mode they are operating with the same frame interval and the same number of frame trigger pulses)
- The number of conversion events per frame is configurable for a sequencer but is then fix for all frames
- In a Multi-Board scenario, the number of conversions per frame must be configured (register value) on all associated PMC cards
- The frame trigger signal must be phase aligned and locked to the sequencer's conversion clock signal(s)
- Frame trigger signals coming from external sources must meet certain timing requirements

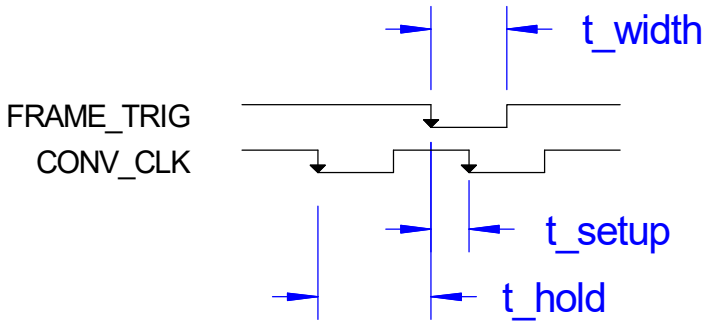


Figure 9-10 : Frame Trigger Timing Requirements

Timing Parameter	Description	Min	Max
t_width	Pulse Width	500ns	½ T_{CONV_CLK}
t_hold	Conversion Clock Event to next Frame Trigger Event	½ T_{CONV_CLK} - 250ns	-
t_setup	Frame Trigger Event to next Conversion Clock Event	250ns	-

Table 9-4 : Frame Trigger Timing Parameter

9.6 Sequencer Conversion Control Signals

9.6.1 Overview

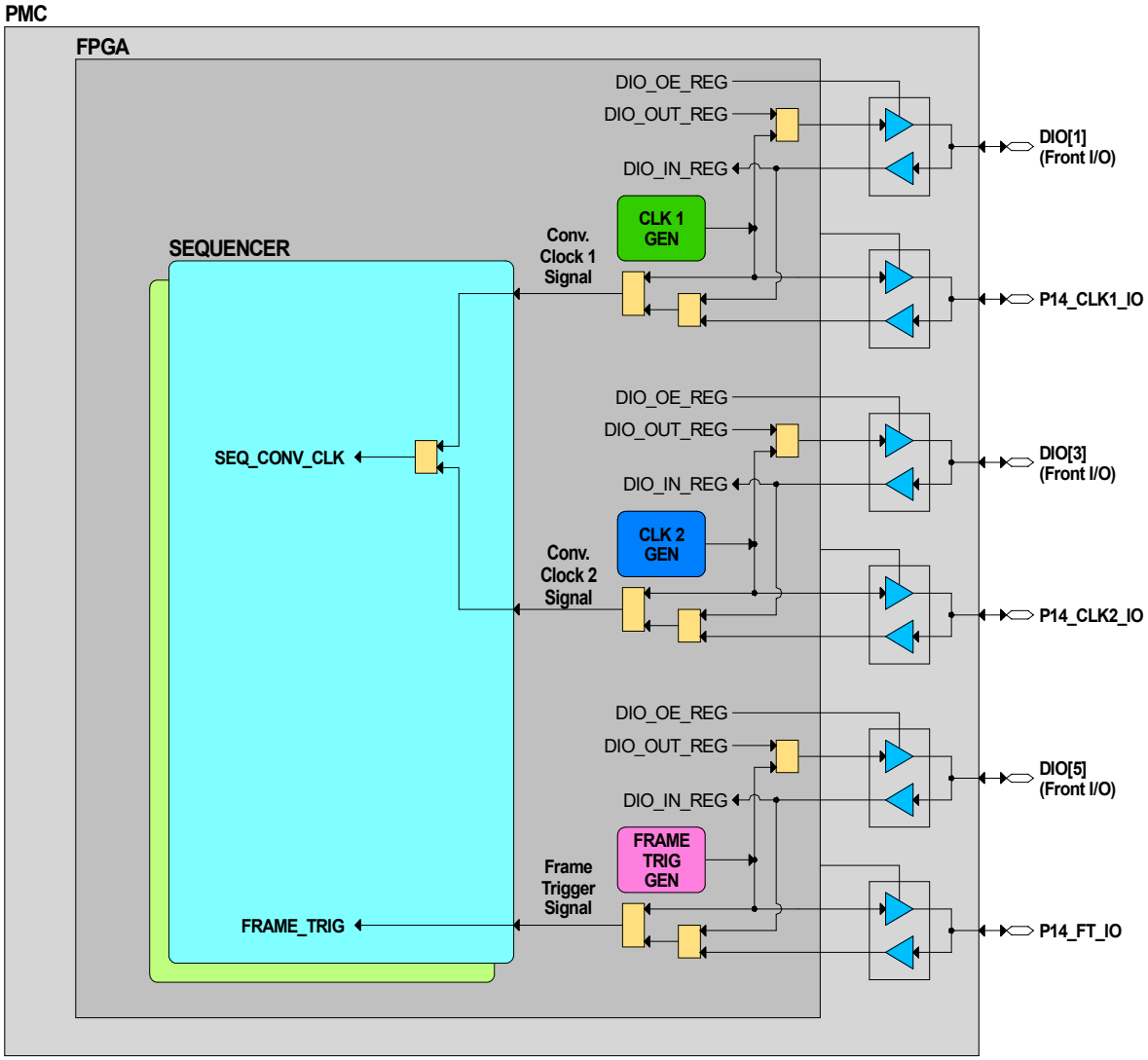


Figure 9-11 : Sequencer Conversion Control Signals Overview

Note that the TPMC543 provides a D/A sequencer and an A/D sequencer.

Note that the Frame Trigger Generator output is generated (phase aligned and locked) for either the Clock 1 Generator output signal or for the Clock 2 Generator output signal.

9.6.2 Conversion Control Signals

Available conversion control signals are:

- Conversion Clock Signal 1
- Conversion Clock Signal 2
- Frame Trigger Signal

A conversion clock signal defines the conversion rate for the sequencer.

The frame trigger signal is used to start a sequence of conversions in Sequencer Frame Mode.

For each conversion control signal, the actual signal source is selectable from the following options:

- On-Board signal generator
- Input signal from the (P14 Rear) I/O interface.

9.6.3 Signal Generators

9.6.3.1 Conversion Clock Generators 1 & 2

The PMC provides two Conversion Clock Signal Generators.

Each conversion clock signal generator provides a dedicated selector for the on-board clock source and a configurable divider.

If enabled, the conversion clock signals are generated continuously with the configured rate.

A conversion clock generator signal may be:

- selected as the source for the appropriate conversion clock signal
- driven out on a dedicated I/O pin
- selected as the associated conversion clock signal for the frame trigger signal generator

9.6.3.2 Frame Trigger Generator

The PMC provides a Frame Trigger Signal Generator for generating a configurable number of frame trigger pulses at a configurable frame trigger interval rate.

The frame trigger signal is always generated for an associated conversion clock generator signal. The frame trigger signal can be generated for either the conversion clock generator 1 signal or for the conversion clock generator 2 signal.

The frame trigger signal is generated as a single pulse (inverted) of the associated conversion clock generator signal (see figure below).

The frame trigger interval is programmable in number of cycles of the associated conversion clock signal.

Frame trigger pulses may be generated continuously or in a configurable number.

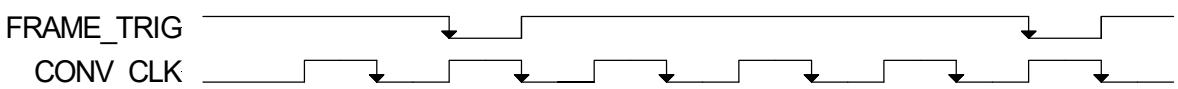


Figure 9-12 : Frame Trigger Signal Example (Frame Interval = 4)

The frame trigger generator signal may be:

- selected as the source of the frame trigger signal
- driven out on a dedicated I/O pin

9.6.4 I/O Signals

The following bi-directional PMC I/O signals are available:

- Conversion Clock Signal 1
- Conversion Clock Signal 2
- Frame Trigger Signal

For each of these signals, the appropriate signal generator output signal may be driven out on either a dedicated (fix) front I/O digital I/O line or on a dedicated (fix) P14 rear I/O pin.

For each of these signals either the dedicated front I/O digital I/O line or the dedicated P14 rear I/O pin may be used as an input. Note that the input function is always available, even if the I/O line is driven by the PMC as an output.

Each of these I/O signals features a dedicated I/O line driver and a dedicated I/O line receiver (both connected to the same I/O pin). When enabled, the driver level is 3.3V LVTTL (TTL compatible). The receivers are accepting LVTTL and/or TTL levels.

9.6.5 Sequencer Conversion Clock Options

The sequencers are operating with a conversion clock signal (for generating conversion pulses for the DAC and ADC devices) that determines the actual D/A conversion rate and A/D sample rate.

Available conversion clock options for a sequencer are:

- Conversion Clock Signal 1
- Conversion Clock Signal 2

Note that in sequencer frame mode, the selected conversion clock source must be phase aligned and locked to the frame trigger signal.

10 I/O Pin Assignment

10.1 Front I/O Connector

Pin-Count	68
Connector Type	Mini D Ribbon (MDR) Receptacle Connector
Source & Order Info	3M N10268-52E2PC or compatible

Table 10-1 : Front I/O Connector Type

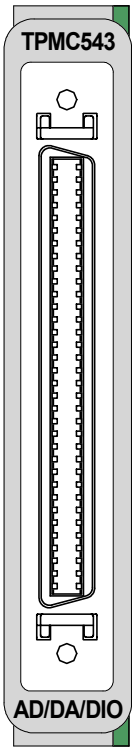
Pin		Pin
1		35
2		36
3		37
…		…
…		…
…		…
32		66
33		67
34		68

Table 10-2 : Front I/O Connector Pin Location

The following I/O pin pairs are assigned to a twisted cable pair inside the matching TA113 Front I/O cable: Pins 1 & 35, Pins 2 & 36, …, Pins 34 & 68.

Signal Type	Direction	Max Level, Range
Analog Current Input	In	Analog Input Range: -25mA … +25mA Differential Input Input Resistance approx. 250Ω (Max ±10.24V per I/O Pin to GND) (Max ±6.25V_{DIFF} per I/O Channel)
Analog High-Voltage Input	In	Analog Input Range (per I/O Pin to GND): -48V … +48V
Analog Output	Out	Analog Output Pin Range (to GND): Voltage Mode: -12V … +12V Current Mode: 0mA … +24mA
Digital I/O Line	In/Out	3.3V LVTTL Driver with Tri-State Capability Input 5V tolerant LVTTL/TTL Programmable common Pull Resistor Reference (open, 5V, 3.3V or GND)

Table 10-3 : Front I/O Signal Types

Care must be taken not to confuse the Analog Current Input I/O pins with the Analog High-Voltage Input I/O pins since the passive analog input circuit part is not protected!

Applying currents greater than |25mA| (or differential voltages greater than |6.25V|) to an analog current input may permanently damage the resistors in the analog current input path!

For the High-Voltage Analog Input Configuration, care must be taken as there may be on-board voltage potentials of about twice the highest signal voltage level.

E.g. the voltage between A/D channel I/O pins is 96V when one A/D channel input voltage is at +48V to ground while the other A/D channel input voltage is at -48V to ground.

This may be extremely dangerous (especially for AC signals)!

Measures must be taken to prevent users from touching card contacts while external signal generators are in operation!

10.1.1 TPMC543-10R I/O Pin Assignment

Signal	Type	Pin		Pin	Type	Signal
ADC#1_IN3+	CI	1		35	CI	ADC#1_IN3-
ADC#1_IN2+	CI	2		36	CI	ADC#1_IN2-
GND		3		37		GND
ADC#1_IN1+	CI	4		38	CI	ADC#1_IN1-
ADC#1_IN0+	CI	5		39	CI	ADC#1_IN0-
ADC#2_IN3+	CI	6		40	CI	ADC#2_IN3-
ADC#2_IN2+	CI	7		41	CI	ADC#2_IN2-
GND		8		42		GND
ADC#2_IN1+	CI	9		43	CI	ADC#2_IN1-
ADC#2_IN0+	CI	10		44	CI	ADC#2_IN0-
ADC#3_IN6/3+	HVI	11		45	HVI	ADC#3_IN7/3-
ADC#3_IN4/2+	HVI	12		46	HVI	ADC#3_IN5/2-
GND		13		47		GND
ADC#3_IN2/1+	HVI	14		48	HVI	ADC#3_IN3/1-
ADC#3_IN0/0+	HVI	15		49	HVI	ADC#3_IN1/0-
ADC#4_IN6/3+	HVI	16		50	HVI	ADC#4_IN7/3-
ADC#4_IN4/2+	HVI	17		51	HVI	ADC#4_IN5/2-
GND		18		52		GND
ADC#4_IN2/1+	HVI	19		53	HVI	ADC#4_IN3/1-
ADC#4_IN0/0+	HVI	20		54	HVI	ADC#4_IN1/0-
DAC#1_ OUT_D	V/CO	21		55		GND
DAC#1_ OUT_C	V/CO	22		56		GND
DAC#1_ OUT_B	V/CO	23		57		GND
DAC#1_ OUT_A	V/CO	24		58		GND
DAC#2_ OUT_D	V/CO	25		59		GND
DAC#2_ OUT_C	V/CO	26		60		GND
DAC#2_ OUT_B	V/CO	27		61		GND
DAC#2_OUT_A	V/CO	28		62		GND
GND		29		63		GND
DIO_1	DIO	30		64	DIO	DIO_2
DIO_3	DIO	31		65	DIO	DIO_4
GND		32		66		GND
DIO_5	DIO	33		67	DIO	DIO_6
DIO_7	DIO	34		68	DIO	DIO_8

CI: Current Input, HVI: High-Voltage Input, V/CO: Voltage/Current Output, DIO: Digital I/O

Table 10-4 : TPMC543-10R Front I/O Pin Assignment

Unused Analog Input Pins (ADC#x…) shall be connected to GND!

Note that the analog outputs may be either used in Voltage Mode or in Current Mode.

Using the analog output in Current Mode requires connecting a load resistor to GND.
Higher load resistance means higher power requirements for the PMC 5V power supply and higher overall heat dissipation. Although an analog output channel would be capable to provide up to 24mA with a 1K load resistor, such high load resistance is not recommended.

Load resistors of less than 680Ω are recommended for D/A channels in Current Mode.
Load resistance for D/A channels in Current Mode shall not exceed 680Ω.

In analog input mode, higher sampling rates may be obtained with a limited number of utilized channels. In general the utilized channels shall be distributed over the ADC devices starting with channel 0 of each ADC device.

Note that the digital I/O lines are merely intended to be used is a static way. Since the digital I/O lines are running in the same I/O cable as the analog input and analog output lines, any dynamic activity on the digital I/O lines will generate noticeable noise in the analog signals.

10.2 P14 Rear I/O Connector

Pin-Count	64
Connector Type	CMC Plug Connector
Source & Order Info	Molex 71436-2864

Table 10-5 : P14 Rear I/O Connector Type

Pin	I/O Signal	Dir.	Level	Pin	I/O Signal	Dir.	Level
1	CNV_CLK_1	In/Out	LVTTL, TTL	2	GND		
3	GND			4			
5				6			
7				8			
9				10			
11				12			
13				14			
15				16			
17				18			
19	CNV_CLK_2	In/Out	LVTTL, TTL	20	GND		
21	GND			22			
23				24			
25				26			
27				28			
29				30			
31				32			
33				34			
35				36			
37	FRAME_TRIG	In/Out	LVTTL, TTL	38	GND		
39	GND			40			
41				42			
43				44			
45				46			
47				48			
49				50			
51				52			
53				54			
55	Reserved	In/Out	LVTTL, TTL	56	GND		
57	GND			58			
59				60			
61				62			
63				64			

Table 10-6 : P14 Rear I/O Pin Assignment

11 Programming Hints

11.1 Global DAC Status Register Read

Whenever the Global DAC Status Register is read right after a register write (e.g. to evaluated the DAC Busy Status right after a manual DAC Reset Request write, DAC Configuration Register write or DAC Data Register write) the read data of the first Global DAC Status Register read must be discarded.

In other words: Whenever the Global DAC Status Register is read right after a register write, a single leading dummy read of the Global DAC Status Register is required.