The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC554

32 / 16 Channels of 16 bit D/A with memory

Version 1.0

User Manual

Issue 1.0.2

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TPMC554-10R

32 Channels of 16 bit D/A with memory (RoHS compliant)

TPMC554-11R

16 Channels of 16 bit D/A with memory (RoHS compliant)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial issue	October 2009
1.0.1	STOP bit added to FIFO X Status/Control Register	October 2010
1.0.2	Pin 67 and 68 of Front I/O Connector are not connected DAC Correction revised	December 2010

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1 Product Description

The TPMC554 is a standard single-wide 32 bit PMC module and provides 32/16 channels of 16 bit analog outputs. All signals are accessible through a HD68 SCSI-3 type front I/O connector. The software selectable output voltage ranges are 0V-5V, 0V-10V, 0V-10.8V, ±5V, ±10V and ±10.8V. The output voltage range can be set individually per channel. The conversion time is typ. 10µs and the DAC outputs are capable to drive a load of 2kΩ, with a capacitance up to 4000pF.

Besides of an individual channel update, the double buffered DACs allow simultaneous update of all channels. Additionally a sequencer on the TPMC554 allows updating enabled channels periodically with a sequence timer range that extends from 10µs to 11.93h.

In addition to the double buffered distributed RAM inside the FPGA the TPMC554 provides 2M x 16 bit external SRAM to store values that are known in advance. This feature can also be used to periodically output any kind of waveform or bit pattern. The size of the FIFO for each DAC channel is adjustable.

Each TPMC554 is factory calibrated. The correction data is stored in an on board serial EEPROM unique to each PMC module.

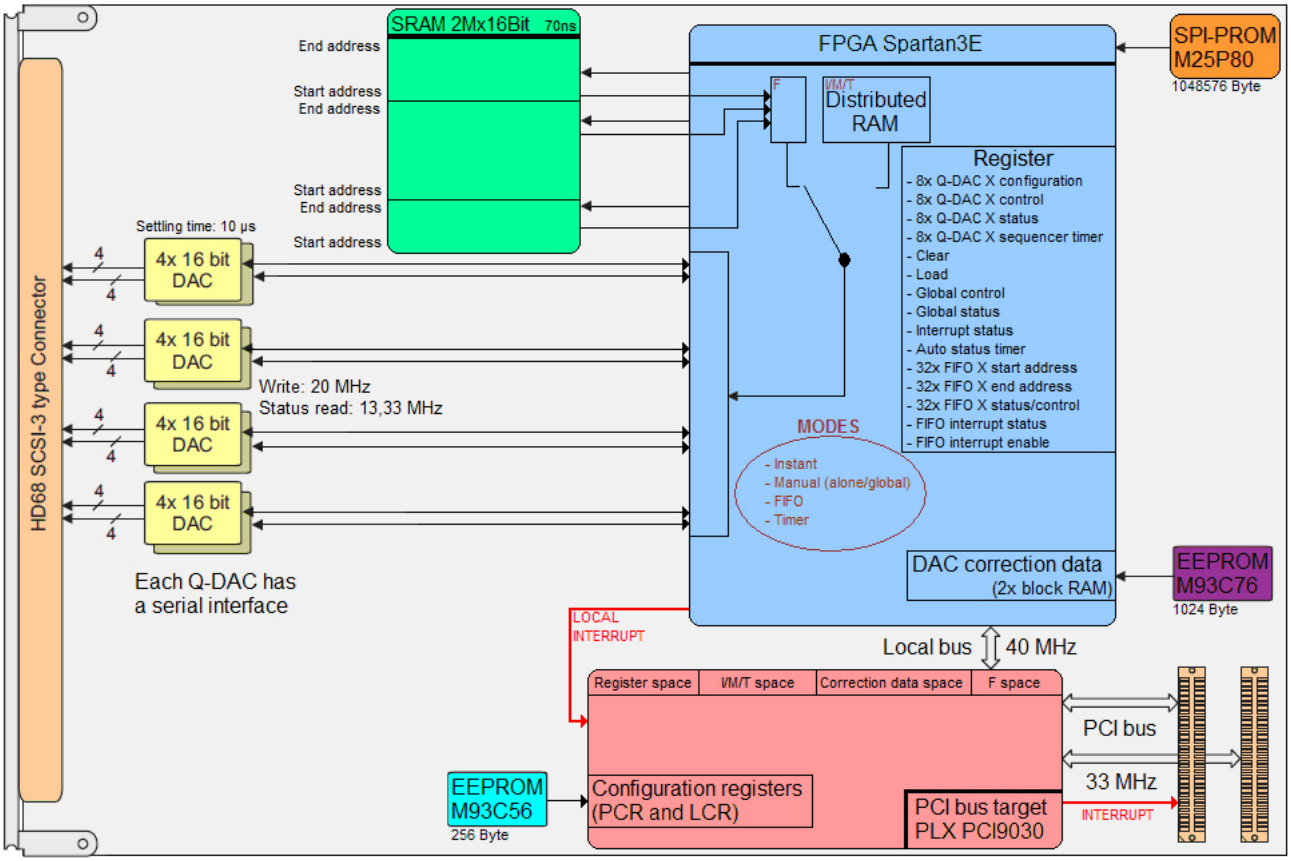

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size	
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9030 (PLX Technology)	
Quad-DAC	AD5754R (Analog Devices)	
SRAM	A64S06161A (Amic)	
I/O Interface		
Number of D/A Channels	TPMC554-10R: 32 D/A channels TPMC554-11R: 16 D/A channels	
D/A Resolution	16 bit	
D/A Output Voltage Range	Selectable: 0V to 5V, 0V to 10V, 0V to 10.8V, ±5V, ±10V, ±10.8V	
D/A Channel Load	max. 2kΩ | 4000pF per D/A channel	
D/A Channel Settling Time	max. 10µs	
D/A Protection	20mA current limit option, thermal shutdown option	
D/A Calibration	Calibration data for gain and offset correction	
D/A INL/DNL Error	±16/±1 LSB	
I/O Connector	Front I/O HD68 / SCSI-3 (AMP 5-787082-7 or compatible)	
Physical Data		
Power Requirements	200mA typical @ 3.3V 600mA typical @ 5V (±10V output, 2kΩ load)	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	TPMC554-10R: 665000 h TPMC554-11R: 678000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	86 g	

Table 2-1 : Technical Specification

3 General notes on the TPMC554 Quad-DACs

The TPMC554 is using Quad-DAC (Q-DAC) devices. Each Q-DAC device provides four D/A channels, internally called A, B, C and D.

The TPMC554-10R provides 32 D/A channels (1 to 32), thus eight Q-DAC devices (1 to 8). The TPMC554-11R provides 16 D/A channels (1 to 16), thus four Q-DAC devices (1 to 4).

The Q-DAC device provides four internal data registers, one for each of the four D/A channels.

To set a certain analog output voltage, the D/A channel data is written to the I/M/T-Space or the F-Space, from where it is transferred to the appropriate Q-DAC internal D/A channel data register automatically. The Q-DAC analog outputs are then updated, depending on the Q-DAC operating mode used.

Each Q-DAC device provides a single serial interface, so all transfers to the Q-DACs are in fact serial data transfers. A data transfer to a Q-DAC takes approx. 1.4µs per D/A channel, data transfer for all four Q-DAC D/A channels takes approx. 5.6µs. A Q-DAC status read takes approx. 3.4µs.

The Q-DAC data transfer engines (parallel/serial) are independent of each other (e.g. data for D/A channels 1, 2, 3 & 4 is transferred one channel after the other since these channels are located in the same Q-DAC, while data for D/A channels 1, 5, 9, 13 could be transferred all at the same time since these channels are located in different Q-DACs.

TPMC554 D/A Channel	Q-DAC	Q-DAC internal Channel
D/A Channel 1	Q-DAC 1	A
D/A Channel 2		B
D/A Channel 3		C
D/A Channel 4		D
D/A Channel 5	Q-DAC 2	A
D/A Channel 6		B
D/A Channel 7		C
D/A Channel 8		D
D/A Channel 9	Q-DAC 3	A
D/A Channel 10		B
D/A Channel 11		C
D/A Channel 12		D
D/A Channel 13	Q-DAC 4	A
D/A Channel 14		B
D/A Channel 15		C
D/A Channel 16		D
D/A Channel 17	Q-DAC 5	A
D/A Channel 18		B
D/A Channel 19		C
D/A Channel 20		D

TPMC554 D/A Channel	Q-DAC	Q-DAC internal Channel
D/A Channel 21	Q-DAC 6	A
D/A Channel 22		B
D/A Channel 23		C
D/A Channel 24		D
D/A Channel 25	Q-DAC 7	A
D/A Channel 26		B
D/A Channel 27		C
D/A Channel 28		D
D/A Channel 29	Q-DAC 8	A
D/A Channel 30		B
D/A Channel 31		C
D/A Channel 32		D

Table 3-1 : D/A Channel to Q-DAC mapping

4 Local Space Addressing

4.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	MEM	1024	32	BIG	Register-Space
1	3 (0x1C)	MEM	64	32	BIG	I/M/T-Space
2	4 (0x20)	MEM	1024	32	BIG	Correction-Data-Space
3	5 (0x24)	MEM	8192	32	BIG	F-Space

Table 4-1 : PCI9030 Local Space Configuration

4.2 Register-Space (1024 Byte)

PCI Base Address: **PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).**

Offset to PCI Base Address 2	Description	Size (Bit)
0x000	Q-DAC 1 Configuration Register	32
0x004	Q-DAC 2 Configuration Register	32
0x008	Q-DAC 3 Configuration Register	32
0x00C	Q-DAC 4 Configuration Register	32
0x010	Q-DAC 5 Configuration Register	32
0x014	Q-DAC 6 Configuration Register	32
0x018	Q-DAC 7 Configuration Register	32
0x01C	Q-DAC 8 Configuration Register	32
0x020	Q-DAC 1 Control Register	32
0x024	Q-DAC 2 Control Register	32
0x028	Q-DAC 3 Control Register	32
0x02C	Q-DAC 4 Control Register	32
0x030	Q-DAC 5 Control Register	32
0x034	Q-DAC 6 Control Register	32
0x038	Q-DAC 7 Control Register	32
0x03C	Q-DAC 8 Control Register	32
0x040	Q-DAC 1 Status Register	32
0x044	Q-DAC 2 Status Register	32
0x048	Q-DAC 3 Status Register	32
0x04C	Q-DAC 4 Status Register	32
0x050	Q-DAC 5 Status Register	32
0x054	Q-DAC 6 Status Register	32
0x058	Q-DAC 7 Status Register	32
0x05C	Q-DAC 8 Status Register	32
0x060	Q-DAC 1 Sequencer Timer Register	32
0x064	Q-DAC 2 Sequencer Timer Register	32
0x068	Q-DAC 3 Sequencer Timer Register	32
0x06C	Q-DAC 4 Sequencer Timer Register	32
0x070	Q-DAC 5 Sequencer Timer Register	32
0x074	Q-DAC 6 Sequencer Timer Register	32
0x078	Q-DAC 7 Sequencer Timer Register	32
0x07C	Q-DAC 8 Sequencer Timer Register	32
0x080	Clear Register	32
0x084	Load Register	32

Offset to PCI Base Address 2	Description	Size (Bit)
0x088	Global Control Register	32
0x08C	Global Status Register	32
0x090	Interrupt Status Register	32
0x094	Auto Status Timer Register	32
0x098	FIFO 1 Start Address Register	32
0x09C	FIFO 2 Start Address Register	32
0x0A0	FIFO 3 Start Address Register	32
0x0A4	FIFO 4 Start Address Register	32
0x0A8	FIFO 5 Start Address Register	32
0x0AC	FIFO 6 Start Address Register	32
0x0B0	FIFO 7 Start Address Register	32
0x0B4	FIFO 8 Start Address Register	32
0x0B8	FIFO 9 Start Address Register	32
0x0BC	FIFO 10 Start Address Register	32
0x0C0	FIFO 11 Start Address Register	32
0x0C4	FIFO 12 Start Address Register	32
0x0C8	FIFO 13 Start Address Register	32
0x0CC	FIFO 14 Start Address Register	32
0x0D0	FIFO 15 Start Address Register	32
0x0D4	FIFO 16 Start Address Register	32
0x0D8	FIFO 17 Start Address Register	32
0x0DC	FIFO 18 Start Address Register	32
0x0E0	FIFO 19 Start Address Register	32
0x0E4	FIFO 20 Start Address Register	32
0x0E8	FIFO 21 Start Address Register	32
0x0EC	FIFO 22 Start Address Register	32
0x0F0	FIFO 23 Start Address Register	32
0x0F4	FIFO 24 Start Address Register	32
0x0F8	FIFO 25 Start Address Register	32
0x0FC	FIFO 26 Start Address Register	32
0x100	FIFO 27 Start Address Register	32
0x104	FIFO 28 Start Address Register	32
0x108	FIFO 29 Start Address Register	32
0x10C	FIFO 30 Start Address Register	32
0x110	FIFO 31 Start Address Register	32
0x114	FIFO 32 Start Address Register	32
0x118	FIFO 1 End Address Register	32
0x11C	FIFO 2 End Address Register	32

Offset to PCI Base Address 2	Description	Size (Bit)
0x120	FIFO 3 End Address Register	32
0x124	FIFO 4 End Address Register	32
0x128	FIFO 5 End Address Register	32
0x12C	FIFO 6 End Address Register	32
0x130	FIFO 7 End Address Register	32
0x134	FIFO 8 End Address Register	32
0x138	FIFO 9 End Address Register	32
0x13C	FIFO 10 End Address Register	32
0x140	FIFO 11 End Address Register	32
0x144	FIFO 12 End Address Register	32
0x148	FIFO 13 End Address Register	32
0x14C	FIFO 14 End Address Register	32
0x150	FIFO 15 End Address Register	32
0x154	FIFO 16 End Address Register	32
0x158	FIFO 17 End Address Register	32
0x15C	FIFO 18 End Address Register	32
0x160	FIFO 19 End Address Register	32
0x164	FIFO 20 End Address Register	32
0x168	FIFO 21 End Address Register	32
0x16C	FIFO 22 End Address Register	32
0x170	FIFO 23 End Address Register	32
0x174	FIFO 24 End Address Register	32
0x178	FIFO 25 End Address Register	32
0x17C	FIFO 26 End Address Register	32
0x180	FIFO 27 End Address Register	32
0x184	FIFO 28 End Address Register	32
0x188	FIFO 29 End Address Register	32
0x18C	FIFO 30 End Address Register	32
0x190	FIFO 31 End Address Register	32
0x194	FIFO 32 End Address Register	32
0x198	FIFO 1 Status/Control Register	32
0x19C	FIFO 2 Status/Control Register	32
0x1A0	FIFO 3 Status/Control Register	32
0x1A4	FIFO 4 Status/Control Register	32
0x1A8	FIFO 5 Status/Control Register	32
0x1AC	FIFO 6 Status/Control Register	32
0x1B0	FIFO 7 Status/Control Register	32
0x1B4	FIFO 8 Status/Control Register	32

Offset to PCI Base Address 2	Description	Size (Bit)
0x1B8	FIFO 9 Status/Control Register	32
0x1BC	FIFO 10 Status/Control Register	32
0x1C0	FIFO 11 Status/Control Register	32
0x1C4	FIFO 12 Status/Control Register	32
0x1C8	FIFO 13 Status/Control Register	32
0x1CC	FIFO 14 Status/Control Register	32
0x1D0	FIFO 15 Status/Control Register	32
0x1D4	FIFO 16 Status/Control Register	32
0x1D8	FIFO 17 Status/Control Register	32
0x1DC	FIFO 18 Status/Control Register	32
0x1E0	FIFO 19 Status/Control Register	32
0x1E4	FIFO 20 Status/Control Register	32
0x1E8	FIFO 21 Status/Control Register	32
0x1EC	FIFO 22 Status/Control Register	32
0x1F0	FIFO 23 Status/Control Register	32
0x1F4	FIFO 24 Status/Control Register	32
0x1F8	FIFO 25 Status/Control Register	32
0x1FC	FIFO 26 Status/Control Register	32
0x200	FIFO 27 Status/Control Register	32
0x204	FIFO 28 Status/Control Register	32
0x208	FIFO 29 Status/Control Register	32
0x20C	FIFO 30 Status/Control Register	32
0x210	FIFO 31 Status/Control Register	32
0x214	FIFO 32 Status/Control Register	32
0x218	FIFO Interrupt Status Register	32
0x21C	FIFO Interrupt Enable Register	32

Table 4-2 : Register-Space Address Map

The Register-Space requires using 32 bit transfer size.

Registers / Register bits for Q-DACs 5 - 8 are supported for 32 D/A channel TPMC554 options only.

4.2.1 Q-DAC X Configuration Register (X = 1-8)

There is a dedicated Q-DAC Configuration Register for each Q-DAC.

Each Q-DAC provides four D/A Channels, internally called A - D. Each Q-DAC also provides internal registers for device configuration.

If the Q-DAC busy bit in the Global Status Register is clear, a write to a Q-DAC X Configuration Register starts the Q-DAC configuration (i.e. the Q-DAC configuration register setting is transferred to the Q-DAC internal configuration register). Each Q-DAC configuration sequence does also include a read of the Q-DAC status (see Q-DAC X Status Register).

Check the Q-DAC busy bit in the Global Status Register to determine when the Q-DAC configuration is done.

Each Q-DAC that is used must be configured first. A D/A Channel can only be used if it's PUx-bit is set.

Writes to a Q-DAC Configuration Register are ignored, when the Q-DAC busy bit is set in the Global Status Register.

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved Set '0' for writes, undefined for reads.	-	-
19	PUD	D/A Channel D Power-Up See PUA description.	R/W	0
18	PUC	D/A Channel C Power-Up See PUA description.	R/W	0
17	PUB	D/A Channel B Power-Up See PUA description.	R/W	0
16	PUA	D/A Channel A Power-Up. When set, this bit places DAC A in normal operating mode. When cleared, this bit places DAC A in power-down mode (default).	R/W	0
15	TSD ENA	TSD Enable Set to enable the Q-DAC thermal shutdown feature. Cleared to disable the thermal shutdown feature (default). The Q-DAC incorporates a thermal shutdown feature that automatically shuts down the device if the max device temperature is exceeded.	R/W	0
14	CL ENA	Clamp Enable Set to enable the current limit clamp (default). The channel current is clamped at 20mA in case of over-current. Clear to disable the current-limit clamp. The channel powers down in case of over-current.	R/W	1

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>13</td><td>CLR SEL</td><td>Q-DAC Clear Select
Selects the D/A Channel default values in case the Q-DAC is cleared using the Clear Register.

<table><tr><th>CLR SEL</th><th>Unipolar Output Range</th><th>Bipolar Output Range</th></tr><tr><td>0</td><td>0V</td><td>0V</td></tr><tr><td>1</td><td>Mid-scale</td><td>Negative Full-scale</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>12</td><td>-</td><td>Reserved
Set '0' for writes, undefined for reads.</td><td>-</td><td>-</td></tr>
<tr><td>11:9</td><td>ORD</td><td>D/A Channel D Output Range
See ORA description.</td><td>R/W</td><td>000</td></tr>
<tr><td>8:6</td><td>ORC</td><td>D/A Channel C Output Range
See ORA description.</td><td>R/W</td><td>000</td></tr>
<tr><td>5:3</td><td>ORB</td><td>D/A Channel B Output Range
See ORA description.</td><td>R/W</td><td>000</td></tr>
<tr><td>2:0</td><td>ORA</td><td>D/A Channel A Output Range

<table><tr><th>ORA</th><th>Output Voltage Range</th></tr><tr><td>000</td><td>+5V</td></tr><tr><td>001</td><td>+10V</td></tr><tr><td>010</td><td>+10.8V</td></tr><tr><td>011</td><td>±5V</td></tr><tr><td>100</td><td>±10V</td></tr><tr><td>101</td><td>±10.8V</td></tr><tr><td>others</td><td>reserved</td></tr></table></td><td>R/W</td><td>000</td></tr>
</table>

Table 4-3 : Q-DAC X Configuration Register (Offset 0x000 …)

4.2.2 Q-DAC X Control Register (X = 1-8)

Bit	Symbol	Description	Access	Reset Value
31:10	-	Reserved Set '0' for writes, undefined for reads.	-	-
9	RDSTA	Read internal Q-DAC status register Only valid for I-Mode and M-Mode (ignored for other QDAC modes). When set, a request for reading the Q-DAC status is logged and the status valid bit in the Q-DAC X Status Register is cleared. When the Q-DAC status read is done, the Q-DAC X Status Register is updated and the status valid bit is set again. The actual Q-DAC status read may be delayed by ongoing processes. Bit clears immediately.	W	0
8	GLM	Enable Global Load Mode for this Q-DAC Used in M-Mode only. When set, this QDAC operates in global load mode. In global load mode, all four analog outputs of the Q-DAC are updated simultaneously along with the analog outputs of other Q-DACs set to global load mode when all available D/A channel data has been transferred to the Q-DACs. When clear, this QDAC operates in standalone mode. In standalone mode, all four analog outputs of the Q-DAC are updated simultaneously when all available D/A channel data has been transferred to the Q-DAC.	R/W	0
7	ASR	Automatic Status Read Can be used for I-Mode, M-Mode, F-Mode and T-Mode. Set to enable automatic status reads of the Q-DAC internal status register. Clear to disable automatic status reads. See Auto Status Timer Register for I-Mode and M-Mode. In T-Mode and F-Mode (if enabled) there is one automatic Q-DAC status read per sequence (approx. 10us after the previous Q-DAC update).	R/W	0
6	-	Reserved Set '0' for writes, undefined for reads.	-	-
5	IRQSEEN	Q-DAC Sequencer Interrupt enable Enables Q-DAC Sequencer interrupts when set. Disables Q-DAC Sequencer interrupts when clear. **(Should be disabled for I-Mode, M-Mode and F-Mode)** See Interrupt Status Register for details.	R/W	0
4	IRQALEN	Q-DAC Alert Interrupt enable Enables Q-DAC Alert interrupts when set. Disables Q-DAC Alert interrupts when clear. See Interrupt Status Register for details.	R/W	0
3	IRQLDEN	Q-DAC Load Interrupt enable Enables Q-DAC Load interrupts when set. Disables Q-DAC Load interrupts when clear. **(Should be disabled for I-Mode, F-Mode and T-Mode)** See Interrupt Status Register for details.	R/W	0
2	-	Reserved Set '0' for writes, undefined for reads.	-	-

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>1:0</td><td>MODE</td><td>Q-DAC Mode

<table>
<tr><th>MODE</th><th>Q-DAC Mode</th><th>Description</th></tr>
<tr><td>00</td><td>I-Mode</td><td>Instant Mode
Q-DAC analog outputs are updated immediately after each D/A Channel data transfer</td></tr>
<tr><td>01</td><td>M-Mode</td><td>Manual Mode
Q-DAC analog outputs are updated simultaneously per software command. D/A Channel data has been transferred to the Q-DAC before.</td></tr>
<tr><td>10</td><td>F-Mode</td><td>FIFO Mode
An internal sequencer timer triggers the data transfer to the Q-DAC and the simultaneous update of the Q-DAC analog outputs.
The corresponding FIFOs in the external SRAM are used as data source for the 4 DAC channels.</td></tr>
<tr><td>11</td><td>T-Mode</td><td>Timer Mode
An internal sequencer timer triggers the data transfer to the Q-DAC and the simultaneous update of the Q-DAC analog outputs.
The corresponding distributed RAM inside the FPGA is used as data source for the 4 DAC channels.</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
</table>

Table 4-4 : Q-DAC X Control Register (Offset 0x020 …)

4.2.3 Q-DAC X Status Register (X = 1-8)

The Q-DAC devices used provide an internal status register, which is reflected in the Q-DAC X Status Registers. The Q-DAC X Status Registers are only updated when a status register read is ordered by writing a ‘1’ to the RDSTA bit or when the ASR option is active in Q-DAC X Control Register.

Bit	Symbol	Description	Access	Reset Value
31:11	-	Reserved Set '0' for writes, undefined for reads.	-	-
10	SVAL	Status is valid This bit indicates that the other register bits are showing the result of a Q-DAC status read (no random data). It does not necessarily indicate that the other register bits are showing the most current Q-DAC status. This bit is automatically set after the first Q-DAC status read (e.g. during Q-DAC configuration). The bit is cleared upon a Q-DAC status read request via the Q-DAC X Control Register in I-Mode or M-Mode. The bit is then automatically set again, when the requested Q-DAC status read is done.	R	0
9	TSD	Thermal Shutdown Alert In the event of an over-temperature situation, this bit is set.	R	0
8	PUREF	Reference Power-Up When set, this bit indicates that the Quad-DAC internal reference is powered-up. Since the TPMC554 Quad-DACs are operating with internal reference, this bit should always be set for any status read from the Quad-DAC.	R	0
7	PUD	DAC D Power-Up See PUA description.	R	0
6	PUC	DAC C Power-Up See PUA description.	R	0
5	PUB	DAC B Power-Up See PUA description.	R	0
4	PUA	DAC A Power-Up ‘0’ when powered down, ‘1’ when powered up. If the Q-DAC is configured with CL ENA bit clear, DAC A will power down automatically on detection of an over-current, PUA will be cleared to reflect this.	R	0
3	OCD	DAC D Over-current Alert See OCA description.	R	0
2	OCC	DAC C Over-current Alert See OCA description.	R	0
1	OCB	DAC B Over-current Alert See OCA description.	R	0
0	OCA	DAC A Over-current Alert In the event of an over-current situation on DAC A, this bit is set.	R	0

Table 4-5 : Q-DAC X Status Register (Offset 0x040 …)

4.2.4 Q-DAC X Sequencer Timer Register (X = 1-8)

Bit	Symbol	Description	Access	Reset Value
31:0	STPV	Sequencer Timer Preload Value Controls the time between consecutive Q-DAC analog output-updates in F-Mode and T-Mode. Actual time between consecutive Q-DAC analog output updates is (STPV + 1) x 10us.	R/W	0

Table 4-6 : Q-DAC X Sequencer Timer Register (Offset 0x060 …)

The Sequencer Timer is programmable from 10µs to 11.93h in 10µs steps. The time base for the sequencer timer is derived from an on board 40 MHz oscillator.

4.2.5 Clear Register

The Clear Register can be used to clear the 4 channels of a specific Q-DAC or to perform a global clear.

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved Set '0' for writes, undefined for reads.	-	-
7	CLR8	There is one clear control bit for each Q-DAC. When set, the Q-DAC clear signal is asserted. Could be used to set all four Q-DAC channels (internal D/A Channel registers and analog outputs) to a value specified by the Q-DACs CLR SEL setting (see Q-DAC Configuration Register).	R/W	0
6	CLR7		R/W	0
5	CLR6		R/W	0
4	CLR5		R/W	0
3	CLR4		R/W	0
2	CLR3		R/W	0
1	CLR2		R/W	0
0	CLR1		R/W	0

Table 4-7 : Clear Register (Offset 0x080)

Do not change the output voltage range while the Q-DAC clear signal is active, as this might put the analog outputs to a value other than 0V.

4.2.6 Load Register

The Load Register can be used to load (=update) the 4 channels of a specific Q-DAC or to perform a global load. **(For M-Mode only)**

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved Set '0' for writes, undefined for reads.	-	-
7	LOAD8	Q-DAC Analog Output Update Request. There is one load control/status bit for each Q-DAC. Only valid for M-Mode (ignored for other Q-DAC modes). When set, a request is logged to update the Q-DAC analog outputs. When the request has been logged, the Q-DAC analog outputs are updated when all available D/A Channel data for this Q-DAC has been transferred to the Q-DAC internal data registers. If the Q-DAC is configured for Global-M-Mode, the update of the Q-DAC analog outputs is delayed until all Q-DACs in Global-M-Mode are ready for updating their analog outputs simultaneously. The bit is automatically cleared when the Q-DAC analog outputs are actually updated.	R/W	0
6	LOAD7		R/W	0
5	LOAD6		R/W	0
4	LOAD5		R/W	0
3	LOAD4		R/W	0
2	LOAD3		R/W	0
1	LOAD2		R/W	0
0	LOAD1		R/W	0

Table 4-8 : Load Register (Offset 0x084)

In M-Mode, after setting a LOAD-bit, software shall check that this bit is clear, before new DAC data for this Q-DAC is written to the I/M/T-Space (since, once written to the I/M/T-Space, the data is transferred to the Q-DAC as soon as possible and may interfere with an ongoing update of the analog outputs).

4.2.7 Global Control Register

Bit	Symbol	Description	Access	Reset Value
31:9	-	Reserved Set '0' for writes, undefined for reads.	-	-
8	MIE	Master Interrupt Enable '0': Interrupts are disabled '1': Interrupts are enabled There are also dedicated enable/disable bits for the various interrupt sources ➔ See Q-DAC X Control Register and FIFO Interrupt Enable Register.	R/W	0
7	SEQST8	Q-DAC Sequencer Start/Stop There is one Sequencer Start/Stop bit for each Q-DAC. 0 : Stop Sequencer 1 : Start Sequencer When the sequencer is running, the Q-DAC busy bit in the global status register is permanently set. When the sequencer is stopped, any Q-DAC data transfer in progress will terminate normally. Check the Q-DAC busy bit in the Global Status Register to determine when the sequencer is actually stopped. For a simultaneous update of the analog outputs of multiple Q-DACs in F-Mode or T-Mode, set the Q-DAC X Sequencer Timer Registers to the same value and start the sequencers using a single write access.	R/W	0
6	SEQST7		R/W	0
5	SEQST6		R/W	0
4	SEQST5		R/W	0
3	SEQST4		R/W	0
2	SEQST3		R/W	0
1	SEQST2		R/W	0
0	SEQST1		R/W	0

Table 4-9 : Global Control Register (Offset 0x088)

Prior a sequencer start in T-Mode, the following steps are required:

1. Setup the Q-DAC Timer in Q-DAC X Sequencer Timer Register

2. Set the Q-DAC Mode to T-Mode in Q-DAC X Control Register

3. Write the Q-DAC data for the first sequence to the I/M/T-Space.

Prior a sequencer start in F-Mode, the following steps are required:

1. Setup the relevant FIFO X Start Address Register(s) and FIFO X End Address Register(s)

2. Setup the relevant FIFO X Status/Control Register(s)

3. Setup the Q-DAC Timer in Q-DAC X Sequencer Timer Register

4. Set the Q-DAC Mode to F-Mode in Q-DAC X Control Register

5. Write the first packet of Q-DAC data to the F-Space.

4.2.8 Global Status Register

Bit	Symbol	Description	Access	Reset Value
31	SDU8	Q-DAC 8 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
30	SDR8		R/C	0
29	SET8		R	0
28	BUSY8		R	0
27	SDU7	Q-DAC 7 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
26	SDR7		R/C	0
25	SET7		R	0
24	BUS7		R	0
23	SDU6	Q-DAC 6 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
22	SDR6		R/C	0
21	SET6		R	0
20	BUSY6		R	0
19	SDU5	Q-DAC 5 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
18	SDR5		R/C	0
17	SET5		R	0
16	BUSY5		R	0
15	SDU4	Q-DAC 4 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
14	SDR4		R/C	0
13	SET4		R	0
12	BUSY4		R	0
11	SDU3	Q-DAC 3 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
10	SDR3		R/C	0
9	SET3		R	0
8	BUSY3		R	0
7	SDU2	Q-DAC 2 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
6	SDR2		R/C	0
5	SET2		R	0
4	BUSY2		R	0

Bit	Symbol	Description	Access	Reset Value
3	SDU1	Q-DAC 1 Sequencer Data Underflow Bit is set when the sequencer reads the D/A Channel data for the next sequence in T-Mode, but the software has not yet confirmed new D/A Channel data by clearing the Sequencer Data Request/Acknowledge bit. The sequencer continues normally and takes the D/A channel data actually found in the I/M/T-Space. The bit is cleared by writing a '1'. Not relevant in F-Mode because the handshake between FIFO and sequencer is handled internally.	R/C	0
2	SDR1	Q-DAC 1 Sequencer Data Request/Acknowledge Bit is set when the sequencer is requesting new D/A Channel data for the next sequence in T-Mode. The bit is cleared by writing a '1'. Not relevant in F-Mode because the handshake between FIFO and sequencer is handled internally.	R/C	0
1	SET1	Q-DAC 1 Settle Indicates Q-DAC analog output settling time. '1' when Q-DAC analog outputs are settling, '0' when Q-DAC analog outputs are stable. This is no physical representation of any kind, just an internal timer that expires 10µs after an update of the Q-DAC analog outputs.	R	0
0	BUSY1	Q-DAC 1 Busy Set in the following cases: (a) Transfer to the Q-DAC is in progress (configuration data transfer or D/A channel data transfer or status read transfer). Note for I-Mode and M-Mode: Data may be written to the I/M/T-Space while a Q-DAC transfer is in progress. E.g. data for D/A channels 3 & 4 may be written to the I/M/T-Space while the data for D/A channel 1 is actually being transferred to the Q-DAC and thus the busy bit is set. (b) Waiting for actual Q-DAC load in M-Mode (after a load request) (c) Sequencer is running Clear when Q-DAC control logic is in Idle state.	R	0

Table 4-10: Global Status Register (Offset 0x08C)

When the SDR-bit is set, software should write new data for this Q-DAC to the I/M/T-Space. When the D/A Channel data for this Q-DAC have been written, software shall clear this bit to acknowledge the request.

Asserted SDR or SDU flags do not stop the sequencer from running. These flags are for informational purposes only.

4.2.9 Interrupt Status Register

Bit	Symbol	Description	Access	Reset Value
31:25	-	Reserved Set '0' for writes, undefined for reads.	-	-
24	IRQFI	FIFO Interrupt There is one FIFO Interrupt bit representing 1-32 FIFOs depending on the amount of FIFOs with interrupts enabled (see FIFO Interrupt Enable Register). Set when the number of unconverted voltage values in one of the corresponding FIFOs falls below a configurable number or one of the corresponding FIFOs has no more unconverted values at all. The FIFO Interrupt bit is automatically cleared if the FIFOs with interrupts enabled are refilled above the FIFO limits which were set in the corresponding FIFO X Status/Control Registers. See FIFO Interrupt Status Register to determine which channel caused the interrupt. See FIFO Interrupt Enable Register for interrupt enable/disable control. **(Should be disabled if the corresponding Q-DACs are running in I-Mode, M-Mode or T-Mode)**	R	0
23	IRQSE8	Q-DAC Sequencer Interrupt There is one Sequencer Interrupt bit for each Q-DAC. Set when the sequencer logic requests a new D/A Channel data set for the next sequence and the interrupt is enabled. Write '1' to clear the interrupt status bit. See Q-DAC X Control Register for interrupt enable/disable control. **(Should be disabled for I-Mode, M-Mode and F-Mode)**	R/C	0
22	IRQSE7		R/C	0
21	IRQSE6		R/C	0
20	IRQSE5		R/C	0
19	IRQSE4		R/C	0
18	IRQSE3		R/C	0
17	IRQSE2		R/C	0
16	IRQSE1		R/C	0
15	IQRLD8	Q-DAC Load Interrupt There is one Load Interrupt bit for each Q-DAC. Set when Q-DAC has actually been loaded in M-Mode (Q-DAC analog outputs just have been updated) and the interrupt is enabled. Write '1' to clear the interrupt status bit. See Q-DAC X Control Register for interrupt enable/disable control. **(Should be disabled for I-Mode, F-Mode and T-Mode)**	R/C	0
14	IQRLD7		R/C	0
13	IQRLD6		R/C	0
12	IQRLD5		R/C	0
11	IQRLD4		R/C	0
10	IQRLD3		R/C	0
9	IQRLD2		R/C	0
8	IQRLD1		R/C	0
7	IRQAL8	Q-DAC Alert Interrupt There is one Alert Interrupt bit for each Q-DAC. Set when the Q-DAC status is read and any of the over-current bits or the thermal alert bit is set and the interrupt is enabled. Write '1' to clear the interrupt status bit. See Q-DAC X Control Register for interrupt enable/disable control.	R/C	0
6	IRQAL7		R/C	0
5	IRQAL6		R/C	0
4	IRQAL5		R/C	0
3	IRQAL4		R/C	0
2	IRQAL3		R/C	0
1	IRQAL2		R/C	0
0	IRQAL1		R/C	0

Table 4-11: Interrupt Status Register (Offset 0x090)

For an interrupt status bit to be set, the interrupt must be enabled prior to the interrupt event.

An interrupt is asserted if the Master Interrupt Enable bit is set in the Global Control Register and there is at least one bit set in the Interrupt Status Register.

4.2.10 Auto Status Timer Register

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:28</td><td>ASRT8</td><td rowspan="8">Q-DAC Automatic Status Read Timer
There is one Automatic Status Read Timer bit for each Q-DAC.
Only valid if the ASR bit is set for Q-DAC (Q-DAC X Control Register) and only valid for I-Mode and M-Mode.
In Auto Status Read Mode a request for reading the Q-DAC status is logged every ASRTx time. Any ongoing transfer of D/A channel data will be terminated normally before the Q-DAC status read transfer is started.</td><td>R/W</td><td>1000</td></tr>
<tr><td>27:24</td><td>ASRT7</td><td>R/W</td><td>1000</td></tr>
<tr><td>23:20</td><td>ASRT6</td><td>R/W</td><td>1000</td></tr>
<tr><td>19:16</td><td>ASRT5</td><td>R/W</td><td>1000</td></tr>
<tr><td>15:12</td><td>ASRT4</td><td>R/W</td><td>1000</td></tr>
<tr><td>11:8</td><td>ASRT3</td><td>R/W</td><td>1000</td></tr>
<tr><td>7:4</td><td>ASRT2</td><td>R/W</td><td>1000</td></tr>
<tr><td>3:0</td><td>ASRT1</td><td>R/W</td><td>1000</td></tr>
</table>

ASRT1	Time
0000	10us
0001	20us
0010	40us
0011	80us
0100	160us
0101	320us
0110	640us
0111	1.280ms
1000	2.560ms
1001	5.120ms
1010	10.240ms
1011	20.480ms
1100	40.960ms
1101	81.920ms
1110	163.840ms
1111	327.680ms

Table 4-12: Auto Status Timer Register (Offset 0x094)

4.2.11 FIFO X Start Address Register (X = 1-32)

Bit	Symbol	Description	Access	Reset Value
31:21	-	Reserved Set '0' for writes, undefined for reads.	-	-
20:0	FSTA	FIFO start address This is the first SRAM address with data for channel X.	R/W	0

Table 4-13: FIFO X Start Address Register (Offset 0x098 …)

4.2.12 FIFO X End Address Register (X = 1-32)

Bit	Symbol	Description	Access	Reset Value
31:21	-	Reserved Set '0' for writes, undefined for reads.	-	-
20:0	FSTO	FIFO end address This is the last SRAM address with data for channel X. When data has been written at this address, the pointer returns to the corresponding FIFO X start address.	R/W	0

Table 4-14: FIFO X End Address Register (Offset 0x118 …)

There are no checks against overlapping memory partitions.

The End Address must be greater than the Start Address.

4.2.13 FIFO X Status/Control Register (X = 1-32)

Bit	Symbol	Description	Access	Reset Value
31	STOP	Stop when empty If this bit is set and there are no more unconverted voltage values in the FIFO (the FIFO is empty) no more values are read from the FIFO and the corresponding DAC channel continuous to output the last voltage that was converted. To be able to output a waveform or a bit pattern stored in the FIFO periodically, this bit must not be set.	R/W	0
30:10	NUMB	Number of unconverted voltage values These bits reflect how full the FIFO currently is	R	0
9	FULL	FIFO full If there is no more space for new data in the FIFO, this bit is set and data written to the FIFO's address space in F-Space gets lost	R	0
8	AEMPTY	FIFO almost empty If the number of unconverted voltage values in the FIFO falls below the adjustable FIFO limit, this bit is set and IRQFIx in the FIFO Interrupt Status Register is set if the interrupt is enabled in FIFO Interrupt Enable Register.	R	1

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>7</td><td>EMPTY</td><td>FIFO empty
If there are no more unconverted voltage values in the FIFO, this bit is set and IRQFIx in the FIFO Interrupt Status Register is set if the interrupt is enabled in FIFO Interrupt Enable Register.</td><td>R</td><td>1</td></tr>
<tr><td>6</td><td>FEN</td><td>FIFO enable
Setting this bit enables the FIFO. Only enabled FIFOs are read out by the sequencer and can cause interrupts.</td><td>R/W</td><td>0</td></tr>
<tr><td>5</td><td>FLUSH</td><td>FIFO flush bit
By setting this bit the FIFO write and read pointers are set to the FIFO start address. The corresponding Q-DAC sequencer must be disabled prior to setting this bit. Bit clears immediately. After changing FIFO start address this bit must be set.</td><td>W</td><td>0</td></tr>
<tr><td>4:0</td><td>FLIM</td><td>FIFO Limit
When the number of unconverted voltage values in the FIFO falls below 2^{FLIM}, the AEMPTY bit is set and IRQFI in the Interrupt Status Register is set if the interrupt is enabled. The number of values at which an interrupt is asserted should be smaller than the FIFO size.
<table>
<tr><th>FLIM</th><th>number of 16bit values</th></tr>
<tr><td>00000</td><td>1</td></tr>
<tr><td>00001</td><td>2</td></tr>
<tr><td>00010</td><td>4</td></tr>
<tr><td>00011</td><td>8</td></tr>
<tr><td>00100</td><td>16</td></tr>
<tr><td>00101</td><td>32</td></tr>
<tr><td>00110</td><td>64</td></tr>
<tr><td>00111</td><td>128</td></tr>
<tr><td>01000</td><td>256</td></tr>
<tr><td>01001</td><td>512</td></tr>
<tr><td>01010</td><td>1K</td></tr>
<tr><td>01011</td><td>2K</td></tr>
<tr><td>01100</td><td>4K</td></tr>
<tr><td>01101</td><td>8K</td></tr>
<tr><td>01110</td><td>16K</td></tr>
<tr><td>01111</td><td>32K</td></tr>
<tr><td>10000</td><td>64K</td></tr>
<tr><td>10001</td><td>128K</td></tr>
<tr><td>10010</td><td>256K</td></tr>
<tr><td>10011</td><td>512K</td></tr>
<tr><td>10100</td><td>1M</td></tr>
<tr><td>10101</td><td>2M -1</td></tr>
<tr><td>others</td><td>reserved</td></tr>
</table></td><td>R/W</td><td>00000</td></tr>
</table>

Table 4-15: FIFO X Status/Control Register (Offset 0x198 …)

4.2.14 FIFO Interrupt Status Register

Bit	Symbol	Description	Access	Reset Value
31	IRQFI32	FIFO X interrupt There is a FIFO X interrupt bit for every FIFO signalising that the number of unconverted voltage values in the FIFO has fallen below the FIFO limit, set in FIFO X Status/Control register or that there are no more unconverted values in the FIFO at all (i. e. the FIFO is empty). FIFO Interrupt has to be enabled in FIFO Interrupt Enable Register for the FIFO X interrupt bit to be set. A FIFO X interrupt will automatically set the FIFO Interrupt bit in the Interrupt Status Register and assert a PCI interrupt if the Master Interrupt Enable bit is set. The FIFO X interrupt bit is automatically cleared if the FIFO is refilled above the FIFO limits which were set in the corresponding FIFO X Status/Control Register. See FIFO X Status/Control Register for the reason of the interrupt. See FIFO Interrupt Enable Register for interrupt enable/disable control.	R	0
30	IRQFI31		R	0
29	IRQFI30		R	0
28	IRQFI29		R	0
27	IRQFI28		R	0
26	IRQFI27		R	0
25	IRQFI26		R	0
24	IRQFI25		R	0
23	IRQFI24		R	0
22	IRQFI23		R	0
21	IRQFI22		R	0
20	IRQFI21		R	0
19	IRQFI20		R	0
18	IRQFI19		R	0
17	IRQFI18		R	0
16	IRQFI17		R	0
15	IRQFI16		R	0
14	IRQFI15		R	0
13	IRQFI14		R	0
12	IRQFI13		R	0
11	IRQFI12		R	0
10	IRQFI11		R	0
9	IRQFI10		R	0
8	IRQFI9		R	0
7	IRQFI8		R	0
6	IRQFI7		R	0
5	IRQFI6		R	0
4	IRQFI5		R	0
3	IRQFI4		R	0
2	IRQFI3		R	0
1	IRQFI2		R	0
0	IRQFI1		R	0

Table 4-16: FIFO Interrupt Status Register (Offset 0x218)

4.2.15 FIFO Interrupt Enable Register

Bit	Symbol	Description	Access	Reset Value
31	IRQFIEN32	FIFO Interrupt enable Enables FIFO interrupts when set. Disables FIFO interrupts when clear. Disabling can be useful if F-Mode shall be used to realize a static waveform generator to output a waveform periodically. For applications like that, the STOP bit in the corresponding FIFO X Status/Control Register must not be set. (Should be disabled if the corresponding Q-DACs are running in I-Mode, M-Mode and T-Mode) See Interrupt Status Register for details.	R/W	0
30	IRQFIEN31		R/W	0
29	IRQFIEN30		R/W	0
28	IRQFIEN29		R/W	0
27	IRQFIEN28		R/W	0
26	IRQFIEN27		R/W	0
25	IRQFIEN26		R/W	0
24	IRQFIEN25		R/W	0
23	IRQFIEN24		R/W	0
22	IRQFIEN23		R/W	0
21	IRQFIEN22		R/W	0
20	IRQFIEN21		R/W	0
19	IRQFIEN20		R/W	0
18	IRQFIEN19		R/W	0
17	IRQFIEN18		R/W	0
16	IRQFIEN17		R/W	0
15	IRQFIEN16		R/W	0
14	IRQFIEN15		R/W	0
13	IRQFIEN14		R/W	0
12	IRQFIEN13		R/W	0
11	IRQFIEN12		R/W	0
10	IRQFIEN11		R/W	0
9	IRQFIEN10		R/W	0
8	IRQFIEN9		R/W	0
7	IRQFIEN8		R/W	0
6	IRQFIEN7		R/W	0
5	IRQFIEN6		R/W	0
4	IRQFIEN5		R/W	0
3	IRQFIEN4		R/W	0
2	IRQFIEN3		R/W	0
1	IRQFIEN2		R/W	0
0	IRQFIEN1		R/W	0

Table 4-17: FIFO Interrupt Enable Register (Offset 0x21C)

4.3 I/M/T-Space (64 Byte)

PCI Base Address: PCI9030 PCI Base Address 3 (Offset 0x1C in PCI Configuration Space).

The I/M/T-Space provides a 16 bit address location for each of the D/A channels and is used for passing D/A Channel data in I-Mode, M-Mode and T-Mode.

The I/M/T-Space is the interface to a 32 x 16 bit wide distributed RAM inside the FPGA. 16 bit or 32 bit transfer sizes may be used.

If a Q-DAC is operating in F-Mode, writes to the I/M/T-Space of the specific 4 channels are not allowed because then they have to be written to one of the corresponding F-Space addresses.

D/A Channels 1 to 4 belong to Q-DAC 1, D/A Channels 5 to 8 belong to Q-DAC 2, and so on.

For I-Mode or M-Mode: If data is written to the I/M/T-Space, the data is transferred to the appropriate Q-DAC (via the Q-DAC serial interface) as soon as possible. Data may be written to the I/M/T-Space while a Q-DAC data transfer is in progress. E.g. data for D/A channels 3 & 4 may be written to the I/M/T-Space while the data for D/A channel 1 is actually being transferred to the Q-DAC and thus the Q-DAC Busy Bit is set in the Global Status Register.

The I/M/T-Space is double buffered. The data is stored in an internal buffer while the DACs are loaded, so that the I/M/T-Space is instantly available for new data after a load command.

16 bit or 32 bit transfer size must be used for accessing the I/M/T-Space.

To optimize data throughput, this space allows 32 bit accesses, which target two subsequent 16 bit words (D/A Channels) (note that the TPMC554 local spaces are set to Big Endian mode).

The I/M/T-Space is readable, but the read values are just showing the value of the previous write to the I/M/T-Space location (they are not read-back from the Q-DAC internal data registers).

Offset to PCI Base Address 3	Description	Q-DAC	Q-DAC internal Channel	Size (Bit)
0x00	D/A Channel 1 Data	Q-DAC 1	A	16
0x02	D/A Channel 2 Data		B	16
0x04	D/A Channel 3 Data		C	16
0x06	D/A Channel 4 Data		D	16
0x08	D/A Channel 5 Data	Q-DAC 2	A	16
0x0A	D/A Channel 6 Data		B	16
0x0C	D/A Channel 7 Data		C	16
0x0E	D/A Channel 8 Data		D	16

Offset to PCI Base Address 3	Description	Q-DAC	Q-DAC internal Channel	Size (Bit)
0x10	D/A Channel 9 Data	Q-DAC 3	A	16
0x12	D/A Channel 10 Data		B	16
0x14	D/A Channel 11 Data		C	16
0x16	D/A Channel 12 Data		D	16
0x18	D/A Channel 13 Data	Q-DAC 4	A	16
0x1A	D/A Channel 14 Data		B	16
0x1C	D/A Channel 15 Data		C	16
0x1E	D/A Channel 16 Data		D	16
0x20	D/A Channel 17 Data	Q-DAC 5	A	16
0x22	D/A Channel 18 Data		B	16
0x24	D/A Channel 19 Data		C	16
0x26	D/A Channel 20 Data		D	16
0x28	D/A Channel 21 Data	Q-DAC 6	A	16
0x2A	D/A Channel 22 Data		B	16
0x2C	D/A Channel 23 Data		C	16
0x2E	D/A Channel 24 Data		D	16
0x30	D/A Channel 25 Data	Q-DAC 7	A	16
0x32	D/A Channel 26 Data		B	16
0x34	D/A Channel 27 Data		C	16
0x36	D/A Channel 28 Data		D	16
0x38	D/A Channel 29 Data	Q-DAC 8	A	16
0x3A	D/A Channel 30 Data		B	16
0x3C	D/A Channel 31 Data		C	16
0x3E	D/A Channel 32 Data		D	16

Table 4-18: I/M/T-Space Address Map

4.4 Correction-Data-Space (1024 Byte)

PCI Base Address: PCI9030 PCI Base Address 4 (Offset 0x20 in PCI Configuration Space).

The correction data values are determined at factory and are stored in this read-only space.

There is an Offset Correction value and a Gain Correction value for each D/A Channel at each voltage range.

16 bit or 32 bit transfer size must be used for accessing the Correction-Data-Space.

The correction data is read only.

See the Programming Hints chapter for data correction formulas.

The correction data is loaded from a serial EEPROM after power-up or PCI reset and is available approx. 8 ms after PCI reset.

The correction factors are stored consecutively in 16 bit values, in order of the D/A Channels 1-32, starting with D/A Channel 1.

Offset to PCI Base Address 4	Description	D/A Channel	Voltage Range
0x000	$Offset_{corr}$	1	0V … +5V
0x002	$Offset_{corr}$	2	0V … +5V
…	…	…	…
0x03E	$Offset_{corr}$	32	0V … +5V
0x040	$Gain_{corr}$	1	0V … +5V
0x042	$Gain_{corr}$	2	0V … +5V
…	…	…	…
0x07E	$Gain_{corr}$	32	0V … +5V
0x080	$Offset_{corr}$	1	0V … +10V
0x082	$Offset_{corr}$	2	0V … +10V
…	…	…	…
0x0BE	$Offset_{corr}$	32	0V … +10V
0x0C0	$Gain_{corr}$	1	0V … +10V
0x0C2	$Gain_{corr}$	2	0V … +10V
…	…	…	…
0x0FE	$Gain_{corr}$	32	0V … +10V

Offset to PCI Base Address 4	Description	D/A Channel	Voltage Range
0x100	$Offset_{corr}$	1	0V … +10.8V
0x102	$Offset_{corr}$	2	0V … +10.8V
…	…	…	…
0x13E	$Offset_{corr}$	32	0V … +10.8V
0x140	$Gain_{corr}$	1	0V … +10.8V
0x142	$Gain_{corr}$	2	0V … +10.8V
…	…	…	…
0x17E	$Gain_{corr}$	32	0V … +10.8V
0x180	$Offset_{corr}$	1	±5V
0x182	$Offset_{corr}$	2	±5V
…	…	…	…
0x1BE	$Offset_{corr}$	32	±5V
0x1C0	$Gain_{corr}$	1	±5V
0x1C2	$Gain_{corr}$	2	±5V
…	…	…	…
0x1FE	$Gain_{corr}$	32	±5V
0x200	$Offset_{corr}$	1	±10V
0x202	$Offset_{corr}$	2	±10V
…	…	…	…
0x23E	$Offset_{corr}$	32	±10V
0x240	$Gain_{corr}$	1	±10V
0x242	$Gain_{corr}$	2	±10V
…	…	…	…
0x27E	$Gain_{corr}$	32	±10V
0x280	$Offset_{corr}$	1	±10.8V
0x282	$Offset_{corr}$	2	±10.8V
…	…	…	…
0x2BE	$Offset_{corr}$	32	±10.8V
0x2C0	$Gain_{corr}$	1	±10.8V
0x2C2	$Gain_{corr}$	2	±10.8V
…	…	…	…
0x2FE	$Gain_{corr}$	32	±10.8V

Table 4-19: Correction-Data-Space Address Map

4.5 F-Space (8192 Byte)

PCI Base Address: PCI9030 PCI Base Address 5 (Offset 0x24 in PCI Configuration Space).

Every channel has its own FIFO.

The 4 FIFOs of a Q-DAC can be activated by selecting F-Mode for the desired Q-DAC and setting the FIFO enable bit in the FIFO X Status/Control Registers. This has the consequence that F-Space has to be used to transfer data and fill the FIFOs.

The FIFOs can be deactivated by selecting one of the other modes in "Q-DAC X Control Register". When the distributed RAM shall be the data source, I/M/T-Space must be used. In addition to that the FIFOs have to be disabled by clearing the FIFO enable bit in the FIFO X Status/Control Registers.

F-Space is a 32 x 128 x 16 bit wide write-only interface to write DAC Data into the next free corresponding memory location in the SRAM (i. e. the FIFO write pointer position). Each of the 32 channels has its own 128 x 16 bit wide address space.

The concept of providing a 128 x 16 bit address space for every channel also allows bursting data into the FIFOs.

The addresses of the F-Space do not represent the actual addresses inside the SRAM, thus it does not matter which address of the 128 x 16 bit address space is used because the internal logic will write the values in order of their appearance into the FIFO and increment the FIFO write pointer.

Example: Any data written to an address between 0x100 and 0x1FE will be written to the address of the FIFO 2 write pointer filling the FIFO of DAC channel 2 which could have any size depending on the distance between FIFO 2 Start Address and FIFO 2 End Address which was set by the user.

DAC channels 1 to 4 belong to Q-DAC 1, DAC channels 5 to 8 belong to Q-DAC 2, and so on.

Offset to PCI Base Address 5	Description	Size (Bit)
0x**00**00	Channel **1** FIFO DAC Data	16
0x**00**02	Channel **1** FIFO DAC Data	16
0x**00**04	Channel **1** FIFO DAC Data	16
…	…	…
0x**00**FE	Channel **1** FIFO DAC Data	16
0x**01**00	Channel **2** FIFO DAC Data	16
0x**01**02	Channel **2** FIFO DAC Data	16
0x**01**04	Channel **2** FIFO DAC Data	16
…	…	…
0x**01**FE	Channel **2** FIFO DAC Data	16

0x**02**00	Channel **3** FIFO DAC Data	16
…	…	…
…	…	…
…	…	…
0x**1F**00	Channel **32** FIFO DAC Data	16
0x**1F**02	Channel **32** FIFO DAC Data	16
0x**1F**04	Channel **32** FIFO DAC Data	16
…	…	…
0x**1F**FE	Channel **32** FIFO DAC Data	16

Table 4-20: F-Space Address Map

To optimize the data throughput, this space allows 32 bit accesses, which targets two subsequent 16 bit words to write two DAC data words at a time and increment the write pointer two times.

The SRAM can be partitioned freely. Each DAC channel has a “FIFO X Start Address Register” and a “FIFO X End Address Register”. These registers can be used to assign a partition of the SRAM to the channel. Since there are no checks of these register values against those of other channels, the partitions of channels can overlap. In this way channels can share and use the same data, e. g. a waveform table.

5 PCI9030 Target Chip

5.1 PCI Configuration Registers (PCR)

5.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	022A 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	118000 00
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFC00
0x1C	PCI Base Address 3 for Local Address Space 1				Y	FFFFFFC0
0x20	PCI Base Address 4 for Local Address Space 2				Y	FFFFFC00
0x24	PCI Base Address 5 for Local Address Space 3				Y	FFFFE000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	s.b. 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt Cap.	PM Cap. ID	N	4801 48 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt Cap.	HS Cap. ID	Y[23:16]	00 00 4C 06
0x4C	VPD Address		VPD Nxt Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Table 5-1 : PCI9030 Header

Subsystem-ID: TPMC554-10R (32 Channels of 16 bit D/A) = 0x000A

TPMC554-11R (16 Channels of 16 bit D/A) = 0x000B

5.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM (M93C56).

The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0xFFFFFC00
0x04	Local Address Space 1 Range	0xFFFFFFC0
0x08	Local Address Space 2 Range	0xFFFFFC00
0x0C	Local Address Space 3 Range	0xFFFFE000
0x10	Expansion ROM Range	0x00000000
0x14	Local Address Space 0 Local Base Address (Remap)	0x00000001
0x18	Local Address Space 1 Local Base Address (Remap)	0x01000001
0x1C	Local Address Space 2 Local Base Address (Remap)	0x02000001
0x20	Local Address Space 3 Local Base Address (Remap)	0x03000001
0x24	Expansion ROM Local Base Address (Remap)	0x00000000
0x28	Local Address Space 0 Bus Region Descriptor	0xD180A0E0
0x2C	Local Address Space 1 Bus Region Descriptor	0xD180A0E0
0x30	Local Address Space 2 Bus Region Descriptor	0xD180A0E0
0x34	Local Address Space 3 Bus Region Descriptor	0x01802022
0x38	Expansion ROM Bus Region Descriptor	0x00000000
0x3C	Chip Select 0 Base Address	0x00000201
0x40	Chip Select 1 Base Address	0x01000021
0x44	Chip Select 2 Base Address	0x02000201
0x48	Chip Select 3 Base Address	0x03001001
0x4C	Interrupt Control/Status	0x0041
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x00780000
0x54	General Purpose I/O Control	0x00392270
0x70	Hidden1 Register for Power Management Data Select	0x00000000
0x74	Hidden 2 Register for Power Management Data Scale	0x00000000

Table 5-2 : PCI9030 Local Configuration Registers

5.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM (M93C56).

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x022A	0x1498	0x0280	0x0000	0x1180	0x0000	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFC00	0x0FFF	0xFFC0
0x30	0x0FFF	0xFC00	0x0FFF	0xE000	0x0000	0x0000	0x0000	0x0001
0x40	0x0100	0x0001	0x0200	0x0001	0x0300	0x0001	0x0000	0x0000
0x50	0xD180	0xA0E0	0xD180	0xA0E0	0xD180	0xA0E0	0x0180	0x2022
0x60	0x0000	0x0000	0x0000	0x0201	0x0100	0x0021	0x0200	0x0201
0x70	0x0300	0x1001	0x0030	0x0041	0x0078	0x0000	0x0039	0x2270
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 5-3 : Configuration EEPROM TPMC554-1x

Subsystem-ID Value (Offset 0x0C): TPMC554-10R 0x000A

TPMC554-11R 0x000B

5.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

6 Functional Description

6.1 Q-DAC Configuration

Each Q-DAC must be configured before usage, right after power-up or reset. See the Q-DAC X Configuration Register for Q-DAC configuration options.

A Q-DAC is being configured by a write to the appropriate Q-DAC X Configuration Register (there is a Q-DAC Configuration Register for each Q-DAC) while the Q-DAC Busy bit in the Global Status Register is clear. Writes to a Q-DAC X Configuration Registers are ignored when the Q-DAC Busy bit is set for this Q-DAC.

When the Q-DAC configuration is started, the Q-DAC Busy bit in the Global Status Register is set and the Q-DAC configuration is transferred to the Q-DAC internal configuration registers via the Q-DAC serial interface.

Check the Q-DAC Busy bits in the Global Status Register to determine when a certain Q-DAC configuration is done.

Steps for Q-DAC configuration:

- Check the Q-DAC Busy bit(s) is (are) clear in the Global Status Register
- Write the Q-DAC configuration setup to the Q-DAC X Configuration Register(s)
- Wait until the Q-DAC Busy bit(s) is (are) clear in the Global Status Register
- Check the Q-DAC X Status Register(s) (e.g. check that all Q-DAC internal DACs are powered-up, etc.)

6.2 Q-DAC Modes

Each Q-DAC (i.e. a group of four D/A channels) can be set to I-Mode, M-Mode, F-Mode or T-Mode operation. The Q-DAC mode is set in the Q-DAC X Control Register.

Each Q-DAC can be set individually which allows a wide field of application.

The Q-DAC mode should be setup soon after Q-DAC configuration and before any other Q-DAC action.

The Q-DAC Busy bit in the Global Status Register shall be checked to be clear before the Q-DAC mode is altered from the default I-Mode.

I-Mode allows an individual update of each of the 32 DAC channels. M-Mode, F-Mode and T-Mode allow a simultaneous update of multiple channels.

In I-Mode, M-Mode and T-Mode the DAC channels receive their data from the 32 x16 bit distributed RAM inside the FPGA which is filled via the I/M/T-Space.

In F-Mode the DACs receive their data from the 2 M x 16 bit external SRAM which is filled via the F-Space. The FIFOs for the channels can be adjusted freely. The FIFO X Start Address Register and FIFO X End Address Register can be used to assign a specific address range of the SRAM to a channel FIFO. F-Mode is used to output signals that are known in advance or to periodically output waveforms.

6.2.1 Summary Table

Mode	Data Source	DAC Load	IRQs
I-Mode	I/M/T-Space	Instantly after a write to the I/M/T-Space	Q-DAC Alert IRQ (IRQAL)
M-Mode		Load Register	Q-DAC Alert IRQ (IRQAL) Q-DAC Load IRQ (IRQLD)
T-Mode		Sequencer Timer	Q-DAC Alert IRQ (IRQAL) Q-DAC Sequencer IRQ (IRQSE)
F-Mode	F-Space	Sequencer Timer	Q-DAC Alert IRQ (IRQAL) Q-DAC FIFO IRQ (IRQFI)

Table 6-1 : Q-DAC Mode Summary Table

The column "Data Source" shows, to what local address space voltage values have to be written, to make sure that these values are converted. "DAC Load" explains what causes the DAC channels to be updated and "IRQs" shows which IRQs can be used in the different modes.

6.2.2 I-Mode (Instant Mode)

A DAC channel is instantly updated when data was written to its storage location in the I/M/T-Space ("Individual DAC Updating").

This mode is ideal when single DAC channels need to be updated on an irregular base.

6.2.2.1 Setting I-Mode

(It is assumed that the Q-DACs are already configured)

Instant Mode is the default Q-DAC mode after power-up or reset.

The following steps may be used if it is desired to set a Q-DAC back to I-Mode:

- Check the Q-DAC Busy bit is clear in the Global Status Register
- Set the Q-DAC Mode to I-Mode in the Q-DAC X Control Register

6.2.2.2 Using I-Mode

Data written to the I/M/T-Space is transferred to the appropriate Q-DAC as soon as possible. The D/A channel analog output is automatically updated when the data has actually been transferred to the Q-DAC.

Each Q-DAC covers four D/A channels and provides a single serial interface.

If any D/A channel data is updated at a rate higher than 100 kHz, data may get lost (depends on what and how many D/A channels are used and whether the Q-DAC status is read; less than four D/A channels per Q-DAC without Q-DAC status read may be updated at a higher rate). The settling of an analog output takes up to 10us (100 kHz).

Max D/A channel data update rate without data loss (without Q-DAC status read):

$$\frac{1}{number\_of\_channels\_used \times 1.4\mu s} \qquad number\_of\_channels\_used = 1 \text{ to } 4$$

Max. D/A channel data update rate without data loss (with Q-DAC status read):

$$\frac{1}{(number\_of\_channels\_used \times 1.4\mu s) + 3.4\mu s} \qquad number\_of\_channels\_used = 1 \text{ to } 4$$

Note, that for fastest D/A channel analog output update rate the used D/A channels should be spread over the various Q-DACs. E.g. when using D/A channels 1, 2, 3 & 4 the D/A channel data must be transferred to Q-DAC 1 one after the other and so the max D/A channel data update rate is 178 kHz. When using D/A channels 1, 5, 9 & 13, the data is transferred to the Q-DACs 1, 2, 3 & 4 at the same time and so the max D/A channel data update rate is 714 kHz. Note also that the analog output settling time for each D/A channel is 10us max (100 kHz).

Software may wait to see the Q-DAC busy bit clear in the Global Status Register before new data is written for a Q-DAC. Up to four D/A channels per Q-DAC could be updated then, using two 32 bit or four 16 bit writes to the appropriate I/M/T-Space locations.

There are no options for a simultaneous load (analog output update) between D/A channels or Q-DACs in this mode. Each D/A channel analog output is updated individually if the D/A channel data has been transferred to the Q-DAC.

6.2.3 M-Mode (Manual Mode)

The data is transferred from the I/M/T-Space to the Q-DACs. When a write command is issued in the Load Register the outputs are updated.

This mode is ideal when groups of DAC channels need to be updated on an irregular base.

6.2.3.1 Setting M-Mode

(It is assumed that the Q-DACs are already configured)

The following steps should be used to set a Q-DAC to M-Mode:

- Check the Q-DAC Busy bit is clear in the Global Status Register
- Set the Q-DAC Mode to M-Mode in the Q-DAC X Control Register (along with the Global Load Mode bit if desired)

6.2.3.2 Using M-Mode

Data written to the I/M/T-Space is transferred to the appropriate Q-DAC as soon as possible, but the Q-DAC analog outputs are not automatically updated when the data transfer is done.

Setting the Load bit in the Load Register logs a request for updating the Q-DAC analog outputs.

In **Standalone M-Mode**, the update of the Q-DAC analog outputs is delayed until all available D/A channel data has been transferred to the Q-DAC. The four D/A channel analog outputs of the Q-DAC are updated simultaneously.

In **Global Load M-Mode**, the update of the Q-DAC analog outputs is delayed until all available D/A channel data has been transferred to all the Q-DACs that are set to Global Load M-Mode. The D/A channel analog outputs of all Q-DACs in Global Load M-Mode are updated simultaneously.

See the Global Load Mode bit in the Q-DAC X Control Register description.

Method A (the load command is set during the data transfer)**:**

- Check the Q-DAC Load bit is clear in the Load Register
- Write new D/A channel data to the I/M/T-Space (i.e. transfer new data to the Q-DAC)
- Set the Q-DAC Load bit in the Load Register (the Q-DAC load is delayed until all available data has been transferred to the Q-DAC)
- Wait until the Q-DAC Load bit is clear in the Load Register (i.e. wait until the Q-DAC analog outputs have been updated)
- Write new D/A channel data to the I/M/T-Space (i.e. transfer new data to the Q-DAC)
- and so on

Method B (data is transferred completely before the load command is set)**:**

- Check the Q-DAC Busy bit is clear in the Global Status Register
- Write Q-DAC data to the I/M/T-Space (i.e. transfer new data to the Q-DAC)
- Wait until the Q-DAC Busy bit is clear in the Global Status Register (i.e. wait until all data has been transferred to the Q-DAC)
- Set the Q-DAC Load bit in the Load Register (quick Q-DAC load response, since the data has already been transferred to the Q-DAC before)
- Wait until the Q-DAC Busy bit is clear in the Global Status Register (i.e. wait until the Q-DAC analog outputs have been updated)
- Write Q-DAC data to the I/M/T-Space (i.e. transfer new data to the Q-DAC)
- and so on

6.2.4 F-Mode (FIFO Mode)

The data is transferred from the FIFOs to the DACs in intervals that are determined by the Q-DAC X Sequencer Timer Register.

This mode is ideal when groups of DAC channels or a single channel need to be updated on a regular base and the data is known in advance or a waveform shall be converted periodically.

6.2.4.1 Preparing for F-Mode

(It is assumed that the Q-DACs are already configured)

- Setup the relevant FIFO X Start Address Register(s)
- Setup the relevant FIFO X End Address Register(s)
- Setup the relevant FIFO X Status/Control Register(s), remember to set the FIFO flush bit
- Set the Q-DAC X Sequencer Timer Register
- Check the Q-DAC Busy bit is clear in the Global Status Register
- Set the Q-DAC Mode to F-Mode in the Q-DAC X Control Register
- If an interrupt shall be initiated if the FIFO(s) is/are about to become empty: enable relevant FIFO interrupt(s) in the FIFO Interrupt Enable Register
- Write the first block(s) of DAC data to the F-Space

6.2.4.2 Starting the Sequencer

If preparing for FIFO Mode is completed, the Sequencer for a Q-DAC is started by setting the Q-DAC Sequencer Start/Stop bit in the Global Control Register.

For a simultaneous D/A channel update between Q-DACs, the Q-DAC timers must be set to the same value and the Q-DAC sequencers must be started simultaneously with the same write access to the Global Control Register.

6.2.4.3 Refilling the FIFO(s)

Polling Mode

- Poll the FIFO (almost) empty flag(s) in the relevant FIFO X Status/Control Register(s) until a bit is set
- Write new DAC data to the appropriate location in the F-Space
- Poll the FIFO (almost) empty flag(s) in the relevant FIFO X Status/Control Register(s) until a bit is set
- and so on

Interrupt Mode

Upon Interrupt: Check the Interrupt Status Register for FIFO interrupt.

Upon FIFO Interrupt:

- Check the FIFO Interrupt Status Register to determine which FIFO is responsible for the interrupt
- optional: Check the FIFO (almost) empty flag(s) in the relevant FIFO X Status/Control Register
- Disable the FIFO Interrupt in the FIFO Interrupt Enable Register
- Write new DAC data to the appropriate location in the F-Space. Either you carry out this task in the Interrupt Service Routine or you start a process outside the ISR to fill the FIFO
- Enable the FIFO Interrupt in the FIFO Interrupt Enable Register
- If the written data was not sufficient to fill the FIFO above the adjustable FIFO limit or another FIFO turned almost empty during the interrupt handling, the interrupt service routine will be called again immediately after returning

6.2.4.4 Waveform generator

To use F-Mode to realize a static waveform generator which periodically outputs a static waveform, simply deactivate the FIFO interrupt in the FIFO Interrupt Enable Register, make sure that the STOP bit in the FIFO X Status/Control Register is not set and ignore the almost empty flag and the empty flag in the FIFO X Status/Control Register. The FIFO will turn "empty" because there are no more unconverted values in it but these values will be converted over and over again.

6.2.4.5 Stopping the Sequencer

The Sequencer is stopped by clearing the Q-DAC Sequencer Start / Stop bit in the Global Control Register.

Any ongoing data transfer to the Q-DAC will continue and terminate normally. Check the Q-DAC Busy bit in the Global Status Register to determine when the Sequencer is actually stopped.

6.2.4.6 Flushing a FIFO

To flush a FIFO (i. e. to reset write pointer and read pointer back to zero position) the according sequencer first has to be stopped. This is done by clearing the Q-DAC Sequencer Start / Stop bit in the Global Control Register. Then the FIFO Flush Bit has to be set in FIFO X Status/Control Register. After that new DAC Data can be written to the F-Space and the sequencer can be restarted.

After changing the FIFO Start Address the FIFO has to be flushed to make sure that the pointers are at the appropriate start position.

6.2.5 T-Mode (Timer / Sequencer Mode)

The data is transferred from the I/M/T-Space to the Q-DACs in intervals that are determined by the Q-DAC X Sequencer Timer Register.

This mode is ideal when groups of DAC channels need to be updated on a regular base.

6.2.5.1 Preparing for T-Mode

(It is assumed that the Q-DACs are already configured)

- Set the Q-DAC X Sequencer Timer Register
- Check the Q-DAC Busy bit is clear in the Global Status Register
- Set the Q-DAC Mode to T-Mode in the Q-DAC X Control Register
- For interrupt controlled sequencer serving only: enable Q-DAC sequencer interrupt in the Q-DAC X Control Register
- Write the Q-DAC data for the first sequence to the I/M/T-Space

6.2.5.2 Starting the Sequencer

If preparing for Timer / Sequencer Mode is completed, the Sequencer for a Q-DAC is started by setting the Q-DAC Sequencer Start/Stop bit in the Global Control Register.

For a simultaneous D/A channel update between Q-DACs, the Q-DAC timers must be set to the same value and the Q-DAC sequencers must be started simultaneously with the same write access to the Global Control Register.

6.2.5.3 Serving the Sequencer

Polling Mode

- Poll the Q-DAC Sequencer Data Request bit in the Global Status Register until the bit is set
- The Q-DAC Sequencer Underflow bit in the Global Status Register may be checked then
- Write new Q-DAC data to the I/M/T-Space
- Clear the Q-DAC Sequencer Data Request bit in the Global Status Register
- Poll the Q-DAC Sequencer Data Request bit in the Global Status Register until the bit is set
- and so on

Interrupt Mode

Upon Interrupt: Check the Interrupt Status Register for Q-DAC sequencer interrupt.

Upon Sequencer Interrupt:

- Check the Q-DAC Sequencer Data Request bit and the Q-DAC Sequencer Underflow bit in the Global Status Register
- Write the Q-DAC data for the next sequence to the appropriate location in the I/M/T-Space (if the data for a D/A channel has not changed, it does not need to be written again).
- Clear the Q-DAC Sequencer Data Request bit in the Global Status Register
- Clear the Q-DAC Sequencer Interrupt bit in the Interrupt Status Register

6.2.5.4 Stopping the Sequencer

The Sequencer is stopped by clearing the Q-DAC Sequencer Start / Stop bit in the Global Control Register.

Any ongoing data transfer to the Q-DAC will continue and terminate normally. Check the Q-DAC Busy bit in the Global Status Register to determine when the Sequencer is actually stopped.

6.3 Q-DAC Status

The Q-DAC devices used provide an internal status register that can be read from the Q-DACs. See the Q-DAC X Status Register for details.

In case of a thermal problem or an overcurrent condition an interrupt is generated if enabled. Thus any errors are quickly detected and reported.

6.3.1 Manual Status Read

Manual Q-DAC status read is supported for I-Mode and M-Mode (not supported for F-Mode and T-Mode).

In I-Mode and M-Mode, setting the Read Status Register bit in the Q-DAC X Control Register logs a request for reading the status of the Q-DAC device.

When the status read request is logged, the Status Valid bit in the Q-DAC X Status Register is cleared. The Status Valid bit in the Q-DAC X Status Register is automatically set again when the Q-DAC status read is done and the Q-DAC X Status Register has been updated.

If there is any Q-DAC data transfer in progress, the Q-DAC status read is delayed until the current Q-DAC data transfer is done. If the Q-DAC is actually waiting for a global simultaneous load in Global Load M-Mode, the Q-DAC status read is delayed until the global simultaneous load is done.

6.3.2 Automatic Status Read

Automatic Q-DAC status read is supported for I-Mode, M-Mode, F-Mode and T-Mode.

Automatic Q-DAC status read is enabled in the Q-DAC X Control Register.

In I-Mode and M-Mode, a request for reading the Q-DAC status is logged every time the Q-DAC Auto Status Timer expires (cyclic timer). See the Auto Status Timer Register for details.

If there is any Q-DAC data transfer in progress, the Q-DAC status read is delayed until the current Q-DAC data transfer is done. If the Q-DAC is actually waiting for a global simultaneous load in Global Load M-Mode, the Q-DAC status read is delayed until the global simultaneous load is done.

In F-Mode and T-Mode, there is one Q-DAC status update per sequence.

7 Programming Hints

7.1 DAC Output Coding

Analog Output	Bipolar Output, Twos Complement Coding			Digital Input
Output Range	±5V	±10V	±10.8V	
Least Significant Bit	152.59µV	305.18µV	329.59µV	
+FSR	4.999847V	9.999695V	10.79967V	0x7FFF
+FSR - 1LSB	4.999695V	9.99939V	10.79934V	0x7FFE
Midscale + 1LSB	152.59µV	305.18µV	329.59µV	0x0001
Midscale	0V	0V	0V	0x0000
Midscale - 1LSB	-152.59µV	-305.18µV	-329.59µV	0xFFFF
-FSR + 1LSB	-4.999847V	-9.999695V	-10.79967V	0x8001
-FSR	-5	-10V	-10.8V	0x8000

Table 7-1 : DAC Output Coding, Bipolar Output Range

Analog Output	Unipolar Output, Straight Binary Coding			Digital Input
Output Range	+5V	+10V	+10.8V	
Least Significant Bit	76.29µV	152.59µV	164.79µV	
FSR	4.999924V	9.999847V	10.799835V	0xFFFF
FSR - 1LSB	4.999847V	9.999695V	10.79967V	0xFFFE
Midscale + 1LSB	2.500076V	5.000153V	5.400165V	0x8001
Midscale	2.5V	5V	5.4V	0x8000
Midscale - 1LSB	2.499924V	4.999847V	5.399835V	0x7FFF
0V + 1LSB	76.29µV	152.59µV	164.79µV	0x0001
0V	0V	0V	0V	0x0000

Table 7-2 : DAC Output Coding, Unipolar Output Range

7.2 DAC Data Correction

There are two errors which affect the DC accuracy of the DACs.

- Offset Error: The difference between the ideal and actual DAC output with zero code as digital input.
- Gain Error: The difference between the ideal gain and the actual gain of the DAC.

The TPMC554 provides correction values for offset and gain for each D/A channel and voltage range.

The data correction values are obtained during factory calibration and are stored in the Correction-Data-Space.

Software may use the correction values in combination with the correction formulas given below to obtain the digital value that has to be written to the DAC to get the desired analog output value.

7.2.1 DAC Correction Formula

7.2.1.1 Unipolar Output Voltage Ranges

The basic formula for correcting the DAC value is:

$$Data = Value \cdot \left(1 - \frac{Gain_{corr}}{262144}\right) - \frac{Offset_{corr}}{4}$$

Value is the digital DAC value that would have been used if the DAC was ideal.

Data is the corrected digital DAC value that must be written to the actual DAC.

$Gain_{corr}$ and $Offset_{corr}$ are the DAC correction values from the Correction-Data-Space. They are stored separately for each of the 32 DAC channels and each output voltage range mode.

The correction values are stored as two's complement 16 bit wide values in the range from –32768 to +32767. For higher accuracy they are scaled to ¼ LSB.

7.2.1.2 Bipolar Output Voltage Ranges

The basic formula for correcting the DAC value is:

$$Data = Value \cdot \left(1 - \frac{Gain_{corr}}{131072}\right) - \frac{Offset_{corr}}{4}$$

Value is the digital DAC value that would have been used if the DAC was ideal.

Data is the corrected digital DAC value that must be written to the actual DAC.

$Gain_{corr}$ and $Offset_{corr}$ are the DAC correction values from the Correction-Data-Space. They are stored separately for each of the 32 DAC channels and each output voltage range mode.

The correction values are stored as two's complement 16 bit wide values in the range from –32768 to +32767. For higher accuracy they are scaled to ¼ LSB.

Floating point arithmetic or scaled integer arithmetic must be used to avoid rounding errors in computing above formulas.

Due to inherent DAC device deviation, the extremes of the full scale range may not be fully reachable, even after calibration.

7.2.2 DAC Correction Values Background

The DAC correction formula is using certain values for offset and gain error correction. These DAC correction values are obtained during factory calibration and are stored in the Correction-Data-Space.

There is one pair of $Offset_{Corr}$ and $Gain_{Corr}$ values for every DAC channel and every output voltage range.

The data correction values are obtained during factory calibration in the following way:

Regression Line

First, the actual DAC D/A function is determined by measuring the analog output voltage at several bit values at a given operating temperature.

Then a straight regression line is calculated that fits best into the actual DAC D/A function.

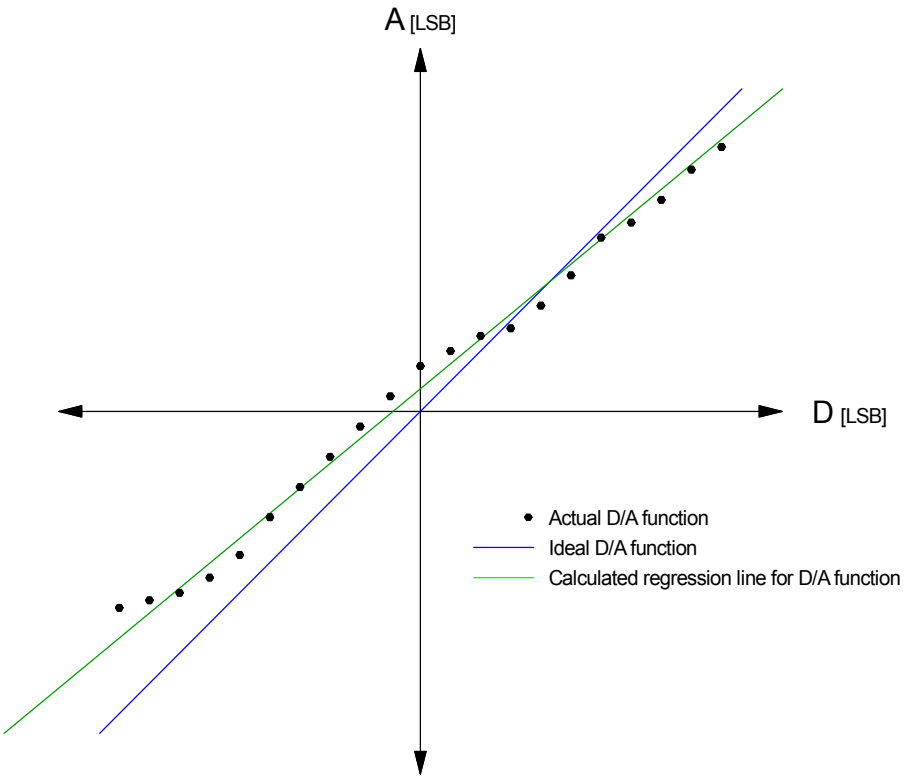

Figure 7-1 : Regression Line

The offset and gain correction values are calculated from the regression line as shown in the following.

Offset Correction Value

The offset correction value stored in the non-volatile memory is the difference between the digital value for ideal D/A function zero output (i.e. 0) and the digital value for regression line zero output.

(Additionally, the difference is weighted by -4)

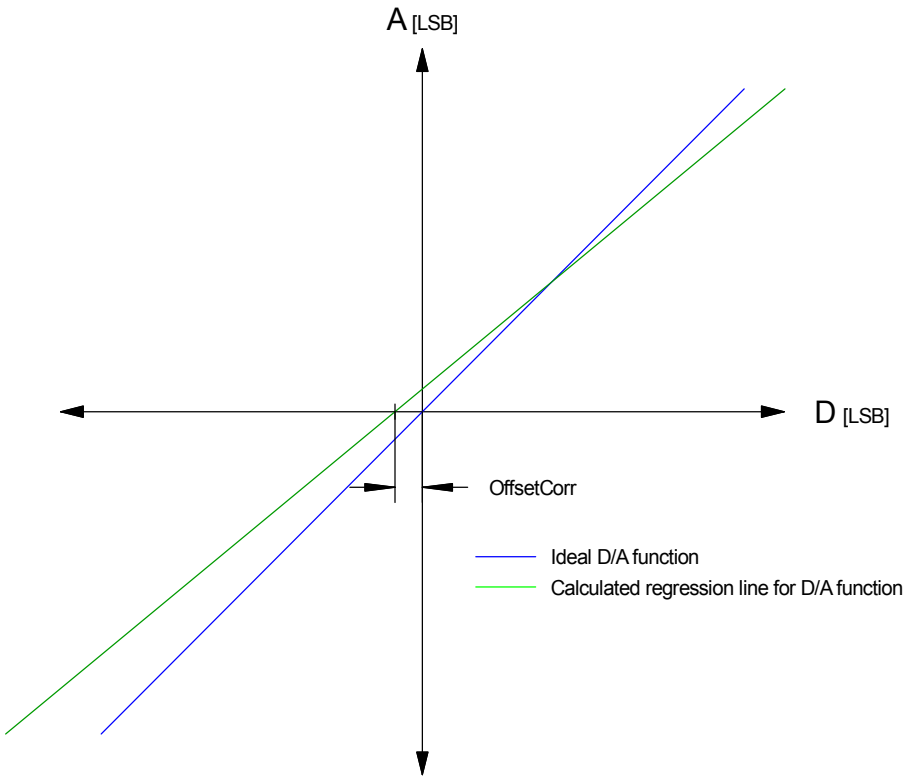

Figure 7-2 : Offset Correction Value

Gain Correction Value

The gain correction value stored in the non-volatile memory is the difference between the digital value for full scale output using the ideal D/A function and the digital value for full scale output using the offset-corrected regression line.

(Additionally, the difference is weighted by 4)

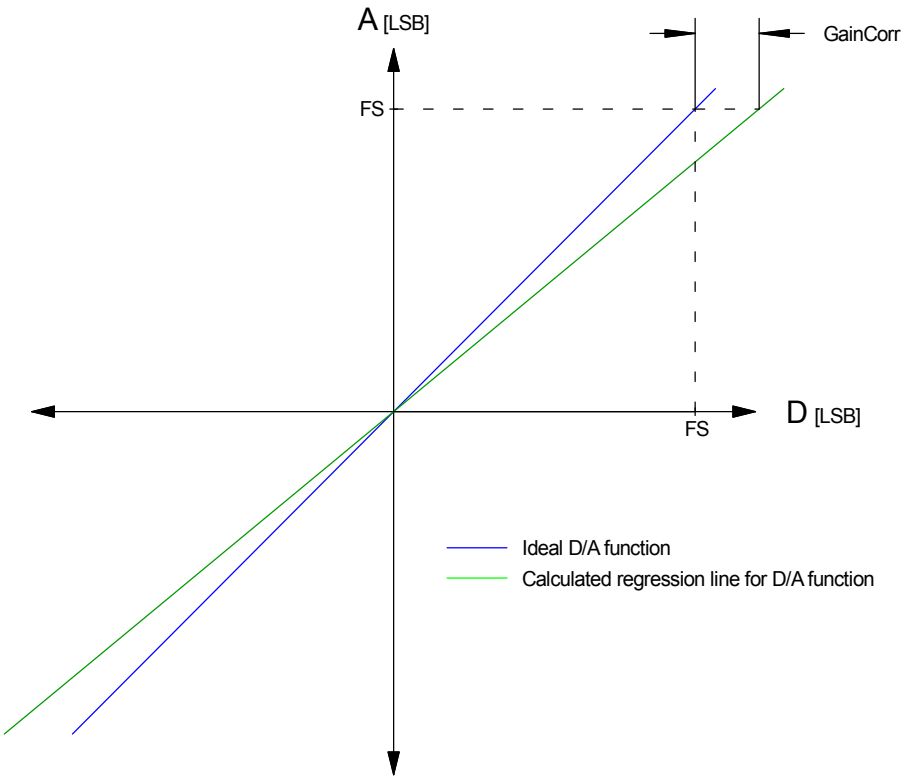

Figure 7-3 : Gain Correction Value

DAC Data Correction

Software may use the DAC correction formulas along with the offset and gain correction values to calculate the corrected digital value that must be written to the DAC for a certain analog result.

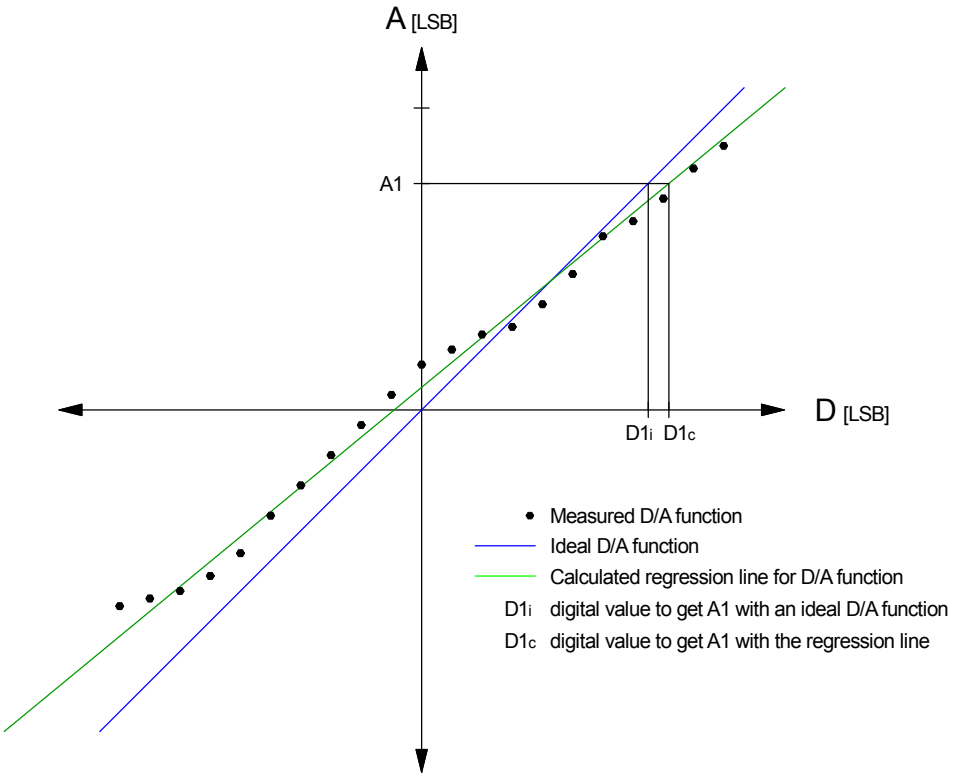

Figure 7-4 : DAC Data Correction

7.3 Interrupts

7.3.1 Interrupt Sources

IRQ	Description
IRQFI	FIFO Interrupt There is one FIFO Interrupt bit representing 1-32 FIFOs depending on the amount of FIFOs with interrupts enabled (see FIFO Interrupt Enable Register). Set when the number of unconverted voltage values in one of the corresponding FIFOs falls below a configurable number or one of the corresponding FIFOs has no more unconverted values at all. The FIFO Interrupt bit is automatically cleared if the FIFOs with interrupts enabled are refilled above the FIFO limits which were set in the corresponding FIFO X Status/Control Registers. See FIFO Interrupt Status Register to determine which channel caused the interrupt.
IRQSE	Q-DAC Sequencer Interrupt There is one Sequencer Interrupt bit for each Q-DAC. Set when the sequencer logic requests a new D/A Channel data set for the next sequence and the interrupt is enabled.
IRQLD	Q-DAC Load Interrupt There is one Load Interrupt bit for each Q-DAC. Set when Q-DAC has actually been loaded in M-Mode (Q-DAC analog outputs just have been updated) and the interrupt is enabled.
IRQAL	Q-DAC Alert Interrupt There is one Alert Interrupt bit for each Q-DAC. Set when the Q-DAC status is read and any of the over-current bits or the thermal alert bit is set and the interrupt is enabled.

Table 7-3 : Interrupt Sources

7.3.2 Interrupt Handling

IRQ	Description	IRQ Enable	IRQ Ack.	Modes
IRQFI	FIFO Interrupt	FIFO Interrupt Enable Register	-	F-Mode
IRQSE	Q-DAC Sequencer Interrupt	Q-DAC X Control Register	Q-DAC Interrupt Status Register	T-Mode
IRQLD	Q-DAC Load Interrupt	Q-DAC X Control Register	Q-DAC Interrupt Status Register	M-Mode
IRQAL	Q-DAC Alert Interrupt	Q-DAC X Control Register	Q-DAC Interrupt Status Register	I-Mode M-Mode F-Mode T-Mode

Table 7-4 : Interrupt Handling

8 Pin Assignment – I/O Connector

8.1 Front I/O Connector

Pin-Count	68
Connector Type	HD68 / SCSI-3
Source & Order Info	AMP 5-787082-7 or compatible

Table 8-1 : I/O Front Connector Type

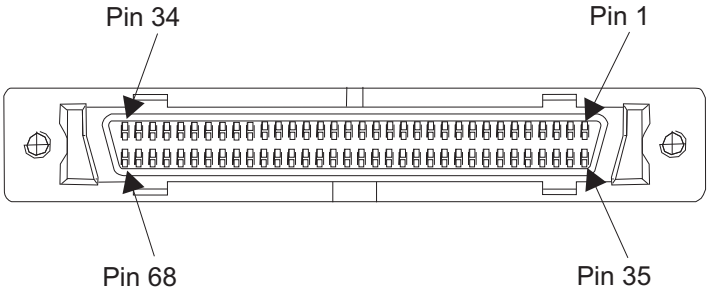

Figure 8-1 : I/O Front Connector View

8.2 Pin Assignment

Each D/A channel should share a twisted cable pair with GND.

Pin	Signal	Pin	Signal
1	D/A Channel 1	35	GND
2	D/A Channel 2	36	GND
3	D/A Channel 3	37	GND
4	D/A Channel 4	38	GND
5	D/A Channel 5	39	GND
6	D/A Channel 6	40	GND
7	D/A Channel 7	41	GND
8	D/A Channel 8	42	GND
9	D/A Channel 9	43	GND
10	D/A Channel 10	44	GND
11	D/A Channel 11	45	GND
12	D/A Channel 12	46	GND
13	D/A Channel 13	47	GND
14	D/A Channel 14	48	GND
15	D/A Channel 15	49	GND
16	D/A Channel 16	50	GND
17	D/A Channel 17	51	GND
18	D/A Channel 18	52	GND
19	D/A Channel 19	53	GND
20	D/A Channel 20	54	GND
21	D/A Channel 21	55	GND
22	D/A Channel 22	56	GND
23	D/A Channel 23	57	GND
24	D/A Channel 24	58	GND
25	D/A Channel 25	59	GND
26	D/A Channel 26	60	GND
27	D/A Channel 27	61	GND
28	D/A Channel 28	62	GND
29	D/A Channel 29	63	GND
30	D/A Channel 30	64	GND
31	D/A Channel 31	65	GND
32	D/A Channel 32	66	GND
33	NC	67	NC
34	NC	68	NC

Table 8-2 : I/O Pin Assignment