The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC600

32 Digital Inputs (24V)

Version 2.0

User Manual

Issue 2.0.0

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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

TPMC600-10R

32 digital inputs front panel I/O

TPMC600-20R

32 digital inputs P14 I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	June 1999
1.1	General Revision	February 2003
1.2	Addition “Technical Specification”	April 2003
1.3	Correction “Debounce Time Register”	September 2003
1.4	New address TEWS LLC	September 2006
1.5	Correction “Technical Specification”	April 2007
1.0.6	New Notation for HW Engineering Documentation Releases	January 2009
1.1.7	Document Update caused by new Hardware Version	January 2009
1.1.8	Updated MTBF Values and Table 4-3 for new Revision	July 2009
1.1.9	General Revision	August 2014
1.1.10	Added Maximum Input Voltage Detail in Table 2-1 Technical Specification	December 2015
2.0.0	User Manual update for TPMC600 V2.0. 16 channel ordering options discarded	June 2021

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1 Product Description

The TPMC600 is a PMC compatible module and has 32 digital inputs galvanically isolated by optocouplers. The individual inputs are separated in groups of 4 sharing a common ground input. These groups are potential free in relation to each other. A high performance input circuit ensures a defined switching point and polarization protection against confusing the pole. All inputs have an electronic debounce circuit with a programmable debounce time.

Two versions of the Module with front or back panel I/O are available. All inputs can generate an interrupt. The signal edge handling is programmable.

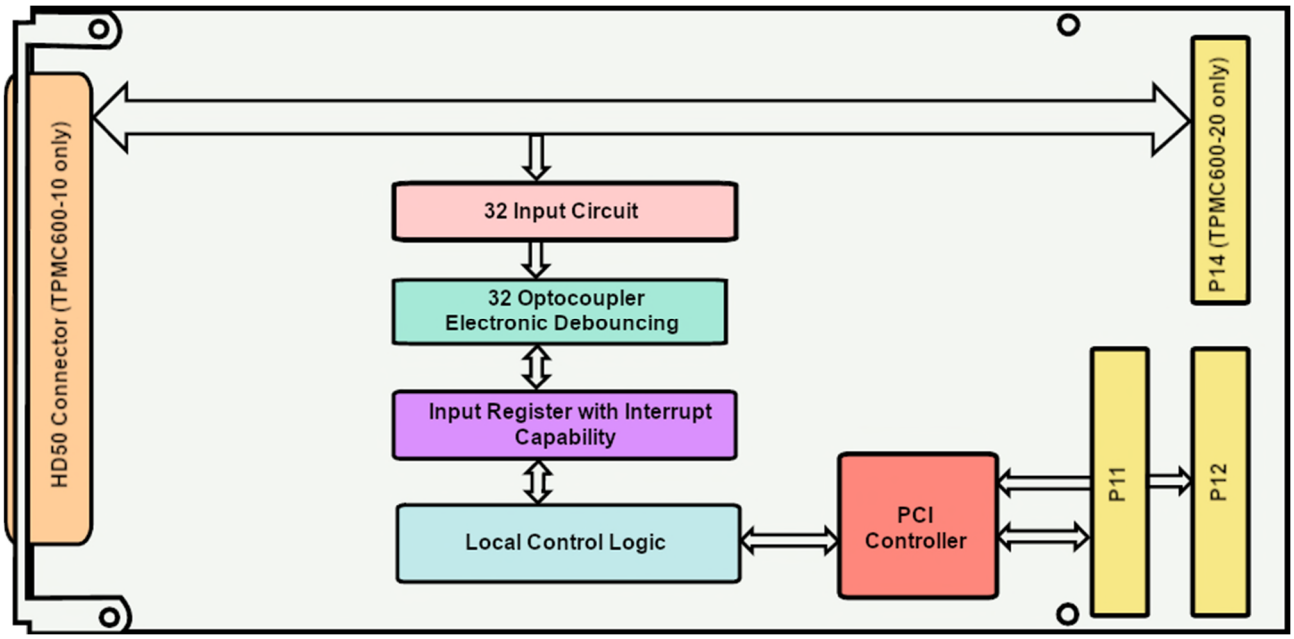

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 3.0 compatible 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	TEWS PCI Interface FPGA	
I/O Interface		
Number of Channels	TPMC600-10R/-20R: 32 digital inputs	
I/O Connector	TPMC600-10R: HD50 connector AMP 787395-5 (Front I/O) TPMC600-20R: PMC P14 I/O MOLEX 71436-2164 (64 pin Mezzanine Connector)	
Input Isolation	Optocoupler for galvanic isolation; also isolated to each other in groups of four inputs	
Input Voltage/Current	24 V DC typical 4.1mA typical @ 24V input voltage	
Input Switching Level	12 V typical, 7.5 V minimum, 14 V maximum	
Input Signal Debouncing	Electronic debouncing (7µs to 440ms in steps of 7µs), common for all input channels, can be disabled	
Input Interrupt	32 input interrupts (trigger on rising, falling or both edges)	
Maximum Input Voltage	28 V DC	
Physical Data		
Power Requirements	33.9mA typical @ +5V DC	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +125°C
MTBF	TPMC600-10R: 427011 h TPMC600-20R: 427880 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	TPMC600-10R: 69.5 g TPMC600-20R: 55.4 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

3.2 Ground for Isolated I/O

I/O Connector's isolated ground signals must be connected to external ground.

4 Addressing

4.1 PCI Configuration Space

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	0258 1498
0x04	Status				Command				Y	0280 0000
0x08	Class Code						Revision ID		N	118000 01
0x0C	not supported		Header Type		not supported		not supported		Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers								Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers								Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0								Y	FFFFFFE0
0x1C	not supported								Y	00000000
0x20	not supported								Y	00000000
0x24	not supported								Y	00000000
0x28	not supported								N	00000000
0x2C	Subsystem ID				Subsystem Vendor ID				N	000A 1498
0x30	not supported								Y	00000000
0x34	Reserved						Cap. Ptr.		N	000000 00
0x38	Reserved								N	00000000
0X3C	MAX_LAT		MIN_GNT		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00
0X40-0XFF	Reserved									00000000

Table 4-1 : PCI Controller Header

4.1.1 PCI Address Space Overview

PCI BAR	PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0x10	MEM	128	32	Little	PCI Controller Register Space
1	0x14	I/O	128	32	Little	
2	0x18	MEM	32	32	Big	Local Register Space

Table 4-2 : PCI Address Space Overview

4.1.1 Serial EEPROM Memory

The serial EEPROM memory contains by default the TEWS PCI Interface FPGA configuration data for compatibility reasons. However, the entire configuration data are stored within and loaded from the internal flash of the PCI target chip.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x0258	0x1498	0x0280	0x0000	0x1180	0x0001	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFFF0	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x01B1	0x7880	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0011	0x0000	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0030	0x0041	0x0078	0x4000	0x0009	0x2000
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-3 : Configuration EEPROM

Subsystem-ID Value (Offset 0x0C): TPMC600-10 0x000A

TPMC600-20 0x0014

4.2 PCI Controller Register Space

4.2.1 PCI Controller Configuration Register Map

The PCI base address for the PCI Controller Configuration Registers is PCI Base Address 0 (PCI Memory Space, Offset 0x10 in the PCI Configuration Space) or PCI Base Address 1 (PCI I/O Space, Offset 0x14 in the PCI Configuration Space).

Do not change hardware dependent bit settings in the PCI Controller Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_FFE0
0x04	Local Address Space 1 Range	0x0000_0000
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Expansion ROM Range	0x0000_0000
0x14	Local Address Space 0 Local Base Address (Remap)	0x0000_0001
0x18	Local Address Space 1 Local Base Address (Remap)	0x0000_0000
0x1C	Local Address Space 2 Local Base Address (Remap)	0x0000_0000
0x20	Local Address Space 3 Local Base Address (Remap)	0x0000_0000
0x24	Expansion ROM Local Base Address (Remap)	0x0000_0000
0x28	Local Address Space 0 Bus Region Descriptor	0x01B1_7880
0x2C	Local Address Space 1 Bus Region Descriptor	0x0000_0000
0x30	Local Address Space 2 Bus Region Descriptor	0x0000_0000
0x34	Local Address Space 3 Bus Region Descriptor	0x0000_0000
0x38	Expansion ROM Bus Region Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0011
0x40	Chip Select 1 Base Address	0x0000_0000
0x44	Chip Select 2 Base Address	0x0000_0000
0x48	Chip Select 3 Base Address	0x0000_0000
0x4C	Interrupt Control/Status	0x0041
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x0078_4000
0x54	General Purpose I/O Control	0x0009_2000
0x70	Hidden1 Register for Power Management Data Select	0x0000_0000
0x74	Hidden 2 Register for Power Management Data Scale	0x0000_0000

Table 4-4 : PCI Controller Configuration Register Map

4.3 Local Register Space

4.3.1 Local Register Map

All local registers of the TPMC600 are accessible in the memory space of the PMC module.

The PCI base address for the Local Registers is PCI Base Address 2 (PCI Memory Space, Offset 0x18 in the PCI Configuration Space).

Offset to PCI Base Address 2	Register Name	Access	Size (Bit)
0x0000	Data Input	R	32
0x0004	Control	R/W	32
0x0008	Rising Edge Interrupt Enable	R/W	32
0x000C	Falling Edge Interrupt Enable	R/W	32
0x0010	Rising Edge Interrupt Status	R/W	32
0x0014	Falling Edge Interrupt Status	R/W	32
0x0018	Debounce Time	R/W	32

Table 4-5 : Local Register Map Overview

After power-on or reset all read/write registers are cleared to '0'.

4.3.1.1 Data Input Register

The Data Input Register is a 32 bit wide read only register that reflects the actual status of the inputs.

Bit	Symbol	Description	Access	Reset Value
31:0		32 bit Input Data Bit 0 represents INPUT 1 and bit 31 represents INPUT32.	R	0x0

Table 4-6 : Data Input Register

4.3.1.2 Control Register

The Control Register is a read/write register.

Bit	Symbol	Description	Access	Reset Value
31:3		Not used and undefined during reads	-	-
2		Debounce Enable bit 1 = enables the debounce function for all 32 inputs 0 = disable	R/W	0x0
1		Not used	-	-
0		Global Interrupt Enable bit 1 = enables interrupt for all 32 inputs 0 = disable The input channels generate interrupts at pin INTA# of the PCI bus	R/W	0x0

Table 4-7 : Control Register

Additional to this Global Interrupt Enable the PCI Interrupt INTA# signal must be enabled in the Interrupt Control/Status Register (INTCSR; 0x4C) of the PCI Controller. Default after PCI Interface FPGA configuration: INTA# is enabled.

4.3.1.3 Rising Edge Interrupt Enable Register

The Rising Edge Interrupt Enable Register is a 32 bit wide read/write register.

Bit	Symbol	Description	Access	Reset Value
31:0		Bit 0 enables the interrupt of input channel 1 for the rising edge, bit 31 enables interrupt of input channel 32. All other bits are equivalent. 1 = Interrupt Rising Edge enabled 0 = Interrupt Rising Edge disabled	R/W	0x0

Table 4-8 : Rising Edge Interrupt Enable Register

4.3.1.4 Falling Edge Interrupt Enable Register

The Falling Edge Interrupt Enable Register is a 32 bit wide read/write register.

Bit	Symbol	Description	Access	Reset Value
31:0		Bit 0 enables the interrupt of input channel 1 for the falling edge, bit 31 enables interrupt of input channel 32. All other bits are equivalent. 1 = Interrupt Falling Edge enabled 0 = Interrupt Falling Edge disabled	R/W	0x0

Table 4-9 : Falling Edge Interrupt Enable Register

4.3.1.5 Rising Edge Interrupt Status Register

The Rising Edge Status Enable Register is a 32 bit wide read/write register.

Bit	Symbol	Description	Access	Reset Value
31:0		Bit 0 reflects the interrupt request status of input 1 for the rising edge, bit 31 reflects the interrupt request status of input 31. All other bits are equivalent. 1 = Interrupt request pending 0 = No interrupt request pending Writing '1' to clear an interrupt request of a specific input.	R/W	0x0

Table 4-10 : Rising Edge Interrupt Status Register

4.3.1.6 Falling Edge Interrupt Status Register

The Falling Edge Status Enable Register is a 32 bit wide read/write register.

Bit	Symbol	Description	Access	Reset Value
31:0		Bit 0 reflects the interrupt request status of input 1 for the falling edge, bit 31 reflects the interrupt request status of input 31. All other bits are equivalent. 1 = Interrupt request pending 0 = No interrupt request pending Writing '1' to clear an interrupt request of a specific input.	R/W	0x0

Table 4-11 : Falling Edge Interrupt Status Register

4.3.1.7 Debounce Time Register

The Debounce Time Register is a word wide read/write register.

Bit	Symbol	Description	Access	Reset Value
31:16		Not used	-	-
15:0		16 bit Debounce Time Value Value 0 sets the debounce time to a minimum of 7µs. This is the default state after power-on or reset. Any debounce time in the range of 7µs to 440ms can be programmed in steps of approx. 7µs. The debounce time is common for all 32 inputs.	R/W	0x0

Table 4-12 : Debounce Time Register

To use the programmable debounce time the Debounce Enable bit of the Control Register must be set to '1'. If this bit is set to '0', no debounce function is active for all inputs.

The following formulas can be used to determine the preload value.

$$t_{db} = (Z+1) \cdot \frac{64}{PCICLK} \cdot 3.5$$

$$Z = \frac{t_{db}}{64 \cdot 3.5} \cdot PCICLK - 1$$

$$t_{\max} = (Z+1) \cdot \frac{64}{PCICLK} \cdot 4$$

$$t_{\min} = (Z+1) \cdot \frac{64}{PCICLK} \cdot 3$$

Figure 4-1: Formula to determine preload value

t_{db}	typical debounce time (s)
Z	preload value
PCICLK	33.33MHz
t_{max}	maximum debounce time (s)
t_{min}	minimum debounce time (s)

Typ. Debounce Time [ms]	Inaccuracy [ms]	Counter dez.	Counter hex.
0.007	± 0.001	0	0000
0.014	± 0.002	1	0001
0.021	± 0.003	2	0002
0.027	± 0.004	3	0003
0.034	± 0.005	4	0004
0.041	± 0.006	5	0005
0.050	± 0.007	6	0006
0.060	± 0.008	7	0007
0.070	± 0.010	9	0009
0.080	± 0.011	10	000A
0.090	± 0.012	12	000C
0.100	± 0.013	13	000D
0.200	± 0.028	28	001C
0.300	± 0042	43	002B
0.400	± 0.057	58	003A

Typ. Debounce Time [ms]	Inaccuracy [ms]	Counter dez.	Counter hex.
0.500	± 0.071	73	0049
0.600	± 0.085	88	0058
0.700	± 0.100	103	0067
0.800	± 0.114	118	0076
0.900	± 0.128	132	0084
1.000	± 0.142	147	0093
2.000	± 0.285	296	0128
3.000	± 0.428	445	01BD
4.000	± 0.571	594	0252
5.000	± 0.714	743	02E7
6.000	± 0.856	891	037B
7.000	± 0.999	1040	0410
8.000	± 1.142	1189	04A5
9.000	± 1.285	1338	053A
10.000	± 1.428	1487	05CF
20.000	± 2.857	2975	0B9F
50.000	± 7.142	7439	1D0F
100.000	± 14.285	14879	3A1F
200.000	± 28.571	29760	7440
250.000	± 35.714	37201	9151
300.000	± 42.856	44641	AE61
350.000	± 50.000	52082	CB72
400.000	± 57.142	59522	E882
440.402	± 62.915	65535	FFFF

Table 4-13: Debounce Time / Examples

5 Configuration Hints

5.1 Local Software Reset

A Local Software Reset signal may be used to reset the on board local logic.

The local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the Miscellaneous Control Register CNTRL (offset 0x50) in the PCI Controller Register Space.

CNTRL[30] PCI Adapter Software Reset:

Value of 1 issues a reset to the local logic. The local logic remains in this reset condition until the PCI Host clears the bit. The contents of the PCI Controller Configuration Registers are not reset.

6 Functional Description

6.1 Digital Inputs

6.1.1 Optical Isolation

The TPMC600 has 32 digital inputs. The standard signal level for these inputs is 24V DC. The switching level of the inputs is between 7.5V and 14V. All inputs are isolated by optocoupler from the computer system and are also isolated against each other in groups of four inputs.

Group	Ground	Input
I1	GND_I1	IN 1 IN 2 IN 3 IN 4
I2	GND_I2	IN 5 IN 6 IN 7 IN 8
I3	GND_I3	IN 9 IN 10 IN 11 IN 12
I4	GND_I4	IN 13 IN 14 IN 15 IN 16
I5	GND_I5	IN 17 IN 18 IN 19 IN 20
I6	GND_I6	IN 21 IN 22 IN 23 IN 24
I7	GND_I7	IN 25 IN 26 IN 27 IN 28
I8	GND_I8	IN 29 IN 30 IN 31 IN 32

Table 6-1 : Isolated Digital Inputs

6.1.2 Debounce Function

A programmable debounce function common for all inputs is implemented on the TPMC600. There is only one debounce time adjustable for all 32 digital inputs.

If the debounce function is enabled, the input pin must be static for the programmed debounce time before the rising or falling edge is recognized as valid. So only after a correct identification the Data Input Register is updated and an interrupt is generated.

The debounce function is disabled after power-on and reset. The debounce time is set to value '0'.

6.1.3 Interrupt Logic

Interrupt generation can be individually programmed for each channel and input transition. To enable the interrupt after a reset, the Global Interrupt Enable bit in the Control Register must be set to the value '1'. Also the respective bit for rising or falling edge in the Rising Edge / Falling Edge Interrupt Enable Register must be set.

The Global Interrupt Enable bit and also all individually interrupt enable bits are disabled after power-on and reset.

7 Programming Hints

7.1 Local Read/Write

The local register design is developed for a long word (32 bit) read/write access. A byte or word access might fail.

8 Installation

8.1 Input Wiring

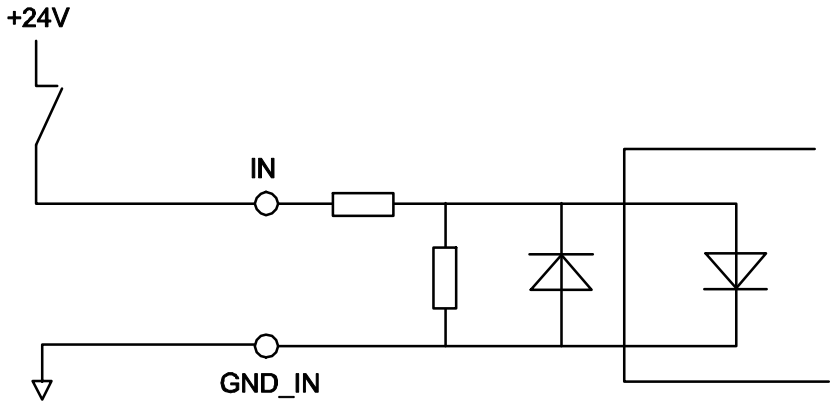

Figure 8-1 : Input Wiring

9 Pin Assignment – I/O Connector

9.1 Front panel I/O

9.1.1 Connector

AMP 787395-5 or compatible

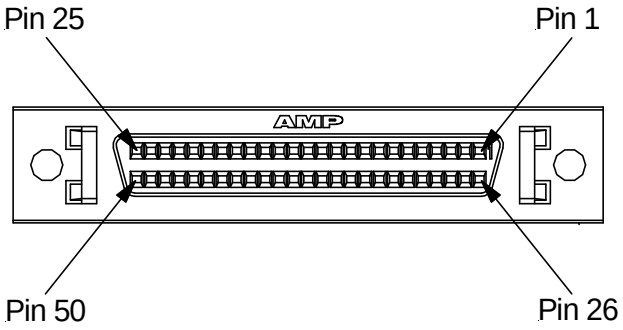

Figure 9-1 : Front Panel I/O Connector Numbering

9.1.2 Front panel I/O Assignment TPMC600-10

The subsequent figure shows the complete assembled pin front panel I/O connector.

Pin	Signal
1	IN 1
2	IN 2
3	IN 3
4	IN 4
5	IN 5
6	IN 6
7	IN 7
8	IN 8
9	IN 9
10	IN 10
11	IN 11
12	IN 12
13	IN 13
14	IN 14
15	IN 15
16	IN 16
17	IN 17
18	IN 18
19	IN 19
20	IN 10
21	IN 21
22	IN 22
23	IN 23
24	IN 24
25	IN 25

Pin	Signal
26	IN 26
27	IN 27
28	IN 28
29	IN 29
30	IN 30
31	IN 31
32	IN 32
33	GND_I1
34	GND_I2
35	GND_I3
36	GND_I4
37	GND_I5
38	GND_I6
39	GND_I7
40	GND_I8
41	NC
42	NC
43	NC
44	NC
45	NC
46	NC
47	NC
48	NC
49	NC
50	NC

Table 9-1 : Pin Assignment Front I/O Connector

9.2 Back panel I/O

9.2.1 Mezzanine Card Connector P14

MOLEX 71436-216 or compatible

9.2.2 Back panel I/O Assignment TPMC600-20

The subsequent figure shows the complete assembled pin back panel I/O connector.

	Signal		Signal
1	IN 1	22	IN 22
2	IN 2	23	IN 23
3	IN 3	24	IN 24
4	IN 4	25	IN 25
5	IN 5	26	IN 26
6	IN 6	27	IN 27
7	IN 7	28	IN 28
8	IN 8	29	IN 29
9	IN 9	30	IN 30
10	IN 10	31	IN 31
11	IN 11	32	IN 32
12	IN 12	33	GND_I1
13	IN 13	34	GND_I2
14	IN 14	35	GND_I3
15	IN 15	36	GND_I4
16	IN 16	37	GND_I5
17	IN 17	38	GND_I6
18	IN 18	39	GND_I7
19	IN 19	40	GND_I8
20	IN 10	41	NC
21	IN 21	42…64	NC

Table 9-2 : Pin Assignment Back I/O Connector