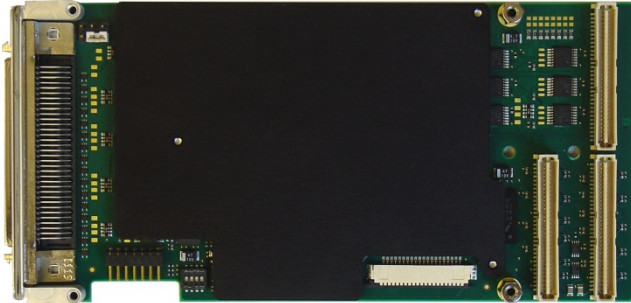


### TPMC632 Reconfigurable FPGA with 64 TTL I/O / 32 Diff. I/O



TPMC632-10R



TPMC632-19R without heat sink

#### Application Information

The TPMC632 is a standard single-width 32 bit PMC module providing a user configurable XC6SLX45T-2 or XC6SLX100T-2 Spartan-6 FPGA. The integrated Spartan-6's PCIe Endpoint Block is connected to a PCIe-to-PCI Bridge which routed to the PMC PCI Interface.

Different variants of the TPMC632 provide ESD-protected TTL lines, ESD-protected differential I/O lines and differential Multipoint-LVDS lines. Also combination of 32 TTL and 16 differential I/O lines are supported.

All lines are individually programmable as input, output or tri-state. The receivers are always enabled, which allows determining the state of each I/O line at any time. This can be used as read back function for lines configured as outputs. Each TTL I/O line has a pull resistor. The pull voltage level is selectable to be either +3.3V, +5V and additionally GND. The differential I/O lines are terminated by 120Ω resistors and the differential Multipoint-LVDS lines are terminated by 100Ω resistors.

The FPGA is connected to a 128 Mbytes, 16 bit wide DDR3 SDRAM. The SDRAM-interface uses a hardwired internal Memory Controller Block of the Spartan-6.

The FPGA is configured by a platform flash or SPI flash. Both configuration flashes are in-system programmable. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using Xilinx "ChipScope").

The TPMC632 provides front panel I/O via a HD68 SCSI-3 type connector and rear panel I/O via P14.

User applications for the TPMC632 with XC6SLX45T-2 FPGA can be developed using the design software ISE WebPACK which can be downloaded free of charge from [www.xilinx.com](http://www.xilinx.com). The larger FPGA densities require a full licensed ISE Design Suite.

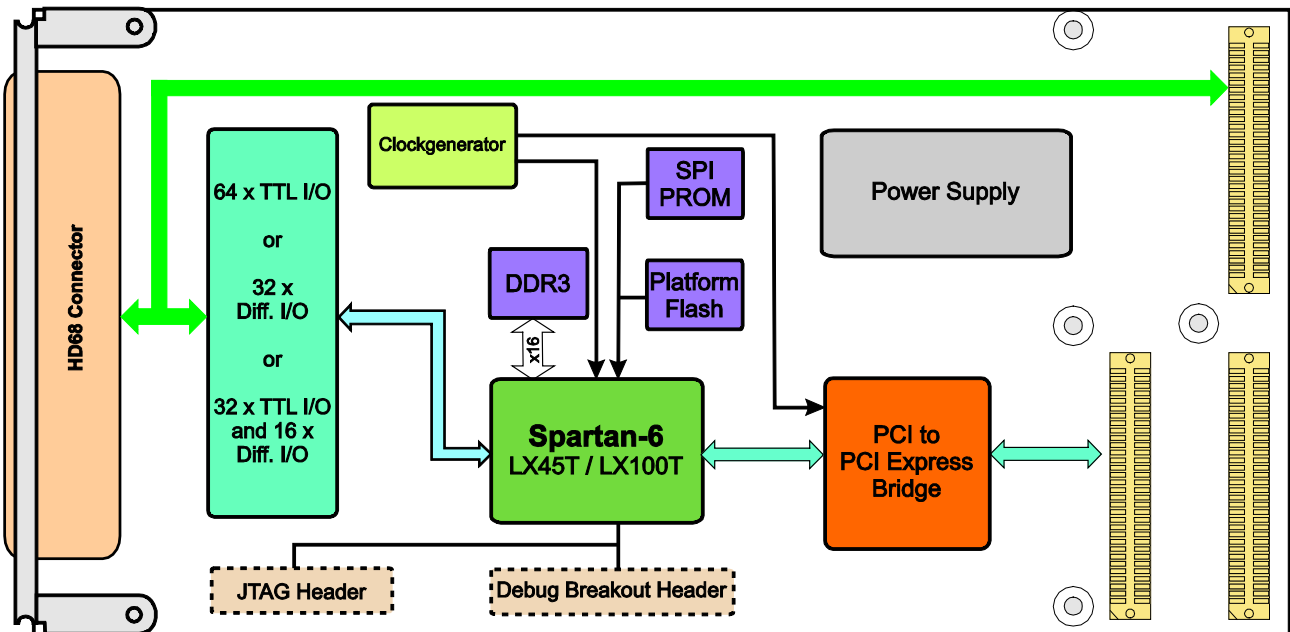
TEWS offers an FPGA Development Kit (TPMC632-FDK) which consists of well documented basic example design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TPMC632. It implements a DMA capable PCIe endpoint with interrupt support, register mapping, DDR3 memory access and basic I/O. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream.

Please note: The basic example design requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (downloadable from [www.xilinx.com](http://www.xilinx.com), a 30 day evaluation license is available).

Software Support (TDRV015-SW-xx) for different operating systems is available.

### Technical Information

- Standard single-width 32 bit PMC module conforming to IEEE P1386.1
- PCI 2.1 compliant interface
- 3.3V and 5V PCI Signaling Voltage
- Board size: 149 mm x 74 mm
- TPMC632-1x: Xilinx XC6SLX45T-2 Spartan6 FPGA configured by serial Flash XCF16PFS
- TPMC632-2x: Xilinx XC6SLX100T-2 Spartan6 FPGA configured by serial Flash XCF32PFS
- Flash device is programmable via JTAG and in-system programmable
- FPGA clock options:
  - Local clock generator as source for the FPGA internal PLL
- 1 DDR3 SDRAM bank, 64M x 16 (128 MB)
- 32 Mbit SPI-EEPROM for User Data or FPGA configuration
- I/O lines
  - 64 TTL I/O, or 32 differential I/O or 32 TTL I/O and 16 differential I/O
  - TTL signaling voltage (maximum current: +/- 32mA), EIA-422/-485 signaling level or M-LVDS Standard (TIA/EIA-899)
  - direction individually programmable
- I/O access:
  - 64 I/O lines on HD68 front connector, parallel to up to 64 I/O lines on rear connector P14
- Operating temperature -40°C to +85°C



### Order Information

#### RoHS Compliant

<b>TPMC632-10R</b>	Spartan-6 FPGA XC6SLX45T-2, 128 MB DDR3, 32bit 33/66 MHz PCI, HD68 and P14 I/O, 64 TTL I/O
<b>TPMC632-11R</b>	Spartan-6 FPGA XC6SLX45T-2, 128 MB DDR3, 32bit 33/66 MHz PCI, HD68 and P14 I/O, 32 RS422
<b>TPMC632-12R</b>	Spartan-6 FPGA XC6SLX45T-2, 128 MB DDR3, 32bit 33/66 MHz PCI, HD68 and P14 I/O, 32 TTL I/O, 16 RS422
<b>TPMC632-13R</b>	Spartan-6 FPGA XC6SLX45T-2, 128 MB DDR3, 32bit 33/66 MHz PCI, HD68 and P14 I/O, 32 M-LVDS
<b>TPMC632-14R</b>	Spartan-6 FPGA XC6SLX45T-2, 128 MB DDR3, 32bit 33/66 MHz PCI, HD68 and P14 I/O, 32 TTL I/O, 16 M-LVDS
<b>TPMC632-20R</b>	Spartan-6 FPGA XC6SLX100T-2, 128 MB DDR3, 32bit 33/66 MHz PCI, HD68 and P14 I/O, 64 TTL I/O
<b>TPMC632-21R</b>	Spartan-6 FPGA XC6SLX100T-2, 128 MB DDR3, 32bit 33/66 MHz PCI, HD68 and P14 I/O, 32 RS422
<b>TPMC632-22R</b>	Spartan-6 FPGA XC6SLX100T-2, 128 MB DDR3, 32bit 33/66 MHz PCI, HD68 and P14 I/O, 32 TTL I/O, 16 RS422
<b>TPMC632-23R</b>	Spartan-6 FPGA XC6SLX100T-2, 128 MB DDR3, 32bit 33/66 MHz PCI, HD68 and P14 I/O, 32 M-LVDS
<b>TPMC632-24R</b>	Spartan-6 FPGA XC6SLX100T-2, 128 MB DDR3, 32bit 33/66 MHz PCI, HD68 and P14 I/O, 32 TTL I/O, 16 M-LVDS

For the availability of non-RoHS compliant (lead solder) products please contact TEWS.

#### Documentation

<b>TPMC632-DOC</b>	User Manual
<b>TPMC632-FDK</b>	FPGA Development Kit for TPMC632, includes TPLD005 Example Design

#### Accessories

<b>TA900-10R</b>	Program and Debug Box, USB, JTAG, 20pin FPC connector, including USB A-USB B and FPC Flexcable
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#### Software

<b>TDRV015-SW-25</b>	Integrity Software Support (for the example design TPLD005 of the TPMC632-FDK)
<b>TDRV015-SW-42</b>	VxWorks Software Support (Legacy and VxBus-Enabled) Software Support (for the example design TPLD005 of the TPMC632-FDK)
<b>TDRV015-SW-65</b>	Windows Software Support (for the example design TPLD005 of the TPMC632-FDK)
<b>TDRV015-SW-82</b>	Linux Software Support (for the example design TPLD005 of the TPMC632-FDK)
<b>TDRV015-SW-95</b>	QNX Software Support (for the example design TPLD005 of the TPMC632-FDK)

For other operating systems please contact TEWS.

#### Related Products

<b>TA304</b>	Cable Kit for Modules with HD68 Connector
<b>TPIM003</b>	PIM I/O Module, HD68 connector, special pin assignment