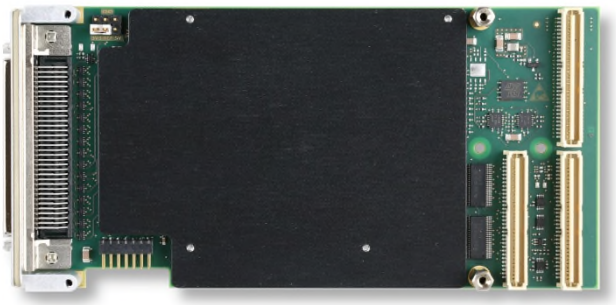
TPMC644 Re-Configurable FPGA with 64 TTL I/O / 32 Diff. I/O



TPMC644-10R

TPMC644-10R without Heatsink

Application Information

The TPMC644 is a standard single-width PCI Mezzanine Card (PMC) providing a user configurable AMD XC7S50 Spartan-7 FPGA, up to 64 front I/O lines and 32 rear I/O lines.

The TPMC644-10R provides 64 ESD-protected TTL (LVTTL) I/O lines using on-board TTL (LVTTL) buffers. The TPMC644-11R provides 32 differential I/O lines using ESD-protected EIA-422 / EIA-485 compatible line transceivers. The TPMC644-12R provides a mix of 16 differential EIA-422 / EIA-485 I/O lines and 32 TTL (LVTTL) I/O lines. The TPMC644-13R provides 32 differential I/O lines using M-LVDS line transceivers. The TPMC644-14R provides a mix of 16 differential M-LVDS I/O lines and 32 TTL (LVTTL) I/O lines.

Each front I/O line is individually programmable as input or output. Each TTL (LVTTL) I/O line has an on-board pull resistor to a common/shared reference. The pull resistor reference is configurable by an on-board jumper to either 3.3V, 5V or GND. The differential front I/O lines have on-board termination resistors.

Additionally the TPMC644 provides 32 + 2 direct FPGA I/O lines on the P14 Rear I/O connector. The User FPGA I/O bank supply for the rear I/O signals is programmable to either 3.3V (for LVTTL/LVCMOS support) or 2.5V (for LVDS support).

The User FPGA is auto-configurable by an on-board SPI Flash. Both the User FPGA (volatile) and the SPI Flash (none-volatile) for User FPGA configuration are in-system programmable via the PCI bus. An on-board JTAG header provides access to the User FPGA JTAG port.

PCI configuration space parameters are configurable by an on-board serial EEPROM.

Software Support (TDRV018-SW-xx) for different operating systems is available.

Technical Information

- Form Factor: Standard single-width 32 bit PMC module conforming to IEEE 1386/1386.1
- PCI 3.0 (33 MHz) compliant interface
- 3.3V PCI signaling with 5V signal tolerance
- AMD XC7S50 7-Series User FPGA accessible on Local Address/Data Bus, PCI to Local Bus Interface handled by on-board PCI/LOC Bridge
- Programmable EEPROM for User PCI Configuration Space Parameters
- In-System-Programmable SPI Flash (non-volatile) for User FPGA Configuration
- User FPGA (volatile) directly In-System-Programmable via PCI bus
- 64 transceiver I/O lines accessible on HD68 front connector
- Single-Ended (64 SE), Differential (32 DF) and Mixed (16 DF + 32 SE) Front I/O transceiver options
- 32 (+ 2) direct FPGA I/O lines additionally accessible on P14 Rear I/O connector
- Rear I/O Bank Supply programmable for LVTTL or LVDS support
- Operating temperature -40 °C to +85 °C

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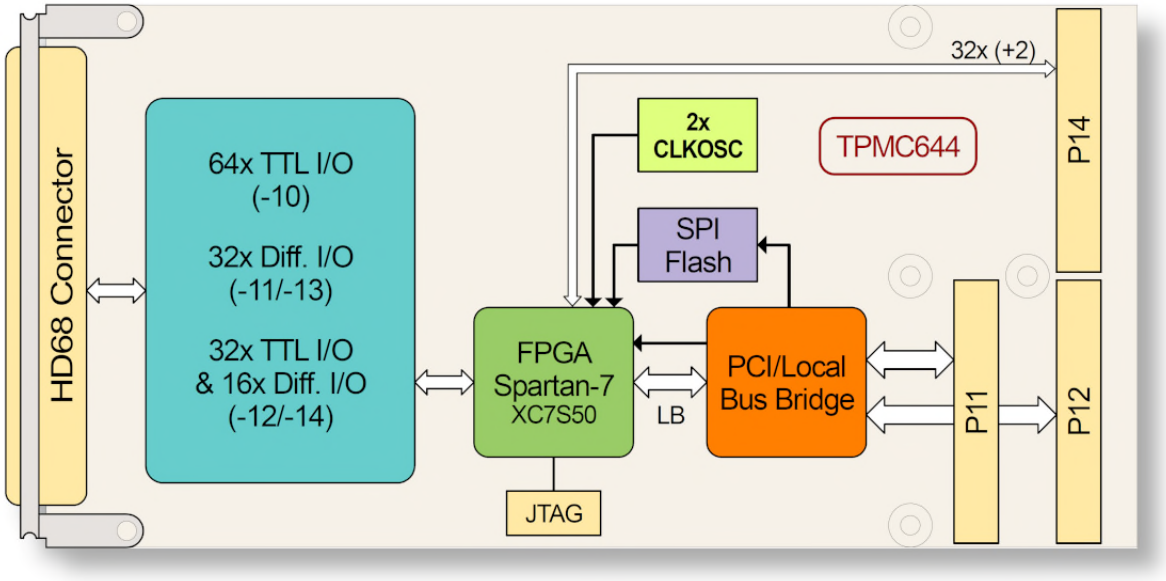

Block Diagram

Order Information

RoHS Compliant

TPMC644-10R	Re-Configurable FPGA with 64 TTL (LVTTL) I/O
TPMC644-11R	Re-Configurable FPGA with 32 Differential EIA-422 / EIA-485 I/O
TPMC644-12R	Re-Configurable FPGA with 16 Differential EIA-422 / EIA-485 I/O and 32 TTL (LVTTL) I/O
TPMC644-13R	Re-Configurable FPGA with 32 Differential M-LVDS I/O
TPMC644-14R	Re-Configurable FPGA with 16 Differential M-LVDS I/O and 32 TTL (LVTTL) I/O

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Software

TDRV018-SW-25	Integrity Software Support
TDRV018-SW-42	VxWorks Software Support
TDRV018-SW-65	Windows Software Support
TDRV018-SW-82	Linux Software Support
TDRV018-SW-95	QNX Software Support

For other operating systems please contact TEWS.

Related Products

TA304	Cable Kit for Modules with HD68 SCSI-3 type connector
TPIM003	PIM I/O Module with HD68 SCSI-3 type connector

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