The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC681

64 Digital Inputs/Outputs

(Bit I/O)

Version 2.0

User Manual

Issue 2.0.0

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TEWS TECHNOLOGIES GmbH

Am Bahnhof 7 25469 Halstenbek, Germany

Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19

e-mail: info@tews.com www.tews.com

TPMC681-10R

64 Digital Inputs/Outputs

HD68 front panel connector

P14 Back I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	June 2005
1.1	Note added for Interrupt Status Register 0/1	December 2005
1.2	TTL Transceivers changed	March 2006
1.3	New address TEWS LLC	September 2006
1.0.4	User Manual Notation changed	November 2008
2.0.0	Document Update due to new Hardware Version	February 2014

Table of Contents

List of Figures

List of Tables

1 Product Description

The TPMC681 is a standard single-width 32 bit PMC module offering 64 ESD-protected TTL I/O lines.

Each I/O line is individually programmable as input, output or tri-state.

The receivers are always enabled, which allows determining the state of each I/O line at any time. This can be used as read back function for lines configured as outputs.

Each I/O line has a pull-up resistor. The pull-up voltage is selectable to be either +3.3V or +5V.

Each input can generate an interrupt. Signal edge handling is programmable to interrupt on rising and/or falling edge of an input signal. Interrupts can be enabled and disabled for each I/O line. For interrupt source detection the status of each bit can be read from interrupt status registers.

The TPMC681 provides front panel I/O via a HD68 SCSI-3 type connector and rear panel I/O via P14.

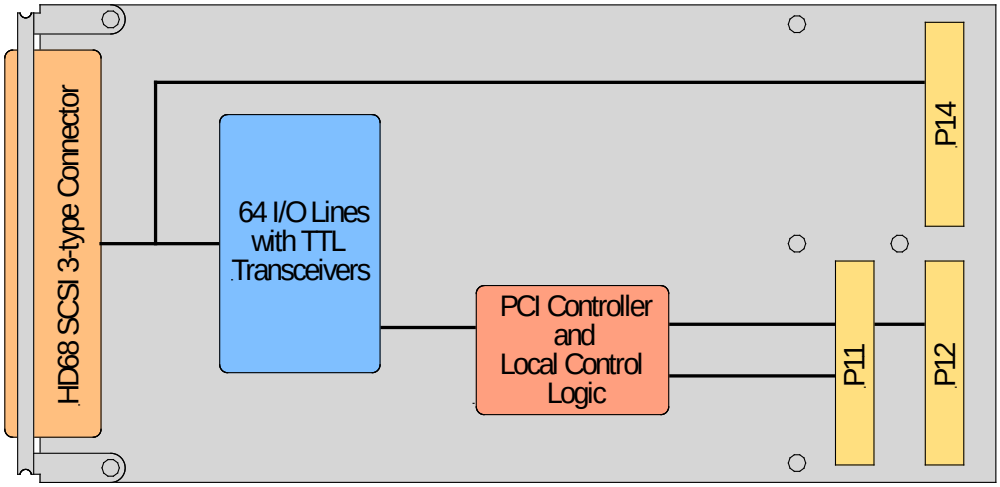


Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size	
Electrical Interface	PCI Rev. 3.0 compatible 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip and Local Control Logic	MachXO2 LCMXO2-4000HC-5BG332I (Lattice)	
TTL Line Transceivers	74LVT126	
I/O Interface		
Number of Channels	64 Bit I/O TTL signaling voltage level (maximum current: +/- 24 mA)	
I/O Connector	Front I/O HD68 SCSI-3 type Connector (TE 5787082-7) PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	45 mA typical (no load) @ +5V DC	
Temperature Range	Operating Storage	-40°C to + 85°C -40°C to +125°C
MTBF	597000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	70 g	

Table 2-1 : Technical Specification

3 Address Map

3.1 PCI Configuration Space

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				Initial Values (Hex Values)
	31 24	23 16	15 8	7 0	
0x00	Device ID 0x02A9 (TPMC681)		Vendor ID 0x1498 (TEWS Technologies)		02A9 1498
0x04	Status		Command		0480 0000
0x08	Class Code			Revision ID	118000 00
0x0C	not supported	Header Type	PCI Latency Timer	Cache Line Size	00 00 00 00
0x10	Base Address Register 0 (BAR0)				FFFFFF80
0x14	Base Address Register 1 (BAR1)				FFFFFF81
0x18	Base Address Register 2 (BAR2)				FFFFFF00
0x1C	not supported				00000000
0x20	not supported				00000000
0x24	not supported				00000000
0x28	CardBus CIS Pointer				00000000
0x2C	Subsystem ID		Subsystem Vendor ID 0x1498 (TEWS Technologies)		000A 1498
0x30	not supported				00000000
0x34	Reserved			Cap. Ptr.	000000 00
0x38	Reserved				00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	00 00 01 00
0x40-0xFF	Reserved				00000000

Table 3-1 : PCI Configuration Space Header

3.1.1 Base Address Register Configuration

For backward compatibility a subset of PCI9030 registers have been implemented within the PLD besides the Local Control Logic. This subset contains all registers that are used by the standard TEWS module driver.

Base Address Register (BAR)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	MEM	128	32	LIT	Configuration Register Space
1	IO	128	32	LIT	
2	MEM	256	32	BIG/LIT	Functional Register Space

Table 3-2 : Base Address Register Configuration

3.1 Configuration Register Space

Offset to PCI Base Address 0/1	Register Name		Size (Bit)
	31 : 16	15 : 0	
0x0 : 0x27	-		-
0x28	Local Address Space 0 Bus Region Descriptor (LAS0BRD)		32
0x2C : 0x4B	-		-
0x4C	-	Interrupt Control/Status (INTCSR)	32
0x50	Serial EEPROM and Initialization Control (CNTRL)		32
0x54	General Purpose I/O Control (GPIOC)		32
0x58 : 0x7B	-		-
0x7C	Configuration Space Revision Register (CREVREG)		32

Table 3-3 : Configuration Register Space

3.2 Functional Register Space

Offset to PCI Base Address 2	Register Name	Size (Bit)
0x00	Output Register 0 (OUT_REG0)	32
0x04	Output Register 1 (OUT_REG1)	32
0x08	Input Register 0 (IN_REG0)	32
0x0C	Input Register 1 (IN_REG1)	32
0x10	Output Enable Register 0 (OE_REG0)	32
0x14	Output Enable Register 1 (OE_REG1)	32
0x18	Interrupt Status Register (ISR0)	32
0x1C	Interrupt Status Register (ISR1)	32
0x20	Positive Edge Interrupt Enable Register (PIER0)	32
0x24	Positive Edge Interrupt Enable Register (PIER1)	32
0x28	Negative Edge Interrupt Enable Register (NIER0)	32
0x2C	Negative Edge Interrupt Enable Register (NIER1)	32
0x30 : 0x7B	-	-
0xFC	Functional Register Space Revision Register (FREVREG)	32

Table 3-4 : Functional Register Space

4 Register Description

4.1 Configuration Register Space

4.1.1 Functional Register Space Descriptor (LAS0BRD)

Bit	Symbol	Description	Access	Reset Value
31 : 25	-	Reserved	R	0
24	ASBYTE_ORDER	Address Space Byte Ordering 1 : activate Big Endian 0 : activate Little Endian	R/W	1
23 : 0	-	Reserved	R	0

Table 4-1 : Functional Register Space Descriptor (LAS0BRD)

4.1.2 Interrupt Control/Status (INTCSR)

Bit	Symbol	Description	Access	Reset Value
15 : 8	-	Reserved	R	0
7	SW_INT	Software Interrupt 1 : generates PCI Interrupt (INTA# output asserted) if PCI Interrupt Enable bit is set (bit [6]=1) 0 : clears PCI Interrupt	R/W	0
6	PCI_INT_EN	PCI Interrupt Enable 1 : enables PCI interrupt 0 : disables PCI interrupt	R/W	1
5 : 3	-	Reserved	R	0
2	LINT_STAT	Local Interrupt (LINTi1) Status 1 : indicates interrupt active 0 : indicates Interrupt not active	R	0
1	LINT_POL	Local Interrupt (LINTi1) Polarity 1 : adjusts active high polarity 0 : adjusts active low polarity	R/W	0
0	LINT_EN	Local Interrupt (LINTi1) Enable 1 : enables Local Control Logic interrupts 0 : disables Local Control Logic interrupts	R/W	1

Table 4-2 : Interrupt Control/Status (INTCSR)

4.1.3 Serial EEPROM and Initialization Control (CNTRL)

Bit	Symbol	Description	Access	Reset Value
31	-	Reserved	R	0
30	SWRST	Software Reset 1 : resets the Functional Register Space. Reset stays active until it is cleared 0 : clears the Functional Register Space reset	R/W	0
29	-	Reserved	R	0
28	EEPRSNT	Serial EEPROM Present 1 : indicates serial EEPROM is present 0 : indicates no serial EEPROM is present	R	1
27	EEDO	Serial EEPROM Data Out Bit This bit is the data output of the serial EEPROM	R	-
26	EEDI	Serial EEPROM Data In Bit This bit is the data input of the serial EEPROM	R/W	0
25	EECS	Serial EEPROM Chip Select 1 : asserts serial EEPROM chip select 0 : de-asserts serial EEPROM chip select	R/W	0
24	EESK	Serial EEPROM Clock Toggling this bit generates a serial EEPROM clock	R/W	0
23 : 0	-	Reserved	R	0

Table 4-3 : Serial EEPROM and Initialization Control (CNTRL)

4.1.4 General Purpose I/O Control (GPIOC)

Bit	Symbol	Description	Access	Reset Value
31 : 12	-	Reserved	R	0
11	GPIO3_DATA	GPIO3 Data Output Function: Stimulates corresponding pin Input Function: Provides state of corresponding pin	R/W	0
10	GPIO3_DDR	GPIO3 Data Direction 1 : activates output function 0 : activates input function	R/W	0
9	-	Reserved	R	0
8	GPIO2_DATA	GPIO2 Data Output Function: Stimulates corresponding pin Input Function: Provides state of corresponding pin	R/W	0
7	GPIO2_DDR	GPIO2 Data Direction 1 : activates output function 0 : activates input function	R/W	0
6	-	Reserved	R	0
5	GPIO1_DATA	GPIO1 Data Internally connected to 1 (backward compatibility). Formerly linked to PROGRAM# pin.	R/W	1
4	GPIO1_DDR	GPIO1 Data Direction GPIO1 represents PROGRAM# state. Hence the direction configuration is not implemented (input only).	R	0
3	-	Reserved	R	0
2	GPIO0_DATA	GPIO0 Data Internally connected to 1 (backward compatibility). Formerly linked to DONE pin.	R	1
1	GPIO0_DDR	GPIO0 Data Direction GPIO0 represents DONE state. Hence the direction configuration is not implemented (input only).	R	0
0	-	Reserved	R	0

Table 4-4 : General Purpose I/O Control (GPIOC)

The GP I/O functionality has been implemented for backward-compatibility reason.

4.1.5 Configuration Space Revision Register (CREVREG)

Bit	Symbol	Description	Access	Reset Value
31 : 0	CREVREG	Firmware Version Register for Configuration Space	R	*)

Table 4-5 : Revision Register (CREVREG)

*) Depends on Firmware Version

4.2 Functional Register Space

4.2.1 Output Register 0 (OUT_REG0)

Bit	Symbol	Description	Access	Reset Value
31	OUT_REG_BIT_31	Output Port bit 31 : 0 Data	R/W	0
30	OUT_REG_BIT_30			
29	OUT_REG_BIT_29			
28	OUT_REG_BIT_28			
27	OUT_REG_BIT_27			
26	OUT_REG_BIT_26			
25	OUT_REG_BIT_25			
24	OUT_REG_BIT_24			
23	OUT_REG_BIT_23			
22	OUT_REG_BIT_22			
21	OUT_REG_BIT_21			
20	OUT_REG_BIT_20			
19	OUT_REG_BIT_19			
18	OUT_REG_BIT_18			
17	OUT_REG_BIT_17			
16	OUT_REG_BIT_16			
15	OUT_REG_BIT_15			
14	OUT_REG_BIT_14			
13	OUT_REG_BIT_13			
12	OUT_REG_BIT_12			
11	OUT_REG_BIT_11			
10	OUT_REG_BIT_10			
9	OUT_REG_BIT_9			
8	OUT_REG_BIT_8			
7	OUT_REG_BIT_7			
6	OUT_REG_BIT_6			
5	OUT_REG_BIT_5			
4	OUT_REG_BIT_4			
3	OUT_REG_BIT_3			
2	OUT_REG_BIT_2			
1	OUT_REG_BIT_1			
0	OUT_REG_BIT_0			

Table 4-6 : Output Register 0 (OUT_REG0)

The output lines are switched in 8 groups of 8 signals with a delay of about 15ns between 2 groups (if PCI clock is 33 MHz). This switching is done after every write access to Output or Output Enable Register.

4.2.2 Output Register 1 (OUT_REG1)

Bit	Symbol	Description	Access	Reset Value
63	OUT_REG_BIT_63	Output Port bit 63 : 32 Data	R/W	0
62	OUT_REG_BIT_62			
61	OUT_REG_BIT_61			
60	OUT_REG_BIT_60			
59	OUT_REG_BIT_59			
58	OUT_REG_BIT_58			
57	OUT_REG_BIT_57			
56	OUT_REG_BIT_56			
55	OUT_REG_BIT_55			
54	OUT_REG_BIT_54			
53	OUT_REG_BIT_53			
52	OUT_REG_BIT_52			
51	OUT_REG_BIT_51			
50	OUT_REG_BIT_50			
49	OUT_REG_BIT_49			
48	OUT_REG_BIT_48			
47	OUT_REG_BIT_47			
46	OUT_REG_BIT_46			
45	OUT_REG_BIT_45			
44	OUT_REG_BIT_44			
43	OUT_REG_BIT_43			
42	OUT_REG_BIT_42			
41	OUT_REG_BIT_41			
40	OUT_REG_BIT_40			
39	OUT_REG_BIT_39			
38	OUT_REG_BIT_38			
37	OUT_REG_BIT_37			
36	OUT_REG_BIT_36			
35	OUT_REG_BIT_35			
34	OUT_REG_BIT_34			
33	OUT_REG_BIT_33			
32	OUT_REG_BIT_32			

Table 4-7 : Output Register 1 (OUT_REG1)

The output lines are switched in 8 groups of 8 signals with a delay of about 15ns between 2 groups (if PCI clock is 33 MHz). This switching is done after every write access to Output or Output Enable Register.

4.2.3 Input Register 0 (IN_REG0)

Read directly from the I/O lines 31 to 0.

Bit	Symbol	Description	Access	Reset Value
31	IN_REG_BIT_31	Input Port bit 31 : 0 Data	R	-
30	IN_REG_BIT_30			
29	IN_REG_BIT_29			
28	IN_REG_BIT_28			
27	IN_REG_BIT_27			
26	IN_REG_BIT_26			
25	IN_REG_BIT_25			
24	IN_REG_BIT_24			
23	IN_REG_BIT_23			
22	IN_REG_BIT_22			
21	IN_REG_BIT_21			
20	IN_REG_BIT_20			
19	IN_REG_BIT_19			
18	IN_REG_BIT_18			
17	IN_REG_BIT_17			
16	IN_REG_BIT_16			
15	IN_REG_BIT_15			
14	IN_REG_BIT_14			
13	IN_REG_BIT_13			
12	IN_REG_BIT_12			
11	IN_REG_BIT_11			
10	IN_REG_BIT_10			
9	IN_REG_BIT_9			
8	IN_REG_BIT_8			
7	IN_REG_BIT_7			
6	IN_REG_BIT_6			
5	IN_REG_BIT_5			
4	IN_REG_BIT_4			
3	IN_REG_BIT_3			
2	IN_REG_BIT_2			
1	IN_REG_BIT_1			
0	IN_REG_BIT_0			

Table 4-8 : Input Register 0 (IN_REG0)

4.2.4 Input Register 1 (IN_REG1)

Read directly from the I/O lines 63 to 32.

Bit	Symbol	Description	Access	Reset Value
63	IN_REG_BIT_63	Input Port bit 63 : 32 Data	R	-
62	IN_REG_BIT_62			
61	IN_REG_BIT_61			
60	IN_REG_BIT_60			
59	IN_REG_BIT_59			
58	IN_REG_BIT_58			
57	IN_REG_BIT_57			
56	IN_REG_BIT_56			
55	IN_REG_BIT_55			
54	IN_REG_BIT_54			
53	IN_REG_BIT_53			
52	IN_REG_BIT_52			
51	IN_REG_BIT_51			
50	IN_REG_BIT_50			
49	IN_REG_BIT_49			
48	IN_REG_BIT_48			
47	IN_REG_BIT_47			
46	IN_REG_BIT_46			
45	IN_REG_BIT_45			
44	IN_REG_BIT_44			
43	IN_REG_BIT_43			
42	IN_REG_BIT_42			
41	IN_REG_BIT_41			
40	IN_REG_BIT_40			
39	IN_REG_BIT_39			
38	IN_REG_BIT_38			
37	IN_REG_BIT_37			
36	IN_REG_BIT_36			
35	IN_REG_BIT_35			
34	IN_REG_BIT_34			
33	IN_REG_BIT_33			
32	IN_REG_BIT_32			

Table 4-9 : Input Register 1 (IN_REG1)

4.2.5 Output Enable Register 0 (OE_REG0)

Bit	Symbol	Description	Access	Reset Value
31	OE_REG_BIT_31	Output Enable bit 31 : 0 0: disables the output buffer 1: enables the output buffer	R/W	0
30	OE_REG_BIT_30			
29	OE_REG_BIT_29			
28	OE_REG_BIT_28			
27	OE_REG_BIT_27			
26	OE_REG_BIT_26			
25	OE_REG_BIT_25			
24	OE_REG_BIT_24			
23	OE_REG_BIT_23			
22	OE_REG_BIT_22			
21	OE_REG_BIT_21			
20	OE_REG_BIT_20			
19	OE_REG_BIT_19			
18	OE_REG_BIT_18			
17	OE_REG_BIT_17			
16	OE_REG_BIT_16			
15	OE_REG_BIT_15			
14	OE_REG_BIT_14			
13	OE_REG_BIT_13			
12	OE_REG_BIT_12			
11	OE_REG_BIT_11			
10	OE_REG_BIT_10			
9	OE_REG_BIT_9			
8	OE_REG_BIT_8			
7	OE_REG_BIT_7			
6	OE_REG_BIT_6			
5	OE_REG_BIT_5			
4	OE_REG_BIT_4			
3	OE_REG_BIT_3			
2	OE_REG_BIT_2			
1	OE_REG_BIT_1			
0	OE_REG_BIT_0			

Table 4-10: Output Enable Register 0 (OE_REG0)

The output lines are switched in 8 groups of 8 signals with a delay of about 15ns between 2 groups (if PCI clock is 33 MHz). This switching is done after every write access to Output or Output Enable Register.

4.2.6 Output Enable Register 1 (OE_REG1)

Bit	Symbol	Description	Access	Reset Value
63	OE_REG_BIT_63	Output Enable bit 63 : 32 0: disables the output buffer 1: enables the output buffer	R/W	0
62	OE_REG_BIT_62			
61	OE_REG_BIT_61			
60	OE_REG_BIT_60			
59	OE_REG_BIT_59			
58	OE_REG_BIT_58			
57	OE_REG_BIT_57			
56	OE_REG_BIT_56			
55	OE_REG_BIT_55			
54	OE_REG_BIT_54			
53	OE_REG_BIT_53			
52	OE_REG_BIT_52			
51	OE_REG_BIT_51			
50	OE_REG_BIT_50			
49	OE_REG_BIT_49			
48	OE_REG_BIT_48			
47	OE_REG_BIT_47			
46	OE_REG_BIT_46			
45	OE_REG_BIT_45			
44	OE_REG_BIT_44			
43	OE_REG_BIT_43			
42	OE_REG_BIT_42			
41	OE_REG_BIT_41			
40	OE_REG_BIT_40			
39	OE_REG_BIT_39			
38	OE_REG_BIT_38			
37	OE_REG_BIT_37			
36	OE_REG_BIT_36			
35	OE_REG_BIT_35			
34	OE_REG_BIT_34			
33	OE_REG_BIT_33			
32	OE_REG_BIT_32			

Table 4-11: Output Enable Register 1 (OE_REG1)

The output lines are switched in 8 groups of 8 signals with a delay of about 15ns between 2 groups (if PCI clock is 33 MHz). This switching is done after every write access to Output or Output Enable Register.

4.2.7 Interrupt Status Register 0 (ISR0)

The Interrupt Status Register signals the lines on which an interrupt event occurred.

Bit	Symbol	Description	Access	Reset Value
31	INT_31	Line 31 : 0 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/W	0
30	INT_30			
29	INT_29			
28	INT_28			
27	INT_27			
26	INT_26			
25	INT_25			
24	INT_24			
23	INT_23			
22	INT_22			
21	INT_21			
20	INT_20			
19	INT_19			
18	INT_18			
17	INT_17			
16	INT_16			
15	INT_15			
14	INT_14			
13	INT_13			
12	INT_12			
11	INT_11			
10	INT_10			
9	INT_9			
8	INT_8			
7	INT_7			
6	INT_6			
5	INT_5			
4	INT_4			
3	INT_3			
2	INT_2			
1	INT_1			
0	INT_0			

Table 4-12: Interrupt Status Register 0 (ISR0)

Please see note in next chapter.

4.2.8 Interrupt Status Register 1 (ISR1)

The Interrupt Status Register signals the lines on which an interrupt event occurred.

Bit	Symbol	Description	Access	Reset Value
63	INT_63	Line 63 : 32 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/W	0
62	INT_62			
61	INT_61			
60	INT_60			
59	INT_59			
58	INT_58			
57	INT_57			
56	INT_56			
55	INT_55			
54	INT_54			
53	INT_53			
52	INT_52			
51	INT_51			
50	INT_50			
49	INT_49			
48	INT_48			
47	INT_47			
46	INT_46			
45	INT_45			
44	INT_44			
43	INT_43			
42	INT_42			
41	INT_41			
40	INT_40			
39	INT_39			
38	INT_38			
37	INT_37			
36	INT_36			
35	INT_35			
34	INT_34			
33	INT_33			
32	INT_32			

Table 4-13: Interrupt Status Register 1 (ISR1)

All interrupt sources are mapped to the local interrupt LINT1#. The local interrupt LINT1# is used in active low-level sensitive mode.

Interrupt request flags are acknowledged by writing '1' to the corresponding bit in ISR0/1.

4.2.9 Positive Edge Interrupt Enable Register 0 (PIER0)

Bit	Symbol	Description	Access	Reset Value
31	PIE_31	Line 31 : 0 Rising Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
30	PIE_30			
29	PIE_29			
28	PIE_28			
27	PIE_27			
26	PIE_26			
25	PIE_25			
24	PIE_24			
23	PIE_23			
22	PIE_22			
21	PIE_21			
20	PIE_20			
19	PIE_19			
18	PIE_18			
17	PIE_17			
16	PIE_16			
15	PIE_15			
14	PIE_14			
13	PIE_13			
12	PIE_12			
11	PIE_11			
10	PIE_10			
9	PIE_9			
8	PIE_8			
7	PIE_7			
6	PIE_6			
5	PIE_5			
4	PIE_4			
3	PIE_3			
2	PIE_2			
1	PIE_1			
0	PIE_0			

Table 4-14: Positive Edge Interrupt Enable Register 0 (PIER0)

4.2.10 Positive Edge Interrupt Enable Register 1 (PIER1)

Bit	Symbol	Description	Access	Reset Value
63	PIE_63	Line 63 : 32 Rising Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
62	PIE_62			
61	PIE_61			
60	PIE_60			
59	PIE_59			
58	PIE_58			
57	PIE_57			
56	PIE_56			
55	PIE_55			
54	PIE_54			
53	PIE_53			
52	PIE_52			
51	PIE_51			
50	PIE_50			
49	PIE_49			
48	PIE_48			
47	PIE_47			
46	PIE_46			
45	PIE_45			
44	PIE_44			
43	PIE_43			
42	PIE_42			
41	PIE_41			
40	PIE_40			
39	PIE_39			
38	PIE_38			
37	PIE_37			
36	PIE_36			
35	PIE_35			
34	PIE_34			
33	PIE_33			
32	PIE_32			

Table 4-15: Positive Edge Interrupt Enable Register 1 (PIER1)

4.2.11 Negative Edge Interrupt Enable Register 0 (NIER0)

Bit	Symbol	Description	Access	Reset Value
31	NIE_31	Line 31 : 0 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
30	NIE_30			
29	NIE_29			
28	NIE_28			
27	NIE_27			
26	NIE_26			
25	NIE_25			
24	NIE_24			
23	NIE_23			
22	NIE_22			
21	NIE_21			
20	NIE_20			
19	NIE_19			
18	NIE_18			
17	NIE_17			
16	NIE_16			
15	NIE_15			
14	NIE_14			
13	NIE_13			
12	NIE_12			
11	NIE_11			
10	NIE_10			
9	NIE_9			
8	NIE_8			
7	NIE_7			
6	NIE_6			
5	NIE_5			
4	NIE_4			
3	NIE_3			
2	NIE_2			
1	NIE_1			
0	NIE_0			

Table 4-16: Negative Edge Interrupt Enable Register 0 (NIER0)

4.2.12 Negative Edge Interrupt Enable Register 1 (NIER1)

Bit	Symbol	Description	Access	Reset Value
63	NIE_63	Line 63 : 32 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
62	NIE_62			
61	NIE_61			
60	NIE_60			
59	NIE_59			
58	NIE_58			
57	NIE_57			
56	NIE_56			
55	NIE_55			
54	NIE_54			
53	NIE_53			
52	NIE_52			
51	NIE_51			
50	NIE_50			
49	NIE_49			
48	NIE_48			
47	NIE_47			
46	NIE_46			
45	NIE_45			
44	NIE_44			
43	NIE_43			
42	NIE_42			
41	NIE_41			
40	NIE_40			
39	NIE_39			
38	NIE_38			
37	NIE_37			
36	NIE_36			
35	NIE_35			
34	NIE_34			
33	NIE_33			
32	NIE_32			

Table 4-17: Negative Edge Interrupt Enable Register 1 (NIER1)

4.2.13 Functional Space Revision Register (FREVREG)

Bit	Symbol	Description	Access	Reset Value
31	FREVREG	Firmware Version Register for Functional Space	R	*)

Table 4-18: Revision Register (FREVREG)

*) Depends on Firmware Version

4.3 Serial EEPROM

The serial EEPROM is **not** used for storing any configuration settings. All configuration data is stored within the internal Flash of the PLD. Hence, the device can be completely be used as memory.

For backward compatibility the serial EEPROM contains the configuration data of the previous version PCI controller.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x02A9	0x1498	0x0280	0x0000	0x1180	0x0000	0x000A	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x0001	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFF00	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x1581	0x20A0	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0081	0x0000	0x0002	0x0000	0x0002
0x70	0x0000	0x0002	0x0030	0x0041	0x0078	0x0000	0x0000	0x0240
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-19: Serial EEPROM Content

5 Configuration Hints

5.1 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- The Functional Space can operate in Big or Little Endian Mode. By default it is set to Big Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Table 5-1 : Data Bus Little/Big Endian

5.2 Local Software Reset

The Functional Register Space is linked to a local reset signal, which can be stimulated via software.

The local reset is active during PCI reset or if the *PCI Adapter Software Reset* bit is set in the multi-purpose register *CNTRL* (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of ‘1’ asserts a reset that remains until the bit is cleared (set to ‘0’). Such a reset does not affect the content of the Local Configuration Registers.

6 Installation

6.1 Pull Up Voltage

The voltage of the pull up resistors can be 3.3V or alternatively 5V, specified by jumper J1 for all I/O lines in common. The default pull up voltage is 3.3V.

J1 Jumper Position	Pull Up Voltage
1 – 2	3.3V (default)
2 – 3	5V

Figure 6-1 : Pull Up Voltage Jumper Setting

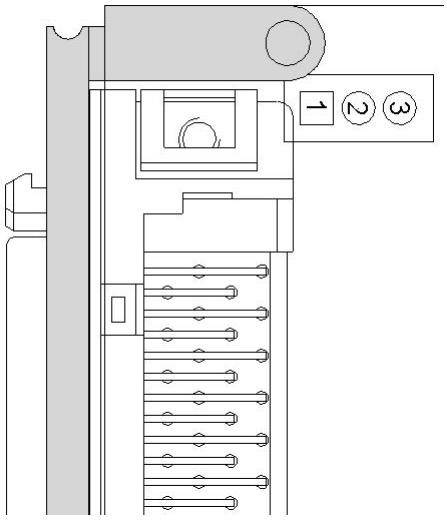


Figure 6-2 : Jumper Position and Pin Labeling

6.2 I/O Interface

Each of the 64 I/O lines is realized with two 74LVT126 buffers as an interface to the FPGA pins. The logic levels of the buffers are TTL compatible, meaning that the minimum input high level is 2.0V and the maximum input low level is 0.8V. The nominal output high voltage is 3.3V.

The buffer outputs are followed by 47Ω serial resistors for signal integrity reasons. The 4.7kΩ pull up resistors guaranty a high level when outputs are tristate and not driven externally.

In contrast to the buffer outputs, which must be explicitly enabled, the buffer inputs are permanently enabled.

As an option the pull up voltage can be set to 5V by jumper J1 to (weakly) drive a higher voltage than 3.3V by setting the output to tristate. This means, instead of toggling the corresponding bit of the output register, the output enable register bit is set to 0 for an output high level or 1 to pull the output low (the OUT_REG bit is '0').

For example, when connecting to a standard 5V CMOS logic input (not TTL compatible levels), a high level of minimum 3.5V is required.

Please note that the pull up resistor can only drive high impedance inputs.

A TVS array protects against ESD shocks.

See the following figure for more information of the TTL I/O circuitry.

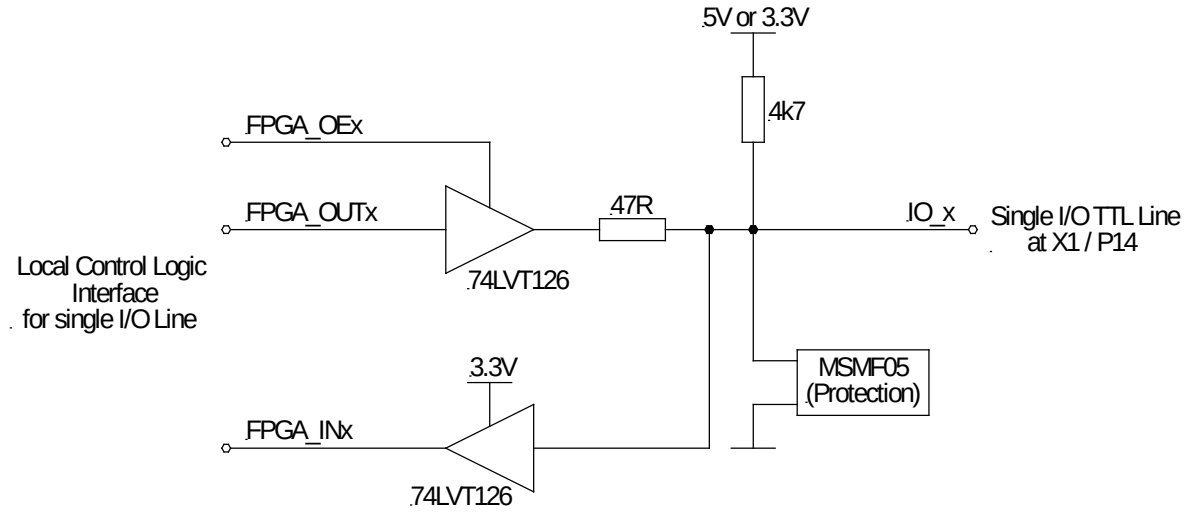


Figure 6-3 : TTL I/O Interface

Please note that the length (and consequently the capacitance) of a flat cable, connected to the TPMC681 module, should be kept as short as possible to prevent large cross talk.

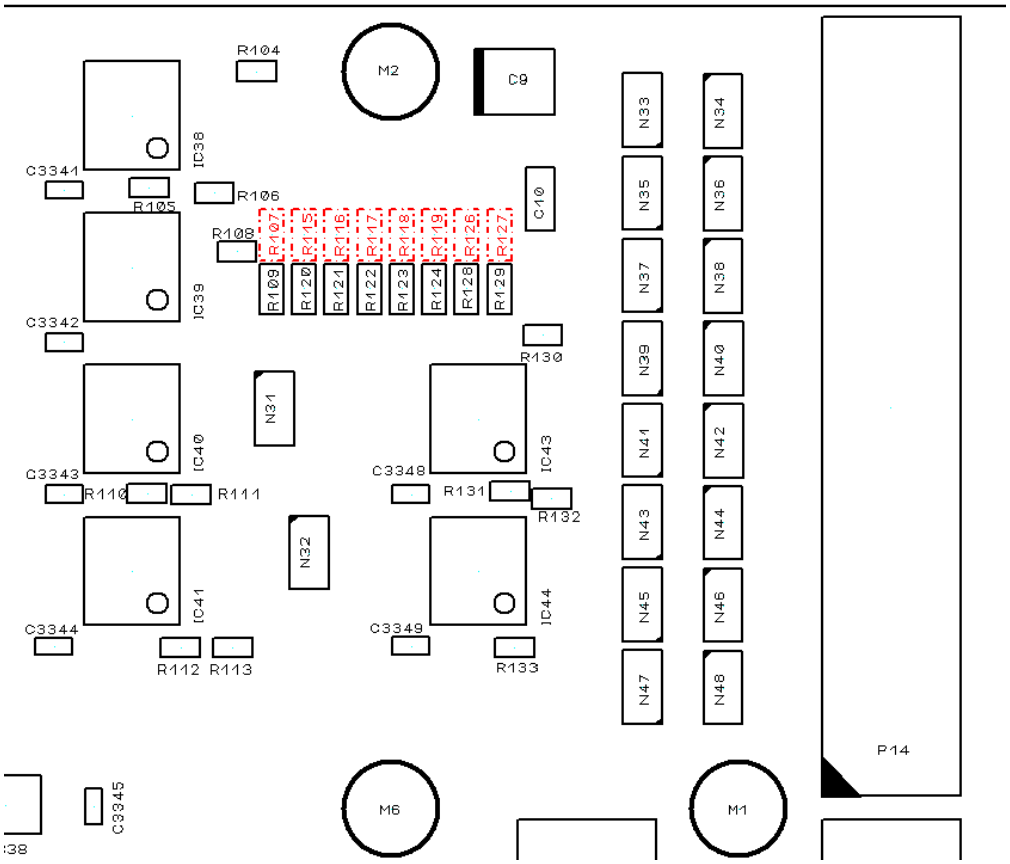
To minimize crosstalk and overshoot/ground bounce the outputs are switched in 8 groups of 8 signals with a delay of about 15ns (@ 33 MHz PCI clock). Therefore a switching process can take about 120ns.

6.3 Back I/O Configuration

The configuration of P14 64 pin Mezzanine “Back I/O” connector lines [56 : 63] can be changed between ground or I/O port signals by zero ohm resistors.

For removing zero ohm resistors, work on a grounded; static free work surface.

The pads of the zero ohm resistors allow making a direct solder connection between the pads after removing the zero ohm resistors.



The following table summarizes which resistors (or rather jumper) implement which function and to which I/O line these belong to.

Back I/O Line	Signal	Jumper Position
56	ground	R107
	I/O Line 56 (default)	R109
57	ground	R115
	I/O Line 57 (default)	R120
58	ground	R116
	I/O Line 58 (default)	R121
59	ground	R117
	I/O Line 59 (default)	R122
60	ground	R118
	I/O Line 60 (default)	R123
61	ground	R119
	I/O Line 61 (default)	R124
62	ground	R126
	I/O Line 62 (default)	R128
63	ground	R127
	I/O Line 63 (default)	R129

Figure 6-4 : Jumper positions for Back I/O options

Caution: Never make simultaneous connections on both jumper positions of one I/O line. Serious damage of the module is possible.

7 Pin Assignment – I/O Connector

7.1 Front Panel I/O Connector

TE 5787082-7 or compatible

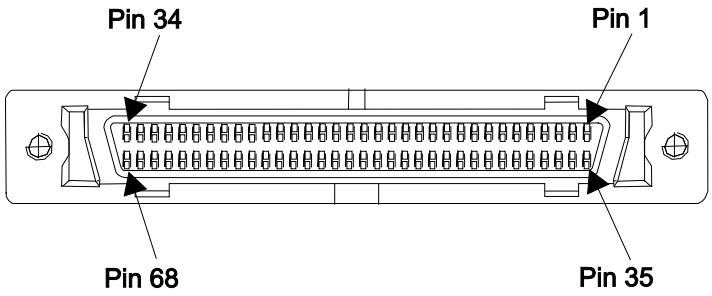


Figure 7-1 : Front Panel I/O Connector Numbering

Pin	Signal	Pin	Signal
1	IO_0	35	IO_1
2	IO_2	36	IO_3
3	IO_4	37	IO_5
4	IO_6	38	IO_7
5	IO_8	39	IO_9
6	IO_10	40	IO_11
7	IO_12	41	IO_13
8	IO_14	42	IO_15
9	GND	43	GND
10	IO_16	44	IO_17
11	IO_18	45	IO_19
12	IO_20	46	IO_21
13	IO_22	47	IO_23
14	IO_24	48	IO_25
15	IO_26	49	IO_27
16	IO_28	50	IO_29
17	IO_30	51	IO_31
18	IO_32	52	IO_33
19	IO_34	53	IO_35
20	IO_36	54	IO_37
21	IO_38	55	IO_39
22	IO_40	56	IO_41
23	IO_42	57	IO_43
24	IO_44	58	IO_45
25	IO_46	59	IO_47
26	GND	60	GND
27	IO_48	61	IO_49
28	IO_50	62	IO_51
29	IO_52	63	IO_53
30	IO_54	64	IO_55
31	IO_56	65	IO_57
32	IO_58	66	IO_59
33	IO_60	67	IO_61
34	IO_62	68	IO_63

Table 7-1 : Pin Assignment Front I/O Connector

7.2 Back I/O PMC Connector

Pin	Signal
1	IO_0
2	IO_1
3	IO_2
4	IO_3
5	IO_4
6	IO_5
7	IO_6
8	IO_7
9	IO_8
10	IO_9
11	IO_10
12	IO_11
13	IO_12
14	IO_13
15	IO_14
16	IO_15
17	IO_16
18	IO_17
19	IO_18
20	IO_19
21	IO_20
22	IO_21
23	IO_22
24	IO_23
25	IO_24
26	IO_25
27	IO_26
28	IO_27
29	IO_28
30	IO_29
31	IO_30
32	IO_31

Pin	Signal
33	IO_32
34	IO_33
35	IO_34
36	IO_35
37	IO_36
38	IO_37
39	IO_38
40	IO_39
41	IO_40
42	IO_41
43	IO_42
44	IO_43
45	IO_44
46	IO_45
47	IO_46
48	IO_47
49	IO_48
50	IO_49
51	IO_50
52	IO_51
53	IO_52
54	IO_53
55	IO_54
56	IO_55
57	IO_56 / GND (opt.)
58	IO_57 / GND (opt.)
59	IO_58 / GND (opt.)
60	IO_59 / GND (opt.)
61	IO_60 / GND (opt.)
62	IO_61 / GND (opt.)
63	IO_62 / GND (opt.)
64	IO_63 / GND (opt.)

Table 7-2 : Pin Assignment P14 I/O Connector