The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC683

32 differential I/O Lines with Interrupts

Version 1.0

User Manual

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TPMC683-10R

32 differential I/O Lines with Interrupts

Style Conventions

Hexadecimal characters are specified with prefix 0x, e.g. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, e.g. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Table of Contents

1 PRODUCT DESCRIPTION 6
2 TECHNICAL SPECIFICATION 7
3 LOCAL SPACE ADDRESSING 8
3.1 PCI9030 Local Space Configuration 8
3.2 FPGA Registers 8
3.2.1 Input Register (IN_REG) 9
3.2.2 Output Register (OUT_REG) 9
3.2.3 Output Enable Register (OE_REG) 9
3.2.4 Positive Edge Interrupt Status Register (PISR) 10
3.2.5 Negative Edge Interrupt Status Register (NISR) 10
3.2.6 Positive Edge Interrupt Enable Register (PIER) 11
3.2.7 Negative Edge Interrupt Enable Register (NIER) 11
4 PCI9030 TARGET CHIP 12
4.1 PCI Configuration Registers (PCR) 12
4.1.1 PCI9030 Header 12
4.2 Local Configuration Register (LCR) 13
4.3 Configuration EEPROM 14
4.4 Local Software Reset 15
5 CONFIGURATION HINTS 16
5.1 Big / Little Endian 16
6 INSTALLATION 18
6.1 I/O Interface 18
7 PIN ASSIGNMENT – I/O CONNECTOR 19
7.1 Front Panel I/O Connector 19
7.1.1 Pin Assignment 20
7.2 Back I/O PMC P14 Connector 21
7.2.1 Pin Assignment 21

List of Figures

FIGURE 1-1 : BLOCK DIAGRAM 6
FIGURE 6-1 : I/O INTERFACE 18
FIGURE 7-1 : I/O FRONT PANEL I/O CONNECTOR 19

List of Tables

TABLE 2-1 : TECHNICAL SPECIFICATION 7
TABLE 3-1 : PCI9030 LOCAL SPACE CONFIGURATION 8
TABLE 3-2 : REGISTER SPACE 8
TABLE 3-3 : INPUT REGISTER (IN_REG) 9
TABLE 3-4 : OUTPUT REGISTER (OUT_REG) 9
TABLE 3-5 : OUTPUT ENABLE REGISTER (OE_REG) 9
TABLE 3-6 : POSITIVE EDGE INTERRUPT STATUS REGISTER (PISR) 10
TABLE 3-7 : NEGATIVE EDGE INTERRUPT STATUS REGISTER (NISR) 10
TABLE 3-8 : POSITIVE EDGE INTERRUPT ENABLE REGISTER (PIER) 11
TABLE 3-9 : POSITIVE EDGE INTERRUPT ENABLE REGISTER (NIER) 11
TABLE 4-1 : PCI9030 HEADER 12
TABLE 4-2 : PCI9030 LOCAL CONFIGURATION REGISTERS 13
TABLE 4-3 : CONFIGURATION EEPROM TPMC683 14
TABLE 5-1 : LOCAL BUS LITTLE/BIG ENDIAN 16
TABLE 7-1 : PIN ASSIGNMENT FRONT PANEL I/O CONNECTOR 20
TABLE 7-2 : PIN ASSIGNMENT REAR I/O PMC P14 CONNECTOR 21

1 Product Description

The TPMC683 is a standard single-width 32 bit PMC module offering 32 differential I/O lines using EIA-422 / EIA-485 compatible, ESD-protected line transceivers.

Each line is individually programmable as input or output. The receivers are always enabled, which allows determining the state of each I/O line at any time. This can be used as read back function for lines configured as outputs.

Each input can generate an interrupt. Signal edge handling is programmable to interrupt on rising, falling or both edges of an input signal. Interrupts can be enabled and disabled for each input line independently. For interrupt source detection, the status of each line can be read from interrupt status registers.

The TPMC683 provides front panel I/O via a HD68 SCSI-3 type connector and rear panel I/O via P14.

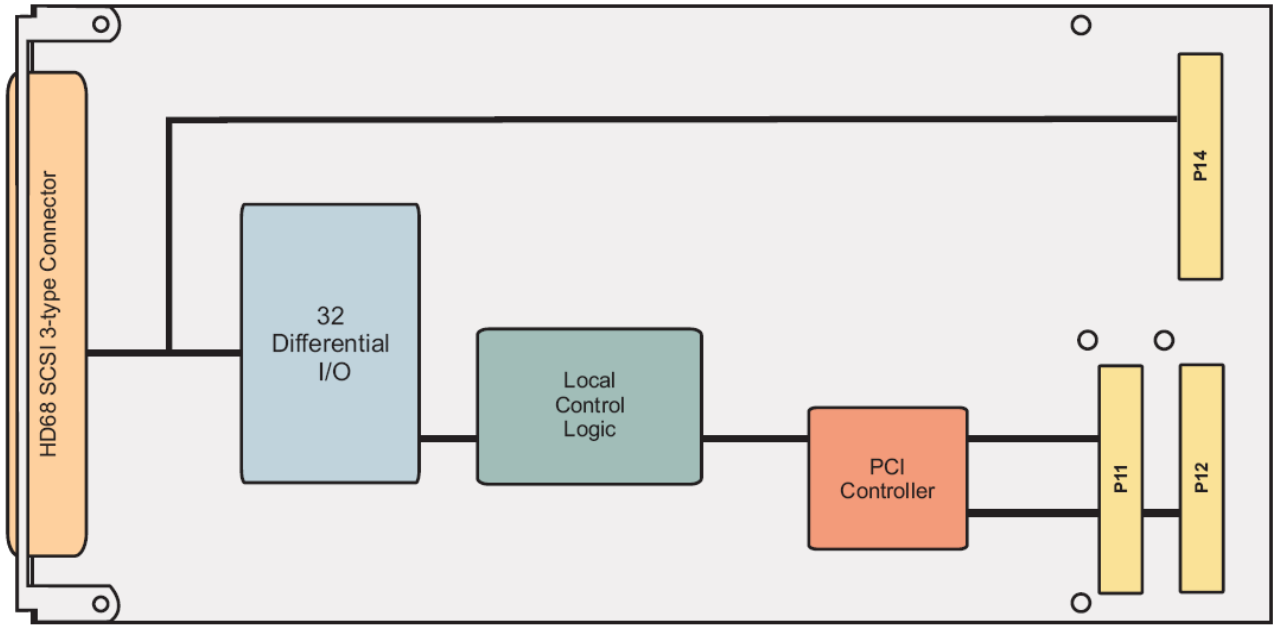

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size	
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9030 (PLX Technology)	
I/O Interface		
Number of Lines	32x Differential I/O with EIA-422/-485 signaling level	
I/O Connectors	Front I/O HD68 SCSI-3 type Connector (AMP 787082-7 or compatible) PMC P14 Rear I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	110mA typical (no load) @ +3.3V DC	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	451000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	80 g	

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	MEM	32	32	BIG	FPGA Registers
1	3 (0x1C)	-	-	-	-	Not Used
2	4 (0x20)	-	-	-	-	Not Used
3	5 (0x24)	-	-	-	-	Not Used

Table 3-1 : PCI9030 Local Space Configuration

3.2 FPGA Registers

PCI Base Address: PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).

Offset to PCI Base Address 2	Register Name	Size (Bit)
0x0000	Input Register (IN_REG)	32
0x0004	Output Register (OUT_REG)	32
0x0008	Output Enable Register (OE_REG)	32
0x000C	Positive Edge Interrupt Status Register (PISR)	32
0x0010	Negative Edge Interrupt Status Register (NISR)	32
0x0014	Positive Edge Interrupt Enable Register (PIER)	32
0x0018	Negative Edge Interrupt Enable Register (NIER)	32

Table 3-2 : Register Space

3.2.1 Input Register (IN_REG)

The Input Register holds the actual status of all input lines at all times. As the input receivers are connected to the output transceivers, the input register also holds the values of the lines which are configured as outputs. This can be used as a read-back function to check correct configuration.

Bit	Symbol	Description	Access	Reset Value
31:0	IN_REG	Digital Value of Input Lines	R	0

Table 3-3 : Input Register (IN_REG)

3.2.2 Output Register (OUT_REG)

The Output Register holds the values for the output transceivers. These values are driven only if the corresponding bits inside the Output Enable Register are set. Lines not enabled in the Output Enable Register are configured as inputs, even though they have a value set inside the Output Register.

Bit	Symbol	Description	Access	Reset Value
31:0	OUT_REG	Output Port	R/W	0

Table 3-4 : Output Register (OUT_REG)

The output lines are switched in 4 groups of 8 signals with a delay of about 30ns between each group. This switching is done after every write access to either the Output or the Output Enable Registers.

3.2.3 Output Enable Register (OE_REG)

The Output Enable Register is used to decide whether an I/O line is configured as input or as output.

Bit	Symbol	Description	Access	Reset Value
31:0	OE_REG	Output Enable for I/O Lines 0 = disables the output transceiver, line is configured as input 1 = enables the output transceiver, line is configured as output	R/W	0

Table 3-5 : Output Enable Register (OE_REG)

The output lines are switched in 4 groups of 8 signals with a delay of about 30ns between each group. This switching is done after every write access to either the Output or the Output Enable Registers.

3.2.4 Positive Edge Interrupt Status Register (PISR)

The Positive Edge Interrupt Status Register holds the status of interrupt requests for all input lines. A positive edge interrupt of an input line is generated when the following conditions are met simultaneously:

- The line (“x”) is actually an input (OE_REG(x) = 0)
- Positive Edge Interrupts are enabled for this input line (PIER(x) = 1)
- A transition from ‘0’ to ‘1’ happens

Bit	Symbol	Description	Access	Reset Value
31:0	PISR	Positive Edge Interrupt Status of Input Lines 0 = no active interrupt request 1 = active interrupt request	R/C	0

Table 3-6 : Positive Edge Interrupt Status Register (PISR)

All interrupt sources are mapped to the PCI9030 LINT1# local interrupt input.

Interrupt request flags are acknowledged by writing ‘1’ to the corresponding bit in the PISR.

3.2.5 Negative Edge Interrupt Status Register (NISR)

The Negative Edge Interrupt Status Register holds the status of interrupt requests for all input lines. A negative edge interrupt of an input line is generated when the following conditions are met simultaneously:

- The line (“x”) is actually an input (OE_REG(x) = 0)
- Negative Edge Interrupts are enabled for this input line (NIER(x) = 1)
- A transition from ‘1’ to ‘0’ happens

Bit	Symbol	Description	Access	Reset Value
31:0	NISR	Negative Edge Interrupt Status of Input Lines 0 = no active interrupt request 1 = active interrupt request	R/C	0

Table 3-7 : Negative Edge Interrupt Status Register (NISR)

All interrupt sources are mapped to the PCI9030 LINT1# local interrupt input.

Interrupt request flags are acknowledged by writing ‘1’ to the corresponding bit in the NISR.

3.2.6 Positive Edge Interrupt Enable Register (PIER)

The Positive Edge Interrupt Enable Register is used to enable the generation of interrupts for positive edges of input lines. The generation of interrupts can be enabled or disabled separately for each input line.

Bit	Symbol	Description	Access	Reset Value
31:0	PIER	Positive Edge Interrupt Enable for Input Lines 0 = interrupt generation disabled 1 = interrupt generation enabled	R/W	0

Table 3-8 : Positive Edge Interrupt Enable Register (PIER)

3.2.7 Negative Edge Interrupt Enable Register (NIER)

The Negative Edge Interrupt Enable Register is used to enable the generation of interrupts for negative edges of input lines. The generation of interrupts can be enabled or disabled separately for each input line.

Bit	Symbol	Description	Access	Reset Value
31:0	NIER	Negative Edge Interrupt Enable for Input Lines 0 = interrupt generation disabled 1 = interrupt generation enabled	R/W	0

Table 3-9 : Positive Edge Interrupt Enable Register (NIER)

4 PCI9030 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	02AB 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	118000 00
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFF00
0x1C	PCI Base Address 3 for Local Address Space 1				Y	00000000
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	000A 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt Cap.	PM Cap. ID	N	4801 48 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt Cap.	HS Cap. ID	Y[23:16]	00 00 4C 06
0x4C	VPD Address		VPD Nxt Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Table 4-1 : PCI9030 Header

4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value	Description
0x00	Local Address Space 0 Range	0x0FFF_FF00	Size of Space
0x04	Local Address Space 1 Range	0x0000_0000	
0x08	Local Address Space 2 Range	0x0000_0000	
0x0C	Local Address Space 3 Range	0x0000_0000	
0x10	Expansion ROM Range	0x0000_0000	
0x14	Local Address Space 0 Local Base Address (Remap)	0x0000_0001	Local Addresses
0x18	Local Address Space 1 Local Base Address (Remap)	0x0000_0000	
0x1C	Local Address Space 2 Local Base Address (Remap)	0x0000_0000	
0x20	Local Address Space 3 Local Base Address (Remap)	0x0000_0000	
0x24	Expansion ROM Local Base Address (Remap)	0x0000_0000	
0x28	Local Address Space 0 Bus Region Descriptor	0x1581_20A0	Space Settings
0x2C	Local Address Space 1 Bus Region Descriptor	0x0000_0000	
0x30	Local Address Space 2 Bus Region Descriptor	0x0000_0000	
0x34	Local Address Space 3 Bus Region Descriptor	0x0000_0000	
0x38	Expansion ROM Bus Region Descriptor	0x0000_0000	
0x3C	Chip Select 0 Base Address	0x0000_0081	Chip Select Range
0x40	Chip Select 1 Base Address	0x0000_0000	
0x44	Chip Select 2 Base Address	0x0000_0000	
0x48	Chip Select 3 Base Address	0x0000_0000	
0x4C	Interrupt Control/Status	0x0041	
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030	
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x807C_4000	PCI_r2.2 enabled
0x54	General Purpose I/O Control	0x0000_0240	
0x70	Hidden1 Register for Power Management Data Select	0x0000_0000	
0x74	Hidden 2 Register for Power Management Data Scale	0x0000_0000	

Table 4-2 : PCI9030 Local Configuration Registers

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x02AB	0x1498	0x0280	0x0000	0x1180	0x0000	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFF00	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x1581	0x20A0	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0081	0x0000	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0030	0x0041	0x807C	0x4000	0x0000	0x0240
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-3 : Configuration EEPROM TPMC683

Subsystem-ID Value (Offset 0x0C): TPMC683-10R 0x000A

4.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 Local Reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

5 Configuration Hints

5.1 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Table 5-1 : Local Bus Little/Big Endian

Standard use of the TPMC683:

Local Address Space 0	32 bit bus in Big Endian Mode
Local Address Space 1	not used
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers (which are called “Local Address Space X Bus Region Descriptor”) for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset to access the Local Bus Configuration Registers:

Symbol	Offset	Name
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 1 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 2 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 3 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

6 Installation

6.1 I/O Interface

Each of the 32 differential I/O line pairs is realized with an input, output and output enable pin at the XILINX FPGA. These are connected to a MAX3078E, which is an ESD-protected RS485/RS422 transceiver, and to a 120Ω termination resistor.

The inputs of the receivers are directly connected to the outputs of the transceivers. This way, it is possible to read the values of the output ports to check the correct settings.

See figure 6-1 for more information of the differential I/O circuitry.

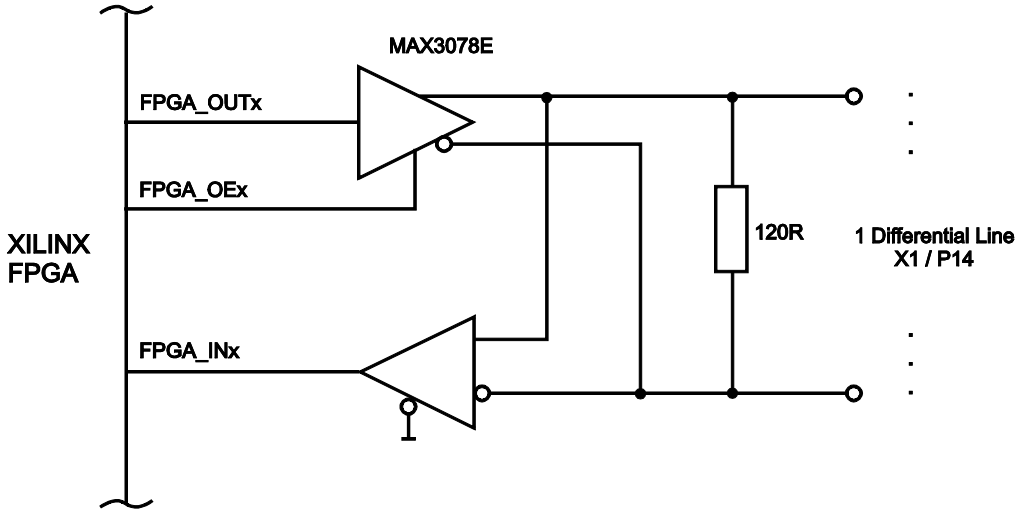

Figure 6-1 : I/O Interface

7 Pin Assignment – I/O Connector

7.1 Front Panel I/O Connector

Pin-Count	68
Connector Type	AMP 787082-7 or compatible (HD68 SCSI-3)

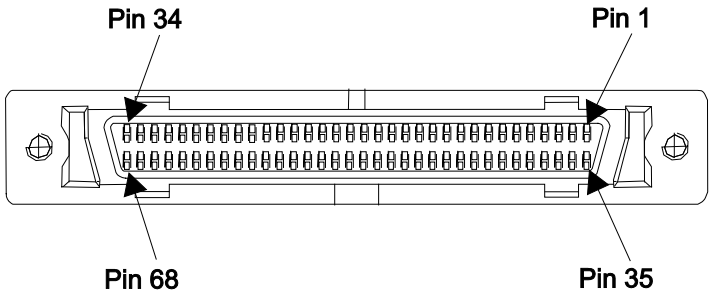

Figure 7-1 : I/O Front Panel I/O Connector

7.1.1 Pin Assignment

Pin	Signal	Level
1	IO_0A/-	Diff. -
2	IO_1A/-	Diff. -
3	IO_2A/-	Diff. -
4	IO_3A/-	Diff. -
5	IO_4A/-	Diff. -
6	IO_5A/-	Diff. -
7	IO_6A/-	Diff. -
8	IO_7A/-	Diff. -
9	GND	GND
10	IO_8A/-	Diff. -
11	IO_9A/-	Diff. -
12	IO_10A/-	Diff. -
13	IO_11A/-	Diff. -
14	IO_12A/-	Diff. -
15	IO_13A/-	Diff. -
16	IO_14A/-	Diff. -
17	IO_15A/-	Diff. -
18	IO_16A/-	Diff. -
19	IO_17A/-	Diff. -
20	IO_18A/-	Diff. -
21	IO_19A/-	Diff. -
22	IO_20A/-	Diff. -
23	IO_21A/-	Diff. -
24	IO_22A/-	Diff. -
25	IO_23A/-	Diff. -
26	GND	GND
27	IO_24A/-	Diff. -
28	IO_25A/-	Diff. -
29	IO_26A/-	Diff. -
30	IO_27A/-	Diff. -
31	IO_28A/-	Diff. -
32	IO_29A/-	Diff. -
33	IO_30A/-	Diff. -
34	IO_31A/-	Diff. -

Pin	Signal	Level
35	IO_0B/+	Diff. +
36	IO_1B/+	Diff. +
37	IO_2B/+	Diff. +
38	IO_3B/+	Diff. +
39	IO_4B/+	Diff. +
40	IO5B/+	Diff. +
41	IO6B/+	Diff. +
42	IO_7B/+	Diff. +
43	GND	GND
44	IO_8B/+	Diff. +
45	IO_9B/+	Diff. +
46	IO_10B/+	Diff. +
47	IO_11B/+	Diff. +
48	IO_12B/+	Diff. +
49	IO_13B/+	Diff. +
50	IO_14B/+	Diff. +
51	IO_15B/+	Diff. +
52	IO_16B/+	Diff. +
53	IO_17B/+	Diff. +
54	IO_18B/+	Diff. +
55	IO_19B/+	Diff. +
56	IO_20B/+	Diff. +
57	IO_21B/+	Diff. +
58	IO_22B/+	Diff. +
59	IO_23B/+	Diff. +
60	GND	GND
61	IO_24B/+	Diff. +
62	IO_25B/+	Diff. +
63	IO_26B/+	Diff. +
64	IO_27B/+	Diff. +
65	IO_28B/+	Diff. +
66	IO_29B/+	Diff. +
67	IO_30B/+	Diff. +
68	IO_31B/+	Diff. +

Table 7-1 : Pin Assignment Front Panel I/O Connector

7.2 Back I/O PMC P14 Connector

7.2.1 Pin Assignment

Pin	Signal	Level
1	IO_0A/-	Diff. -
2	IO_0B/+	Diff. +
3	IO_1A/-	Diff. -
4	IO_1B/+	Diff. +
5	IO_2A/-	Diff. -
6	IO_2B/+	Diff. +
7	IO_3A/-	Diff. -
8	IO_3B/+	Diff. +
9	IO_4A/-	Diff. -
10	IO_4B/+	Diff. +
11	IO_5A/-	Diff. -
12	IO_5B/+	Diff. +
13	IO_6A/-	Diff. -
14	IO_6B/+	Diff. +
15	IO_7A/-	Diff. -
16	IO_7B/+	Diff. +
17	IO_8A/-	Diff. -
18	IO_8B/+	Diff. +
19	IO_9A/-	Diff. -
20	IO_9B/+	Diff. +
21	IO_10A/-	Diff. -
22	IO_10B/+	Diff. +
23	IO_11A/-	Diff. -
24	IO_11B/+	Diff. +
25	IO_12A/-	Diff. -
26	IO_12B/+	Diff. +
27	IO_13A/-	Diff. -
28	IO_13B/+	Diff. +
29	IO_14A/-	Diff. -
30	IO_14B/+	Diff. +
31	IO_15A/-	Diff. -
32	IO_15B/+	Diff. +

Pin	Signal	Level
33	IO_16A/-	Diff. -
34	IO_16B/+	Diff. +
35	IO_17A/-	Diff. -
36	IO_17B/+	Diff. +
37	IO_18A/-	Diff. -
38	IO_18B/+	Diff. +
39	IO_19A/-	Diff. -
40	IO_19B/+	Diff. +
41	IO_20A/-	Diff. -
42	IO_20B/+	Diff. +
43	IO_21A/-	Diff. -
44	IO_21B/+	Diff. +
45	IO_22A/-	Diff. -
46	IO_22B/+	Diff. +
47	IO_23A/-	Diff. -
48	IO_23B/+	Diff. +
49	IO_24A/-	Diff. -
50	IO_24B/+	Diff. +
51	IO_25A/-	Diff. -
52	IO_25B/+	Diff. +
53	IO_26A/-	Diff. -
54	IO_26B/+	Diff. +
55	IO_27A/-	Diff. -
56	IO_27B/+	Diff. +
57	IO_28A/-	Diff. -
58	IO_28B/+	Diff. +
59	IO_29A/-	Diff. -
60	IO_29B/+	Diff. +
61	IO_30A/-	Diff. -
62	IO_30B/+	Diff. +
63	IO_31A/-	Diff. -
64	IO_31B/+	Diff. +

Table 7-2 : Pin Assignment Rear I/O PMC P14 Connector