The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC700

32/16 Digital Outputs (24 V, 0.5 A)

Version 2.0

User Manual

Issue 2.0.1

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TPMC700-10R

32 digital outputs front panel I/O

TPMC700-11R

16 digital outputs front panel I/O

TPMC700-20R

32 digital outputs P14 I/O

TPMC700-21R

16 digital outputs P14 I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	September 1999
1.1	General Revision	April 2003
1.2	Description of optical isolation corrected	March 2004
1.3	Added differences of V1.1	June 2005
1.4	New address TEWS LLC	September 2006
1.1.0	New notation of HW Engineering Documentation Releases	November 2011
1.1.1	General Revision	August 2014
2.0.0	General Board Redesign to Version 2.0 due to component obsolescence. Fully backward compatible.	September 2024
2.0.1	Extension of tables describing the Pin Assignments. General revision.	November 2025

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1 Product Description

The TPMC700 is a PMC compatible module which provide 32 (16) digital outputs with galvanic isolation via optocouplers. All outputs resist short-circuits and are protected against thermal overload. The output drivers are capable of driving 0.5 A continuous per channel as a high side switch. A hardware watchdog forces all outputs into safe state (disabled) in case of a trigger failure.

The TPMC700-1xR provides front panel I/O with a HD50 SCSI-2 type connector, the TPMC700-2xR provides P14 I/O.

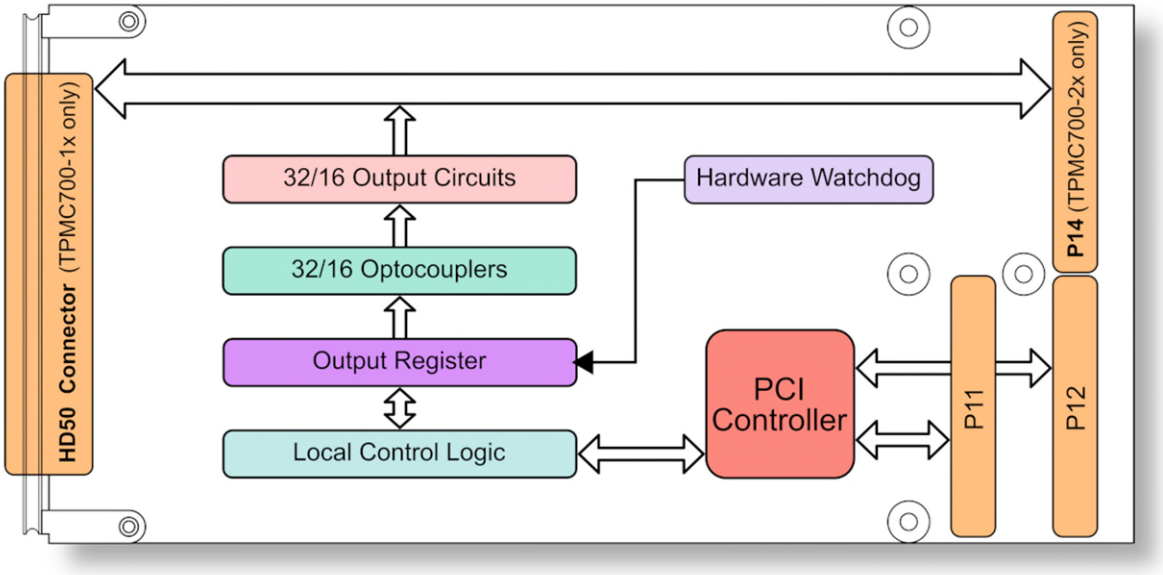

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size
Electrical Interface	PCI Rev. 3.0 compatible 33 MHz / 32 bit PCI 3.3 V and 5 V PCI Signaling Voltage

I/O Interface	
Number of Outputs	TPMC700-10R/-20R: 32 digital outputs TPMC700-11R/-21R: 16 digital outputs
Output Isolation	Optocouplers for galvanic isolation between system and output lines
External Output Voltage	24 VDC typical, 6 VDC minimum, 48 VDC maximum
Output Current	0.5 A typical (0.3 A for voltages over 32 V)
Short Circuit Current	0.8 A typical
Output Voltage Drop	1.1 V typical @ 0.5 A
Output Protection	Overload, short circuit, GND and Vs open wire protection, thermal shutdown
Watchdog	Maximum trigger distance = 120 ms
I/O Connector	TPMC700-10R/-11R: HD50 SCSI-2 type connector (AMP 787395-5) or compatible TPMC700-20R/-21R: PMC P14 I/O (64 pin Mezzanine Connector)

Physical Data		
Power Requirements	75 mA typical @ +5 VDC	
Temperature Range	Operating Storage	-25 °C to +85 °C -40 °C to +125 °C
MTBF	TPMC700-10R: 711 000 h TPMC700-11R: 858 000 h TPMC700-20R: 711 000 h TPMC700-21R: 858 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	72 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

3.2 Ground for Isolated I/O

I/O Connector's isolated ground signals must be connected to external ground.

4 Addressing

4.1 PCI Device Identification

The offset values relate to the PCI Header.

	Offset	
Vendor ID	0x00	0x1498 (TEWS Technologies)
Device ID	0x02	0x02BC (TPMC700)
Revision ID	0x08	0x00
Class Code	0x09	0x118000 (Other Data Acquisition/Signal Processing Controllers)
Subsystem Vendor ID	0x2C	0x1498 (TEWS Technologies)
Subsystem ID	0x2E	0x000A (TPMC700-10R) 0x000B (TPMC700-11R) 0x0014 (TPMC700-20R) 0x0015 (TPMC700-21R)

Table 4-1 : PCI Device Identification

4.2 PCI Address Space Overview

The local on board addressable regions are accessed from the PCI side by using the BAR2 Base Address.

PCI BAR	PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0x10	MEM	128	32	Little	PCI Controller Register Space
1	0x14	I/O	128	32	Little	
2	0x18	MEM	16	32	Big	Local Register Space

Table 4-2 : PCI Address Space Overview

4.3 PCI Controller Register Space

The PCI Controller Register Spaces are factory reserved.

4.4 Local Register Space

The PCI base address for the Local Registers is PCI Base Address 2 (PCI Memory Space, Offset 0x18 in the PCI Configuration Space).

Offset to BAR2	Register Name	Size (Bit)
0x0000	Data Output Register	32
0x0004	Control Register	32

Table 4-3 : Local Register Space

4.4.1 Data Output Register

The Data Output Register is a long word wide read/write register used to set or clear the outputs lines.

Bit	Symbol	Description	Access	Reset Value
31:0	OUTPUT 32 … OUTPUT 1	Set or clear the corresponding output line 1 = active 0 = inactive Bit 0 represents OUT 1, Bit 31 represents OUT 32 accordingly	R/W	0

Table 4-4 : Data Output Register

After power-on or reset the Data Output Register is cleared to '0', all outputs are inactive.

4.4.2 Control Register

The Control Register is a 32 bit read/write register.

Bit	Symbol	Description	Access	Reset Value
31:4	-	Reserved (0 for reads)	-	0
3	WDOG_STAT	Watchdog Status bit 1 = indicate that the watchdog has recognized a failure and has disabled all output channels. The Data Output Register is locked. Writing '1' to this bit unlocks the Data Output Register. 0 = signals normal operation	R/W	0
2	-	Reserved (0 for reads)	-	0
1	WDOG_EN	Watchdog Enable bit for all 32 outputs 1 = enable watchdog function 0 = disable	R/W	0
0	-	Reserved (0 for reads)	-	0

Table 4-5 : Control Register

The watchdog status is only active if the watchdog is enabled.

5 Functional Description of Digital Outputs

5.1 Optical Isolation

The TPMC700 has 32 (TPMC700-10R/-20R) or 16 (TPMC700-11R/-21R) digital outputs. The standard signal level for these outputs is 24 VDC. All outputs are isolated by optocouplers from the system and in two ground groups (output OUT 1-16 and output OUT 17-32) against each other.

Within these two groups there are four subgroups for the VS power supply which allow different supply voltages in groups of four, but referenced to the same GND.

Group	Supply	Ground	Output
O1	VS_O1	GND_OA	OUT 1 OUT 2 OUT 3 OUT 4
O2	VS_ O2		OUT 5 OUT 6 OUT 7 OUT 8
O3	VS_ O3		OUT 9 OUT 10 OUT 11 OUT 12
O4	VS_ O4		OUT 13 OUT 14 OUT 15 OUT 16
O5	VS_ O5	GND_OB	OUT 17 OUT 18 OUT 19 OUT 20
O6	VS_ O6		OUT 21 OUT 22 OUT 23 OUT 24
O7	VS_ O7		OUT 25 OUT 26 OUT 27 OUT 28
O8	VS_ O8		OUT 29 OUT 30 OUT 31 OUT 32

Table 5-1 : Isolated Digital Outputs summary

5.2 Output Polarity

Each output can be individually switched to the according power supply VS_Ox (high side switch).

5.3 Overload Protection

The output drivers used on the TPMC700 are ‘smart drivers’ TDE1707. The maximum continuous output current is 0.5 A. The output circuits are protected against overload, short circuit and over temperature. In case of such failure the corresponding output is switched off until the error condition is removed. The output returns automatically to normal operation, i.e. the state programmed in the Data Output Register.

5.4 Output Watchdog

Writing ‘1’ into bit 1 of the Control Register the hardware watchdog function is enabled. The status of the watchdog is indicated at bit 3 of the Control Register.

Any software accesses (read or write) to the Data Output Register will retrigger the watchdog. The maximum time between two accesses is set to 120ms. If the time expires without a software access all outputs go into “OFF” state. At the same time the watchdog status will change from ‘0’ to ‘1’ and locks the Data Output Register. This prevents a write access to the Data Output Register. The output register content is not affected by that.

Writing ‘1’ to the watchdog status (bit 3 Control Register) clears this bit and also unlocks the Data Output Register. After unlocking the Data Output Register the output stays in the “OFF” state till the next write access to this register.

The watchdog is disabled after power-on or reset.

6 Programming Hints

6.1 Local Read/Write

The local register set supports long word (32 bit) read/write access only. A byte or word access has undefined result.

Use only 32 bit read/write accesses to the TPMC700.

7 Installation

7.1 Output Wiring

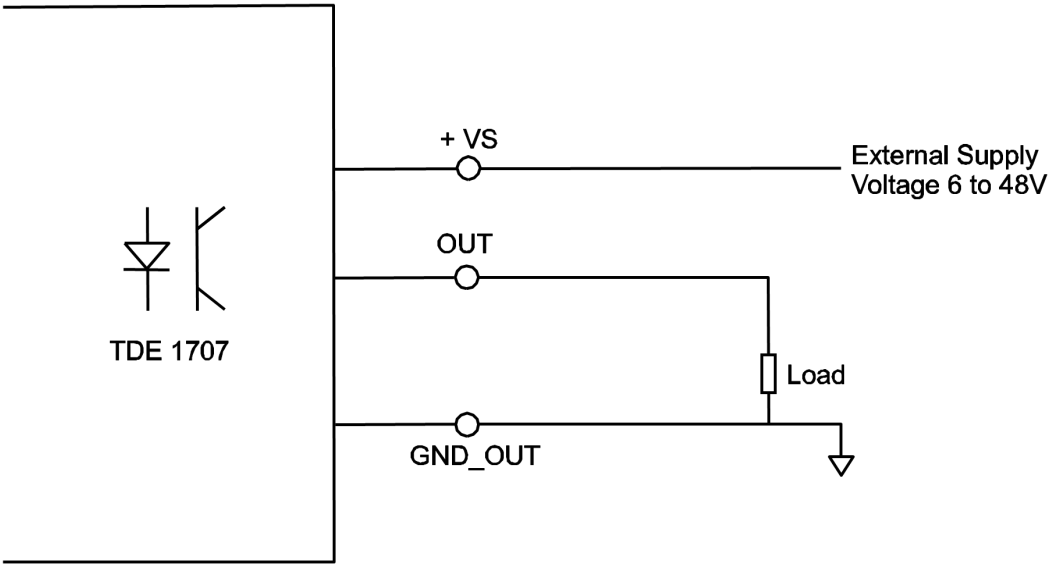

Figure 7-1 : Output Wiring

8 Pin Assignment – I/O Connector

8.1 Front Panel I/O

8.1.1 HD50 Connector

AMP 787395-5 or compatible.

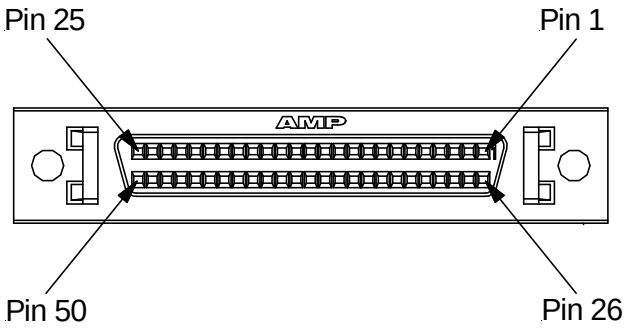

Figure 8-1 : Front Panel I/O Connector Numbering

8.1.3 Front Panel I/O Assignment TPMC700-1xR

The subsequent table shows the complete assembled pin front panel I/O connector. Bear in mind that variant -11R does not provide the channels 16 up to 32. Consequently, these are unconnected.

Pin	Signal	Description	Pin	Signal	Description
1	VS_O1	Power Supply for OUT 1 … OUT 4	26	OUT 10	Output 10
2			27	OUT 11	Output 11
3	VS_O2	Power Supply for OUT 5 … OUT 8	28	OUT 12	Output 12
4			29	OUT 13	Output 13
5	VS_O3	Power Supply for OUT 9 … OUT 12	30	OUT 14	Output 14
6			31	OUT 15	Output 15
7	VS_O4	Power Supply for OUT 13 … OUT 16	32	OUT 16	Output 16
8			33	OUT 17	Output 17
9	VS_O5	Power Supply for OUT 17 … OUT 20	34	OUT 18	Output 18
10			35	OUT 19	Output 19
11	VS_O6	Power Supply for OUT 21 … OUT 24	36	OUT 20	Output 20
12			37	OUT 21	Output 21
13	VS_O7	Power Supply for OUT 25 … OUT 28	38	OUT 22	Output 22
14			39	OUT 23	Output 23
15	VS_O8	Power Supply for OUT 29 … OUT 32	40	OUT 24	Output 24
16			41	OUT 25	Output 25
17	OUT 1	Output 1	42	OUT 26	Output 26
18	OUT 2	Output 2	43	OUT 27	Output 27
19	OUT 3	Output 3	44	OUT 28	Output 28
20	OUT 4	Output 4	45	OUT 29	Output 29
21	OUT 5	Output 5	46	OUT 30	Output 30
22	OUT 6	Output 6	47	OUT 31	Output 31
23	OUT 7	Output 7	48	OUT 32	Output 32
24	OUT 8	Output 8	49	GND_OA	Ground for OUT 1 … OUT 16
25	OUT 9	Output 9	50	GND_OB	Ground for OUT 17 … OUT 32

Table 8-1 : Pin Assignment Front I/O Connector TPMC700-1xR

Please check the maximum current of the used connection cable. Some standard cables (AWG28 50 pol.) are limited to 0.75 A per lead.

8.2 Back panel I/O

8.2.1 Mezzanine Card Connector P14

MOLEX 71436-216 or compatible.

8.2.2 Rear I/O Assignment TPMC700-2xR

The subsequent table shows the complete Rear I/O connector. Bear in mind that variant -21R does not provide the channels 16 up to 32. Consequently, these are unconnected.

Pin	Signal	Description	Pin	Signal	Description
1	VS_O1	Power Supply for OUT 1 … OUT 4	33	OUT 17	Output 17
2			34	OUT 18	Output 18
3	VS_O2	Power Supply for OUT 5 … OUT 8	35	OUT 19	Output 19
4			36	OUT 20	Output 20
5	VS_O3	Power Supply for OUT 9 … OUT 12	37	OUT 21	Output 21
6			38	OUT 22	Output 22
7	VS_O4	Power Supply for OUT 13 … OUT 16	39	OUT 23	Output 23
8			40	OUT 24	Output 24
9	VS_O5	Power Supply for OUT 17 … OUT 20	41	OUT 25	Output 25
10			42	OUT 26	Output 26
11	VS_O6	Power Supply for OUT 21 … OUT 24	43	OUT 27	Output 27
12			44	OUT 28	Output 28
13	VS_O7	Power Supply for OUT 25 … OUT 28	45	OUT 29	Output 29
14			46	OUT 30	Output 30
15	VS_O8	Power Supply for OUT 29 … OUT 32	47	OUT 31	Output 31
16			48	OUT 32	Output 32
17	OUT 1	Output 1	49	GND_OA	Ground for OUT 1 … OUT 16
18	OUT 2	Output 2	50	GND_OB	Ground for OUT 17 … OUT 32
19	OUT 3	Output 3	51	Not connected	
20	OUT 4	Output 4	52		
21	OUT 5	Output 5	53		
22	OUT 6	Output 6	54		
23	OUT 7	Output 7	55		
24	OUT 8	Output 8	56		
25	OUT 9	Output 9	57		
26	OUT 10	Output 10	58		
27	OUT 11	Output 11	59		
28	OUT 12	Output 12	60		
29	OUT 13	Output 13	61		
30	OUT 14	Output 14	62		
31	OUT 15	Output 15	63		
32	OUT 16	Output 16	64		

Table 8-2 : Pin Assignment Rear I/O Connector TPMC700-2xR